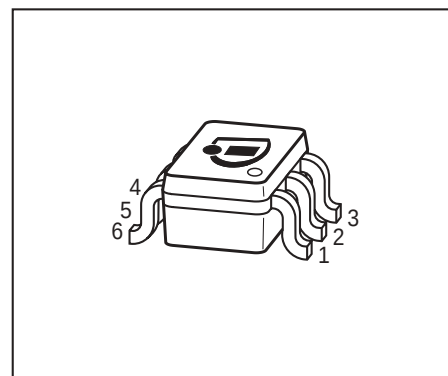
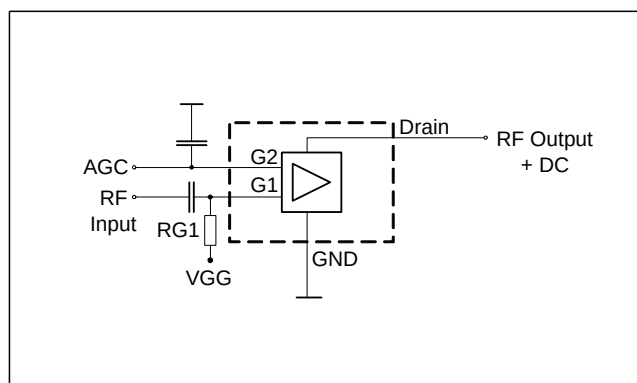
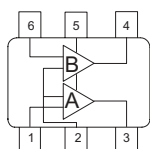


DUAL N-Channel MOSFET Tetrode

- Two gain controlled input stage for UHF and VHF -tuners e.g. (NTSC, PAL)
- Two AGC amplifiers in one single package
- Integrated gate protection diodes
- High AGC-range, low noise figure, high gain
- Improved cross modulation at gain reduction



BG3130 BG3130R



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BG3130	SOT363	1=G1*	2=G2	3=D*	4=D**	5=S	6=G1**	KAs
BG3130R	SOT363	1=G1*	2=S	3=D*	4=D**	5=G2	6=G1**	KHs

* For amp. A; ** for amp. B
180° rotated tape loading orientation available

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	1	
Gate 1/ gate 2-source voltage	$\pm V_{G1/G2S}$	6	V
Total power dissipation	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point ¹⁾	R_{thchs}	≤ 280	K/W

Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Drain-source breakdown voltage $I_D = 10 \mu A$, $V_{G1S} = 0 V$, $V_{G2S} = 0 V$	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10 mA$, $V_{G2S} = 0 V$, $V_{DS} = 0 V$	$+V_{(BR)G1SS}$	6	-	15	
Gate2-source breakdown voltage $+I_{G2S} = 10 mA$, $V_{G1S} = 0 V$, $V_{DS} = 0 V$	$+V_{(BR)G2SS}$	6	-	15	
Gate1-source leakage current $V_{G1S} = 6 V$, $V_{G2S} = 0 V$	$+I_{G1SS}$	-	-	50	μA
Gate2-source leakage current $V_{G2S} = 8 V$, $V_{G1S} = 0 V$, $V_{DS} = 0 V$	$+I_{G2SS}$	-	-	50	nA
Drain current $V_{DS} = 5 V$, $V_{G1S} = 0 V$, $V_{G2S} = 4.5 V$	I_{DSS}	-	-	10	μA
Drain-source current $V_{DS} = 5 V$, $V_{G2S} = 4 V$, $R_{G1} = 120 k\Omega$	I_{DSX}	-	10	-	mA
Gate1-source pinch-off voltage $V_{DS} = 5 V$, $V_{G2S} = 4 V$, $I_D = 20 \mu A$	$V_{G1S(p)}$	-	0.7	-	V
Gate2-source pinch-off voltage $V_{DS} = 5 V$, $I_D = 20 \mu A$	$V_{G2S(p)}$	-	0.6	-	

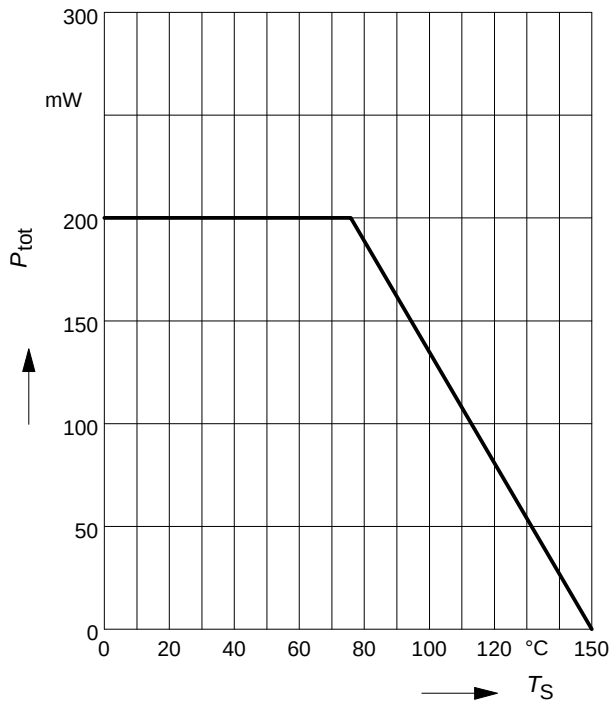
¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics $V_{DS} = 5V$, $V_{G2S} = 4V$, ($I_D = 14\text{ mA}$) (verified by random sampling)					
Forward transconductance	g_{fs}	-	33	-	mS
Gate1 input capacitance $f = 10\text{ MHz}$	C_{g1ss}	-	1.9	-	pF
Output capacitance $f = 10\text{ MHz}$	C_{dss}	-	1.1	-	
Power gain $f = 800\text{ MHz}$ $f = 45\text{ MHz}$	G_p	- -	24 31	- -	dB
Noise figure $f = 800\text{ MHz}$ $f = 45\text{ MHz}$	F	- -	1.3 1.7	- -	
Gain control range $V_{G2S} = 4 \dots 0\text{ V}$, $f = 800\text{ MHz}$	ΔG_p	45	-	-	
Cross-modulation $k=1\%$, $f_w=50\text{MHz}$, $f_{unw}=60\text{MHz}$ AGC = 0 dB AGC = 10 dB AGC = 40 dB	X_{mod}	90 - 96	- 87 100	- - -	-

Total power dissipation $P_{\text{tot}} = f(T_S)$

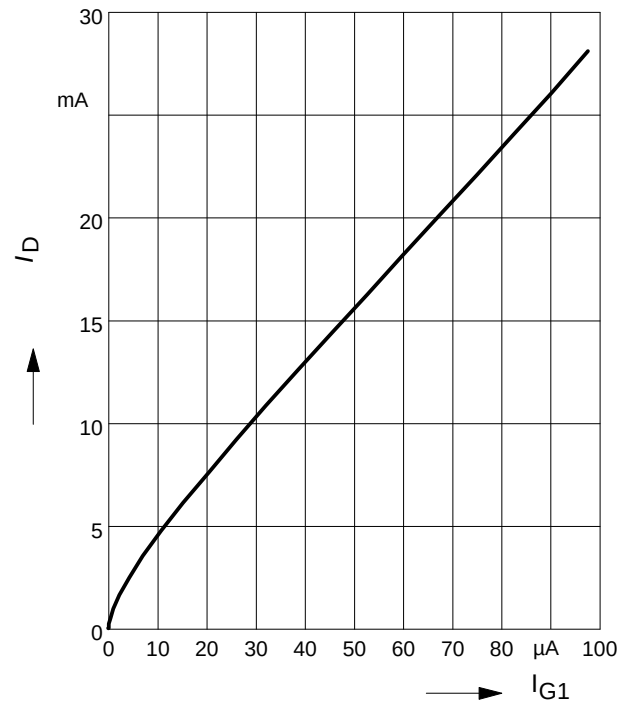
amp. A = amp. B



Drain current $I_D = f(I_{G1})$

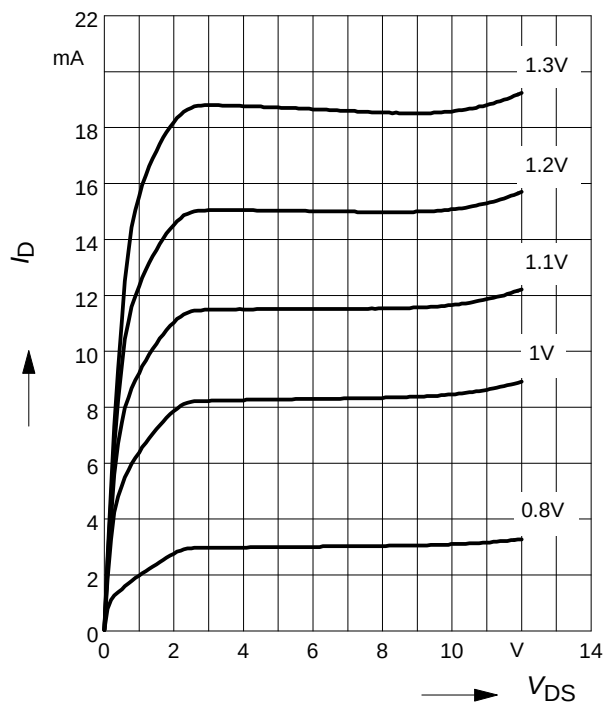
$V_{G2S} = 4V$

amp. A = amp. B



Output characteristics $I_D = f(V_{DS})$

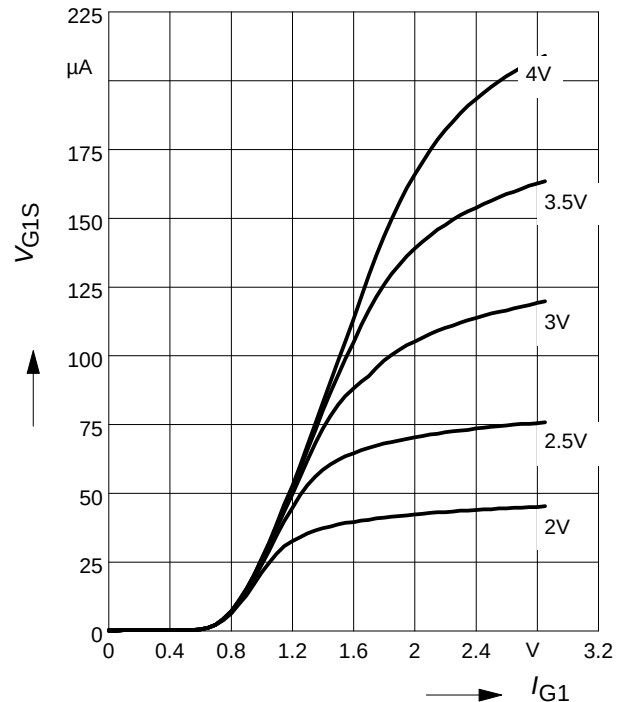
amp. A = amp. B



Gate 1 current $I_{G1} = f(V_{G1S})$

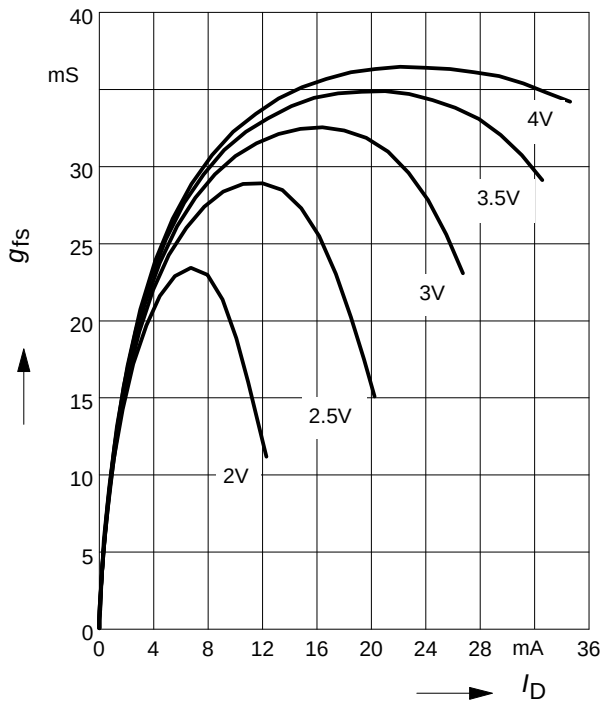
$V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$

amp. A = amp. B

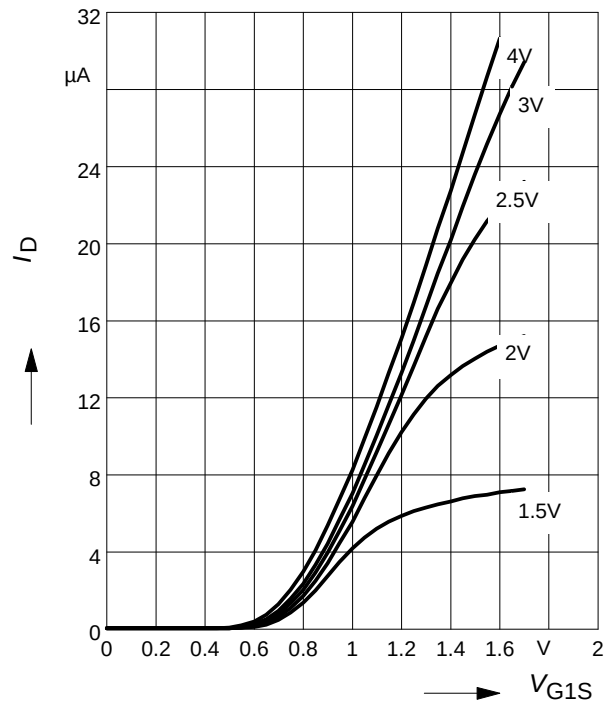


Gate 1 forward transconductance

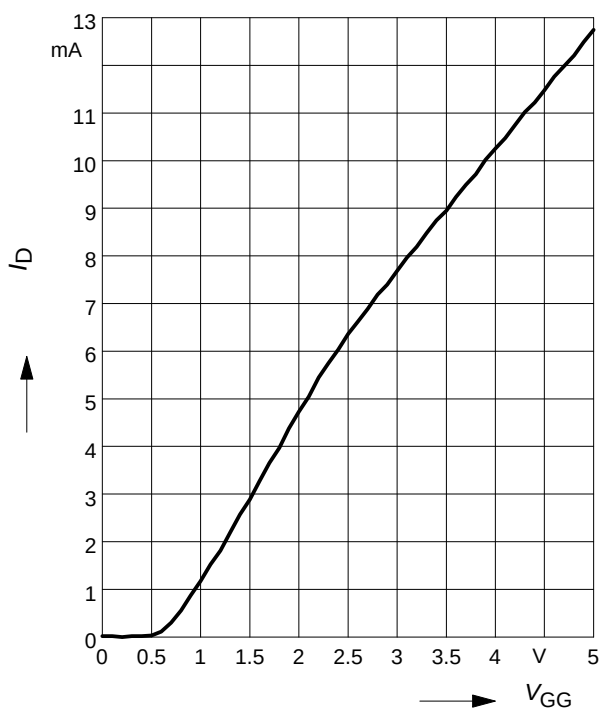
$g_{fs} = f(I_D)$, $V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$
amp. A = amp. B


Drain current $I_D = f(V_{G1S})$

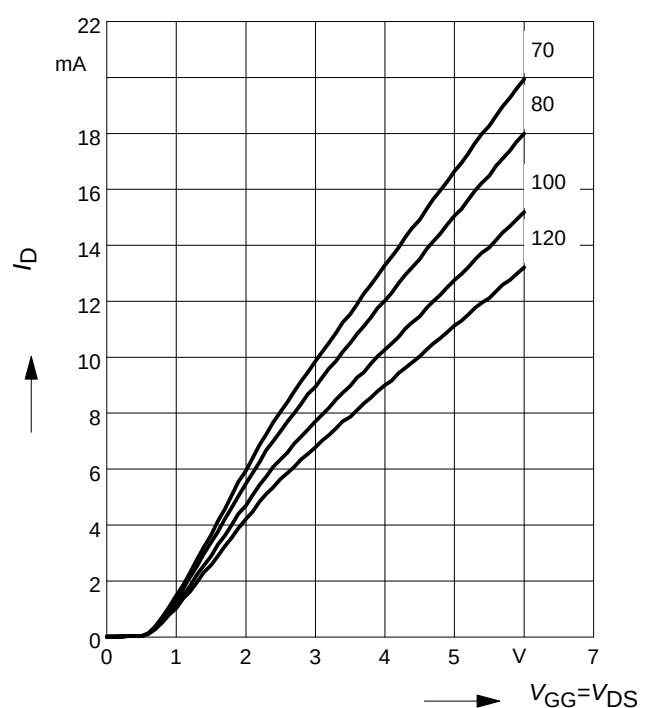
$V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$
amp. A = amp. B

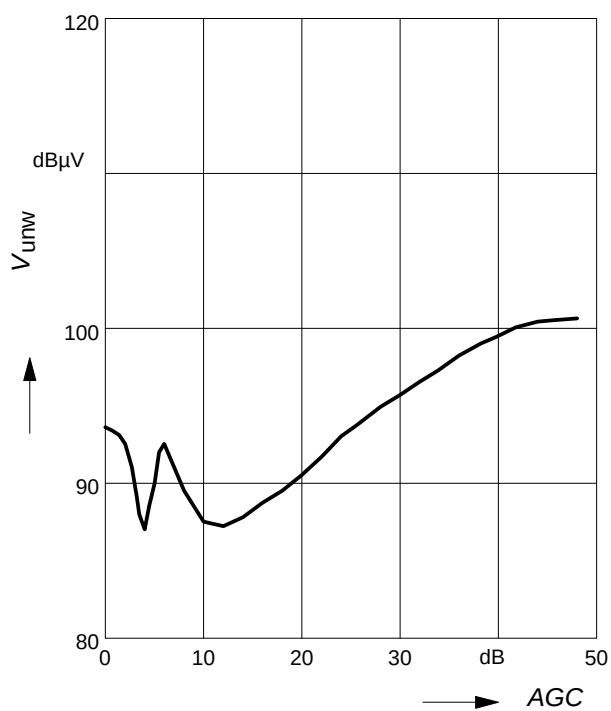
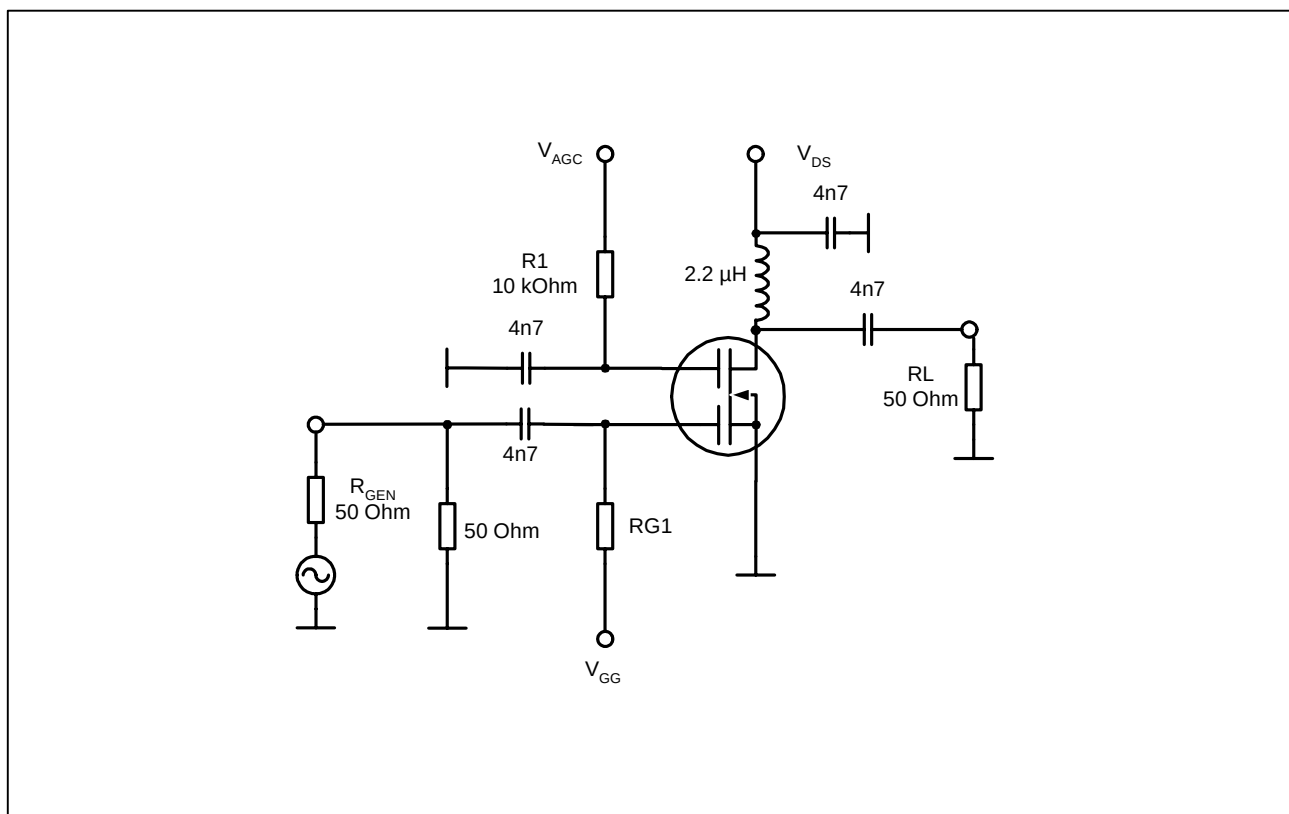

Drain current $I_D = f(V_{GG})$ amp.A=amp.B

$V_{DS} = 5V$, $V_{G2S} = 4V$, $R_{G1} = 120k\Omega$
(connected to V_{GG} , $V_{GG} = \text{gate1 supply voltage}$)


Drain current $I_D = f(V_{GG})$

$V_{G2S} = 4V$, $R_{G1} = \text{Parameter in } k\Omega$
amp. A = amp. B



Crossmodulation $V_{unw} = (AGC)$
 $V_{DS} = 5\text{ V}, R_{g1} = 68\text{ k}\Omega$

Crossmodulation test circuit


Technical drawing of a 2x3 grid of rectangular features. The drawing shows a top view with dimensions: 0.3 (width of one feature), 0.9 (height of one feature), 0.7 (height of one feature), 1.6 (total height), and 0.65 (width of one feature). The features are arranged in a 2x3 grid with a dashed center line.

The diagram illustrates the marking scheme for the BCR108S component. It shows a component with a central marking area. The marking area contains the text '12 s' and a date code box. Labels indicate the following:

- Manufacturer:** Infineon Technologies
- Date code (Year/Month):** 2005, June
- Laser marking:** 12 s
- Type code:** BCR108S
- Pin 1 marking:** WH s

An example marking is shown with the text 'WH s' and '2005, June'.

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