

Memory FRAM

2 M (256 K × 8) Bit SPI

MB85RS2MT

■ DESCRIPTION

MB85RS2MT is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 262,144 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

MB85RS2MT adopts the Serial Peripheral Interface (SPI).

The MB85RS2MT is able to retain data without using a back-up battery, as is needed for SRAM.

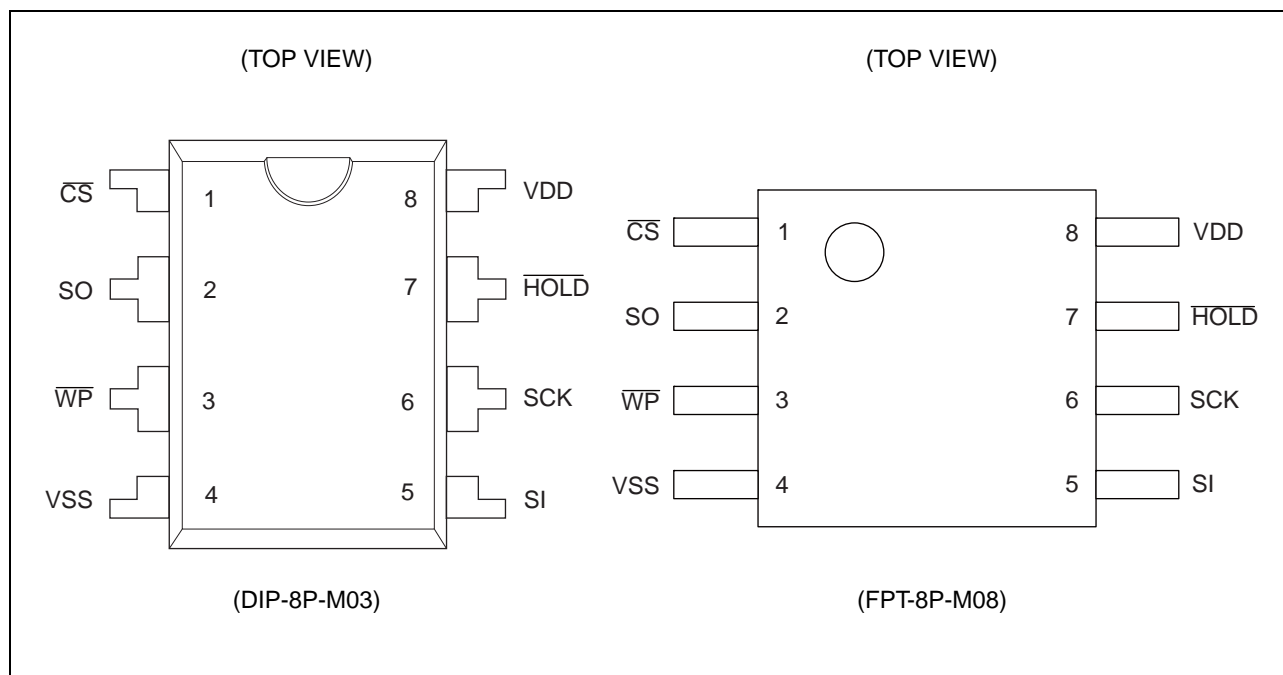
The memory cells used in the MB85RS2MT can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

MB85RS2MT does not take long time to write data like Flash memories or E²PROM, and MB85RS2MT takes no wait time.

■ FEATURES

- Bit configuration : 262,144 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 25 MHz (Max)
For FSTRD command 2.7 V to 3.6 V, 40 MHz (Max)
- High endurance : 10^{13} times / byte
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption : Operating power supply current 10.6 mA (Max@25 MHz) (TBD)
Standby current 150 μA (Max) (TBD)
Sleep current 10 μA (Max) (TBD)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M08)
8-pin plastic DIP (DIP-8P-M03)
RoHS compliant

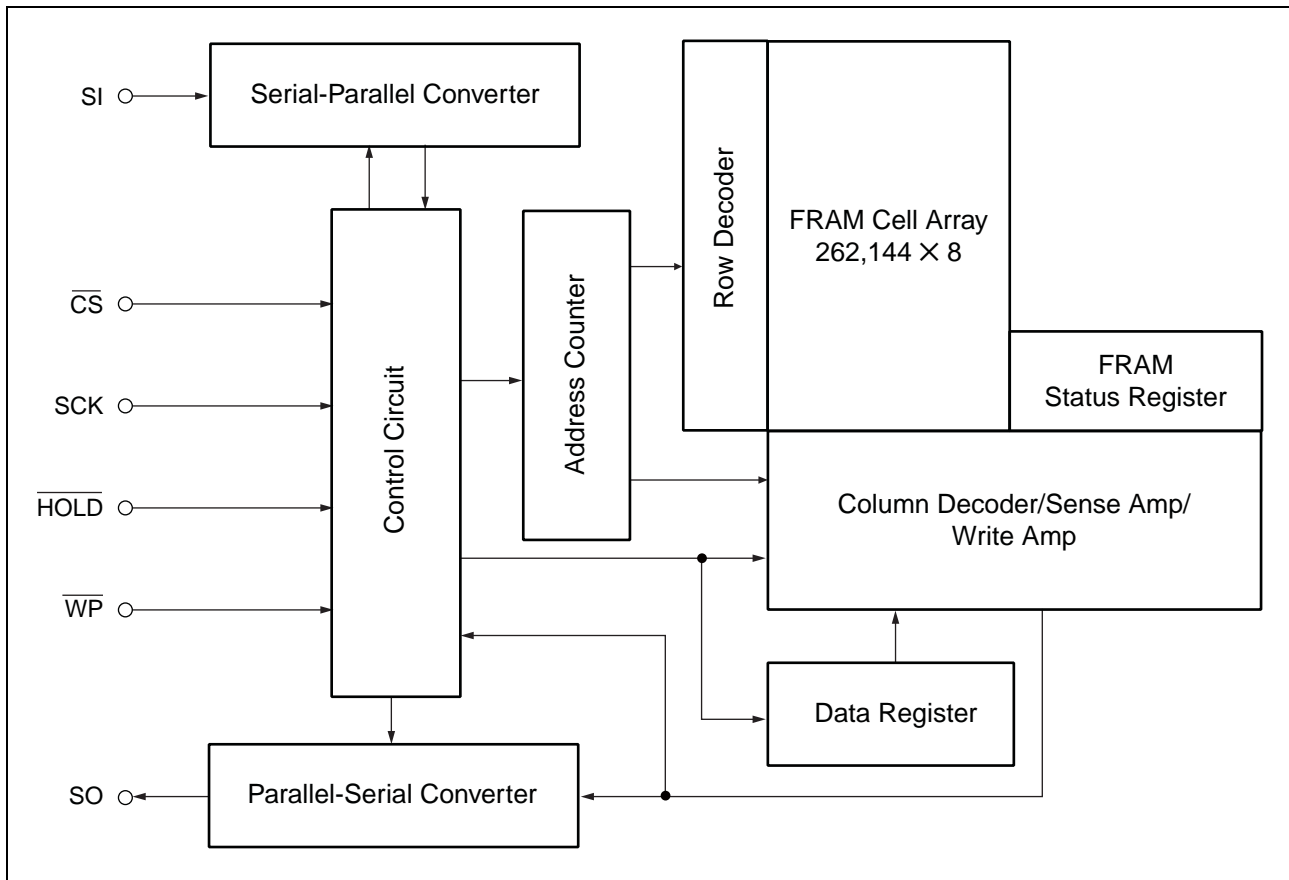
PIN ASSIGNMENT



PIN FUNCTIONAL DESCRIPTIONS

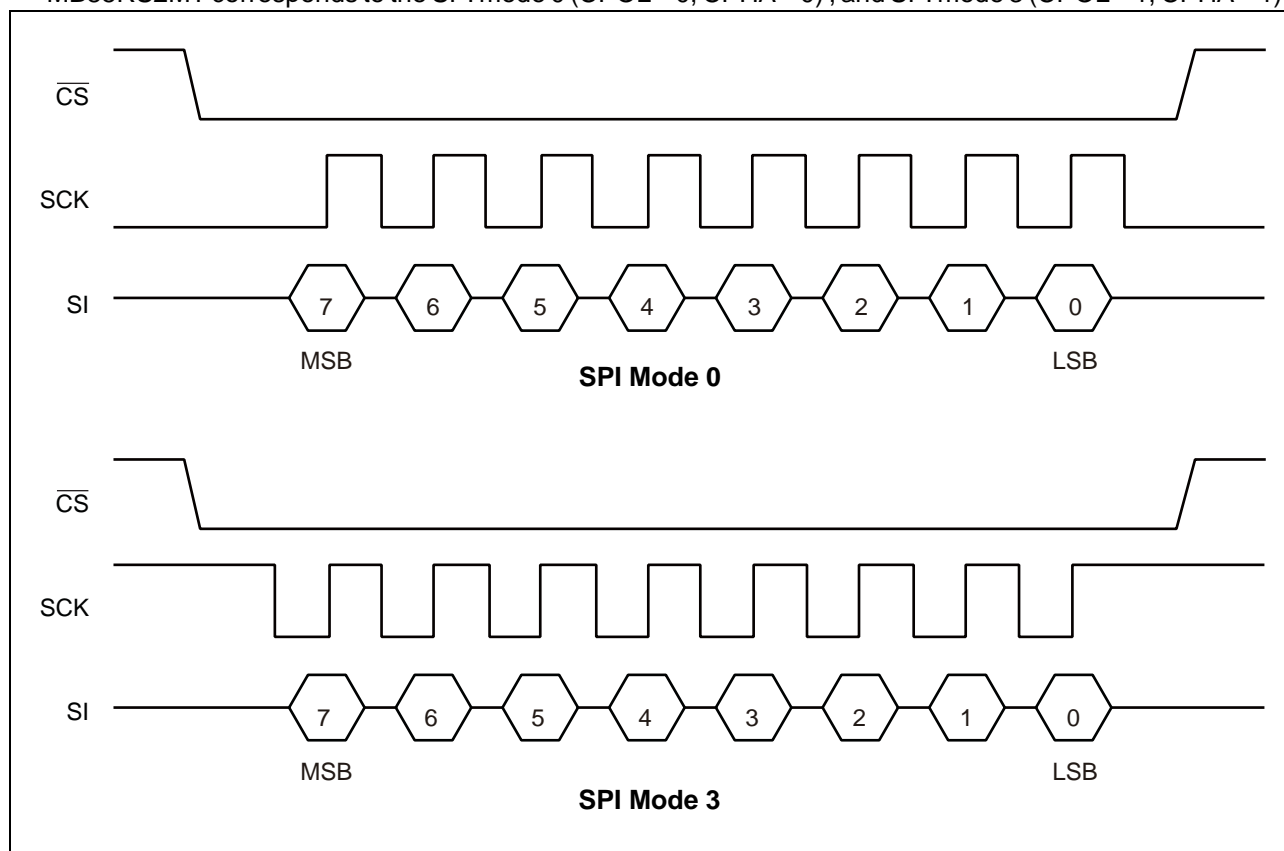
| Pin No. | Pin Name | Functional description |
|---------|-------------------|--|
| 1 | \overline{CS} | Chip Select pin This is an input pin to make chips select. When \overline{CS} is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When \overline{CS} is "L" level, device is in select (active) status. \overline{CS} has to be "L" level before inputting op-code. |
| 3 | \overline{WP} | Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with \overline{WP} and WPEN. See "■ WRITING PROTECT" for detail. |
| 7 | \overline{HOLD} | Hold pin This pin is used to interrupt serial input/output without making chips deselect. When \overline{HOLD} is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, \overline{CS} has to be retained "L" level. |
| 6 | SCK | Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge. |
| 5 | SI | Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data. |
| 2 | SO | Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby. |
| 8 | VDD | Supply Voltage pin |
| 4 | VSS | Ground pin |

■ BLOCK DIAGRAM



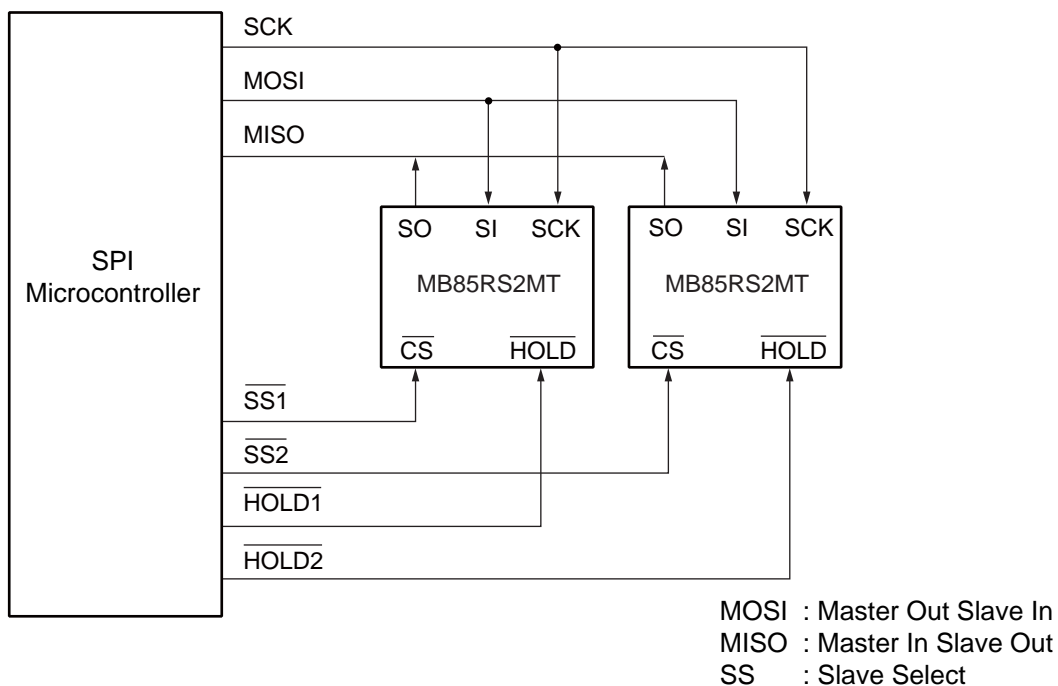
■ SPI MODE

MB85RS2MT corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).

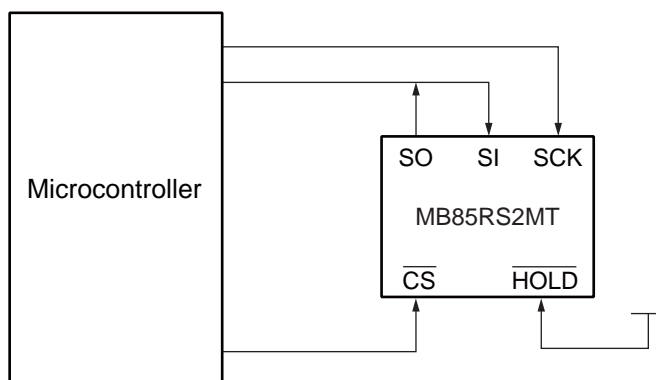


■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS2MT works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

| Bit No. | Bit Name | Function |
|---------|----------|---|
| 7 | WPEN | Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with \overline{WP} input. Writing with the WRSR command and reading with the RDSR command are possible. |
| 6 to 4 | — | Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command. |
| 3 | BP1 | Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible. |
| 2 | BP0 | |
| 1 | WEL | Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. The rising edge of \overline{CS} after WRSR command recognition. The rising edge of \overline{CS} after WRITE command recognition. |
| 0 | 0 | This is a bit fixed to "0". |

■ OP-CODE

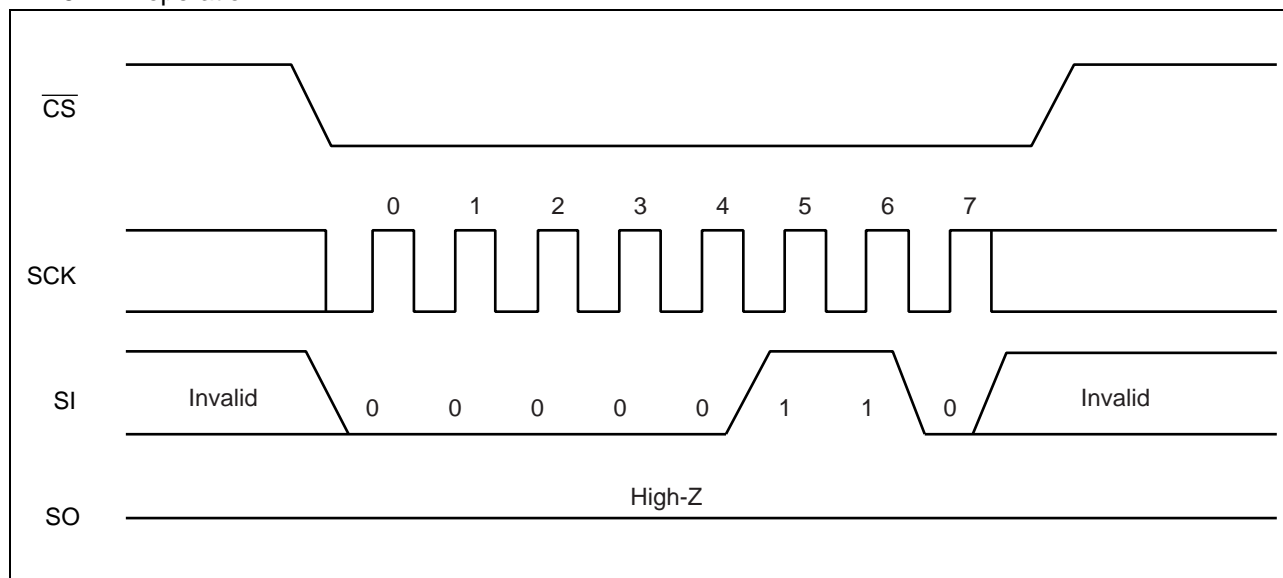
MB85RS2MT accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If \overline{CS} is risen while inputting op-code, the command are not performed.

| Name | Description | Op-code |
|-------|--------------------------|------------------------|
| WREN | Set Write Enable Latch | 0000 0110 _B |
| WRDI | Reset Write Enable Latch | 0000 0100 _B |
| RDSR | Read Status Register | 0000 0101 _B |
| WRSR | Write Status Register | 0000 0001 _B |
| READ | Read Memory Code | 0000 0011 _B |
| WRITE | Write Memory Code | 0000 0010 _B |
| RDID | Read Device ID | 1001 1111 _B |
| FSTRD | Fast Read Memory Code | 0000 1011 _B |
| SLEEP | Sleep Mode | 1011 1001 _B |

■ COMMAND

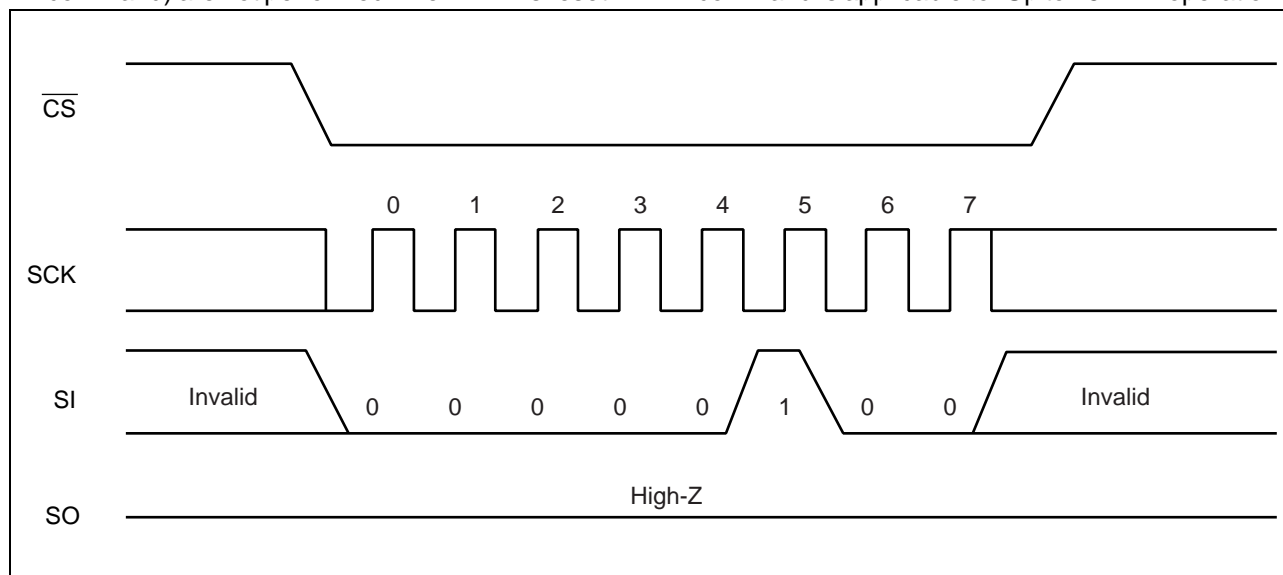
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) . WREN command is applicable to "Up to 25 MHz operation".



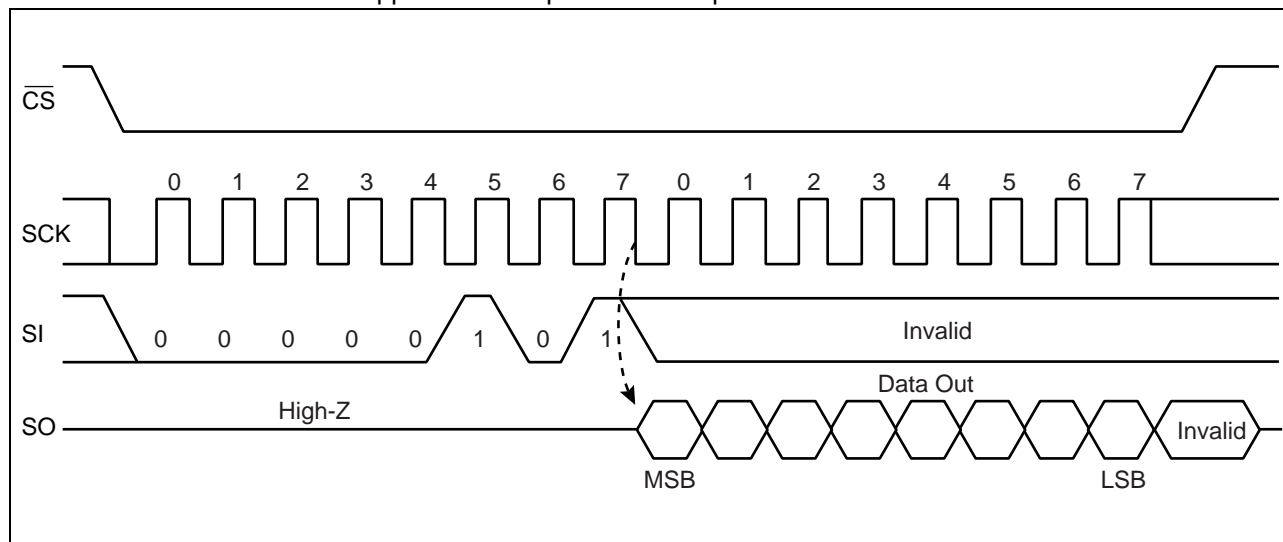
• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset. WRDI command is applicable to "Up to 25 MHz operation".



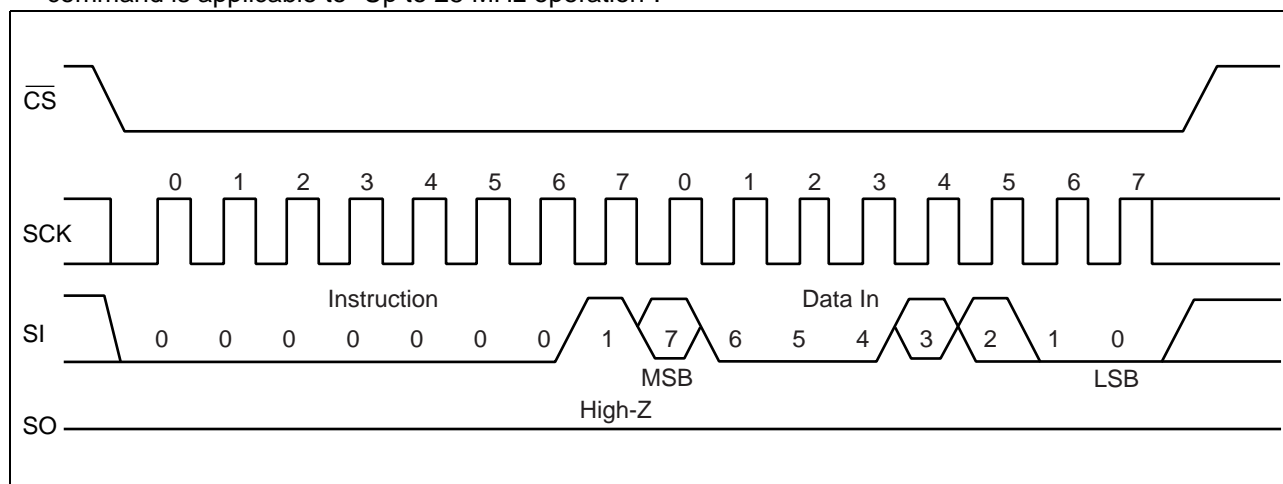
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of \overline{CS} . RDSR command is applicable to "Up to 25 MHz operation".



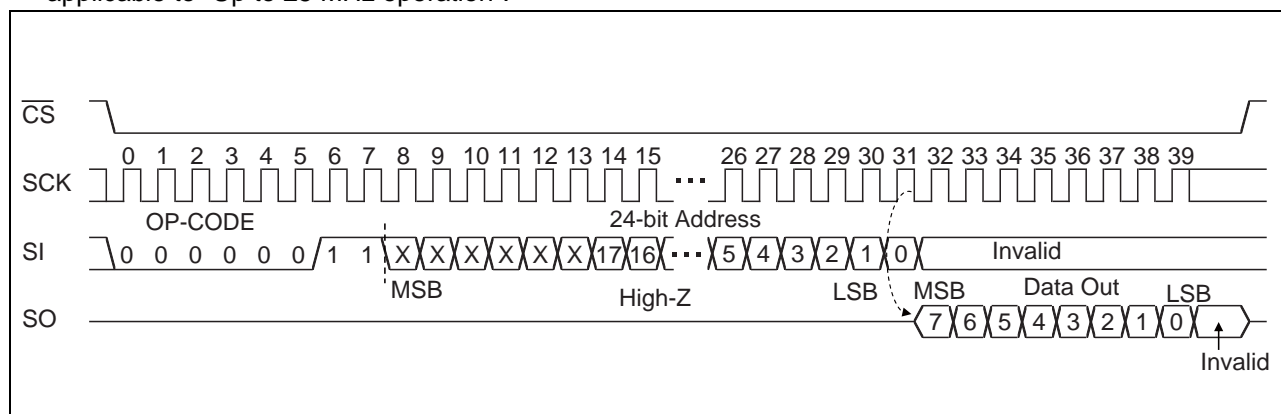
• WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. \overline{WP} signal level shall be fixed before performing WRSR command, and do not change the \overline{WP} signal level until the end of command sequence. WRSR command is applicable to "Up to 25 MHz operation".



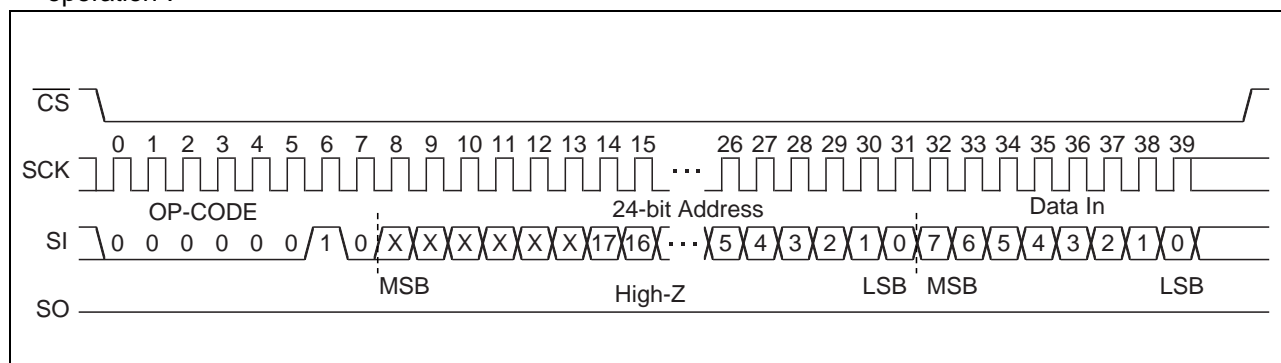
• READ

The READ command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. READ command is applicable to "Up to 25 MHz operation".



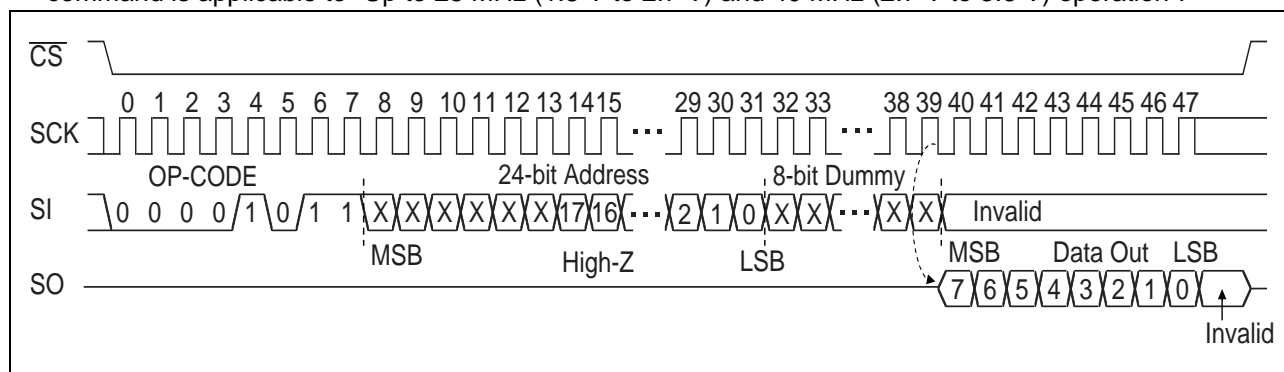
• WRITE

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 6-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen \overline{CS} will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely. WRITE command is applicable to "Up to 25 MHz operation".



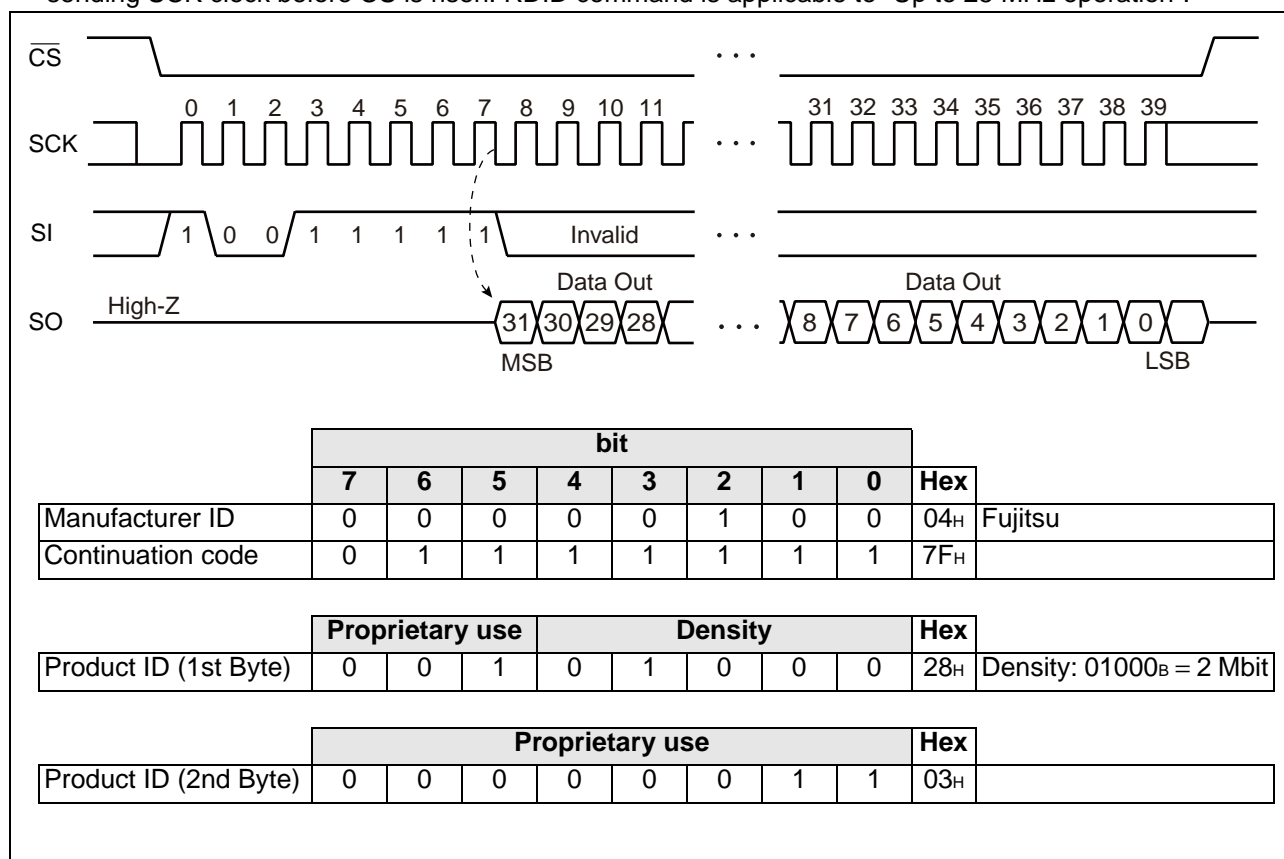
• FSTRD

The FSTRD command reads FRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. FSTRD command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 40 MHz (2.7 V to 3.6 V) operation”.



• RDID

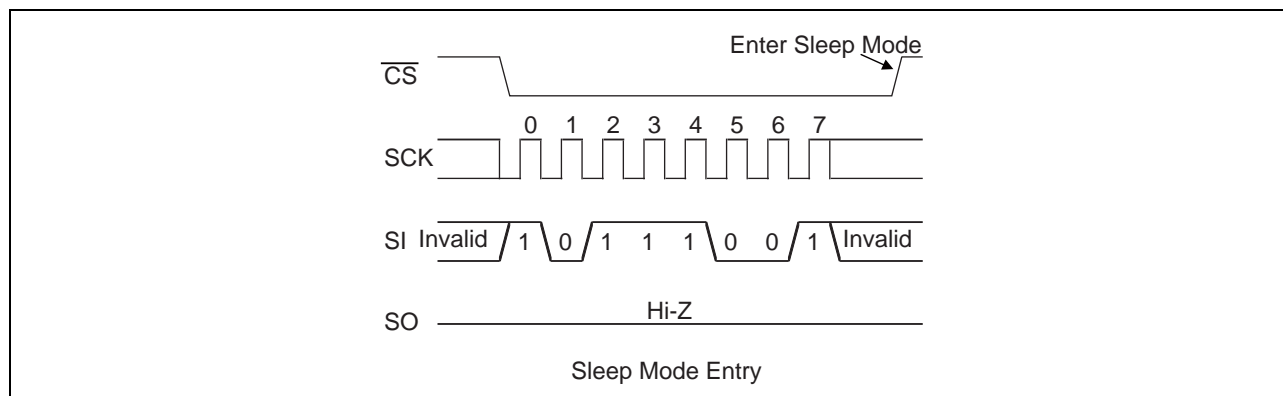
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit after 32-bit Device ID output by continuously sending SCK clock before CS is risen. RDID command is applicable to “Up to 25 MHz operation”.



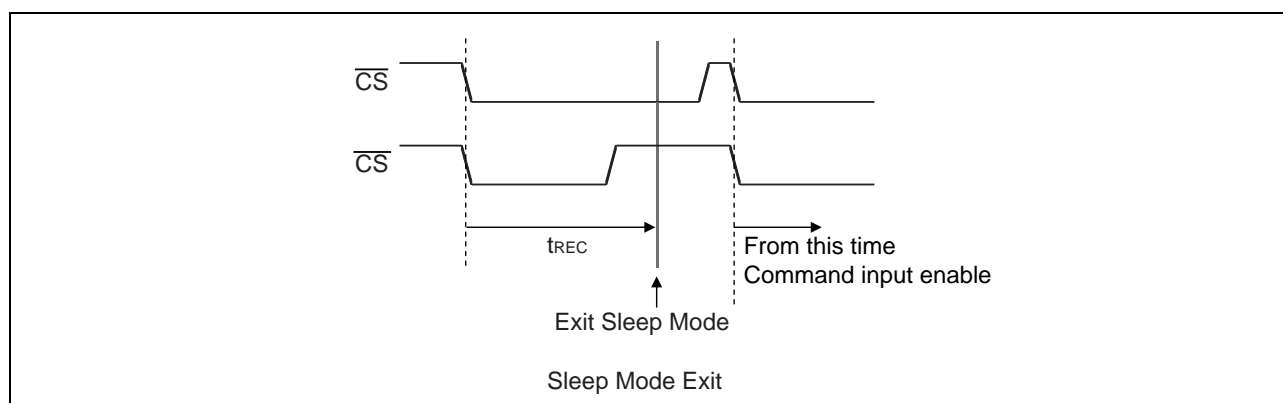
• SLEEP

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of \overline{CS} after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of \overline{CS} after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a Hi-Z state.



Returning to a normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μ s) time from the falling edge of \overline{CS} (see the figure below). It is possible to return \overline{CS} to H level before t_{REC} time. However, it is prohibited to bring down \overline{CS} to L level again during t_{REC} period.



■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1 | BP0 | Protected Block |
|-----|-----|--|
| 0 | 0 | None |
| 0 | 1 | 30000 _H to 3FFFF _H (upper 1/4) |
| 1 | 0 | 20000 _H to 3FFFF _H (upper 1/2) |
| 1 | 1 | 00000 _H to 3FFFF _H (all) |

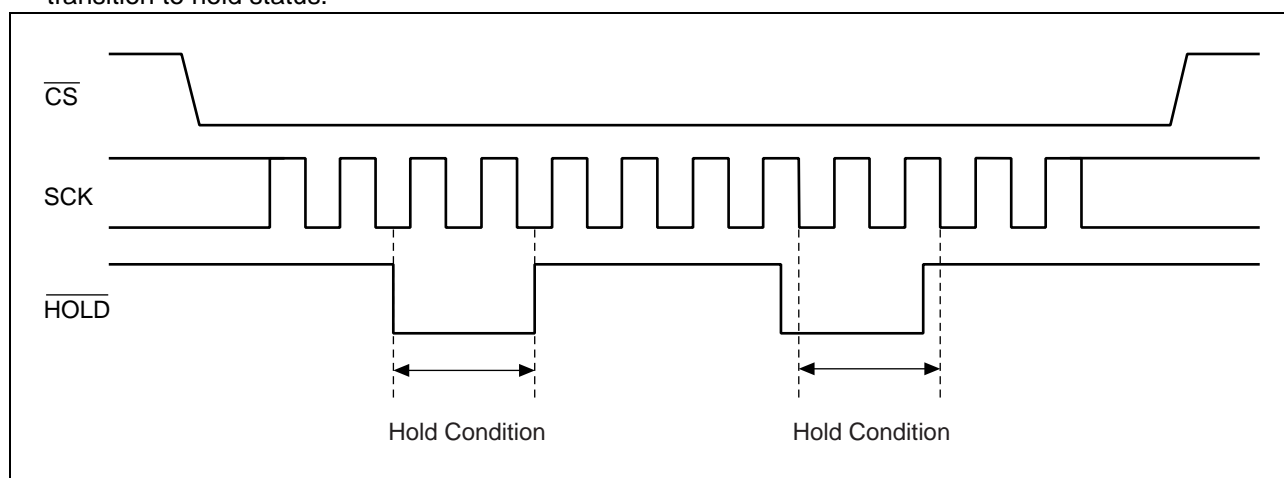
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, \overline{WP} as shown in the table.

| WEL | WPEN | \overline{WP} | Protected Blocks | Unprotected Blocks | Status Register |
|-----|------|-----------------|------------------|--------------------|-----------------|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Unprotected | Unprotected |
| 1 | 1 | 0 | Protected | Unprotected | Protected |
| 1 | 1 | 1 | Protected | Unprotected | Unprotected |

■ HOLD OPERATION

Hold status is retained without aborting a command if \overline{HOLD} is "L" level while \overline{CS} is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a \overline{HOLD} pin input is transitioned to the hold condition as shown in the diagram below. In case the \overline{HOLD} pin transitioned to "L" level when SCK is "L" level, return the \overline{HOLD} pin to "H" level at SCK being "L" level. In the same manner, in case the \overline{HOLD} pin transitioned to "L" level when SCK is "H" level, return the \overline{HOLD} pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If \overline{CS} is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|-------------------------------|-----------|--------|----------------|------|
| | | Min | Max | |
| Power supply voltage* | V_{DD} | - 0.5 | + 4.0 | V |
| Input voltage* | V_{IN} | - 0.5 | $V_{DD} + 0.5$ | V |
| Output voltage* | V_{OUT} | - 0.5 | $V_{DD} + 0.5$ | V |
| Operation ambient temperature | T_A | - 40 | + 85 | °C |
| Storage temperature | T_{stg} | - 55 | + 125 | °C |

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|-------------------------------|----------|---------------------|-----|---------------------|------|
| | | Min | Typ | Max | |
| Power supply voltage* | V_{DD} | 1.8 | 3.3 | 3.6 | V |
| Input high voltage* | V_{IH} | $V_{DD} \times 0.7$ | — | $V_{DD} + 0.5$ | V |
| Input low voltage* | V_{IL} | - 0.5 | — | $V_{DD} \times 0.3$ | V |
| Operation ambient temperature | T_A | - 40 | — | + 85 | °C |

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value(TBD) | | | Unit |
|--------------------------------|------------|--|----------------|-----|------|---------|
| | | | Min | Typ | Max | |
| Input leakage current*1 | $ I_{LI} $ | $0 \leq \overline{CS} < V_{DD}$ | — | — | 200 | μA |
| | | $\overline{CS} = V_{DD}$ | — | — | 1 | |
| | | $\overline{WP}, \overline{HOLD}, SCK$ $SI = 0 V \text{ to } V_{DD}$ | — | — | 1 | |
| Output leakage current*2 | $ I_{LO} $ | $SO = 0 V \text{ to } V_{DD}$ | — | — | 1 | μA |
| Operating power supply current | I_{DD} | $SCK = 25 \text{ MHz}$ | — | — | 10.6 | mA |
| Standby current | I_{SB} | All inputs V_{SS} or $SCK = SI = \overline{CS} = V_{DD}$ | — | 35 | 150 | μA |
| Sleep current | I_{ZZ} | $\overline{CS} = V_{DD}$ All inputs V_{SS} or V_{DD} | — | — | 10 | μA |
| Output high voltage | V_{OH} | $I_{OH} = -2 \text{ mA}$ | $V_{DD} - 0.5$ | — | — | V |
| Output low voltage | V_{OL} | $I_{OL} = 2 \text{ mA}$ | — | — | 0.4 | V |

*1 : Applicable pin : \overline{CS} , \overline{WP} , \overline{HOLD} , SCK , SI

*2 : Applicable pin : SO

2. AC Characteristics

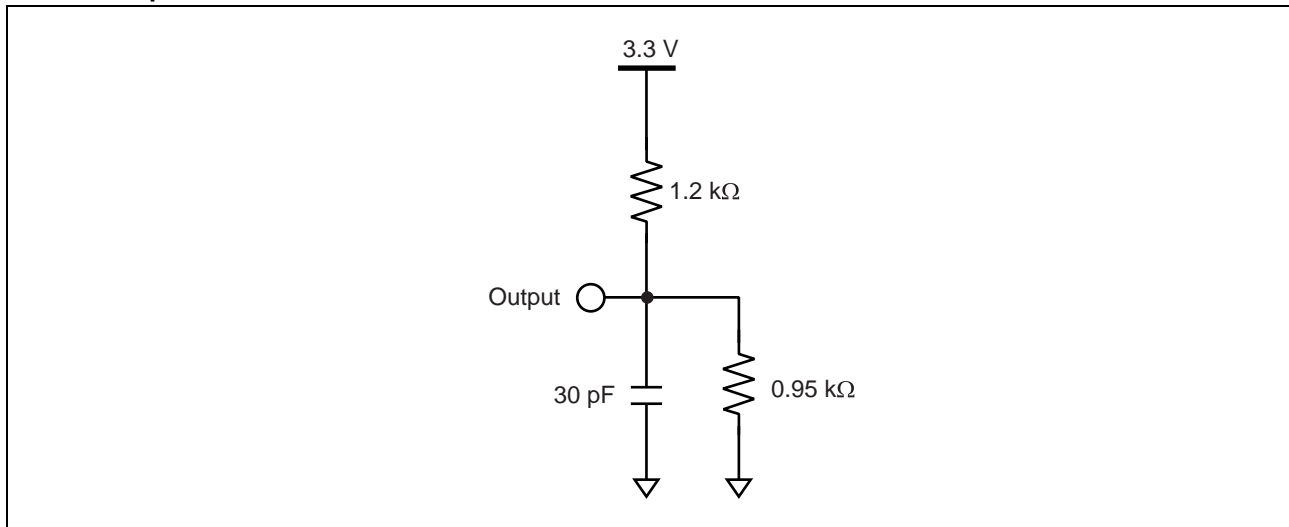
| Parameter | Symbol | Value (TBD) | | | | Unit |
|---|------------------|----------------------------------|-----|----------------------------------|-----|------|
| | | Up to 25 MHz operation* | | | | |
| | | V _{DD} = 1.8 V to 2.7 V | | V _{DD} = 2.7 V to 3.6 V | | |
| | | Min | Max | Min | Max | |
| SCK clock frequency (All commands except FSTRD command) | f _{CK} | 0 | 25 | 0 | 25 | MHz |
| SCK clock frequency (for FSTRD command) | f _{CK} | 0 | 25 | 0 | 40 | MHz |
| Clock high time | t _{CH} | 15 | — | 11 | — | ns |
| Clock low time | t _{CL} | 15 | — | 11 | — | ns |
| Chip select set up time | t _{CSU} | 10 | — | 10 | — | ns |
| Chip select hold time | t _{CSH} | 10 | — | 10 | — | ns |
| Output disable time | t _{OD} | — | 12 | - | 12 | ns |
| Output data valid time | t _{ODV} | — | 18 | - | 9 | ns |
| Output hold time | t _{OH} | 0 | — | 0 | — | ns |
| Deselect time | t _D | 40 | — | 40 | — | ns |
| Data in rising time | t _R | — | 50 | - | 50 | ns |
| Data falling time | t _F | — | 50 | - | 50 | ns |
| Data set up time | t _{SU} | 5 | — | 5 | — | ns |
| Data hold time | t _H | 5 | — | 5 | — | ns |
| HOLD set uptime | t _{HS} | 10 | — | 10 | — | ns |
| HOLD hold time | t _{HH} | 10 | — | 10 | — | ns |
| HOLD output floating time | t _{HZ} | — | 20 | — | 20 | ns |
| HOLD output active time | t _{LZ} | — | 20 | — | 20 | ns |
| SLEEP recovery time | t _{REC} | — | 400 | — | 400 | μs |

* : All commands except FSTRD are applicable to “Up to 25 MHz operation”.

AC Test Condition

| | |
|-------------------------------|---|
| Power supply voltage | : 1.8 V to 3.6 V |
| Operation ambient temperature | : - 40 °C to + 85 °C |
| Input voltage magnitude | : $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$ $0 \leq V_{IL} \leq V_{DD} \times 0.3$ |
| Input rising time | : 5 ns |
| Input falling time | : 5 ns |
| Input judge level | : $V_{DD}/2$ |
| Output judge level | : $V_{DD}/2$ |

AC Load Equivalent Circuit

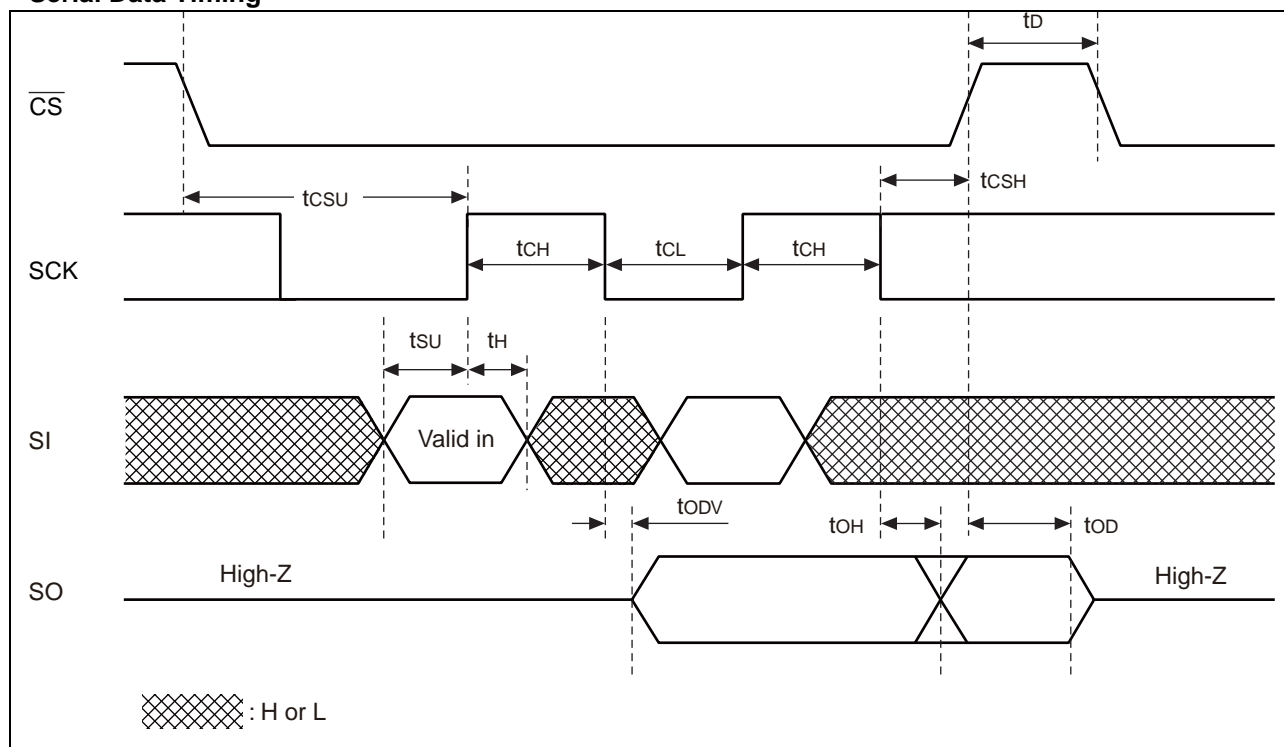


3. Pin Capacitance

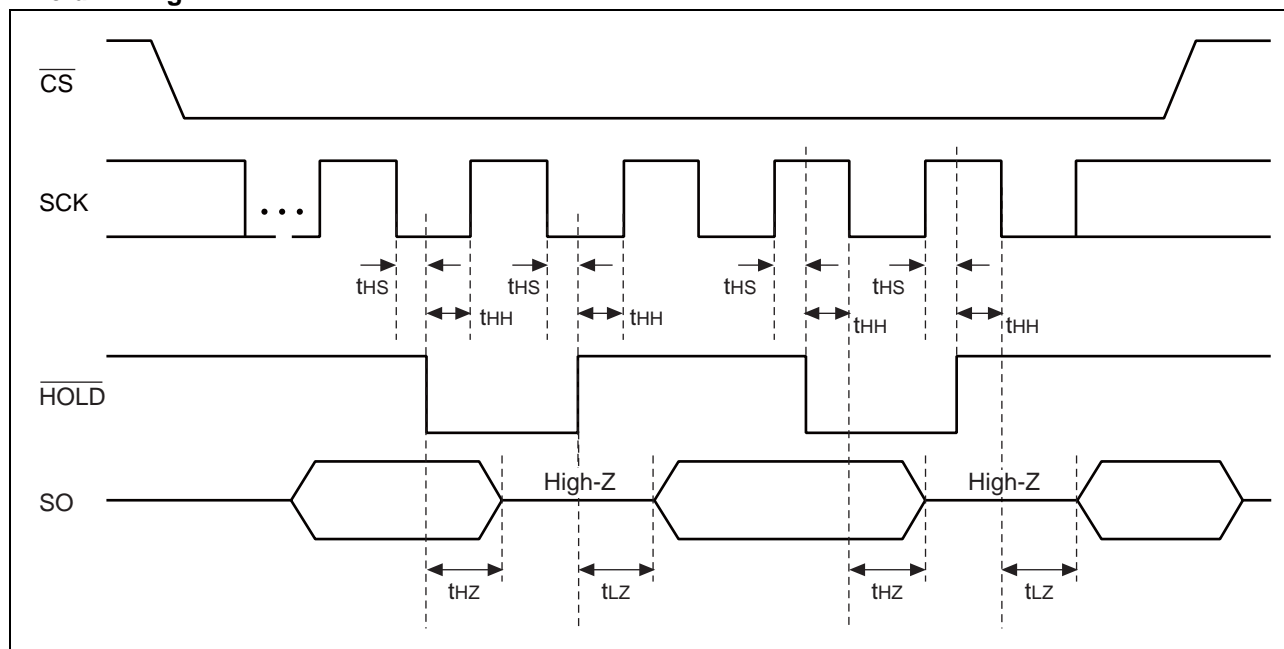
| Parameter | Symbol | Condition | Value | | Unit |
|--------------------|--------|--|-------|-----|------|
| | | | Min | Max | |
| Output capacitance | C_o | $V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$, $f = 1\text{ MHz}$, $T_A = +25\text{ }^{\circ}\text{C}$ | — | 6 | pF |
| Input capacitance | C_i | | — | 8 | pF |

■ TIMING DIAGRAM

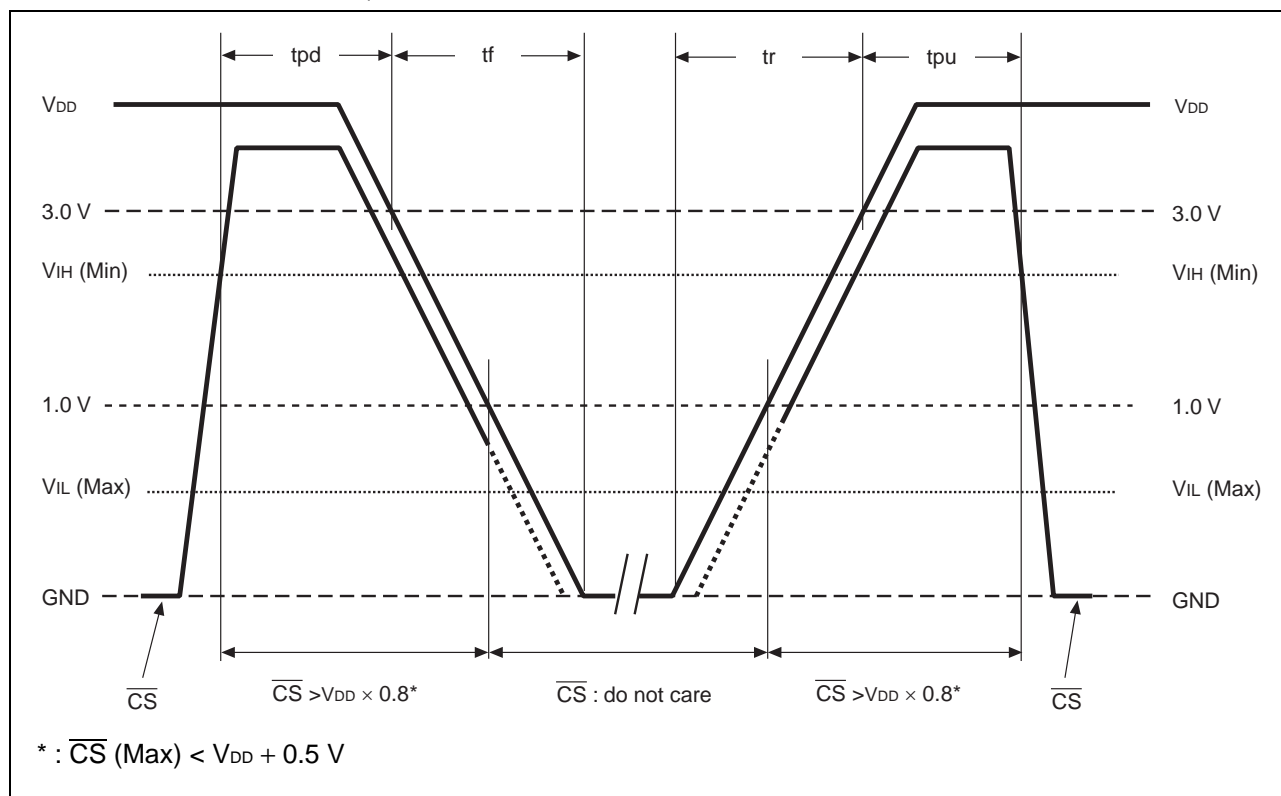
• Serial Data Timing



• Hold Timing



POWER ON/OFF SEQUENCE



| Parameter | Symbol | Value | | Unit |
|--|--------|-------|-----|------|
| | | Min | Max | |
| \overline{CS} level hold time at power OFF | tpd | 0 | — | ns |
| \overline{CS} level hold time at power ON | tpu | 250 | — | ns |
| Power supply rising time | tr | 0.05 | — | ms/V |
| Power supply falling time | tf | 0.1 | — | ms/V |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

FRAM CHARACTERISTICS

| Parameter | Value | | Unit | Remarks |
|----------------------|-----------|-----|------------|--|
| | Min | Max | | |
| Read/Write Endurance | 10^{13} | — | Times/byte | Operation Ambient Temperature $T_A = +85^\circ\text{C}$ Total numbers of reading and writing |
| Data Retention | 10 | — | Years | Operation Ambient Temperature $T_A = +85^\circ\text{C}$ Retention time of the first reading/writing data right after shipment |

Note : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

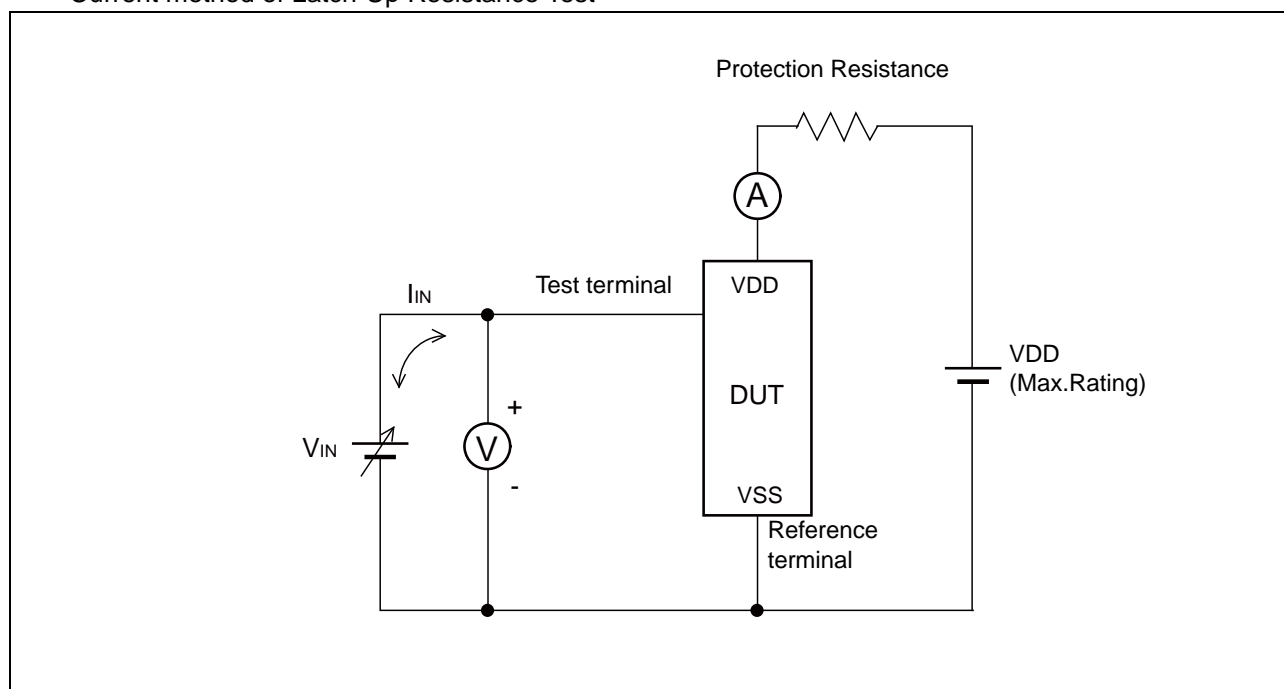
NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

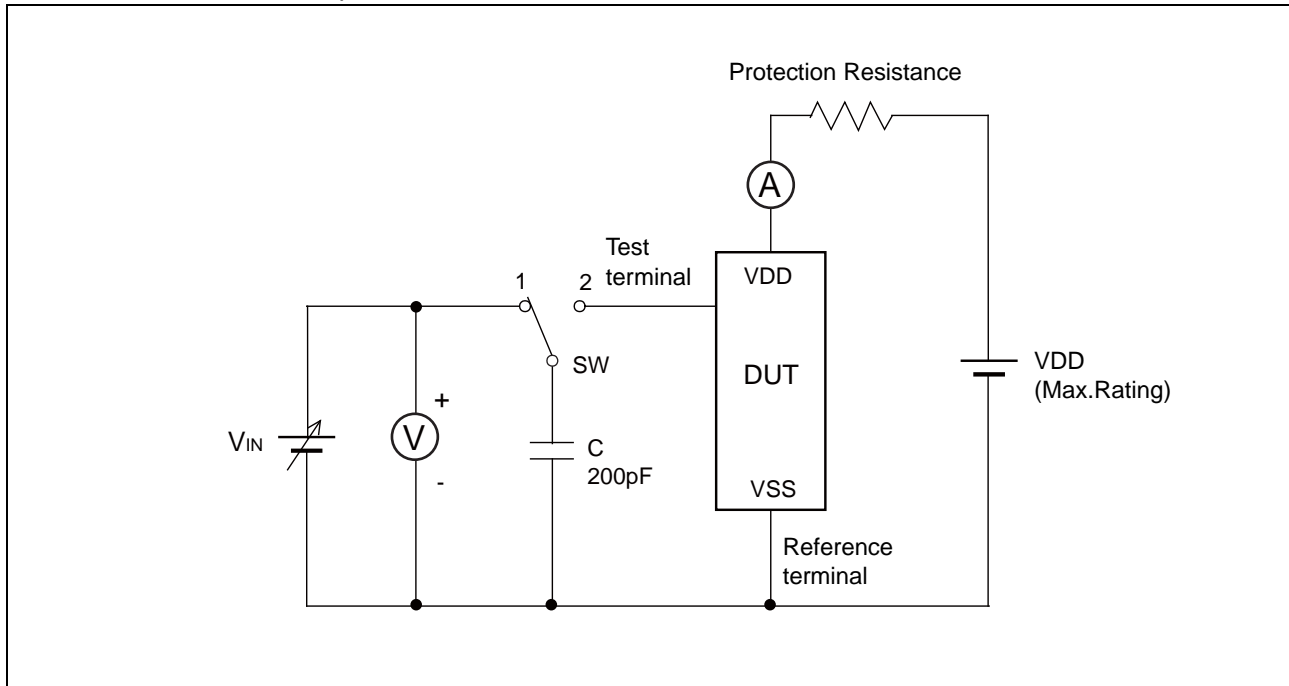
| Test | DUT | Value |
|--|--|-------|
| ESD HBM (Human Body Model) JESD22-A114 compliant | MB85RS2MTPF-G-JNE2 MB85RS2MTPH-G-JNE1 | — |
| ESD MM (Machine Model) JESD22-A115 compliant | | — |
| ESD CDM (Charged Device Model) JESD22-C101 compliant | | — |
| Latch-Up (I-test) JESD78 compliant | | — |
| Latch-Up (V_{supply} overvoltage test) JESD78 compliant | | — |
| Latch-Up (Current Method) Proprietary method | | — |
| Latch-Up (C-V Method) Proprietary method | | — |

• Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
 Confirm the latch up does not occur under $I_{IN} = \pm 300$ mA.
 In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

- C-V method of Latch-Up Resistance Test

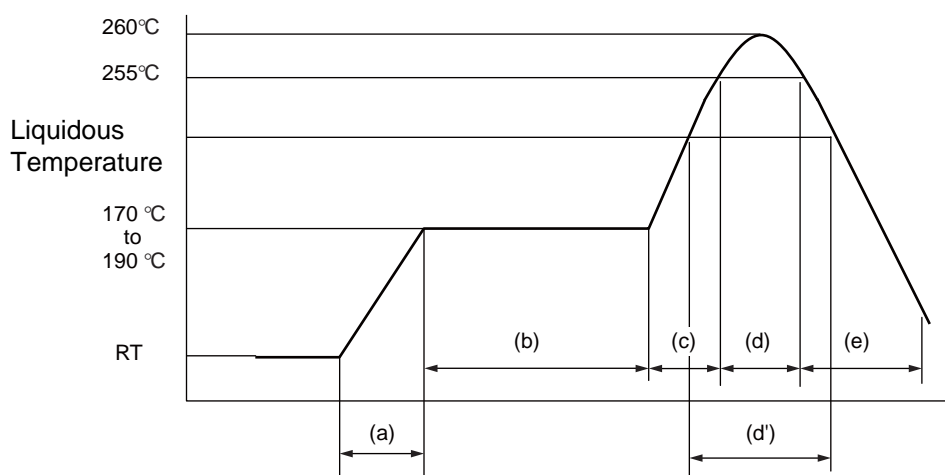


Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ MB85RS2MTPF (8-pin plastic SOP) REFLOW CONDITIONS AND FLOOR LIFE

| Item | Condition | |
|----------------------|---|--|
| Method | IR (infrared reflow) , Convection | |
| Times | 2 | |
| Floor life | Before unpacking | Please use within 2 years after production. |
| | From unpacking to 2nd reflow | Within 8 days |
| | In case over period of floor life | Baking with 125 °C+/-3 °C for 24hrs+2hrs/-0hrs is required. Then please use within 8 days. (Please remember baking is up to 2 times) |
| Floor life condition | Between 5 °C and 30 °C and also below 70%RH required. (It is preferred lower humidity in the required temp range.) | |

Reflow Profile



- (a) Average ramp-up rate : 1 °C/s to 4 °C/s
 (b) Preheat & Soak : 170 °C to 190 °C, 60 s to 180 s
 (c) Average ramp-up rate : 1 °C/s to 4 °C/s
 (d) Peak temperature : Temperature 260 °C Max; 255 °C within 10 s
 (d') Liquidous temperature : Up to 230 °C within 40 s or
 Up to 225 °C within 60 s or
 Up to 220 °C within 80 s
 (e) Cooling : Natural cooling or forced cooling

Note : Temperature on the top of the package body is measured.

■ RESTRICTED SUBSTANCES

This product complies with the regulation below (Based on current knowledge as of November 2011).

- EU RoHS Directive (2002/95/EC)
- China RoHS (Administration on the Control of Pollution Caused by Electronic Information Products
(电子信息产品污染控制管理办法))
- Vietnam RoHS (30/2011/TT-BCT)

Restricted substances in each regulation are as follows.

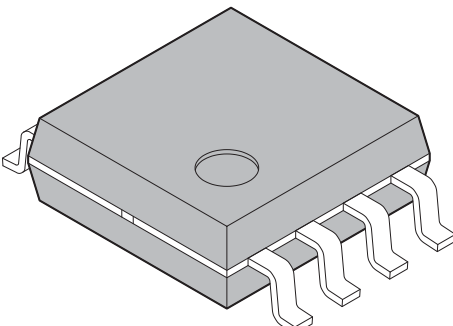
| Substances | Threshold | Contain status* |
|---------------------------------------|-----------|-----------------|
| Lead and its compounds | 1,000 ppm | ○ |
| Mercury and its compounds | 1,000 ppm | ○ |
| Cadmium and its compounds | 100 ppm | ○ |
| Hexavalent chromium compound | 1,000 ppm | ○ |
| Polybrominated biphenyls (PBB) | 1,000 ppm | ○ |
| Polybrominated diphenyl ethers (PBDE) | 1,000 ppm | ○ |

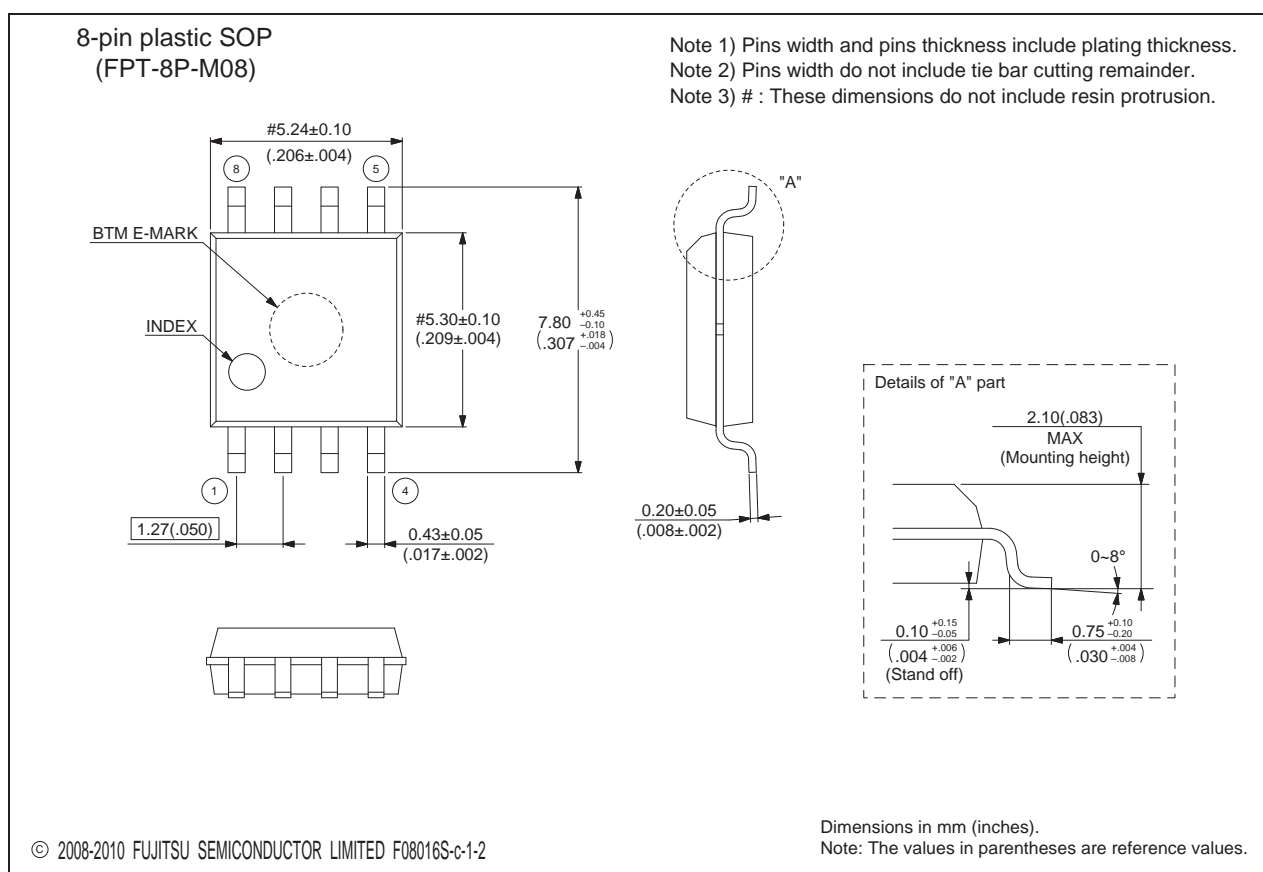
* : The mark of "○" shows below a threshold value.

■ ORDERING INFORMATION

| Part number | Package | Shipping form | Minimum shipping quantity |
|----------------------|-----------------------------------|-----------------------|---------------------------|
| MB85RS2MTPF-G-JNE2 | 8-pin plastic SOP (FPT-8P-M08) | Tube | 1 |
| MB85RS2MTPF-G-JNERE2 | 8-pin plastic SOP (FPT-8P-M08) | Embossed Carrier tape | 2000 |
| MB85RS2MTPH-G-JNE1 | 8-pin plastic DIP (DIP-8P-M03) | Tube | 1 |

■ PACKAGE DIMENSION

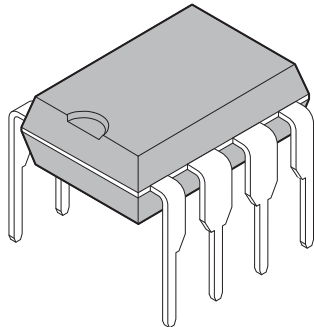
| | | |
|--|--------------------------------|-------------------|
|  <p>8-pin plastic SOP</p> <p>(FPT-8P-M08)</p> | Lead pitch | 1.27 mm |
| | Package width × package length | 5.30 mm × 5.24 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 2.10 mm Max |
| | | |

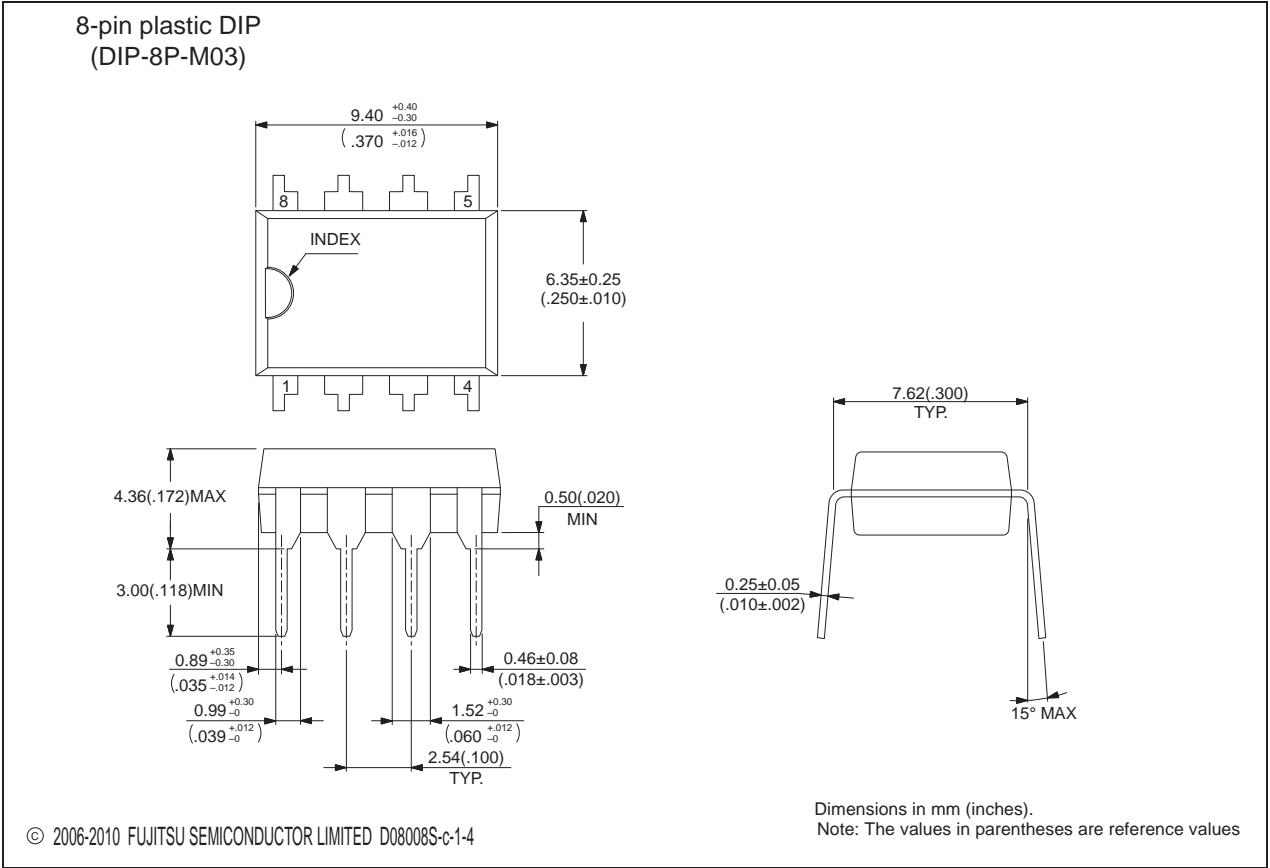


Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

(Continued)

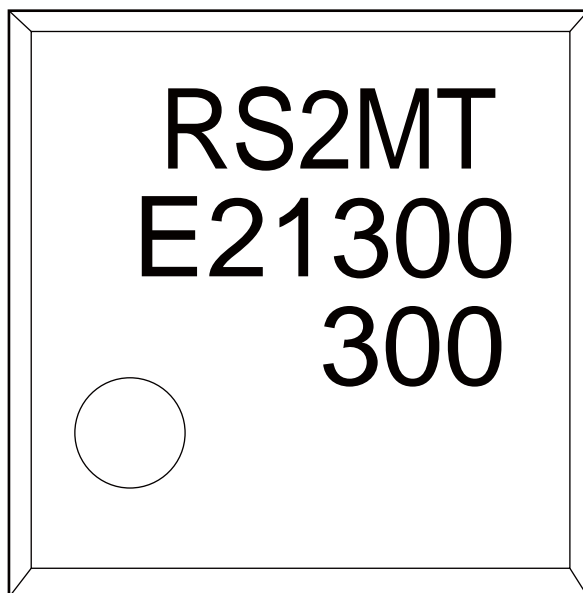
| | | |
|---|----------------|--------------|
| <div>8-pin plastic DIP</div> <div></div> <div>(DIP-8P-M03)</div> | Lead pitch | 2.54 mm |
| | Sealing method | Plastic mold |
| | | |
| | | |
| | | |
| | | |



Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

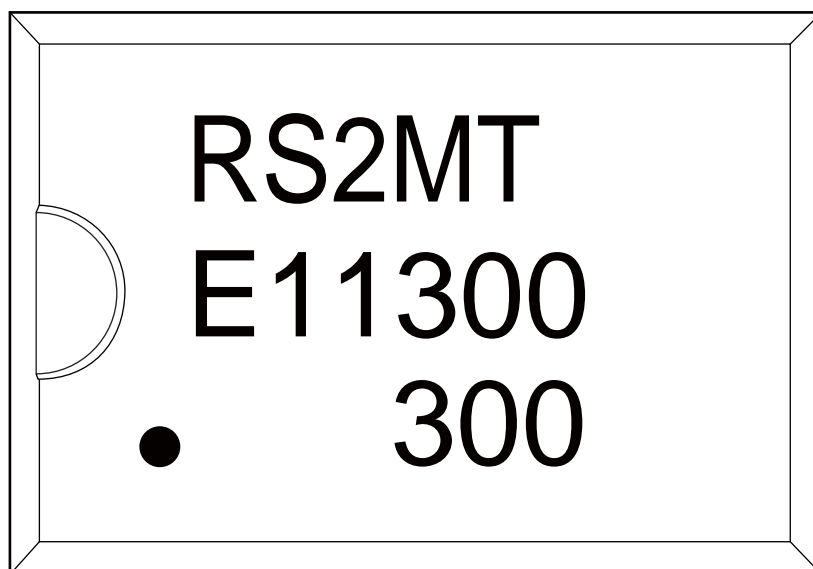
■ MARKING

[MB85RS2MTPF-G-JNE2]
[MB85RS2MTPF-G-JNERE2]



[FPT-08P-M08]

[MB85RS2MTPH-G-JNE1]



[DIP-08P-M03]

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://sg.fujitsu.com/semiconductor/>

Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

30F, Kerry Parkside, 1155 Fang Dian Road, Pudong District,
Shanghai 201204, China

Tel : +86-21-6146-3688 Fax : +86-21-6146-3660

<http://cn.fujitsu.com/fss/>

Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

2/F, Green 18 Building, Hong Kong Science Park,

Shatin, N.T., Hong Kong

Tel : +852-2736-3232 Fax : +852-2314-4207

<http://cn.fujitsu.com/fsp/>

All Rights Reserved.

FUJITSU SEMICONDUCTOR LIMITED, its subsidiaries and affiliates (collectively, "FUJITSU SEMICONDUCTOR") reserves the right to make changes to the information contained in this document without notice. Please contact your FUJITSU SEMICONDUCTOR sales representatives before order of FUJITSU SEMICONDUCTOR device.

Information contained in this document, such as descriptions of function and application circuit examples is presented solely for reference to examples of operations and uses of FUJITSU SEMICONDUCTOR device. FUJITSU SEMICONDUCTOR disclaims any and all warranties of any kind, whether express or implied, related to such information, including, without limitation, quality, accuracy, performance, proper operation of the device or non-infringement. If you develop equipment or product incorporating the FUJITSU SEMICONDUCTOR device based on such information, you must assume any responsibility or liability arising out of or in connection with such information or any use thereof. FUJITSU SEMICONDUCTOR assumes no responsibility or liability for any damages whatsoever arising out of or in connection with such information or any use thereof.

Nothing contained in this document shall be construed as granting or conferring any right under any patents, copyrights, or any other intellectual property rights of FUJITSU SEMICONDUCTOR or any third party by license or otherwise, express or implied.

FUJITSU SEMICONDUCTOR assumes no responsibility or liability for any infringement of any intellectual property rights or other rights of third parties resulting from or in connection with the information contained herein or use thereof.

The products described in this document are designed, developed and manufactured as contemplated for general use including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high levels of safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (including, without limitation, use in nuclear facility, aircraft flight control system, air traffic control system, mass transport control system, medical life support system and military application), or (2) for use requiring extremely high level of reliability (including, without limitation, submersible repeater and artificial satellite). FUJITSU SEMICONDUCTOR shall not be liable for you and/or any third party for any claims or damages arising out of or in connection with above-mentioned uses of the products.

Any semiconductor devices fail or malfunction with some probability. You are responsible for providing adequate designs and safeguards against injury, damage or loss from such failures or malfunctions, by incorporating safety design measures into your facility, equipments and products such as redundancy, fire protection, and prevention of overcurrent levels and other abnormal operating conditions.

The products and technical information described in this document are subject to the Foreign Exchange and Foreign Trade Control Law of Japan, and may be subject to export or import laws or regulations in U.S. or other countries. You are responsible for ensuring compliance with such laws and regulations relating to export or re-export of the products and technical information described herein. All company names, brand names and trademarks herein are property of their respective owners.

Edited: Sales Promotion Department