FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27254-3E

ASSP for Power Management Applications

2 ch DC/DC Converter IC Built-in Switching FET, Synchronous Rectification, and Down Conversion Support

MB39C015

■ DESCRIPTION

The MB39C015 is a current mode type 2-channel DC/DC converter IC built-in voltage detection, synchronous rectifier, and down conversion support. The device is integrated with a switching FET, oscillator, error amplifier, PWM control circuit, reference voltage source, and voltage detection circuit.
External inductor and decoupling capacitor are needed only for the external component.
As combining with external parts enables a DC/DC converter with a compact and high load response characteristic, this is suitable as the built-in power supply for such as mobile phone/PDA, DVDs, and HDDs.

■ FEATURES

- High efficiency : 96% (Max)
- Output current (DC/DC) : 800 mA/ch (Max)
- Input voltage range : 2.5 V to 5.5 V
- Operating frequency : 2.0 MHz (Typ)
- No flyback diode needed
- Low dropout operation : For 100% on duty
- Built-in high-precision reference voltage generator : 1.30 V ± 2%
- Consumption current in shutdown mode : 1 μA or less
- Built-in switching FET : P-ch MOS 0.3 Ω (Typ) N-ch MOS 0.2 Ω (Typ)
- High speed for input and load transient response in the current mode
- Over temperature protection
- Packaged in a compact package : QFN-24

■ APPLICATIONS

- Flash ROMs
- MP3 players
- Electronic dictionary devices
- Surveillance cameras
- Portable GPS navigators
- DVD drives
- IP phones
- Network hubs
- Mobile phones etc.

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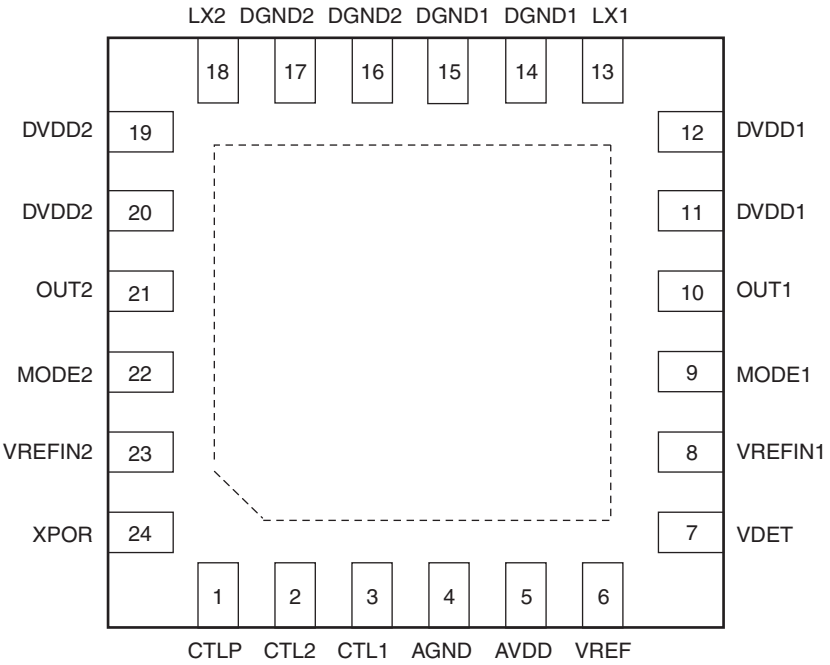
■ PIN ASSIGNMENT

(Top View)

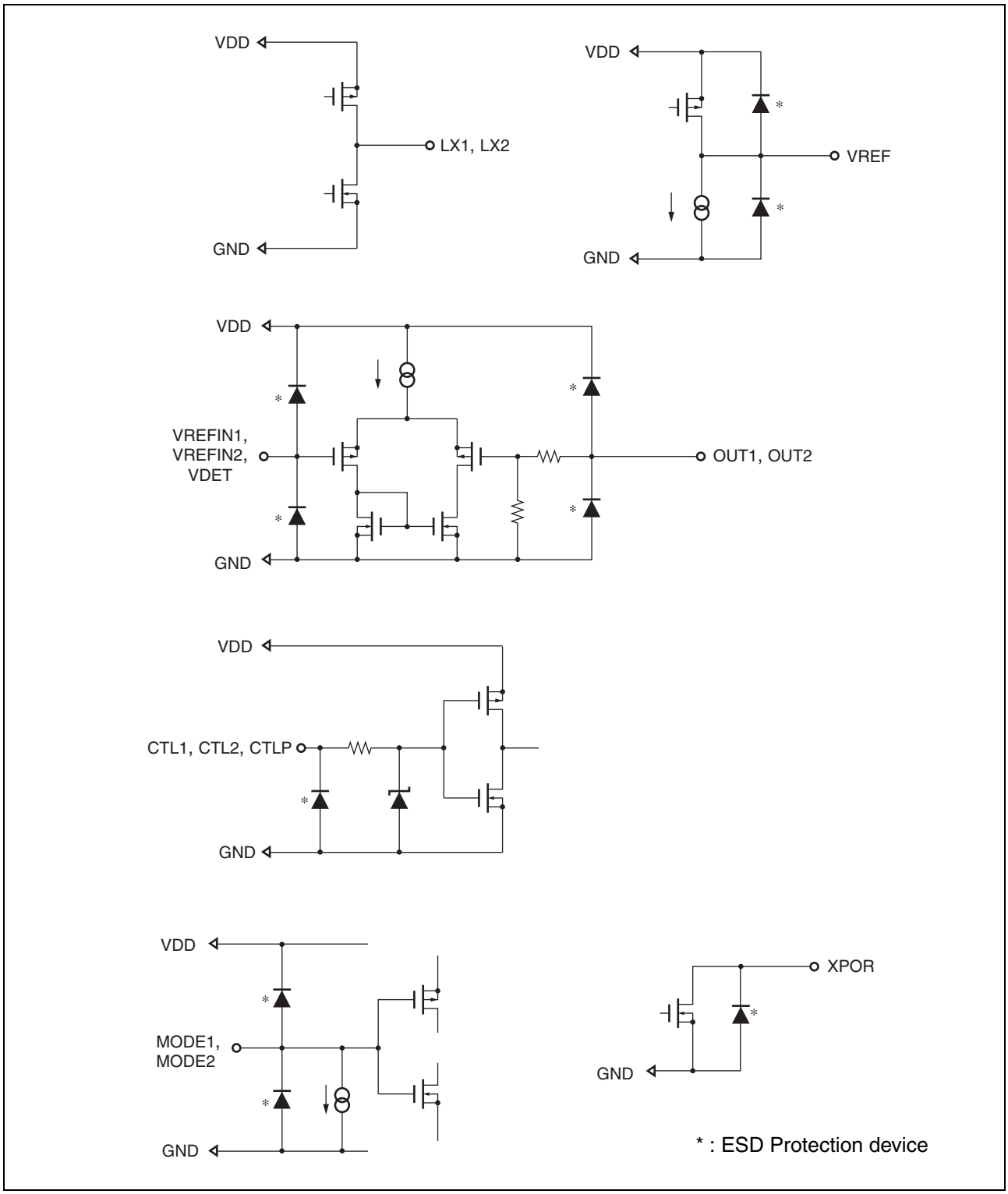


(LCC-24P-M10)

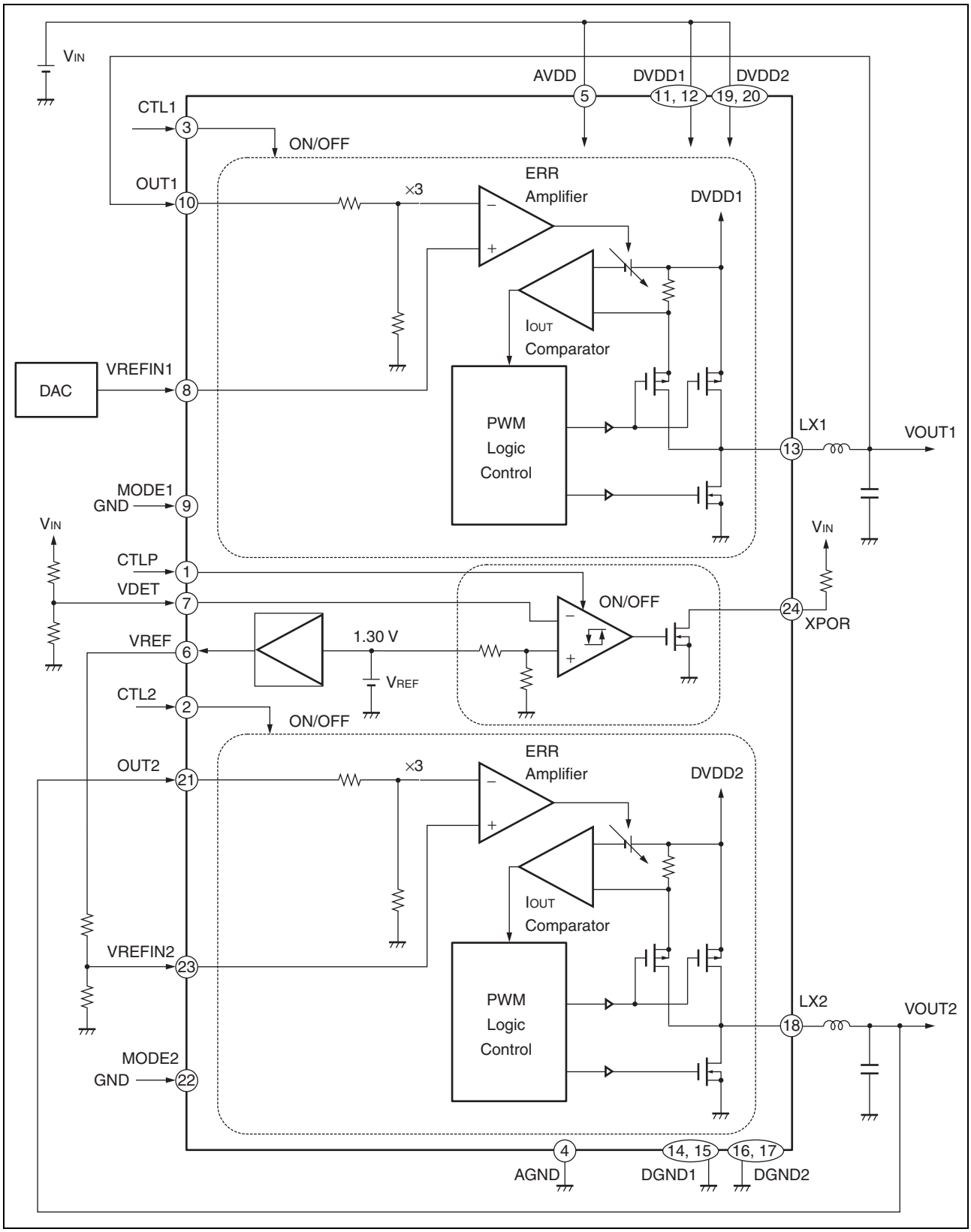
■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	CTLP	I	Voltage detection circuit block control input pin. (L : Voltage detection function stop, H : Normal operation)
2/3	CTL2/CTL1	I	DC/DC converter block control input pin. (L : Shut down, H : Normal operation)
4	AGND	—	Control block ground pin.
5	AVDD	—	Control block power supply pin.
6	VREF	O	Reference voltage output pin.
7	VDET	I	Voltage detection input pin.
8/23	VREFIN1/VREFIN2	I	Error amplifier (Error Amp) non-inverted input pin.
9/22	MODE1/MODE2	I	Use pin at L level or leave open.
10/21	OUT1/OUT2	I	Output voltage feedback pin.
11, 12/ 19, 20	DVDD1/DVDD2	—	Drive block power supply pin.
13/18	LX1/LX2	O	Inductor connection output pin. High impedance during shut down.
14, 15/ 16, 17	DGND1/DGND2	—	Drive block ground pin.
24	XPOR	O	VDET circuit output pin. Connected to an N-ch MOS open drain circuit.

■ I/O PIN EQUIVALENT CIRCUIT DIAGRAM



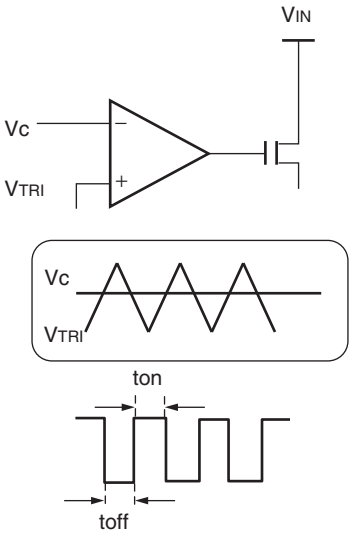
■ BLOCK DIAGRAM



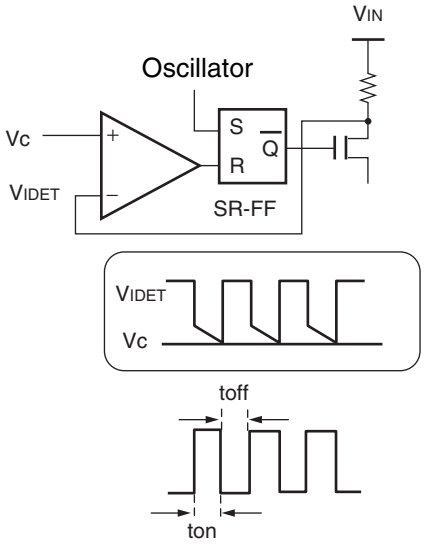
- **Current mode**
  - Original voltage mode type :
    Stabilize the output voltage by comparing two items below and on-duty control.
    - Voltage (V_C) obtained through negative feedback of the output voltage by Error Amp
    - Reference triangular wave (V_{TRI})

  - Current mode type :
    Instead of the triangular wave (V_{TRI}), the voltage (V_{IDET}) obtained through I-V conversion of the sum of currents that flow in the oscillator (rectangular wave generation circuit) and SW FET is used.
    Stabilize the output voltage by comparing two items below and on-duty control.
    - Voltage (V_C) obtained through negative feedback of the output voltage by Error Amp
    - Voltage (V_{IDET}) obtained through I-V conversion of the sum of current that flow in the oscillator (rectangular wave generation circuit) and SW FET

Voltage mode type model



Current mode type model



Note : The above models illustrate the general operation and an actual operation will be preferred in the IC.

■ FUNCTION OF EACH BLOCK

- PWM Logic control circuit

The built-in P-ch and N-ch MOS FETs are controlled for synchronization rectification according to the frequency (2.0 MHz) oscillated from the built-in oscillator (square wave oscillation circuit).

- I_{OUT} Comparator circuit

This circuit detects the current (I_{LX}) which flows to the external inductor from the built-in P-ch MOS FET. By comparing V_{IDET} obtained through I-V conversion of peak current I_{PK} of I_{LX} with the Error Amp output, the built-in P-ch MOS FET is turned off via the PWM Logic Control circuit.

- Error Amp phase compensation circuit

This circuit compares the output voltage to reference voltages such as VREF. This IC has a built-in phase compensation circuit that is designed to optimize the operation of this IC.
This needs neither to be considered nor addition of a phase compensation circuit and an external phase compensation device.

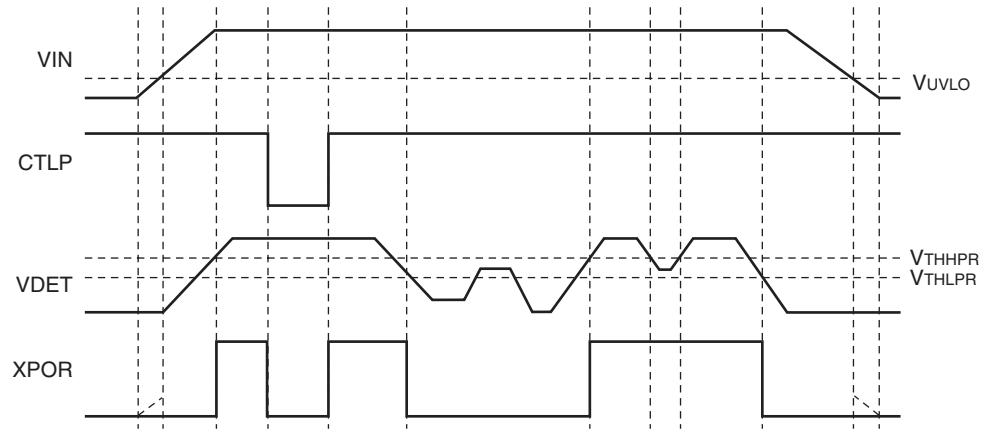
- VREF circuit

A high accuracy reference voltage is generated with BGR (bandgap reference) circuit. The output voltage is 1.30 V (Typ).

- Voltage Detection (VDET) circuit

The voltage detection circuit monitors the voltage at the VDET pin. Normally, use the XPOR pin through pull-up with an external resistor. When the V_{DET} pin voltage reaches 0.6 V, it reaches the H level.

Timing chart example : (XPOR pin pulled up to VIN)



V_{UVLO} : UVLO threshold voltage
V_{THHPR}, V_{THLPR} : XPOR threshold voltage

- Protection circuit

This IC has a built-in over-temperature protection circuit.
The over-temperature protection circuit turns off both N-ch and P-ch switching FETs when the junction temperature reaches + 135 °C. When the junction temperature comes down to + 110 °C, the switching FET is returned to the normal operation. Since the PWM control circuit of this IC is in the control method in current mode, the current peak value is also monitored and controlled as required.

• Function table

MODE	Input			Output			
	CTL1	CTL2	CTLP	CH1 function	CH2 function	VDET function	VREF function
Shutdown mode	L			Stopped			
Operating mode	H	L	L	Operation	Stopped	Stopped	Outputs 1.3 V
	L	H	L	Stopped	Operation	Stopped	
	L	L	H	Stopped	Stopped	Operation	
	H	H	L	Operation	Operation	Stopped	
	L	H	H	Stopped	Operation	Operation	
	H	L	H	Operation	Stopped	Operation	
	H			Operation			

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	AVDD = DVDD1 = DVDD2	−0.3	+6.0	V
Signal input voltage	V_{ISIG}	OUT1/OUT2 pins	−0.3	V_{DD} + 0.3	V
		CTLP, CTL1/CTL2, MODE1/MODE2 pins	−0.3	V_{DD} + 0.3	
		VREFIN1/VREFIN2 pins	−0.3	V_{DD} + 0.3	
		VDET pin	−0.3	V_{DD} + 0.3	
XPOR pull-up voltage	V_{IXPOR}	XPOR pin	−0.3	+6.0	V
LX voltage	V_{LX}	LX1/LX2 pins	−0.3	V_{DD} + 0.3	V
LX Peak current	I_{PK}	I_{LX1}/I_{LX2}	—	1.8	A
Power dissipation	P_D	Ta ≤ +25 °C	—	3125*1, *2, *3	mW
			—	1563*1, *2, *4	
		Ta = +85 °C	—	1250*1, *2, *3	mW
			—	625*1, *2, *4	
Operating ambient temperature	Ta	—	−40	+85	°C
Storage temperature	T_{STG}	—	−55	+125	°C

*1 : Power dissipation value between + 25 °C and + 85 °C is obtained by connecting these two points with straight line.

*2 : When mounted on a four-layer epoxy board of 11.7 cm × 8.4 cm

*3 : Connection at exposure pad with thermal via. (Thermal via 9 holes)

*4 : Connection at exposure pad, without a thermal via.

Notes: • The use of negative voltages below − 0.3 V to the AGND, DGND1, and DGND2 pin may create parasitic transistors on LSI lines, which can cause abnormal operation.
• This device can be damaged if the LX1 pin and LX2 pin are short-circuited to AVDD and DVDD1/DVDD2, or AGND and DGND1/DGND2.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	AVDD = DVDD1 = DVDD2	2.5	3.7	5.5	V
VREFIN voltage	V_{REFIN}	—	0.15	—	1.30	V
CTL voltage	V_{CTL}	CTLP, CTL1, CTL2	0	—	5.0	V
LX current	I_{LX}	I_{LX1}/I_{LX2}	—	—	800	mA
VREF output current	I_{ROUT}	2.5 V ≤ AVDD = DVDD1 = DVDD2 < 3.0 V	—	—	0.5	mA
		3.0 V ≤ AVDD = DVDD1 = DVDD2 ≤ 5.5 V	—	—	1	
XPOR current	I_{POR}	—	—	—	1	mA
Inductor value	L	—	—	2.2	—	µH

Note : The output current from this device has a situation to decrease if the power supply voltage (V_{IN}) and the DC/DC converter output voltage (V_{OUT}) differ only by a small amount. This is a result of slope compensation and will not damage this device.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, AVDD = DVDD1 = DVDD2 = 3.7 V, VOUT1/VOUT2 setting value = 2.5 V, MODE1/MODE2 = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
DC/DC converter block	Input current	I_{REFIN}	8, 23	VREFIN = 0.15 V to 1.3 V	− 100	0	+ 100	nA
	Output voltage	V_{OUT}	10, 21	VREFIN = 0.833 V, OUT = −100 mA	2.45	2.50	2.55	V
	Input stability	LINE		2.5 V ≤ AVDD = DVDD1 = DVDD2 ≤ 5.5 V*1	—	—	10	mV
	Load stability	LOAD		−100 mA ≥ OUT ≥ −800 mA	—	—	10	mV
	OUT pin input impedance	R_{OUT}		OUT = 2.0 V	0.6	1.0	1.5	MΩ
	LX Peak current	I_{PK}	13, 18	Output shorted to GND	0.9	1.2	1.7	A
	Oscillation frequency	fosc		—	1.6	2.0	2.4	MHz
	Rise delay time	t_{PG}	2, 3, 10, 21	C1/C2 = 4.7 µF, OUT = 0 A, OUT1/OUT2 : 0 → 90% V_{OUT}	—	45	80	µs
	SW NMOS-FET OFF voltage	V_{NOFF}	13, 18	—	—	− 10*	—	mV
	SW PMOS-FET ON resistance	R_{ONP}		LX1/LX2 = −100 mA	—	0.30	0.48	Ω
	SW NMOS-FET ON resistance	R_{ONN}		LX1/LX2 = −100 mA	—	0.20	0.42	Ω
	LX leak current	I_{LEAKM}		0 ≤ LX ≤ VDD*2	− 1.0	—	+ 8.0	µA
		I_{LEAKH}		VDD = 5.5 V, 0 ≤ LX ≤ VDD*2	− 2.0	—	+ 16.0	µA
Protection circuit block	Overheating protection (Junction Temp.)	T_{OTPH}	—	—	+ 120*	+ 135*	+ 160*	°C
		T_{OTPL}			+ 95*	+ 110*	+ 125*	°C
	UVLO threshold voltage	V_{THHUV}	5, 11, 12, 19, 20	—	2.17	2.30	2.43	V
		V_{THLUV}			2.03	2.15	2.27	V
	UVLO hysteresis width	V_{HYSUV}		—	0.08	0.15	0.25	V
Voltage detection circuit block	XPOR threshold voltage	V_{THHPR}	7	—	575	600	625	mV
		V_{THLPR}			558	583	608	mV
	XPOR hysteresis width	V_{HYSPR}		—	—	17	—	mV
	XPOR output voltage	V_{OL}	24	XPOR = 25 µA	—	—	0.1	V
	XPOR output current	I_{OH}		XPOR = 5.5 V	—	—	1.0	µA

* : Standard design value

(Continued)

(Continued)
(Ta = +25 °C, AVDD = DVDD1 = DVDD2 = 3.7 V, VOUT1/VOUT2 setting value = 2.5 V, MODE1/MODE2 = 0 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Control block	CTL threshold voltage	V_{THHCT}	1, 2, 3	—	0.55	0.95	1.45	V
		V_{THLCT}		—	0.40	0.80	1.30	V
	CTL pin input current	I_{ICTL}		0 V ≤ CTLP/CTL1/CTL2 ≤ 3.7 V	—	—	1.0	µA
Reference voltage block	VREF voltage	V_{REF}	6	VREF = 0 mA	1.274	1.300	1.326	V
	VREF Load stability	L_{OADREF}		VREF = –1.0 mA	—	—	20	mV
General	Shut down power supply current	I_{VDD1}	5, 11, 12, 19, 20	CTLP/CTL1/CTL2 = 0 V State of all circuits OFF*3	—	—	1.0	µA
		I_{VDD1H}		CTLP/CTL1/CTL2 = 0 V, VDD = 5.5 V State of all circuits OFF*3	—	—	1.0	µA
	Power supply current (DC/DC mode)	I_{VDD31}		1. CTLP = 0 V, CTL1 = 3.7 V, CTL2 = 0 V 2. CTLP = 0 V, CTL1 = 0 V, CTL2 = 3.7 V OUT = 0 A	—	3.5	10	mA
		I_{VDD32}		CTLP = 0 V, CTL1/CTL2 = 3.7 V, OUT = 0 A	—	7.0	20.0	mA
	Power supply current (voltage detection mode)	I_{VDD5}		CTLP = 3.7 V, CTL1/CTL2 = 0 V,	—	15	24	µA
	Power-on invalid current	I_{VDD}		1. CTL1 = 3.7 V, CTL2 = 0 V 2. CTL1 = 0 V, CTL2 = 3.7 V VOUT1/VOUT2 = 90% OUT = 0 A*4	—	1000	2000	µA

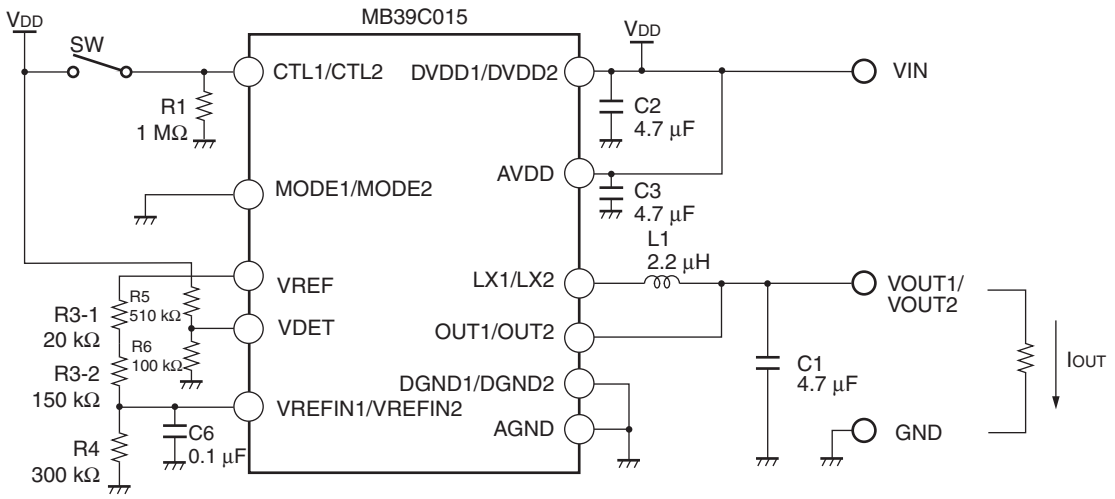
*1 : The minimum value of AVDD = DVDD1 = DVDD2 is the 2.5 V or VOUT setting value + 0.6 V, whichever is higher.

*2 : The + leak at the LX1 pin and LX2 pin includes the current of the internal circuit.

*3 : Sum of the current flowing into the AVDD, the DVDD1, and the DVDD2 pins.

*4 : Current consumption based on 100% ON-duty (High side FET in full ON state). The SW FET gate drive current is not included because the device is in full ON state (no switching operation). Also the load current is not included.

■ TEST CIRCUIT FOR MEASURING TYPICAL OPERATING CHARACTERISTICS



Output voltage = VREFIN × 3.01

Component	Specification	Vendor	Part Number	Remarks
R1	1 MΩ	KOA	RK73G1JTTD D 1 MΩ	
R3-1 R3-2	20 kΩ 150 kΩ	SSM SSM	RR0816-203-D RR0816-154-D	VOUT1/VOUT2 = 2.5 V Setting
R4	300 kΩ	SSM	RR0816-304-D	
R5	510 kΩ	KOA	RK73G1JTTD D 510 kΩ	
R6	100 kΩ	SSM	RR0816-104-D	
C1	4.7 µF	TDK	C2012JB1A475K	
C2	4.7 µF	TDK	C2012JB1A475K	
C3	0.1 µF	TDK	C1608JB1E104K	
C6	0.1 µF	TDK	C1608JB1H104K	For adjusting slow start time
L1	2.2 µH	TDK	VLF4012AT-2R2M	

Note : These components are recommended based on the operating tests authorized.

TDK : TDK Corporation

SSM : SUSUMU Co., Ltd

KOA : KOA Corporation

■ APPLICATION NOTES

[1] Selection of components

- **Selection of an external inductor**

Basically it dose not need to design inductor. This IC is designed to operate efficiently with a 2.2 μH inductor.

The inductor should be rated for a saturation current higher than the LX peak current value during normal operating conditions, and should have a minimal DC resistance. (100 mΩ or less is recommended.)

LX peak current value I_{PK} is obtained by the following formula.

$$I_{PK} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{fosc} \times \frac{1}{2} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}}$$

L : External inductor value

I_{OUT} : Load current

V_{IN} : Power supply voltage

V_{OUT} : Output setting voltage

D : ON-duty to be switched (= V_{OUT}/V_{IN})

fosc : Switching frequency (2.0 MHz)

ex) When V_{IN} = 3.7 V, V_{OUT} = 2.5 V, I_{OUT} = 0.8 A, L = 2.2 μH, fosc = 2.0 MHz
The maximum peak current value I_{PK};

$$I_{PK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times fosc \times V_{IN}} = 0.8\ A + \frac{(3.7\ V - 2.5\ V) \times 2.5\ V}{2 \times 2.2\ \mu H \times 2.0\ MHz \times 3.7\ V} \fallingdotseq 0.89\ A$$

- **I/O capacitor selection**
- Select a low equivalent series resistance (ESR) for the VDD input capacitor to suppress dissipation from ripple currents.

- Also select a low equivalent series resistance (ESR) for the output capacitor. The variation in the inductor current causes ripple currents on the output capacitor which, in turn, causes ripple voltages an output equal to the amount of variation multiplied by the ESR value. The output capacitor value has a significant impact on the operating stability of the device when used as a DC/DC converter. Therefore, FUJITSU SEMICONDUCTOR generally recommends a 4.7 μF capacitor, or a larger capacitor value can be used if ripple voltages are not suitable. If the V_{IN}/V_{OUT} voltage difference is within 0.6 V, the use of a 10 μF output capacitor value is recommended.

- Types of capacitors
  Ceramic capacitors are effective for reducing the ESR and afford smaller DC/DC converter circuit. However, power supply functions as a heat generator, therefore avoid to use capacitor with the F-temperature rating (− 80% to + 20%) . FUJITSU SEMICONDUCTOR recommends capacitors with the B-temperature rating (± 10% to ± 20%).
  Normal electrolytic capacitors are not recommended due to their high ESR.
  Tantalum capacitor will reduce ESR, however, it is dangerous to use because it turns into short mode when damaged. If you insist on using a tantalum capacitor, FUJITSU SEMICONDUCTOR recommends the type with an internal fuse.

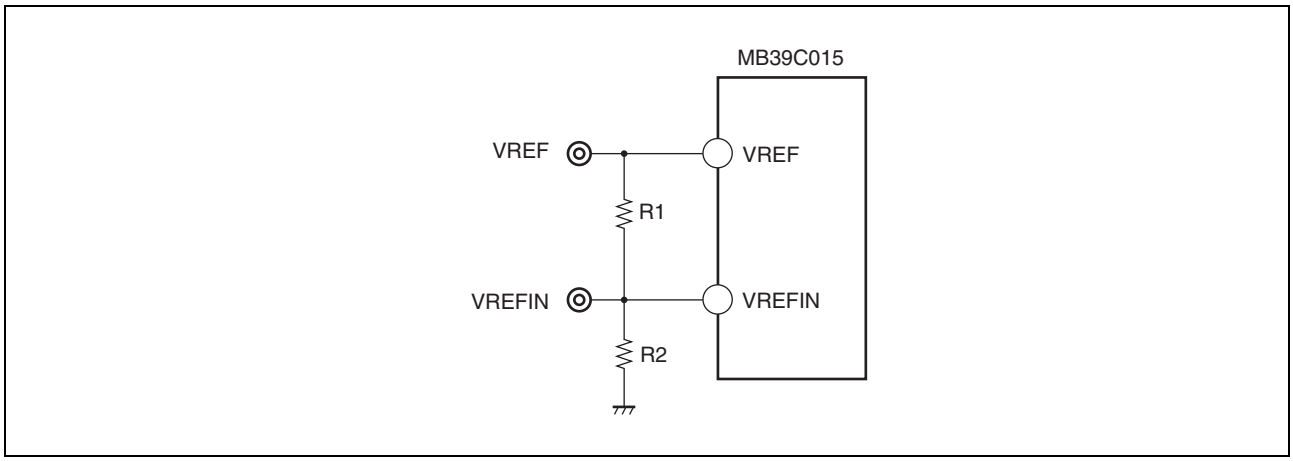
[2] Output voltage setting

The output voltage V_{OUT} (V_{OUT1} or V_{OUT2}) of this IC is defined by the voltage input to VREFIN (VREFIN1 or VREFIN2) . Supply the voltage for inputting to VREFIN from an external power supply, or set the VREF output by dividing it with resistors.

The output voltage when the VREFIN voltage is set by dividing the VREF voltage with resistors is shown in the following formula.

$$V_{OUT} = 3.01 \times V_{REFIN}, \quad V_{REFIN} = \frac{R2}{R1 + R2} \times V_{REF}$$

(V_{REF} = 1.30 V)



Note : Refer to "■ APPLICATION CIRCUIT EXAMPLES" for the an example of this circuit.

Although the output voltage is defined according to the dividing ratio of resistance, select the resistance value so that the current flowing through the resistance does not exceed the VREF current rating (1 mA) .

[3] About conversion efficiency

The conversion efficiency can be improved by reducing the loss of the DC/DC converter circuit.

The total loss (P_{LOSS}) of the DC/DC converter is roughly divided as follows :

$$P_{LOSS} = P_{CONT} + P_{SW} + P_C$$

P_{CONT} : Control system circuit loss (The power used for this IC to operate, including the gate driving power for internal SW FETs)

P_{SW} : Switching loss (The loss caused during switching of the IC's internal SW FETs)

P_C : Continuity loss (The loss caused when currents flow through the IC's internal SW FETs and external circuits)

The IC's control circuit loss (P_{CONT}) is extremely small, less than 100 mW (with no load).

As the IC contains FETs which can switch faster with less power, the continuity loss (P_C) is more predominant as the loss during heavy-load operation than the control circuit loss (P_{CONT}) and switching loss (P_{SW}) .

Furthermore, the continuity loss (P_C) is divided roughly into the loss by internal SW FET ON-resistance and by external inductor series resistance.

$$P_C = I_{OUT}^2 \times (RDC + D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle (= V_{OUT} / V_{IN})

R_{ONP} : Internal P-ch SW FET ON resistance

R_{ONN} : Internal N-ch SW FET ON resistance

RDC : External inductor series resistance

I_{OUT} : Load current

The above formula indicates that it is important to reduce RDC as much as possible to improve efficiency by selecting components.

[4] Power dissipation and heat considerations

The IC is so efficient that no consideration is required in most cases. However, if the IC is used at a low power supply voltage, heavy load, high output voltage, or high temperature, it requires further consideration for higher efficiency.

The internal loss (P) is roughly obtained from the following formula :

$$P = I_{OUT}^2 \times (D \times R_{ONP} + (1 - D) \times R_{ONN})$$

D : Switching ON-duty cycle ($= V_{OUT} / V_{IN}$)

R_{ONP} : Internal P-ch SW FET ON resistance

R_{ONN} : Internal N-ch SW FET ON resistance

I_{OUT} : Output current

The loss expressed by the above formula is mainly continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

In this IC with R_{ONP} greater than R_{ONN}, the larger the on-duty cycle, the greater the loss.

When assuming $V_{IN} = 3.7$ V, Ta $= +70$ °C, for example, $R_{ONP} = 0.36\ \Omega$ and $R_{ONN} = 0.30\ \Omega$ according to the graph “MOS FET ON resistance vs. Operating ambient temperature”. The IC's internal loss P is 123 mW at $V_{OUT} = 2.5$ V and $I_{OUT} = 0.6$ A. According to the graph “Power dissipation vs. Operating ambient temperature”, the power dissipation at an operating ambient temperature Ta of $+70$ °C is 300 mW and the internal loss is smaller than the power dissipation.

[5] XPOR threshold voltage setting [V_{PORH}, V_{PORL}]

Set the detection voltage by applying voltage to the VDET pin via an external resistor calculated according to this formula.

$$V_{PORH} = \frac{R3 + R4}{R4} \times V_{THHPR}$$

$$V_{PORL} = \frac{R3 + R4}{R4} \times V_{THLPR}$$

$V_{THHPR} = 0.600$ V

$V_{THLPR} = 0.583$ V

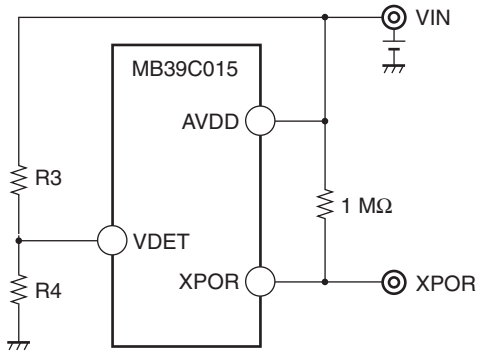
Example for setting detection voltage to 3.7 V

R3 = 510 kΩ

R4 = 100 kΩ

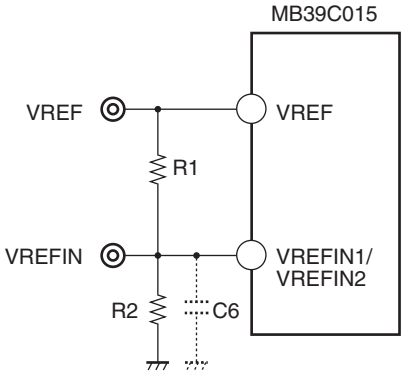
$$V_{PORH} = \frac{510\ k\Omega + 100\ k\Omega}{100\ k\Omega} \times 0.600 = 3.66 \div 3.7\ [V]$$

$$V_{PORL} = \frac{510\ k\Omega + 100\ k\Omega}{100\ k\Omega} \times 0.583 = 3.56 \div 3.6\ [V]$$



[6] Transient response

Normally, I_{OUT} is suddenly changed while V_{IN} and V_{OUT} are maintained constant, responsiveness including the response time and overshoot/undershoot voltage is checked. As this IC has built-in Error Amp with an optimized design, it shows good transient response characteristics. However, if ringing upon sudden change of the load is high due to the operating conditions, add capacitor C6 (e.g. 0.1 μF). (Since this capacitor C6 changes the start time, check the start waveform as well.) This action is not required for DAC input.

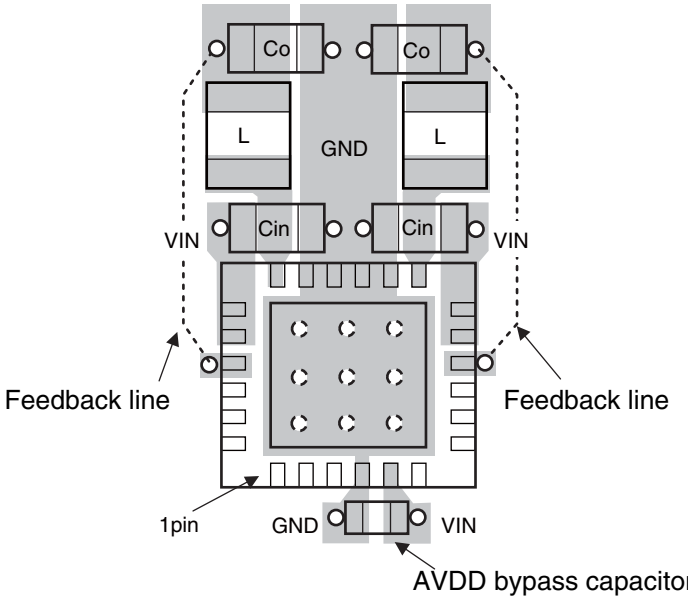


[7] Board layout, design example

The board layout needs to be designed to ensure the stable operation of this IC.
Follow the procedure below for designing the layout.

- Arrange the input capacitor (Cin) as close as possible to both the VDD and GND pins. Make a through hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- Large AC currents flow between this IC and the input capacitor (Cin), output capacitor (Co), and external inductor (L). Group these components as close as possible to this IC to reduce the overall loop area occupied by this group. Also try to mount these components on the same surface and arrange wiring without through hole wiring. Use thick, short, and straight routes to wire the net (The layout by planes is recommended.).
- Arrange a bypass capacitor for AVDD as close as possible to both the AVDD and AGND pins. Make a through hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- The feedback wiring to the OUT should be wired from the voltage output pin closest to the output capacitor (Co). The OUT pin is extremely sensitive and should thus be kept wired away from the LX1 and pin LX2 pin of this IC as far as possible.
- If applying voltage to the VREFIN1/VREFIN2 pins through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange them so that the GND pin of VREFIN1/VREFIN2 resistor is close to the IC's AGND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current. If installing a bypass capacitor for the VREFIN, put it close to the VREFIN pin.
- If applying voltage to the VDET pin through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange so that the GND pin of the VDET resistor is close to the IC's AGND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current.
- Try to make a GND plane on the surface to which this IC will be mounted. For efficient heat dissipation when using the QFN-24 package, FUJITSU SEMICONDUCTOR recommends providing a thermal via in the footprint of the thermal pad.

• Example of arranging IC SW system parts



• Notes for circuit design

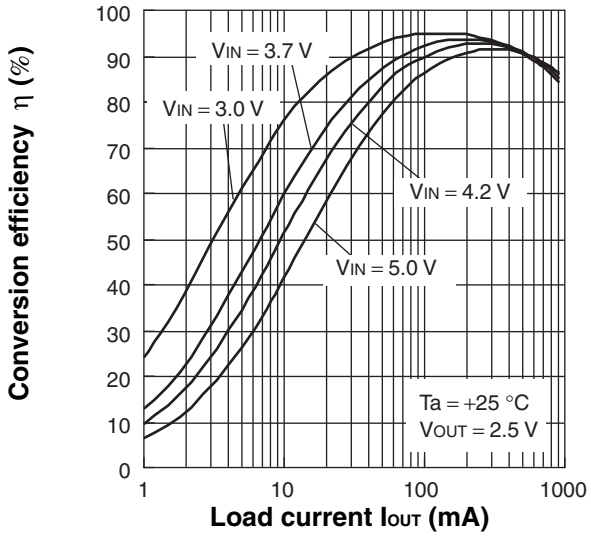
The switching operation of this IC works by monitoring and controlling the peak current which, incidentally, serves as a form of short-circuit protection. However, do not leave the output short-circuited for long periods of time. If the output is short-circuited where V_{IN} < 2.9 V, the current limit value (peak current to the inductor) tends to rise. Leaving in the short-circuit state, the temperature of this IC will continue rising and activate the thermal protection.
Once the thermal protection stops the output, the temperature of the IC will go down and operation will be restarted, after which the output will repeat the starting and stopping.
Although this effect will not destroy the IC, the thermal exposure to the IC over prolonged hours may affect the peripherals surrounding it.

■ EXAMPLE OF STANDARD OPERATION CHARACTERISTICS

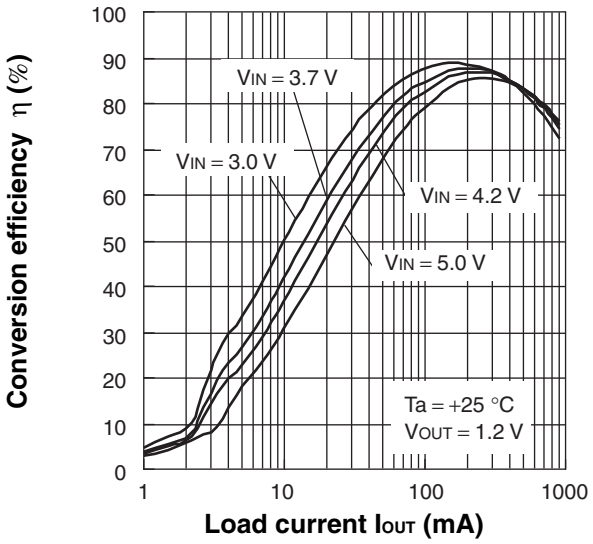
(Shown below is an example of characteristics for connection according to "■ TEST CIRCUIT FOR MEASURING TYPICAL OPERATING CHARACTERISTICS".)

• Characteristics CH1

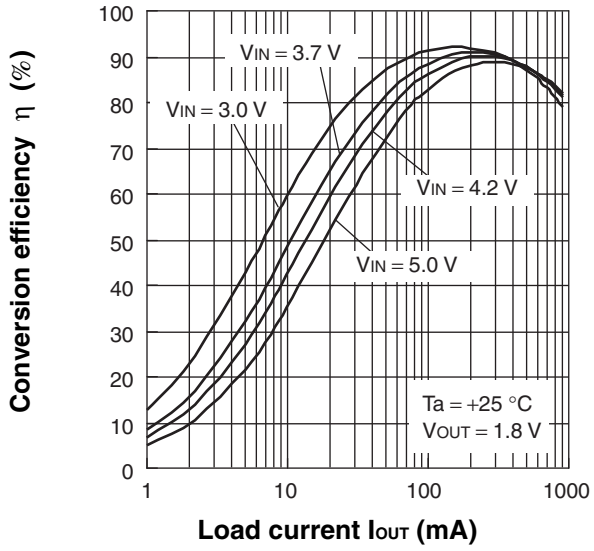
Conversion efficiency vs. Load current



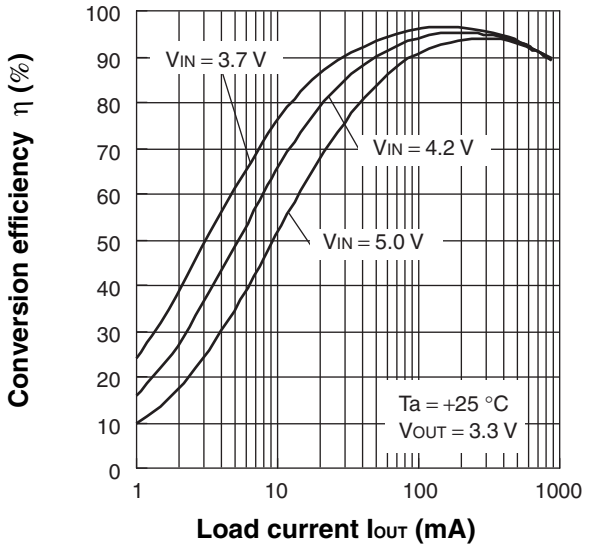
Conversion efficiency vs. Load current



Conversion efficiency vs. Load current



Conversion efficiency vs. Load current



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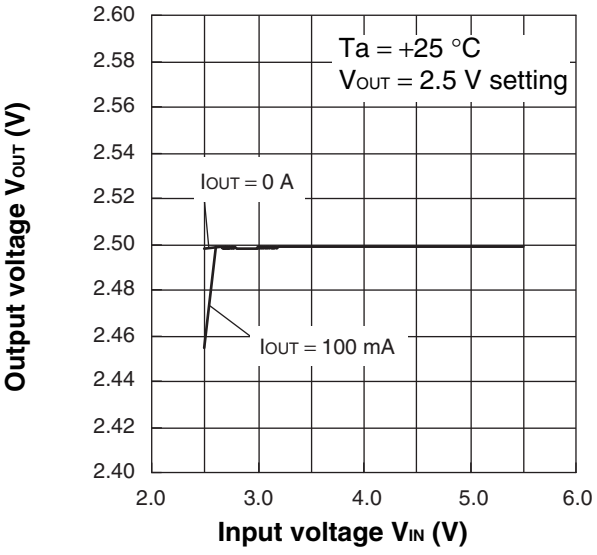
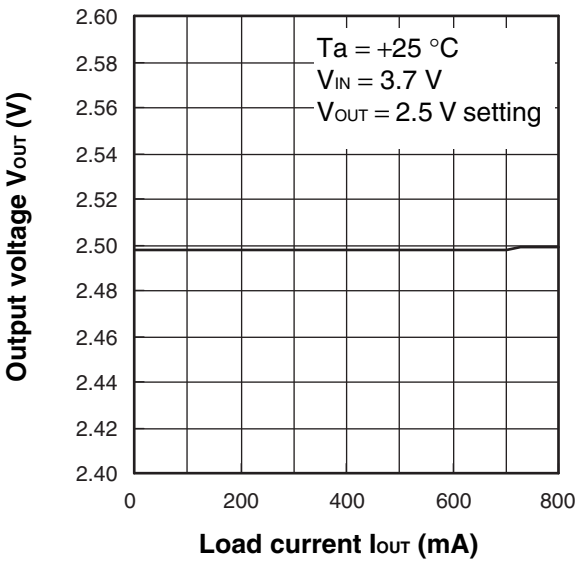
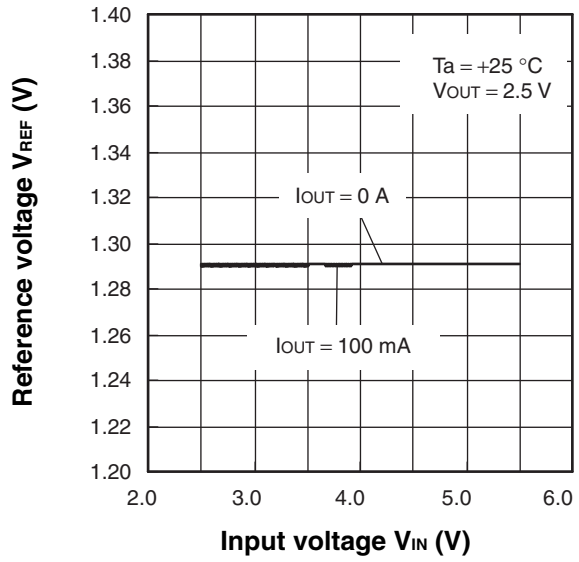
Output voltage vs. Input voltage



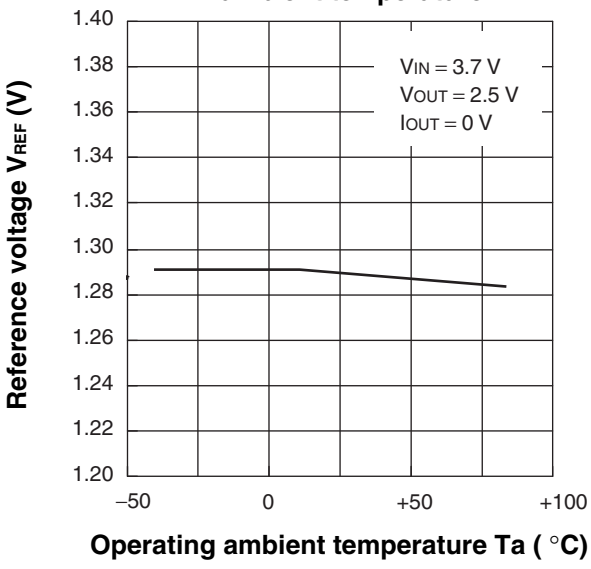
Output voltage vs. Load current



Reference voltage vs. Input voltage



Reference voltage vs. Operating ambient temperature



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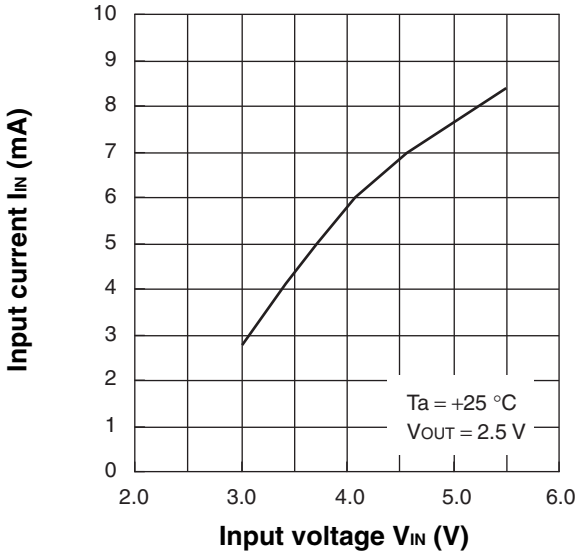
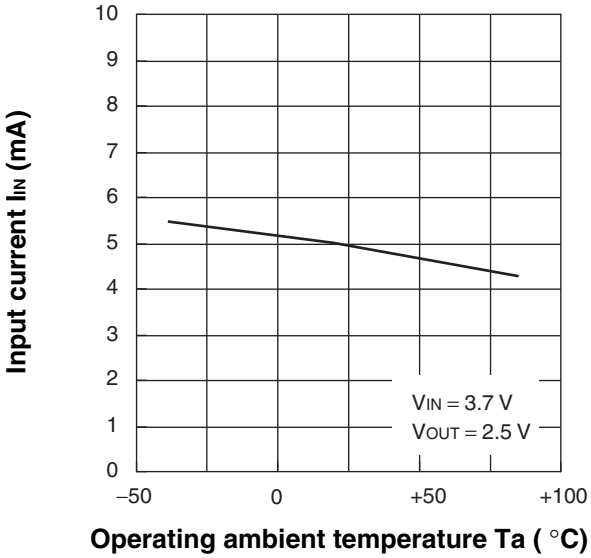
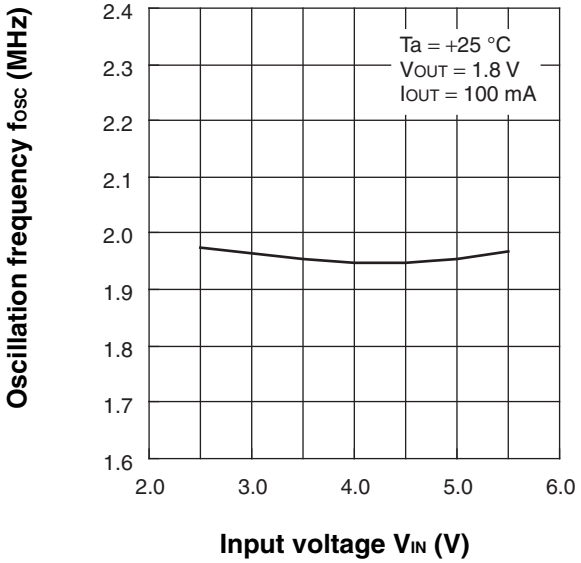
Input current vs. Input voltage



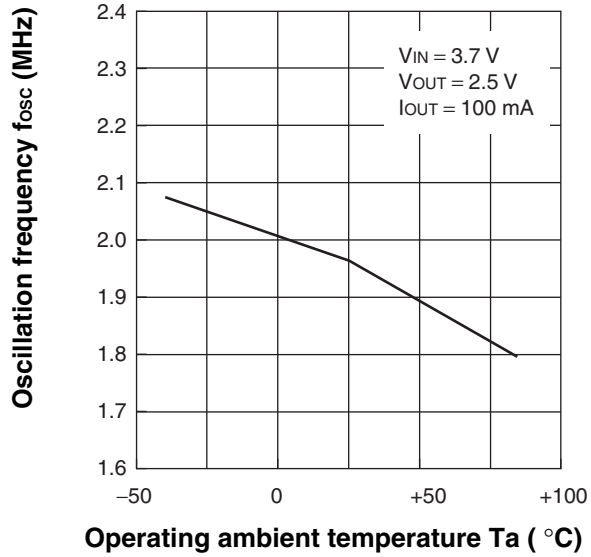
Input current vs. Operating ambient temperature



Oscillation frequency vs. Input voltage



Oscillation frequency vs. Operating ambient temperature



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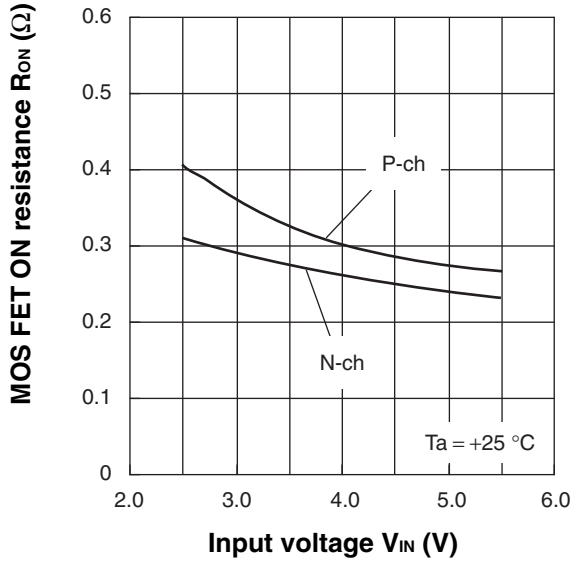
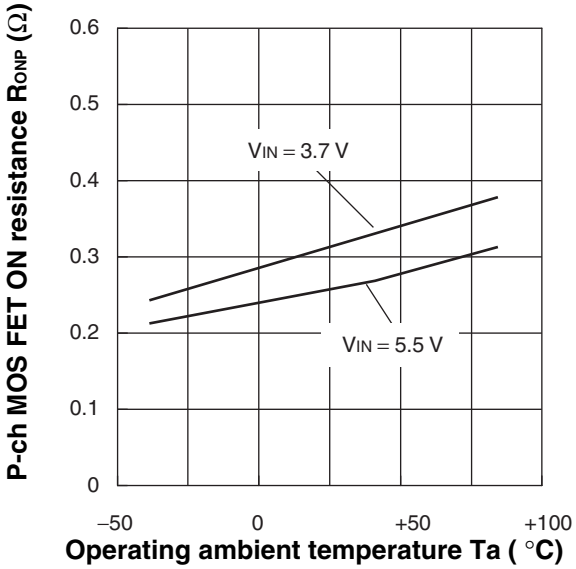
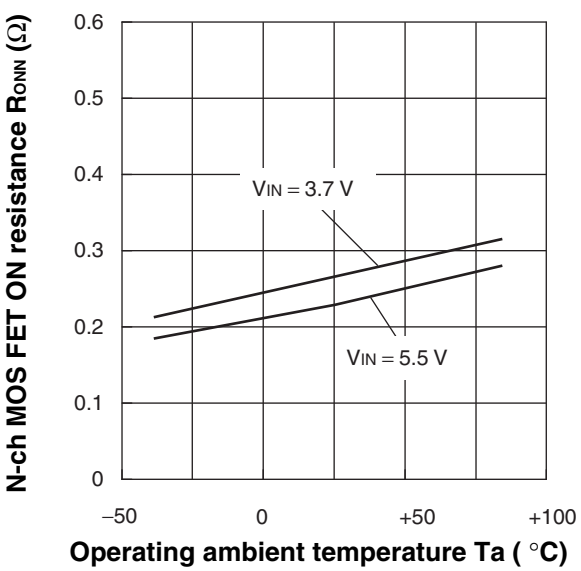
MOS FET ON resistance vs. Input voltage



P-ch MOS FET ON resistance vs. Operating ambient temperature



N-ch MOS FET ON resistance vs. Operating ambient temperature



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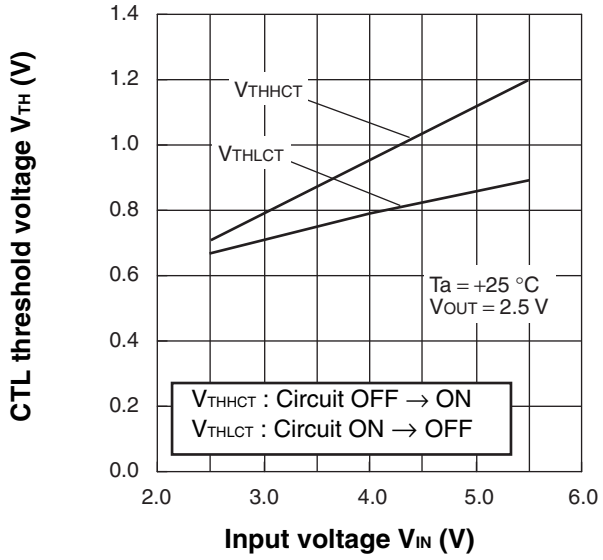
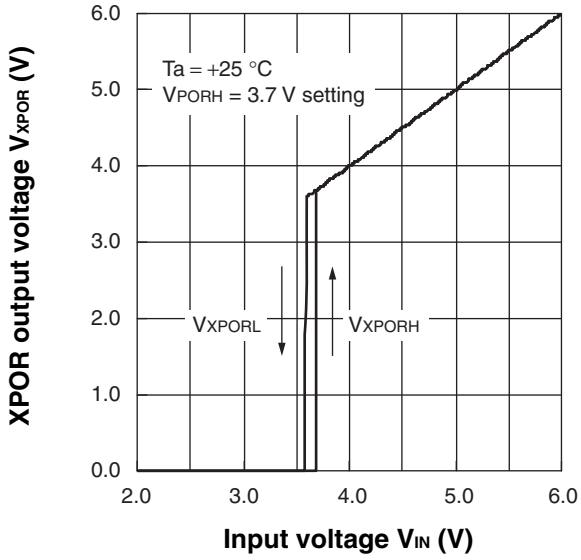
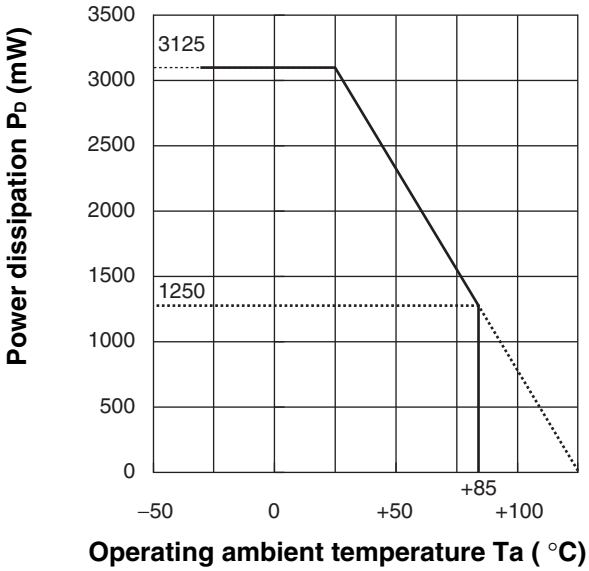
CTL threshold voltage V_{TH} vs. Input voltage



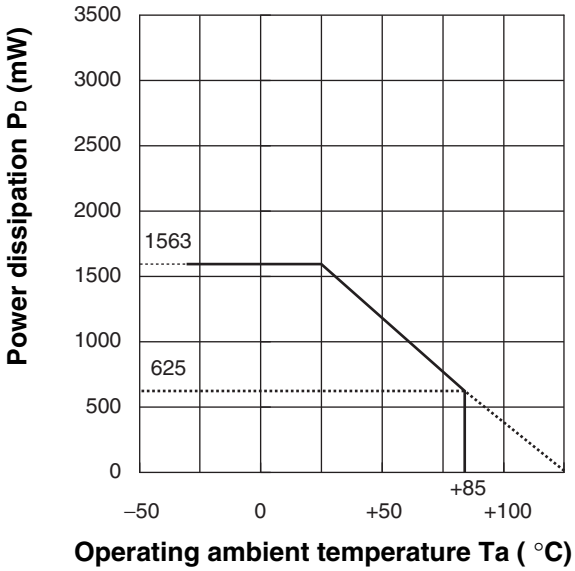
XPOR output voltage V_{XPOR} vs. Input voltage



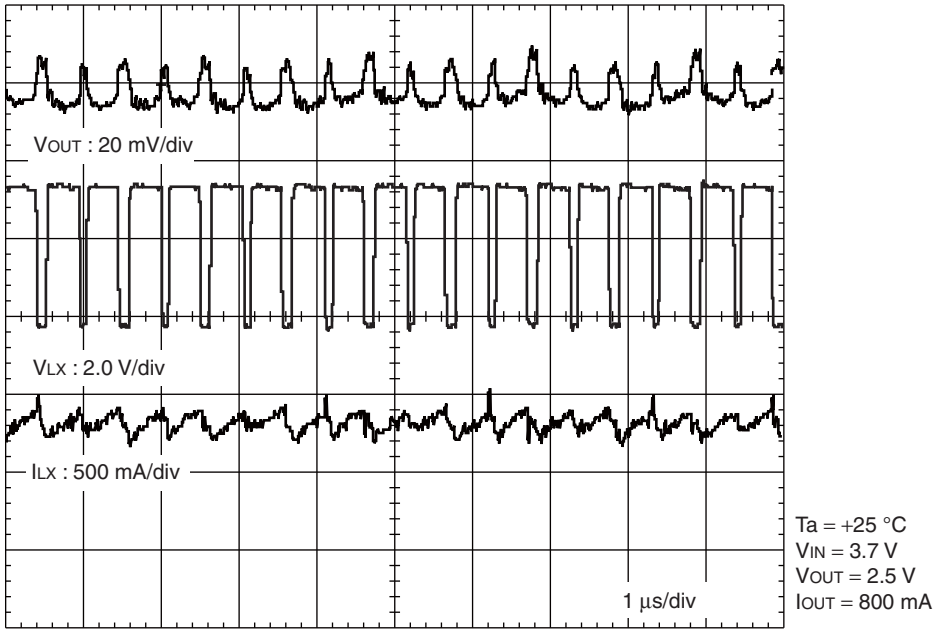
Power dissipation vs. Operating ambient temperature (with thermal via)



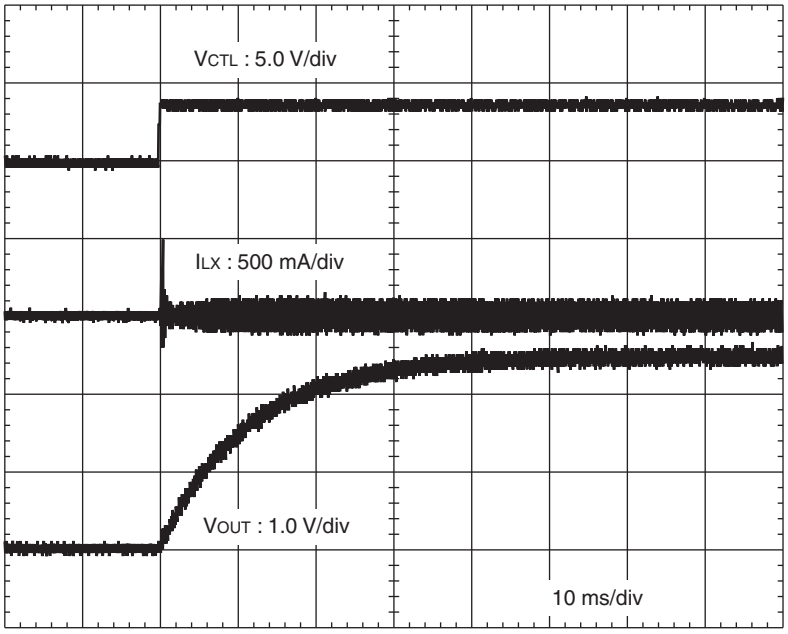
Power dissipation vs. Operating ambient temperature (without thermal via)



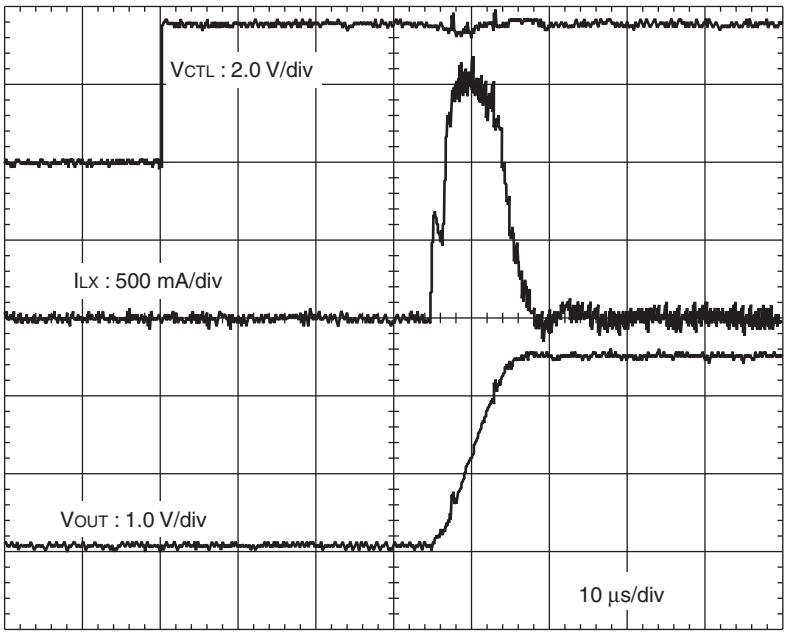
• Switching waveforms



• Startup waveform

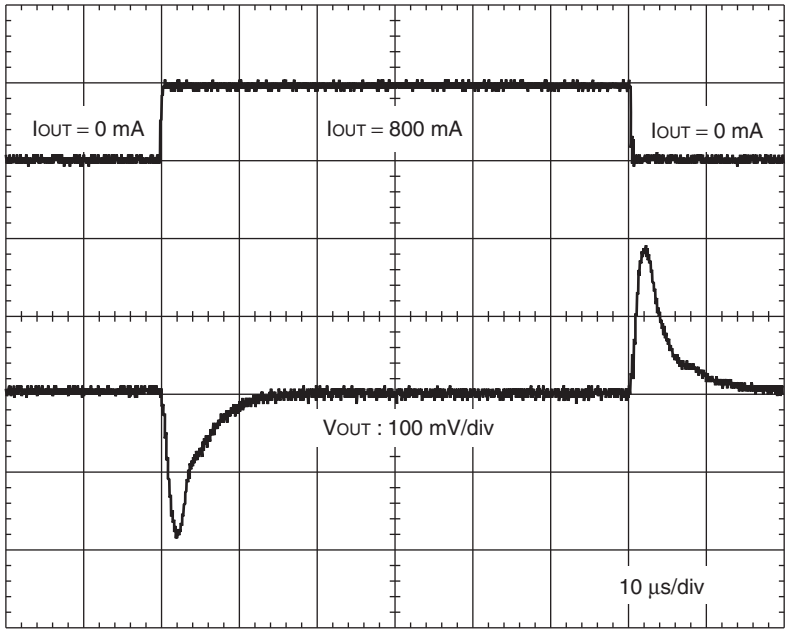


Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
IOUT = 0 A
VREFIN capacitor value = 0.1 µF



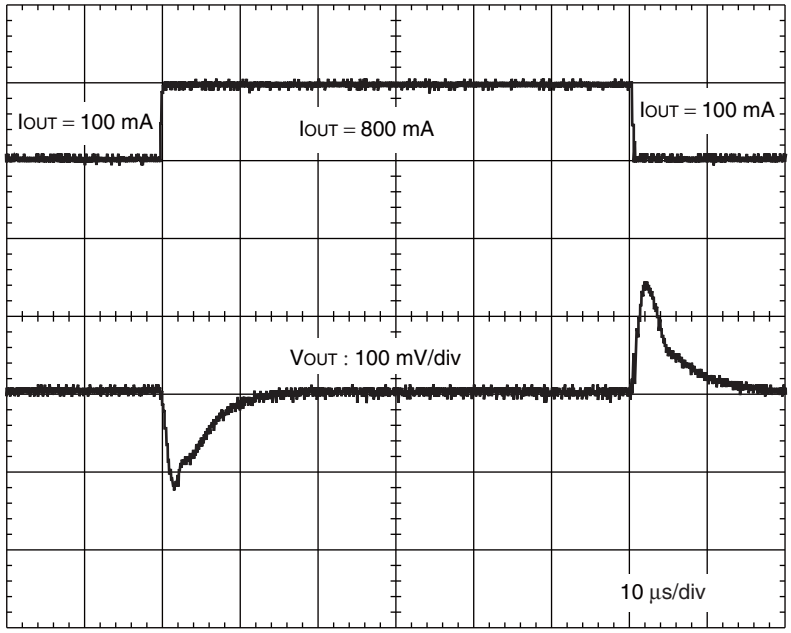
Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
IOUT = 0 A
No VREFIN capacitor

• Output waveforms at sudden load changes (0 mA ↔ 800 mA)



Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
VREFIN capacitor value = 0.1 µF

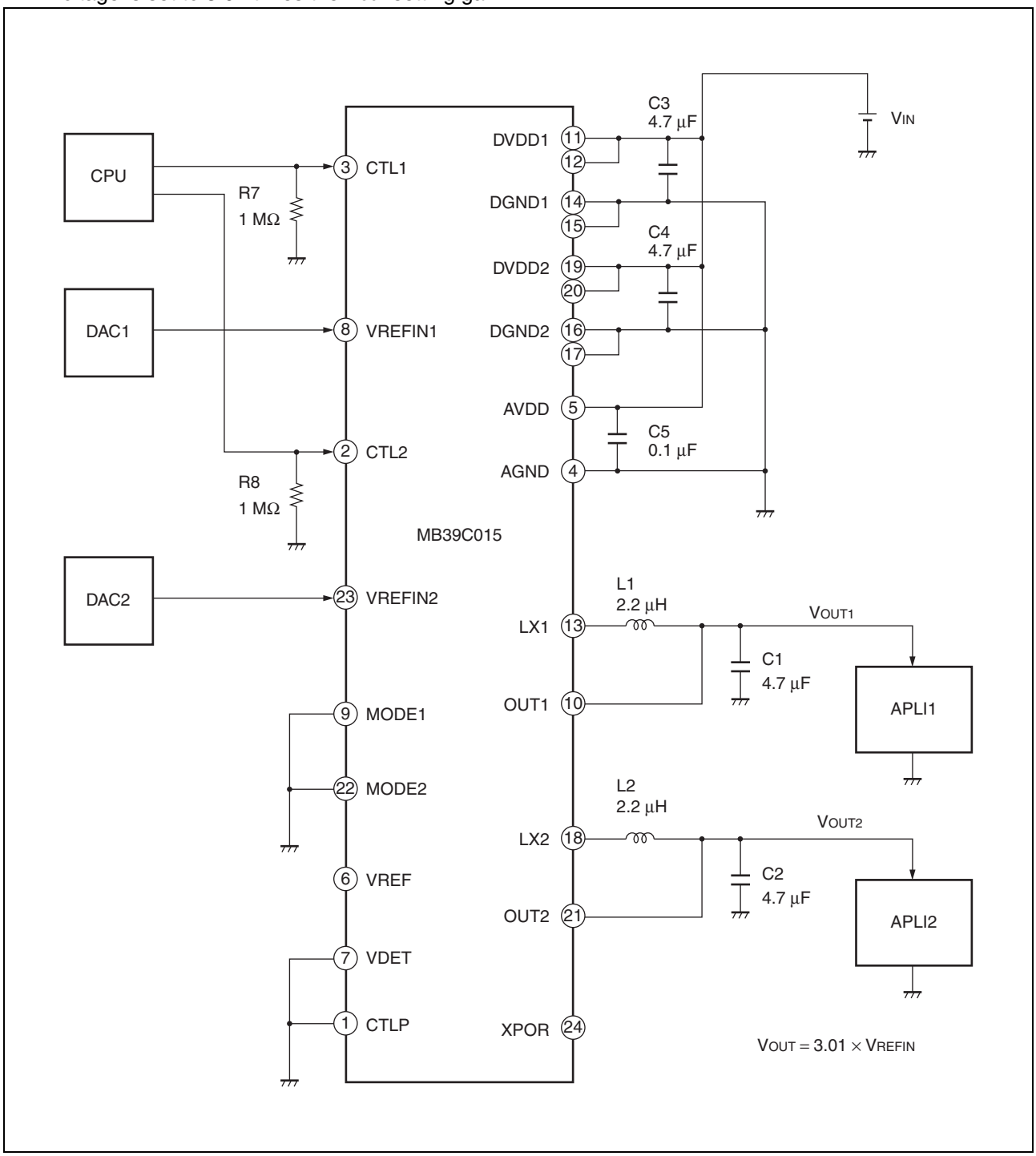
• Output waveforms at sudden load changes (100 mA ↔ 800 mA)



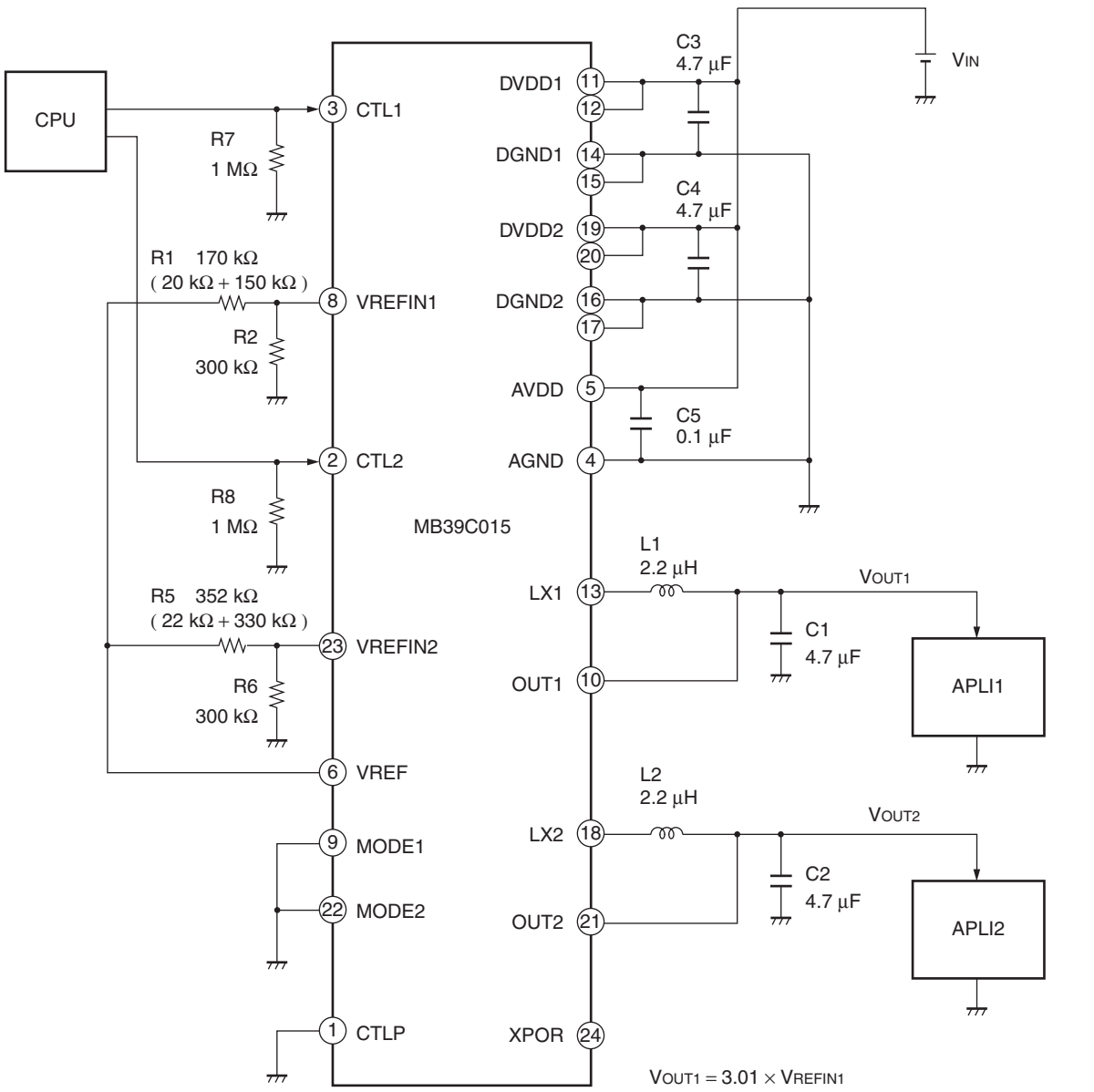
Ta = +25 °C
VIN = 3.7 V
VOUT = 2.5 V
VREFIN capacitor value = 0.1 µF

■ APPLICATION CIRCUIT EXAMPLES

- **APPLICATION CIRCUIT EXAMPLE 1**
- An external voltage is input to the reference voltage external input (VREFIN1, VREFIN2) , and the V_{OUT} voltage is set to 3.01 times the V_{OUT} setting gain.



- **APPLICATION CIRCUIT EXAMPLE 2**
- The voltage of VREF pin is input to the reference voltage external input (VREFIN1, VREFIN2) by dividing resistors. The V_{OUT1} voltage is set to 2.5 V and V_{OUT2} voltage is set to 1.8 V.



• **APPLICATION CIRCUIT EXAMPLE COMPONENTS LIST**

Component	Item	Part Number	Specification	Package	Vendor
L1	Inductor	VLF4012AT-2R2M	2.2 μH, RDC = 76 mΩ	SMD	TDK
		MIPW3226D2R2M	2.2 μH, RDC = 100 mΩ	SMD	FDK
L2	Inductor	VLF4012AT-2R2M	2.2 μH, RDC = 76 mΩ	SMD	TDK
		MIPW3226D2R2M	2.2 μH, RDC = 100 mΩ	SMD	FDK
C1	Ceramic capacitor	C2012JB1A475K	4.7 μF (10 V)	2012	TDK
C2	Ceramic capacitor	C2012JB1A475K	4.7 μF (10 V)	2012	TDK
C3	Ceramic capacitor	C2012JB1A475K	4.7 μF (10 V)	2012	TDK
C4	Ceramic capacitor	C2012JB1A475K	4.7 μF (10 V)	2012	TDK
C5	Ceramic capacitor	C1608JB1E104K	0.1 μF (50 V)	2012	TDK
R1	Resistor	RK73G1JTTD D 20 kΩ RK73G1JTTD D 150 kΩ	20 kΩ 150 kΩ	1608 1608	KOA KOA
R2	Resistor	RK73G1JTTD D 300 kΩ	300 kΩ	1608	KOA
R5	Resistor	RK73G1JTTD D 22 kΩ RK73G1JTTD D 330 kΩ	22 kΩ 330 kΩ	1608 1608	KOA KOA
R6	Resistor	RK73G1JTTD D 300 kΩ	300 kΩ	1608	KOA
R7	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA
R8	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA

TDK : TDK Corporation
FDK : FDK Corporation
KOA : KOA Corporation

■ USAGE PRECAUTIONS

1. Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions adversely affect the reliability of the LSI.

2. Use the devices within recommended operating conditions

The recommended operating conditions are the conditions under which the LSI is guaranteed to operate. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance

4. Take appropriate static electricity measures

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages

The use of negative voltages below −0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

■ ORDERING INFORMATION

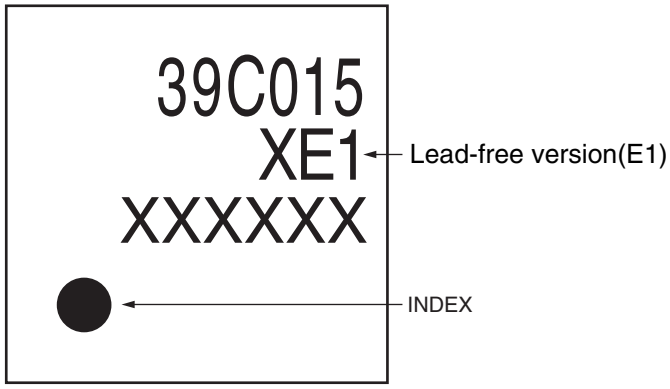
Part number	Package	Remarks
MB39C015WQN	24-pin plastic QFN (LCC-24P-M10)	Exposed PAD

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

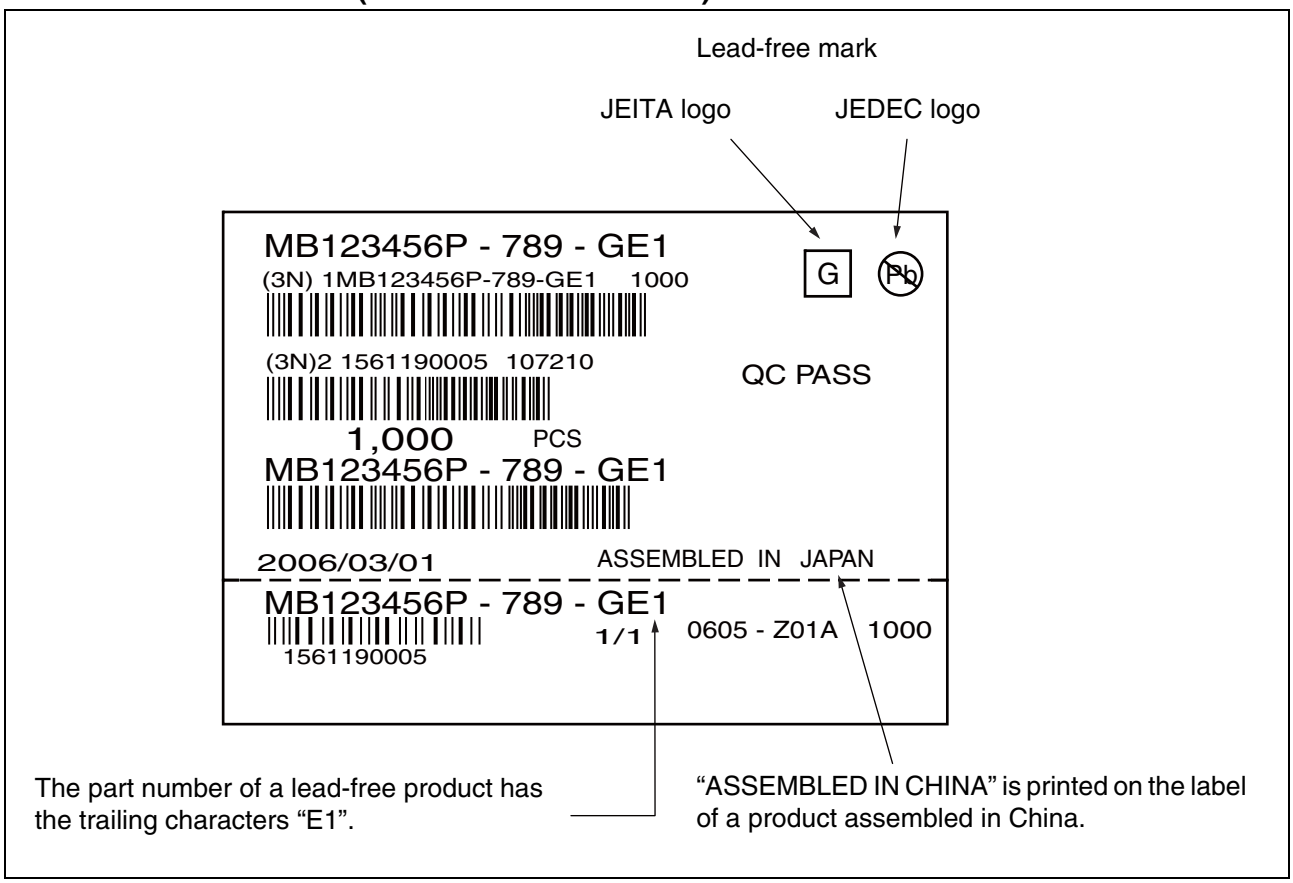
The LSI products of FUJITSU SEMICONDUCTOR with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

A product whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (LEAD FREE VERSION)



■ LABELING SAMPLE (LEAD FREE VERSION)



■ EVALUATION BOARD SPECIFICATION

The MB39C015 Evaluation Board provides the proper for evaluating the efficiency and other characteristics of the MB39C015.

• Terminal information

Symbol	Functions
VIN	Power supply terminal In standard condition 3.1 V to 5.5 V* * : When the VIN/VOUT difference is to be held within 0.6 V or less, such as for devices with a standard output voltage (VOUT1 = 2.5 V) when VIN < 3.1 V, FUJITSU SEMICONDUCTOR recommends changing the output capacity (C1, C2) to 10 μF.
VOUT1, VOUT2	Output terminals (VOUT1: CH1, VOUT2: CH2)
VCTL	Power supply terminal for setting the CTL1, CTL2 and CTLP terminals. Use by connecting with CTL1,CTL2 and CTLP.
CTL1, CTL2	Direct supply terminal of CTL (CTL1 : for CH1, CTL2 : for CH2) CTL1, CTL2 = 0 V to 0.8 V (Typ.) : Shutdown CTL1, CTL2 = 0.95 V (Typ.) to V_{IN} (5 V Max) : Normal operation
MODE1, MODE2	TEST terminal MODE1, MODE2 = OPEN or GND
VREF	Reference voltage output terminal VREF = 1.30 V (Typ.)
VREFIN1, VREFIN2	External reference voltage input terminals (VREFIN1 : for CH1, VREFIN2 : for CH2) When an external reference voltage is supplied, connect it to the terminal for each channel.
VDET	Voltage input terminal for voltage detection
CTLP	Voltage detection circuit block control terminal CTLP = L : Voltage detection circuit block stop CTLP = H : Normal operation
XPOR	Voltage detection circuit output terminal The N-ch MOS open drain circuit is connected.
VXPOR	Pull-up voltage terminal for the XPOR terminal
PGND	Ground terminal Connect power supply GND to the PGND terminal next to the VIN terminal. Connect output (load) GND to the PGND terminal between the VOUT1 terminal and the VOUT2 terminal.
AGND	Ground terminal

• Startup terminal information

Terminal name	Condition	Functions
CTL1	L : Open H : Connect to VCTL	ON/OFF switch for CH1 L : Shutdown H : Normal operation.
CTL2	L : Open H : Connect to VCTL	ON/OFF switch for CH2 L : Shutdown H : Normal operation.
CTLP	L : Open H : Connect to VCTL	ON/OFF switch for the voltage detection block L: Stops the voltage detection circuit H: Normal operation.

• Jumper information

JP	Functions
JP1	Short-circuited in the layout pattern of the board (normally used shorted).
JP2	Short-circuited in the layout pattern of the board (normally used shorted).
JP3	Normally used shorted (0 Ω)
JP6	Normally used shorted (0 Ω)

• Setup and checkup

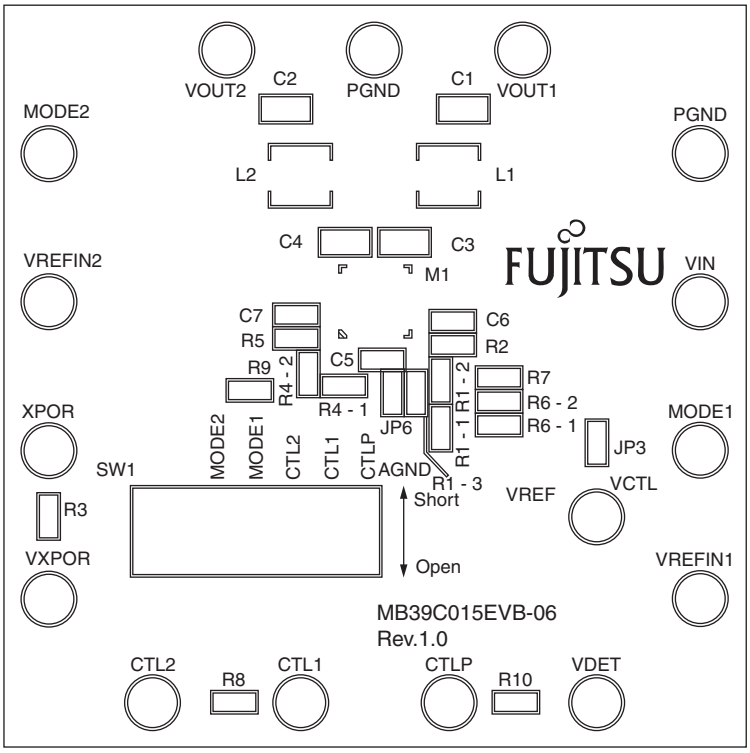
(1) Setup

1. Connect the CTL1 terminal and the CTL2 terminal to the VCTL terminal.
2. Put it into “L” state by connecting the CTLP terminal to the AGND pad.
3. Connect the power supply terminal to the VIN terminal, and the power supply GND terminal to the PGND terminal. Make sure PGND is connected to the PGND terminal next to the VIN terminal. (Example of setting power-supply voltage : 3.7 V)

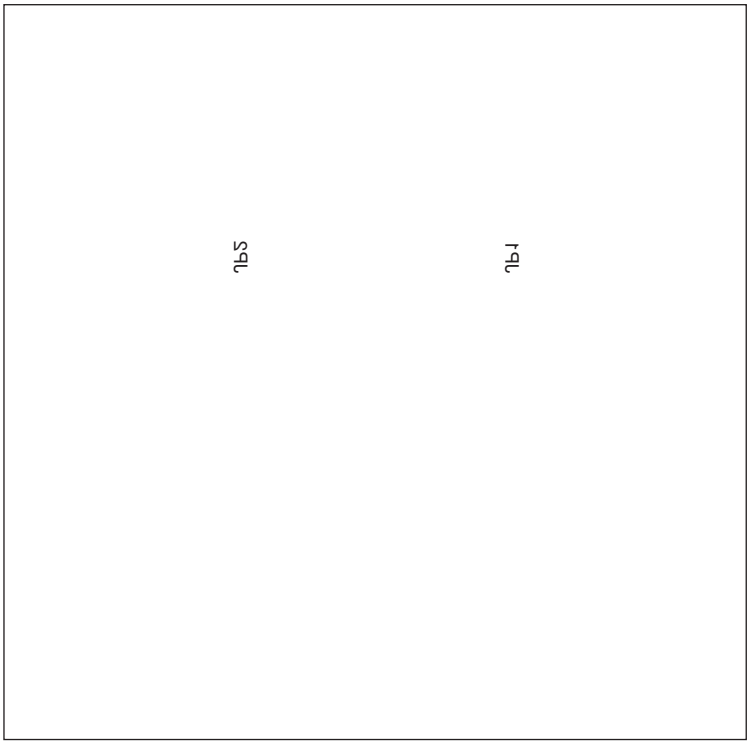
(2) Checkup

Supply power to VIN. The IC is operating normally if VOUT1 = 2.5 V (Typ) and VOUT2 = 1.8 V (Typ).

- Component layout on the evaluation board (Top View)

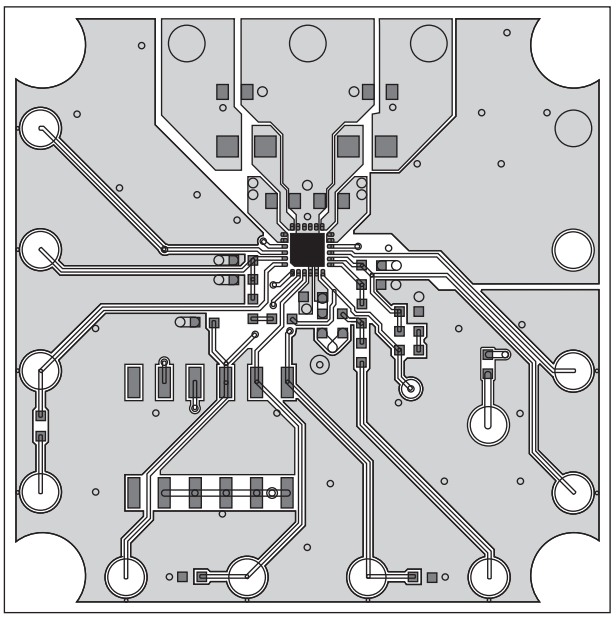


Top Side (Component side)

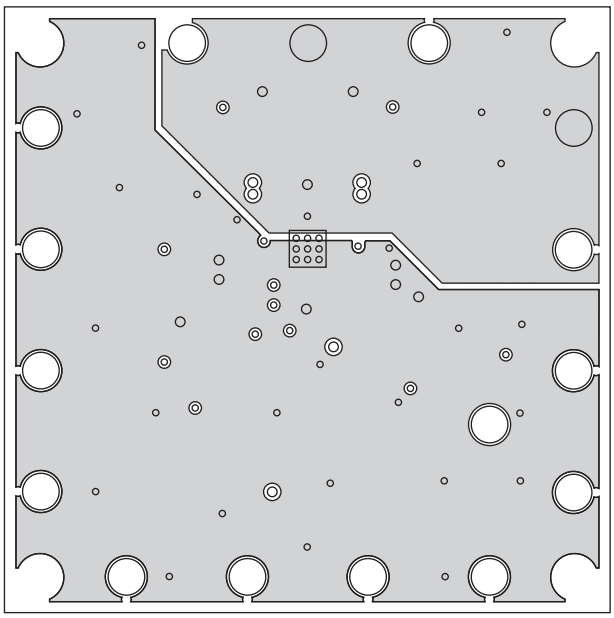


Bottom Side (Soldering side)

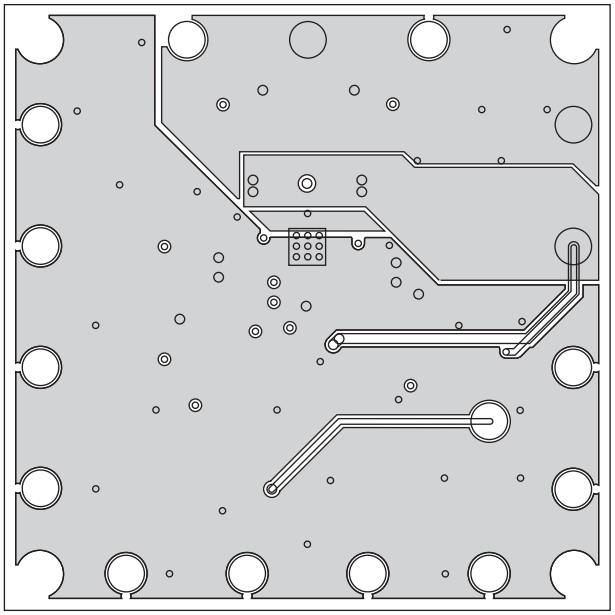
- Evaluation board layout (Top View)



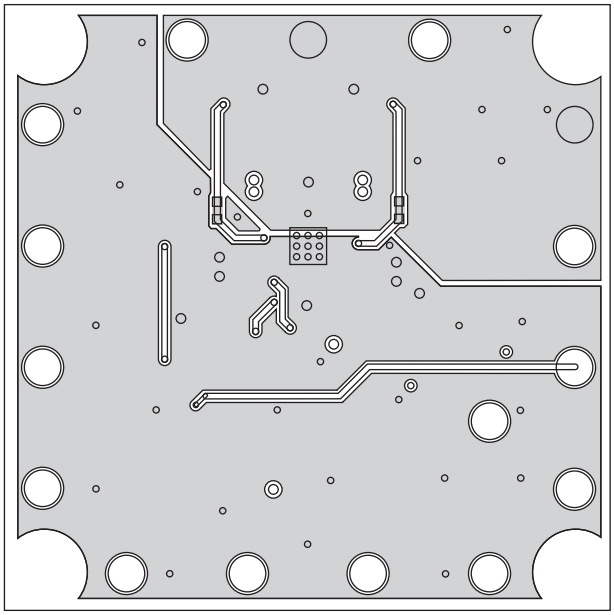
Top Side (Layer1)



Inside GND (Layer2)

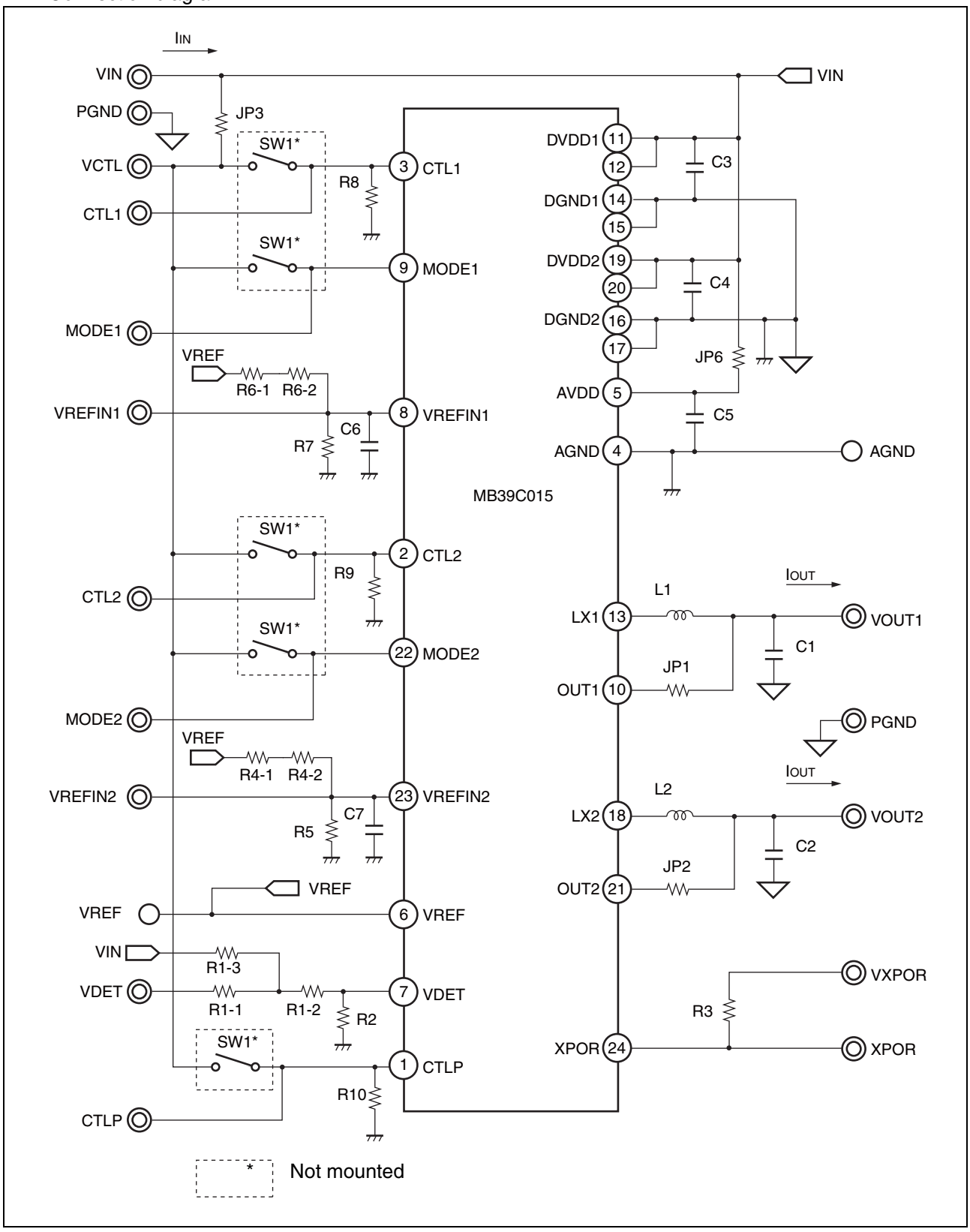


Inside VIN & GND (Layer3)



Bottom Side (Layer4)

• Connection diagram



• Component list

COMPONENT	Part Name	MODEL NUMBER	SPECIFICATION	PACKAGE	VENDOR	REMARK
M1	IC	MB39C015WQN	—	QFN-24	FSL	
L1	Inductor	VLF4012AT-2R2M	2.2 µH, RDC = 76 mΩ	SMD	TDK	
L2	Inductor	VLF4012AT-2R2M	2.2 µH, RDC = 76 mΩ	SMD	TDK	
C1	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK	
C2	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK	
C3	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK	
C4	Ceramic capacitor	C2012JB1A475K	4.7 µF (10 V)	2012	TDK	
C5	Ceramic capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	
C6	Ceramic capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	
C7	Ceramic capacitor	C1608JB1H104K	0.1 µF (50 V)	1608	TDK	
R1-1	Jumper	RK73Z1J	50 mΩ Max, 1 A	1608	KOA	
R1-2	Resistor	RR0816P-304-D	300 kΩ ± 0.5%	1608	SSM	
R1-3	Jumper	RK73Z1J	50 mΩ Max, 1 A	1608	KOA	
R2	Resistor	RR0816P-753-D	75 kΩ ± 0.5%	1608	SSM	
R3	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA	
R4-1	Resistor	RR0816P-223-D	22 kΩ ± 0.5%	1608	SSM	
R4-2	Resistor	RR0816P-334-D	330 kΩ ± 0.5%	1608	SSM	
R5	Resistor	RR0816P-304-D	300 kΩ ± 0.5%	1608	SSM	
R6-1	Resistor	RR0816P-203-D	20 kΩ ± 0.5%	1608	SSM	
R6-2	Resistor	RR0816P-154-D	150 kΩ ± 0.5%	1608	SSM	
R7	Resistor	RR0816P-304-D	300 kΩ ± 0.5%	1608	SSM	
R8	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA	
R9	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA	
R10	Resistor	RK73G1JTTD D 1 MΩ	1 MΩ ± 0.5%	1608	KOA	
SW1	Switch	—	—	—	—	Not mounted
JP1	Jumper	—	—	—	—	Pattern-shorted
JP2	Jumper	—	—	—	—	Pattern-shorted
JP3	Jumper	RK73Z1J	50 mΩ Max, 1 A	1608	KOA	
JP6	Jumper	RK73Z1J	50 mΩ Max, 1 A	1608	KOA	

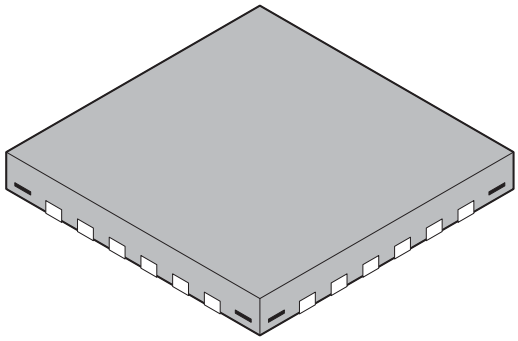
Note : These components are recommended based on the operating tests authorized.

FSL : FUJITSU SEMICONDUCTOR LIMITED
TDK : TDK Corporation
KOA : KOA Corporation
SSM : SUSUMU Co., Ltd

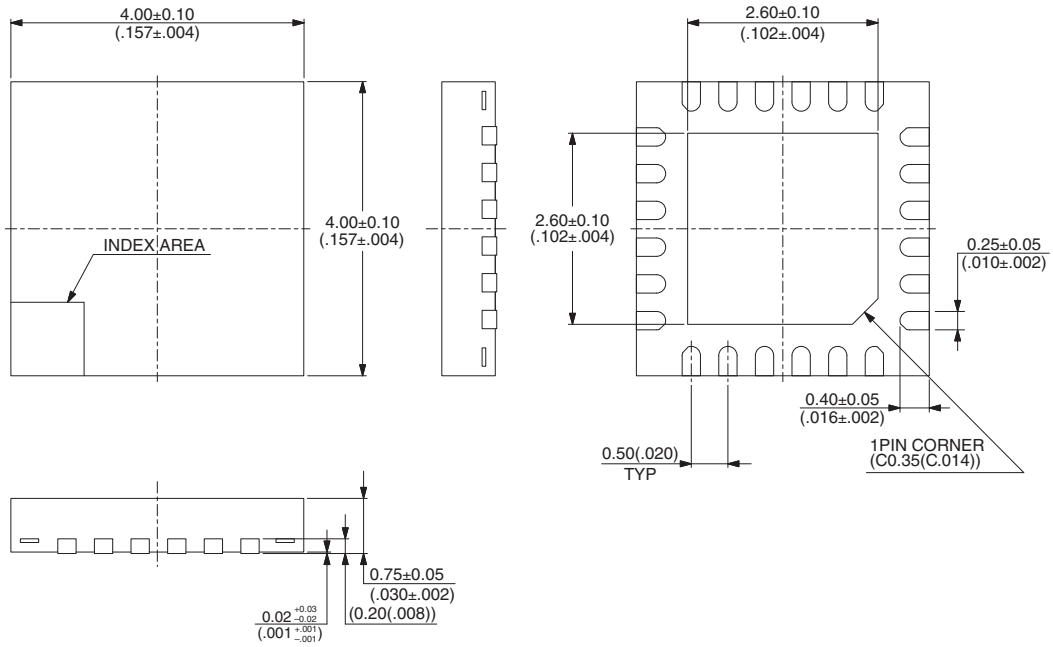
■ EV BOARD ORDERING INFORMATION

EV Board Part No.	EV Board Version No.	Remarks
MB39C015EVB-06	MB39C015EVB-06 Rev.1.0	QFN-24

■ PACKAGE DIMENSION

24-pin plastic QFN		
 (LCC-24P-M10)	Lead pitch	0.50 mm
	Package width × package length	4.00 mm × 4.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm Max
	Weight	0.04 g

24-pin plastic QFN
(LCC-24P-M10)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ CONTENTS

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