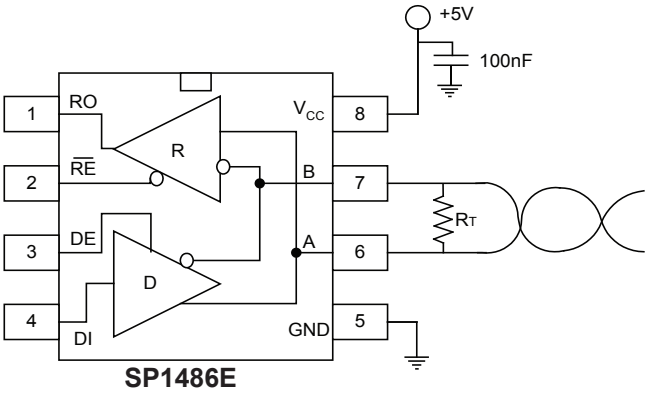
SP1486E

+5V, 20Mbps PROFIBUS RS485/RS422 Transceivers
Advanced Failsafe, 1/8th Unit Load, ±15kV ESD-Protected

FEATURES

- Recommended for PROFIBUS applications
- High differential output drive, minimum 2.1V into 54Ω load
- 5.0V Single Supply Operation
- 1ns driver and reveiver skew
- 20 Mbps data rate
- 1/8th Unit Load, 256 transceivers on bus
- **Robust ESD Protection for RS485 pins**
  - **±15kV Air-Gap Discharge**
  - **±15kV Human Body Model**
  - **±8kV Contact Discharge**
- Hot Swap glitch protection on control inputs
- Receiver failsafe on open, short or terminated lines
- Driver short circuit current limit and thermal shutdown for overload protection
- Very low 300µA static power consumption
- 1µA shutdown mode



SP1486E

APPLICATIONS

- High Speed RS485 Communications
- Industrial Process Control
- PROFIBUS applications

DESCRIPTION

SP1486E is a half duplex differential line transceiver suitable for high speed bidirectional communication on multipoint bus transmission lines. Each device contains one differential driver and one differential receiver. Devices comply with TIA/EIA-485 and TIA/EIA-422 standards and also meet the higher drive and tighter skew requirements of PROFIBUS applications. Lead-free and RoHS compliant packages are available for all models.

PROFIBUS is in wide use in industrial control and automation applications and the SP1486E is ruggedized for use in harsh operating conditions. Receivers are specially designed to fail-safe to a logic high output state if the inputs are left un-driven or shorted. All RS485 bus-pins are protected against severe ESD events up to ±15kV (Air-Gap and Human Body Model) and up to ±8kV Contact Discharge (IEC 1000-4-2). Drivers are protected from excess current flow caused by bus contention or output short-circuits by both an internal current limit and a thermal-overload shutdown. Devices are rated for Industrial (-40 to +85ºC) or Extended (-40 to +125ºC) operating temperatures. Receivers have exceptionally high input impedance, which places only 1/8th the standard load on a shared bus. Up to 256 transceivers may coexist while preserving full signal margin.

All devices operate from a single 5.0 V power supply and draw negligible quiescent power. Both driver and receiver can be enabled and disabled independently and the device enters a low power shutdown mode if both driver and receiver are disabled. The bus-pin outputs of disabled modules are in high impedance state. The high impedance driver output is maintained over the entire common-mode voltage range from -7 to +12V.

PIN ASSIGNMENTS

Pin Name	Pin Function	Pin Function
1	RO	Receiver Output. When $\overline{RE}$ is low and if (A – B) ≥ -40mV, RO is High. If (A – B) ≤ - 200mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode. $\overline{RE}$ is a hot-swap input.
3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode. DE is a hot-swap input.
4	DI	Driver Input. With DE high, a low level on DI forces non-inverting output low and inverting output high. Similarly, a high level on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting Receiver Input and Non-inverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	Vcc	Positive Supply Vcc. Bypass Vcc to GND with a 0.1uF capacitor.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage (V_{CC}).....+ 7.0V
Input voltage at control input pins ($\overline{RE}$, DE) ..... -0.3V to V_{CC}+0.3V
Driver input voltage (DI) .....-0.3V to V_{CC}+0.3V
Driver output voltage (A, B) .....+13V
Receiver output voltage (RO) .....-0.3V to (Vcc + 0.3V)
Receiver input voltage (A, B) .....+13V
Package Power Dissipation.....450mW @ T_A=25°C
Maximum Junction Temperature..... 150°C
8-Pin SOICN $Ø_{JA}$ =.....128.4°C/W
Storage Temperature.....-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Vcc=5V ±10%, T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are Vcc=5V and T_A=25°C

Recommended Operating Conditions		Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}		4.5	5	5.5	V
Input Voltage on A and B pins		-7		12	V
High-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		2		V_{CC}	V
Low-level input voltage (DI, DE or $\overline{RE}$), V_{IL}		0		0.8	V
Output Current	Driver	-60		60	mA
	Receiver	-8		8	
Signaling Rate,				20	Mbps
Operating Free Air Temperature, T_A	Industrial Grade (E)	-40		85	°C
	Extended Temp Grade (M)	-40		125	
Junction Temperature, T_J		-40		150	°C

Note: The least positive (most negative) limit is designated as the maximum value.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital Input Signals: DI, DE, $\overline{RE}$							
Logic input thresholds		High, V_{IH}		2.0			V
		Low, V_{IL}				0.8	
Logic Input Current		T_A=25°C, after first transition				±1	µA
Input Hysteresis		T_A=25°C			100		mV
Driver							
Differential Driver Output (VOD)		No Load				V_{CC}	V
Differential Driver Output		R_L=100Ω (RS422)		2.1		V_{CC}	V
		R_L=54Ω (RS485)		2.1	2.7	V_{CC}	
Differential Driver Output		V_{CM}=-7 to +12V		2.1	2.7	V_{CC}	
Change in Magnitude of Differential Output Voltage (ΔVOD) (Note 1)		R_L=54 or 100Ω				±0.2	V
Driver Common Mode Output Voltage (V_{OC})		R_L=54 or 100Ω				3	V
Change in Common Mode Output Voltage (ΔVOC)		R_L=54 or 100Ω				±0.2	V
Driver Short Circuit Current Limit		-7V≤V_{OUT}≤+12V				±250	mA
Receiver							
Receiver Input Resistance		-7V≤V_{CM}≤12V		96			KΩ
Input Current (A, B pins)		DE=0, $\overline{RE}$=0, Vcc=0 or 5.5V	V_{IN}=12V			125	µA
			V_{IN}=-7V	-100			
Receiver Differential Threshold (VA-VB)		-7V≤V_{CM}≤12V		-200	-125	-40	mV
Receiver Input Hysteresis					25		mV
Receiver Output Voltage	V_{OH}	I_{OUT}=-8mA, V_{ID}=-40mV		Vcc-1.5			V
	V_{OL}	I_{OUT}=8mA, V_{ID}=-200mV				0.4	
High-Z Receiver Output Current		V_{CC}=5.5V, 0≤V_{OUT}≤V_{CC}				± 1	µA
Receiver Output Short Circuit Current		0V≤V_{RO}≤V_{CC}				± 95	mA
Supply and Protection							
Supply Current	IQ, Active Mode	No load, DI=0 or V_{CC}			0.30	1	mA
	Shutdown Mode	DE=0, RE=Vcc, DI=V_{CC} or 0				1	µA
Thermal Shutdown Temperature		Junction temperature			165		°C
Thermal Shutdown Hysteresis					15		

Notes:
1. Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.
2. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns the device does not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. In this low power mode most circuitry is disabled and supply current is typically 1nA.
3. Characterized, not 100% tested

TIMING CHARACTERISTICS

Unless otherwise noted Vcc= +5.0±0.5V, ambient temperature T_A from -40 to +85ºC

DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate	Duty Cycle 40 to 60%	20			Mbps
Driver Propagation Delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF,		12	20	ns
Driver Output Rise/Fall Time (t_R, t_F)			6	10	ns
Driver Differential Skew (t_{PLH} – t_{PHL})			1	5	ns
Driver Enable to Output High (t_{DZH})	R_L = 500Ω, C_L = 50pF,			50	ns
Driver Enable to Output Low (t_{DZL})				50	ns
Driver Disable from Output High (t_{DHZ})				50	ns
Driver Disable from Output Low (t_{DLZ})				50	ns
Shutdown to Driver Output Valid (t_{DZV})				150	ns

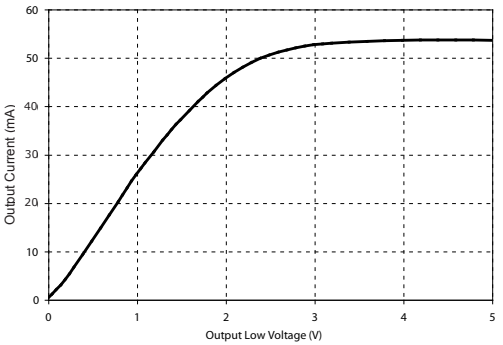
RECEIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate	Duty Cycle 40 to 60%	20			Mbps
Receiver Propagation Delay (t_{PLH}, t_{PHL})	C_L=15pF, V_{ID}=±2V,			40	ns
Propagation Delay Skew (t_{PLH}, t_{PHL})			1	5	ns
Receiver Output Rise/Fall Time	C_L=15pF			15	ns
Receiver Enable to Output High (t_{ZH})	C_L=15pF, R_L=1kΩ			50	ns
Receiver Enable to Output Low (t_{ZL})	C_L=15pF, R_L=1kΩ			50	ns
Receiver Disable from Output High (t_{HZ})	C_L=15pF, R_L=1kΩ			50	ns
Receiver Disable from Output Low (t_{LZ})	C_L=15pF, R_L=1kΩ			50	ns
Shutdown to Receiver Output Valid (t_{ROV})				3500	ns
Time to Shutdown (Note 2,3)		50	200	600	ns

FUNCTION TABLES

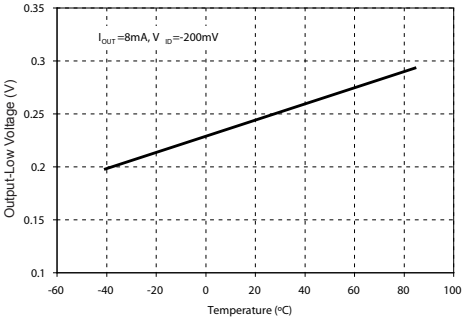
Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	V_A - V_B	RO
0	X	≥ -40mV	1
0	X	≤-200mV	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

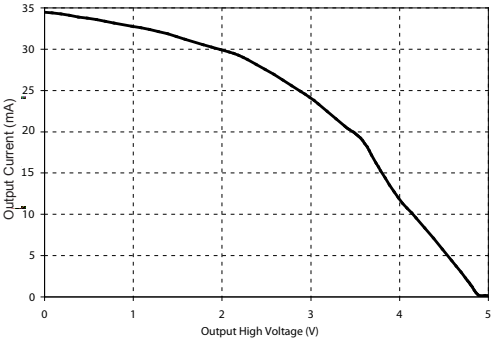
Note: Receiver inputs -200mV < VA - VB < -40mV, should be considered indeterminate



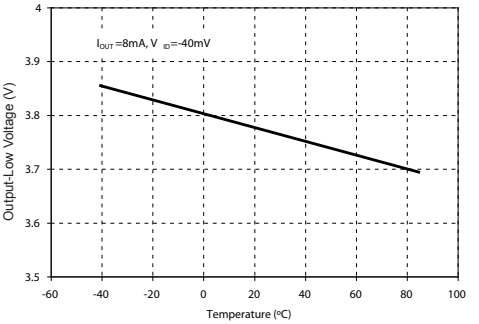
Output Current vs Receiver Output Low Voltage



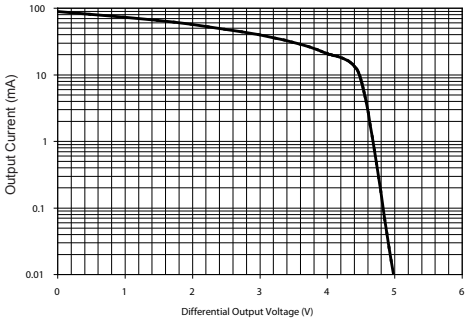
Receiver Output Low Voltage vs Temperature



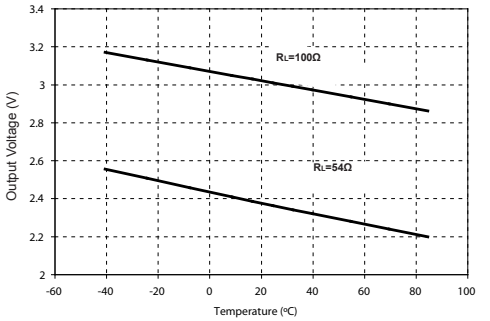
Output Current vs Receiver Output High Voltage



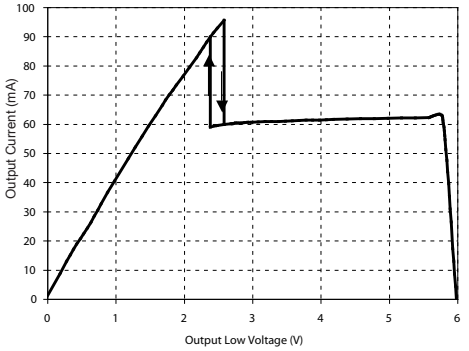
Receiver Output High Voltage vs Temperature



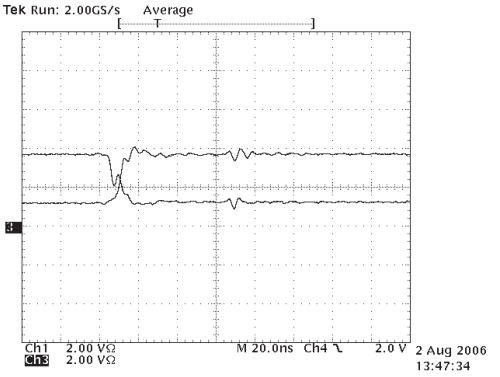
Driver Output Current vs Differential Output Voltage



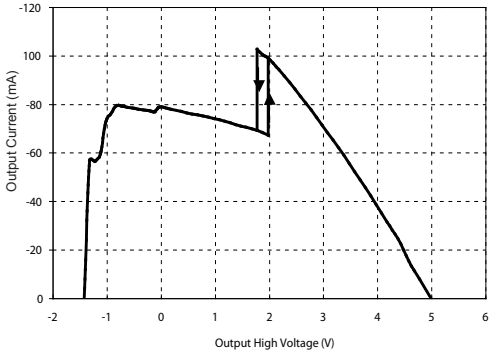
Driver Differential Output Voltage vs Temperature



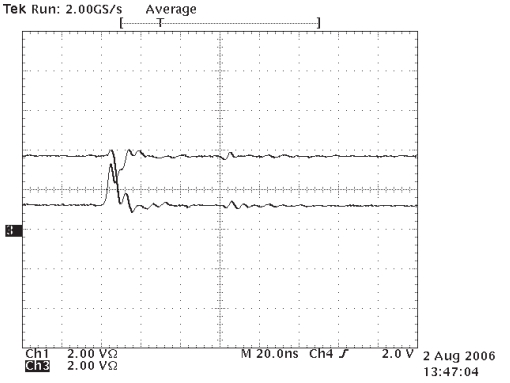
Output Current vs Driver Output Low Voltage



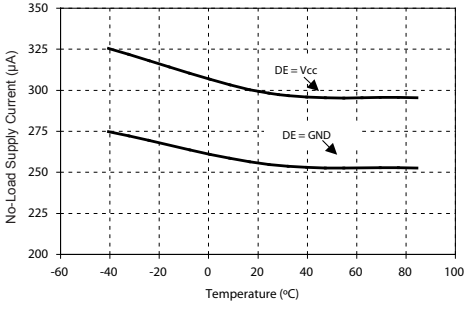
Driver Output Waveforms High to Low



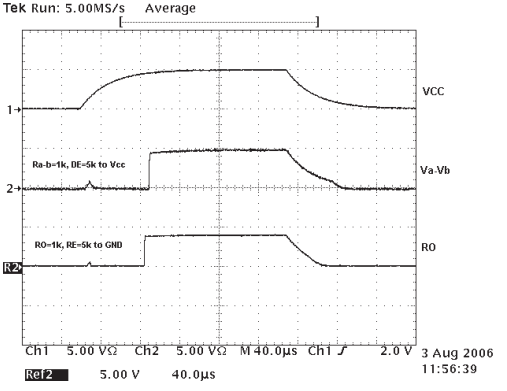
Output Current vs Driver Output High Voltage



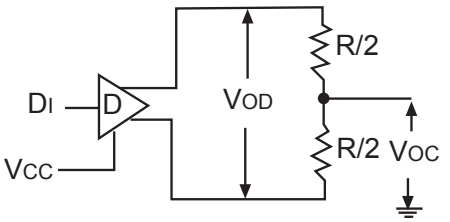
Driver Output Waveform Low to High



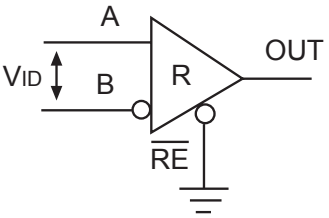
No-load Supply Current vs Temperature



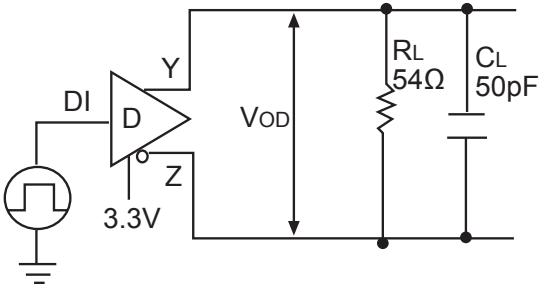
Driver and Receiver Hot Swap Performance vs. Vcc



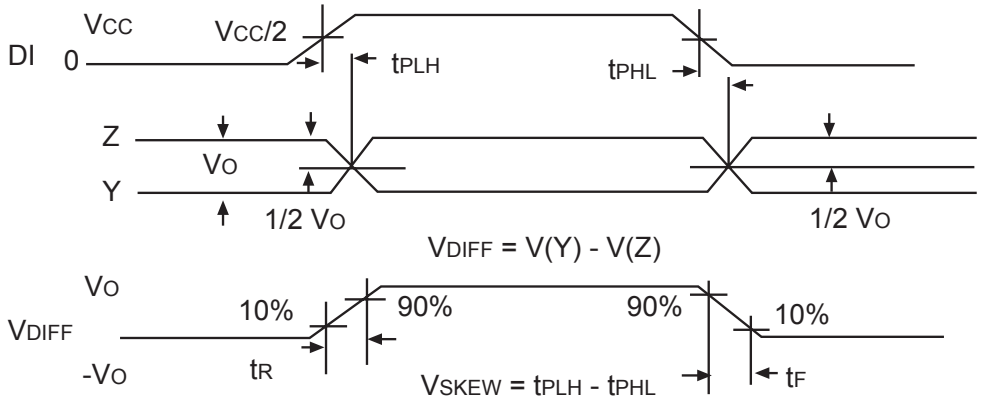
Driver DC Test Circuit



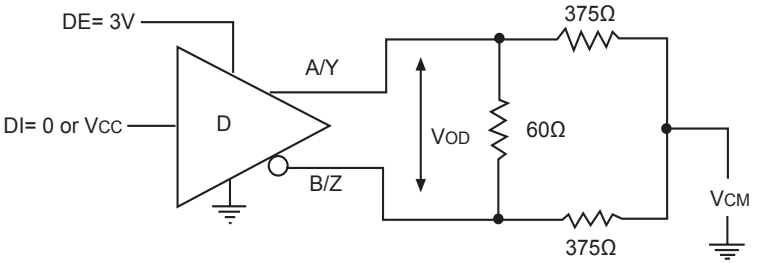
Receiver DC Test Circuit



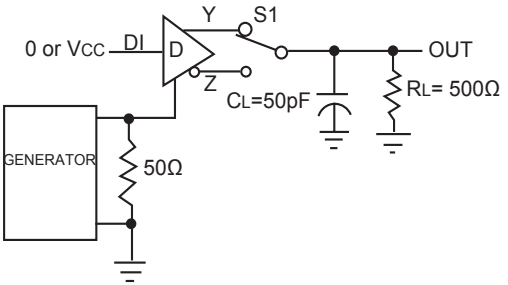
Driver Propagation Delay Time Test Circuit and Timing Diagram

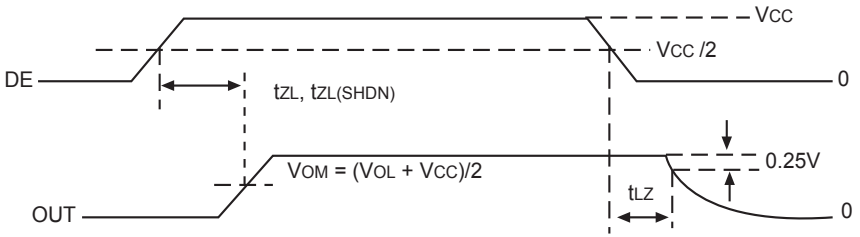


Driver Differential Output Test Circuit

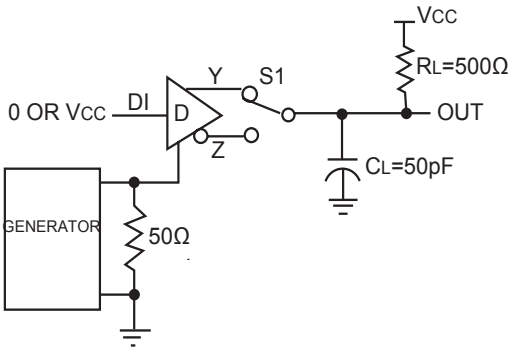


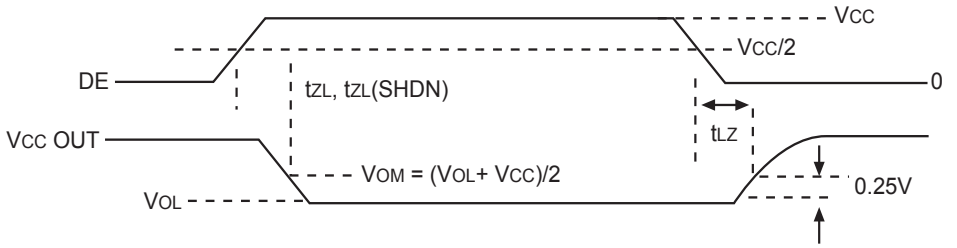
Driver Enable and Disable Times Test Circuit and Timing Diagram



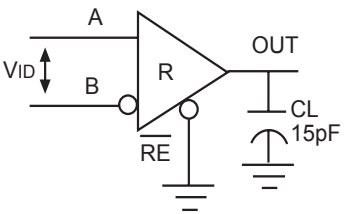


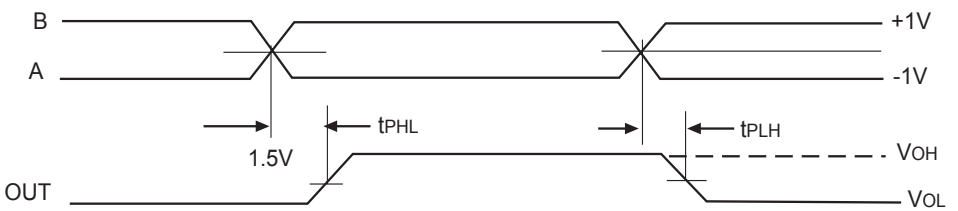
Driver Enable and Disable Times Test Circuit and Timing Diagram



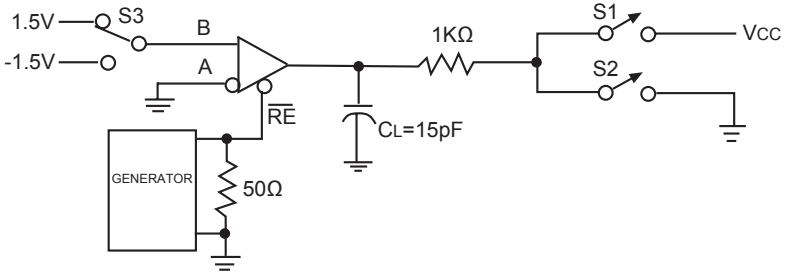


Receiver Propagation Delay Test Circuit and Timing Diagram

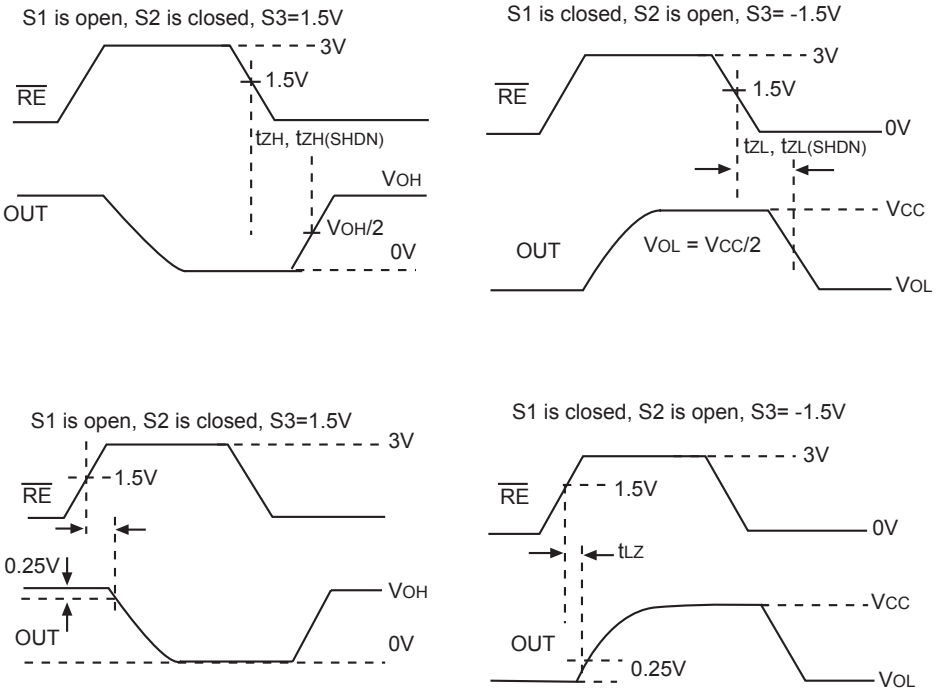




Receiver Enable and Disable Times Test Circuit



Receiver Enable and DisableTiming Diagram



DETAILED DESCRIPTION

SP1486E is an advanced RS485/RS422 transceiver, ideal for PROFIBUS applications. Each device contains one high speed driver and receiver capable of speeds up to 20Mbps with low skew.

The device is designed for reliability in demanding operating conditions. It features a fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. Control inputs (DE and $\overline{RE}$) also feature a hot-swap capability allowing live insertion without error data transfer.

The device operates from a single 5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

PROFIBUS (EN50170 or DIN19245)

The PROFIBUS standard originated in Europe but has spread worldwide as an industrial fieldbus for use in process automation and factory control. There are a number of different implementations, but one of the most widely used is PROFIBUS-DP (Process Field Bus - Distributed Peripherals). DP uses RS485 as its physical layer along with a proprietary data-link layer.

ADVANCED FAIL SAFE

Ordinary RS485 differential receivers will be in an indeterminate state whenever A - B is less than ±200mV. This situation can occur whenever the data bus is not being actively driven. The Advanced Failsafe feature of the SP1486E guarantees a logic-high receiver output if the receiver's differential inputs are shorted, open-circuit, or if they are shunted by a termination resistor.

The receiver thresholds of the SP1486E are very precise and offset by at least a 40mV noise margin from ground. This results in a logic-high receiver output at zero volts input differential while maintaining compliance with the EIA/TIA-485 standard of ±200mV.

HOT-SWAP CAPABILITY

When a micro-processor or other logic device undergoes its power-up sequence its logic-outputs are typically at high impedance. In this state they are unable to drive the DE and $\overline{RE}$ signals to a defined logic level. During this period, noise, parasitic coupling or leakage from other devices could cause standard CMOS enable inputs to drift to an incorrect logic level.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may be suddenly applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

The SP1486E contains a special power-on-reset circuit that holds DE low and $\overline{RE}$ high for approximately 10 microseconds. After this initial power-up sequence the hot-swap circuit becomes transparent, allowing for normal, unskewed enable and disable timings.

±15KV ESD PROTECTION

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs have extra protection against static electricity. Sipex uses state of the art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the SP1486E keeps working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the SP1486E are characterized for protection to the following limits

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2
- ±15kV Air-gap

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The SP1486E helps you design equipment to meet IEC 1000-4-2, without sacrificing board-space and cost for external ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2. Series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to EC 1000-4-2 is generally lower than that measured using the human body model.

The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

MACHINE MODEL

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

256 TRANSCEIVERS ON THE BUS

The standard RS485 receiver input impedance is 12kΩ (1 unit load). A standard driver can drive up to 32 unit loads. The SP1486E has only a 1/8th unit load receiver input impedance (96kΩ), thereby allowing eight times as many, up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

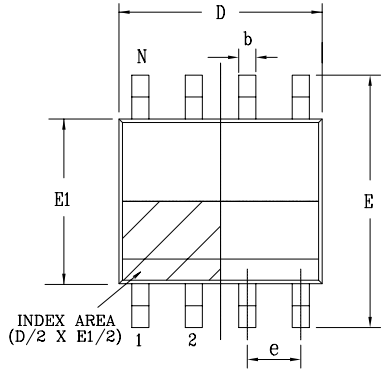
Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown devices typically draw only 50nA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shut-down.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ apply when the parts are shut down. The drivers and receivers take longer to become enabled from low-power shutdown mode $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

DRIVER OUTPUT PROTECTION

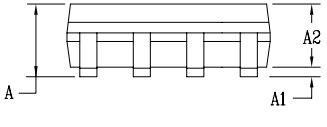
Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver-current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL

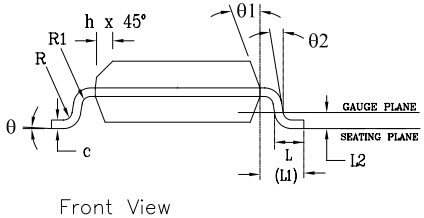


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



Side View



Front View

Solved by Sipex	SIPEX CORPORATION	
	8 PIN SOICN PACKAGE OUTLINE	
Packaging Approval:	Drawing No: 8-PIN SOICN	
By: JL / Date: 07/19/06	Revision: B	Sheet: 1 OF 1

Part number	Temperature range	Package Type
SP1486EEN-L	From -40 to +85°C	Lead Free NSOIC 8 pin
SP1486EMN-L	From -40 to +125°C	Lead Free NSOIC 8 pin

For availability of “M” temperatures (-40 to +125ºC) or in other packages contact factory.

For Tape and Reel add “/TR”. Example: SP1486EEN-L/TR = lead free and Tape and Reel. SP1486EEN/TR = standard in Tape and Reel.

Reel quantity is 2,500 for NSOIC.

Solved by Sipex™

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