

S1F75510

Charge-pump DC/DC Converter & Voltage Regulator

Preliminary

■ DESCRIPTION

The S1F75510 is a power IC designed for use with medium or small capacity TFT-LCD panel modules.

A single chip of this IC is capable of generating three different levels of positive and negative output voltages simultaneously, which are necessary to drive the LCD, by use of a single input power of +2.7 through +3.6V. Since the S1F75510 does not require external transistors nor diodes as its voltage conversion circuit, its built-in CMOS transistors constituting a complete charge pump type DC/DC converter, it is most suitable for the purpose of reducing the current consumption levels of the LCD modules.

Moreover, the charge pump type DC/DC converter of the S1F75510 can be operated upon the frequencies, which are to be switched over by the mode changing signals, using either of the built-in clock signals or external clock signals optimal to respective cases.

This function can drastically suppress the current consumption of this IC while under light load state, thus exhibiting very high power conversion efficiencies.

■ FEATURES

- Supply voltage 2.7V to 3.6V single power input
- Self consumption current (normal mode/blank mode) 300 μ A / 30 μ A (TBD)
 - Normal mode: Boosting by use of the internal clock
 - Blank mode: Selectable between boosting by use of the internal clock or by use of the external clock.
- Conversion efficiency of the charge pump 90% or more respectively
- Built-in voltage conversion circuits constituted by charge pump type DC/DC converter,
 - x2 boosting circuit in the positive direction
 - x3 boosting circuit in the positive direction
 - x3 boosting circuit in the negative direction
- Built-in voltage stabilizing circuit
- Capable of outputting the positive supply voltage V_{OUT2} for the source driver
 - x2 boosting circuit in the positive direction + voltage stabilizing circuit
 - Output voltage: +5.0V \pm 3% (TBD)
- Capable of outputting the positive supply voltage V_{OUT3} for the gate driver
 - x3 boosting circuit in the positive direction
 - Output voltage: +15V
 - $V_{OUT3} = V_{OUT2} \times 3$
- Capable of outputting the negative supply voltage V_{OUT4} for the gate driver
 - x3 boosting circuit in the negative direction
 - Output voltage: -10V
 - $V_{OUT4} = V_{OUT2} \times -2$
- Built-in electric charge discharging circuit
- Built-in shut down function
- Shipping state SSOP3-24pin
- This IC is not of the radiation resistant design nor of the light resistance design.

S1F75510

■ BLOCK DIAGRAM

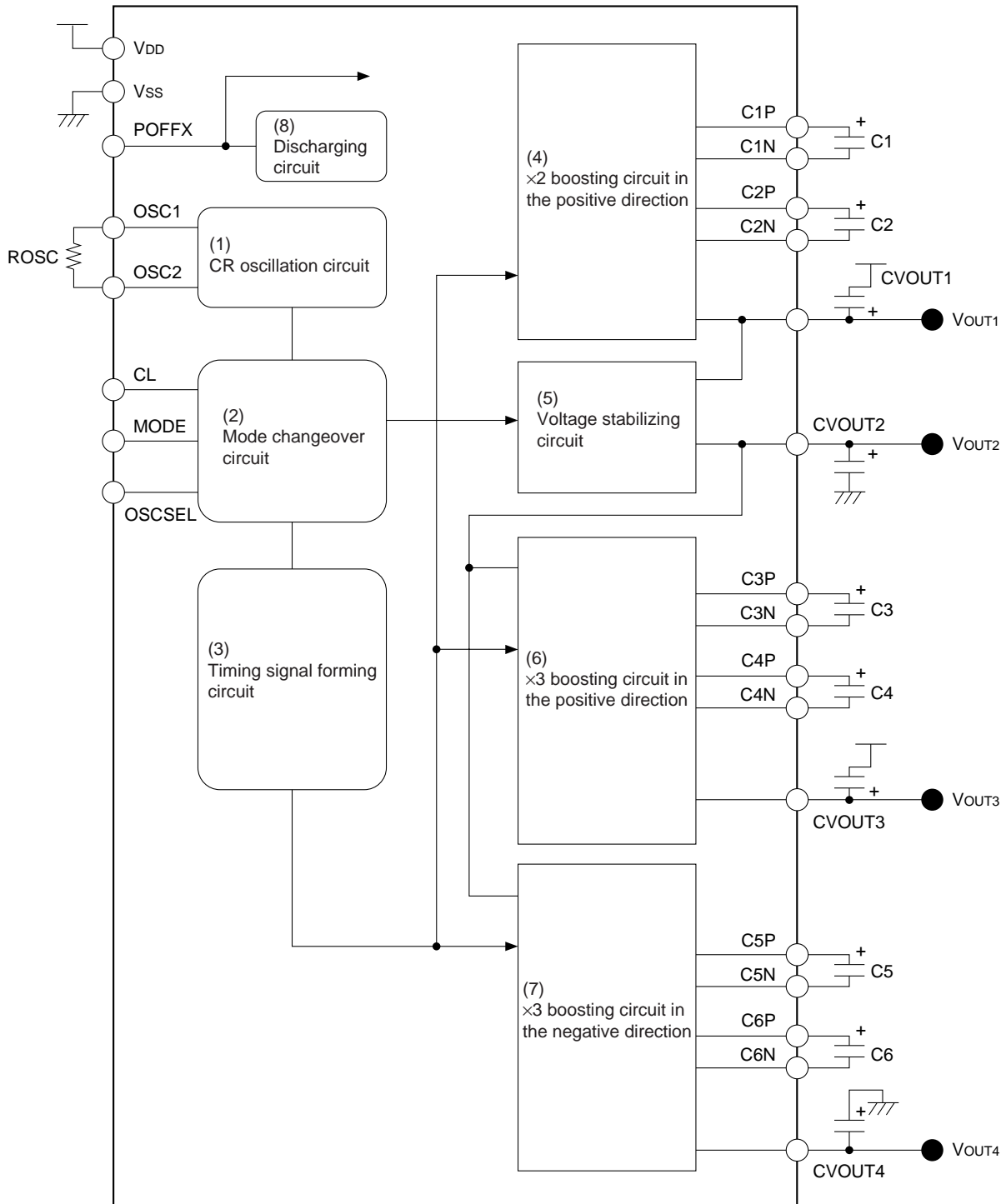


Fig. 1 Block diagram

■ DESCRIPTIONS FOR THE BLOCK DIAGRAM

(1) CR oscillation circuit

The oscillation circuit is constituted by connecting a resistor between the OSC1 pin and the OSC2 pin. The clock signals being generated by this oscillation circuit will become effective as boosting clock signals while the mode changeover signal MODE is on the VDD level (normal mode) or while the mode changeover signal MODE is on the VSS level and, at the same time, when the internal/external clock selection signal OSCSEL is on the VDD level (blank mode · internal clock). When the MODE is set to the VSS level and, at the same time, when the OSCSEL is set to the VSS level (blank mode · external clock), the oscillation will be interrupted.

(2) Mode changeover circuit

The operation modes of the boosting circuit and voltage stabilizing circuit are being switched over by the mode changeover signal MODE. Also, it selects the clock signals to feed to the timing signal forming circuit from either of the external clock signals or internal clock signals.

(3) Timing signal forming circuit

This circuit generates the charge pump boosting clock signals. This circuit outputs timing signals of the clock type (internal clock or external clock) having been selected by the mode changeover circuit to drive respective boosting circuits. When the shut down signal POFFX is set to the VSS level, the timing signal stops to interrupt the boosting operation.

(4) X2 boosting circuit in the positive direction

This circuit makes X2 boosting in the positive direction by charge pump boosting upon the inputted supply voltage VDD – VSS using the VSS potential as the reference voltage. The X2 boosted output will enter into the voltage stabilizing circuit.

(5) Voltage stabilizing circuit

This circuit generates the positive supply voltage VOUT2 for the source driver. ON the basis of the built-in reference, this circuit stabilizes the output from the above "(4) X2 boosting circuit in the positive direction" by use of the series regulator.

(6) X3 boosting circuit in the positive direction

This circuit generates the positive supply voltage VOUT3 for the gate driver. This circuit effects X3 boosting in the positive direction by charge pump boosting upon the voltage VOUT2 – VSS using the VSS potential as the reference voltage.

(7) X3 boosting circuit in the negative direction

This circuit generates the negative supply voltage VOUT4 for the gate driver. This circuit effects X3 boosting in the negative direction by charge pump boosting upon the voltage VOUT2 – VSS using the VOUT2 potential as the reference voltage.

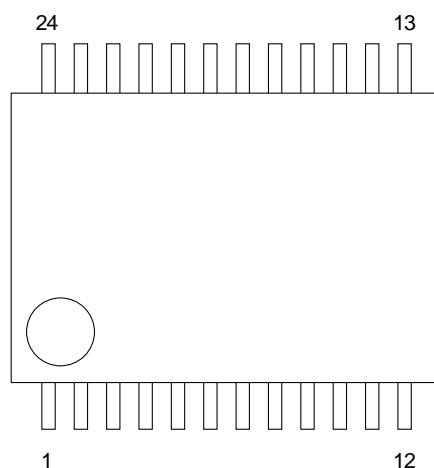
(8) Electric charge discharging circuit

This circuit discharges the electric charge remaining in the VOUT3 pin and VOUT4 pin to the VSS level. This circuit will work when the POFFX pin is set to the VSS level.

S1F75510

■ PIN ASSIGNMENT

SSOP3–24pin S1F75510M0A0



Pin No.	Pin name	Pin No.	Pin name
1	C3N	13	MODE
2	C3P	14	CL
3	C4P	15	POFFX
4	C4N	16	OSC1
5	VOUT3	17	OSC2
6	VDD	18	OSCSEL
7	C1N	19	VOUT2
8	C1P	20	VOUT4
9	VOUT1	21	C6P
10	C2P	22	C6N
11	C2N	23	C5N
12	VSS	24	C5P

■ PIN DESCRIPTION

(1) CR oscillation circuit · Mode changeover circuit · Timing signal forming circuit · Electric charge discharging circuit

Pin name	I/O	Pin No.	Function													
POFFX	I	15	This is the shut down pin. Set it to the VDD level while the IC is in operation. When this signal is set to the VSS level, operations of all the circuits will be interrupted bringing the IC into the shut down state. The electric charge discharging circuit discharges the electric charge remaining in the VOUT3 pin and VOUT4 pin to the VSS level.													
OSC1	I	16	This is the CR oscillation circuit gate input pin. This is the pin to connect the oscillation resistor. Fix it to the VSS level in case the built-in oscillation circuit will not be used.													
OSC2	O	17	This is the CR oscillation circuit drain input pin. Connect the oscillation resistor between this pin and the OSC1 pin.													
CL	I	14	This is the boosting external clock signal input pin. Input the charge pump clock signals under the blank mode into this pin.													
MODE	I	13	This is the mode changeover pin.													
OSCSEL	I	18	This is the pin for selection between the internal clock and external clock signals. <table border="1" data-bbox="686 1075 1460 1993"> <thead> <tr> <th>MODE</th> <th>OSCSEL</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td rowspan="2">HIGH(VDD)</td> <td>HIGH(VDD)</td> <td>Normal mode</td> </tr> <tr> <td>LOW(VSS)</td> <td>The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate.</td> </tr> <tr> <td rowspan="2">LOW(VSS)</td> <td>HIGH(VDD)</td> <td>Blank mode (internal oscillation) The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate under low current consumption state.</td> </tr> <tr> <td>LOW(VSS)</td> <td>Blank mode (external oscillation) The boosting clock signals are being generated by the external clock. The built-in oscillation circuit will be interrupted and the voltage stabilizing circuit will operate under low current consumption state.</td> </tr> </tbody> </table>	MODE	OSCSEL	Function	HIGH(VDD)	HIGH(VDD)	Normal mode	LOW(VSS)	The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate.	LOW(VSS)	HIGH(VDD)	Blank mode (internal oscillation) The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate under low current consumption state.	LOW(VSS)	Blank mode (external oscillation) The boosting clock signals are being generated by the external clock. The built-in oscillation circuit will be interrupted and the voltage stabilizing circuit will operate under low current consumption state.
MODE	OSCSEL	Function														
HIGH(VDD)	HIGH(VDD)	Normal mode														
	LOW(VSS)	The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate.														
LOW(VSS)	HIGH(VDD)	Blank mode (internal oscillation) The boosting clock signals are being generated through the internal oscillation. The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate under low current consumption state.														
	LOW(VSS)	Blank mode (external oscillation) The boosting clock signals are being generated by the external clock. The built-in oscillation circuit will be interrupted and the voltage stabilizing circuit will operate under low current consumption state.														

S1F75510

(2) x2 boosting circuit in the positive direction

Pin name	I/O	Pin No.	Function
VOUT1	O	9	This is the output pin of the x2 boosting circuit in the positive direction.
C1P	(O)	8	This is the pin to connect the positive side of the VOUT1 output voltage generating flying capacitor C1.
C1N	(O)	7	This is the pin to connect the negative side of the VOUT1 output voltage generating flying capacitor C1.
C2P	(O)	10	This is the pin to connect the positive side of the VOUT1 output voltage generating flying capacitor C2.
C2N	(O)	11	This is the pin to connect the negative side of the VOUT1 output voltage generating flying capacitor C2.

(3) Voltage stabilizing circuit

Pin name	I/O	Pin No.	Function
VOUT1	I	9	This is the input power pin (+) for the voltage stabilizing circuit. This pin is being connected to the output pin of the x2 boosting circuit in the positive direction internally, inside this IC.
VOUT2	O	19	This is the output pin of the voltage stabilizing circuit.

(4) x3 boosting circuit in the positive direction

Pin name	I/O	Pin No.	Function
VOUT3	O	5	This is the output pin of the x3 boosting circuit in the positive direction.
C3P	(O)	2	This is the pin to connect the positive side of the VOUT3 output voltage generating flying capacitor C3.
C3N	(O)	1	This is the pin to connect the negative side of the VOUT3 output voltage generating flying capacitor C3.
C4P	(O)	3	This is the pin to connect the positive side of the VOUT3 output voltage generating flying capacitor C4.
C4N	(O)	4	This is the pin to connect the negative side of the VOUT3 output voltage generating flying capacitor C4.

(5) X3 boosting circuit in the negative direction

Pin name	I/O	Pin No.	Function
VOUT4	O	20	This is the output pin of the X3 boosting circuit in the negative direction.
C5P	(O)	24	This is the pin to connect the positive side of the VOUT4 output voltage generating flying capacitor C5.
C5N	(O)	23	This is the pin to connect the negative side of the VOUT4 output voltage generating flying capacitor C5.
C6P	(O)	21	This is the pin to connect the positive side of the VOUT4 output voltage generating flying capacitor C6.
C6N	(O)	22	This is the pin to connect the negative side of the VOUT4 output voltage generating flying capacitor C6.

(6) Power pins

Pin name	I/O	Pin No.	Function
VDD	I	6	This is the input power pin (+).
VSS	I	12	This is the input power pin (-).

S1F75510

■ FUNCTIONAL DESCRIPTION

● Operational description

Generating voltage levels are:

- Positive boosting supply voltage necessary for the voltage stabilizing circuit (VOUT1)
- Positive stabilized supply voltage necessary for the source driver (VOUT2)
- Positive and negative boosting supply voltages necessary for the gate driver (VOUT3 and VOUT4)

The VOUT1 supply voltage is being generated by the charge pump type DC/DC converter (x2 boosting circuit in the positive direction). It makes x2 boosting in the positive direction of the potential difference occurring between the VDD – VSS using the VSS potential as the reference voltage.

The VOUT2 supply voltages is being generated by the series regulator stabilizing the potential difference occurring between the VOUT1 – VSS using the VSS potential as the reference voltage.

The VOUT3 supply voltage is being generated by the charge pump type DC/DC converter (x3 boosting circuit in the positive direction). It makes x3 boosting in the positive direction of the potential difference occurring between the VOUT2 – VSS using the VSS potential as the reference voltage.

The VOUT4 supply voltage is being generated by the charge pump type DC/DC converter (x3 boosting circuit in the negative direction). It makes x3 boosting in the negative direction of the potential difference occurring between the VOUT2 – VSS using the VOUT2 potential as the reference voltage.

Indicated below is the system configuration diagram for the power circuit.

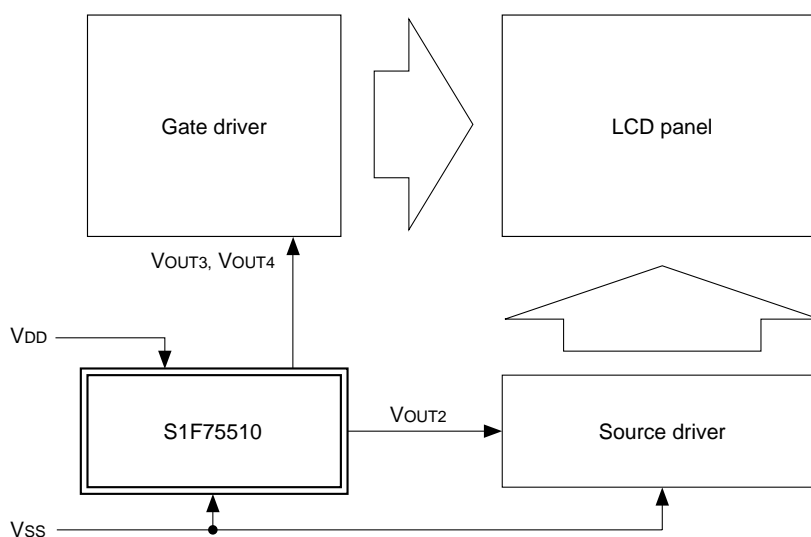


Fig. 2 System configuration diagram

Indicated below is the potential correlation diagram inside the system as is shown in Fig. 2.

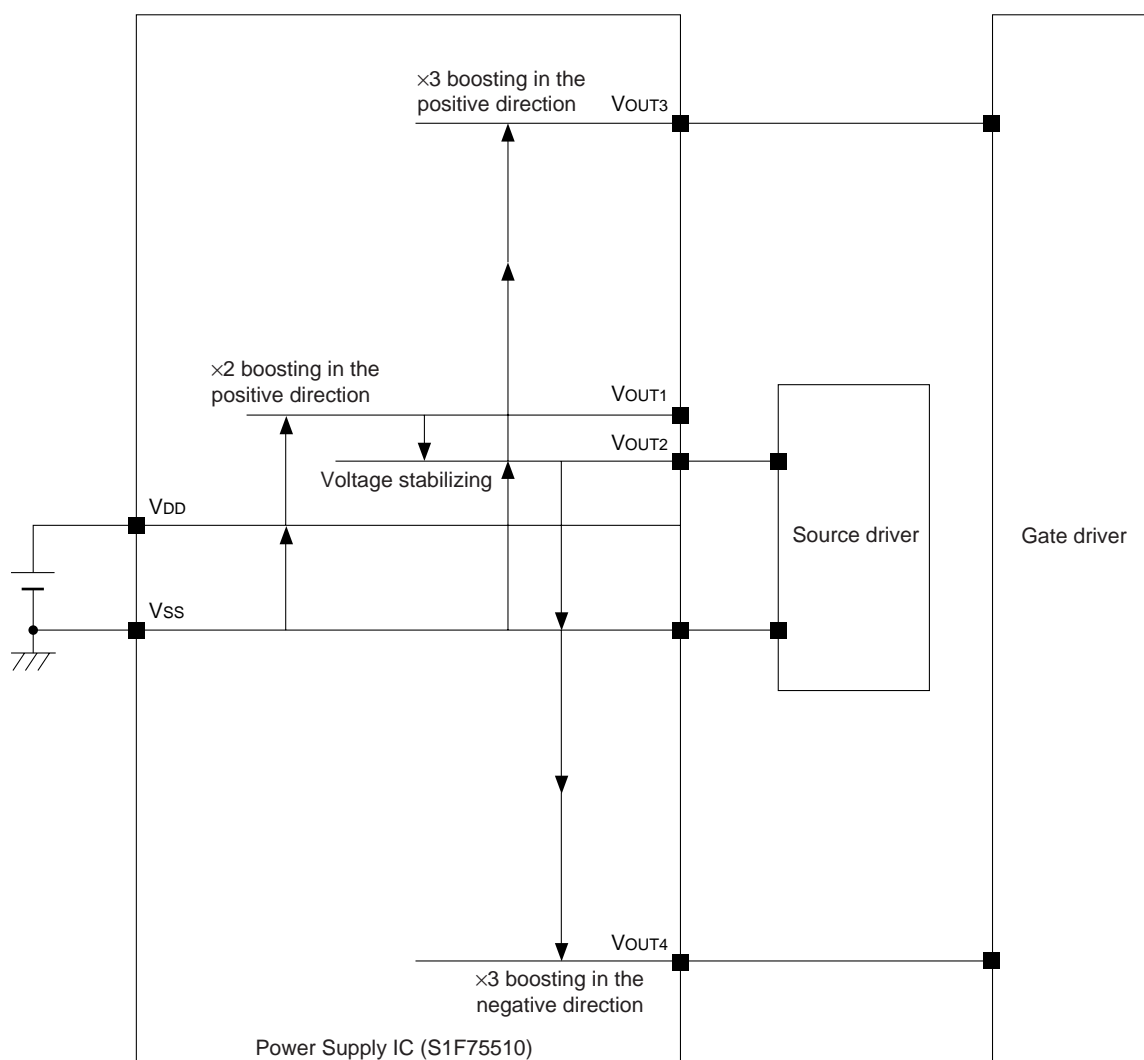


Fig. 3 Potential correlation diagram inside the system

● CR oscillation circuit

The S1F75510 incorporates a CR oscillation circuit as the oscillation circuit for the boosting clock signals. This circuit is to be used connecting the external oscillation resistor ROSC between the OSC1 pin and the OSC2 pin. The CR oscillation circuit will stop operation under the blank mode and when using the external clock (MODE = Vss level and OSCSEL = Vss level) or under the shut down state (POFFX = Vss level). Also, the oscillation will be interrupted by setting the OSC1 pin to the VSS level and, at the same time, setting the OSC2 pin into open state.

As the external oscillation resistance, we recommend use of ROSC = 1 MΩ.

S1F75510

● Mode changeover circuit

By external settings of the mode changeover signal MODE and the internal/external clock selection signal OSCSEL, the charge pump boosting can be driven under optimum frequencies. Since the current consumption of the IC can be suppressed drastically under the blank mode, it is possible to achieve high power conversion efficiency even under light load operations.

MODE pin	OSCSEL pin	Mode name	Max. output current	Built-in CR oscillation circuit	Built in voltage stabilizing circuit
HIGH(VDD)	HIGH(VDD) LOW(VSS)	Normal mode	VOUT2:(10mA) (TBD)	In operation	In normal operation
			VOUT3:(100μA) (TBD)		
			VOUT4:(100μA) (TBD)		
LOW(VSS)	HIGH(VDD)	Blank mode	VOUT2:(200μA) (TBD)	In operation	In low current consumption operation
			VOUT3:(10μA) (TBD)		
	LOW(VSS)	Blank mode	VOUT2:(200μA) (TBD)	In standstill	In low current consumption operation
			VOUT3:(10μA) (TBD)		
			VOUT4:(10μA) (TBD)		

● Timing signal forming circuit

This circuit generates the clock signals necessary for charge pump boosting using the internal oscillation or using external clock signals.

Two different types of capacitors are being used as the charge pump capacitors, one being the flying capacitor which shifts between the charging state and the discharging state and the other being the smoothing capacitor which preserves the electric charge. The operating frequency of the flying capacitor should equal to the frequency of the charge pump clock being generated by this timing signal forming circuit.

Under the shut down state (POFFX = Vss level), the charge pump clock stops operation and all the boosting operations of this IC will be interrupted. The operating frequencies of the flying capacitor are as follows.

MODE pin	OSCSEL pin	Mode name	Operating frequencies of the flying capacitor		
			×2 boosting in the positive direction	×3 boosting in the positive direction	×3 boosting in the negative direction
HIGH(VDD)	HIGH(VDD) LOW(VSS)	Normal mode	(TBD) kHz	(TBD) kHz	(TBD) kHz
			(Typ.10 kHz)	(Typ.10 kHz)	(Typ.10 kHz)
LOW(VSS)	HIGH(VDD)	Blank mode	(TBD) kHz	(TBD) kHz	(TBD) kHz
			(Typ.625 Hz)	(Typ.625 Hz)	(Typ.625 Hz)
	LOW(VSS)	Blank mode CL=(TBD) Hz (Min.300 Hz)	(TBD) Hz (Min.150 Hz)	(TBD) Hz (Min.150 Hz)	(TBD) Hz (Min.150 Hz)

● X2 boosting circuit in the positive direction

The X2 boosting circuit in the positive direction generates the voltages necessary to input into the voltage stabilizing circuit. It makes X2 boosting in the positive direction of the potential difference occurring between the $V_{DD} - V_{SS}$ using the V_{SS} potential as the reference voltage to output through the V_{OUT1} pin.

Under the blank mode, since the boosting operation is being carried out with the flying capacitor C2 stopping its operation, the current consumption can be suppressed accordingly.

The theoretical equation (output voltage value under the idealistic non-load state) for the V_{OUT1} becomes as follows:

$$V_{OUT1} = (V_{DD} - V_{SS}) \times 2$$

Actually, when a load is connected to the V_{OUT1} , the output voltage will drop to the value represented by the equation indicated below.

$$V_{OUT1} = (V_{DD} - V_{SS}) \times 2 - R_{VOUT1} \times I_{VOUT1}$$

R_{VOUT1} : Output impedance of the x2 boosting circuit in the positive direction

I_{VOUT1} : Load current

● Voltage stabilizing circuit

The voltage stabilizing circuit stabilizes the voltage being output through the V_{OUT1} pin by the series regulator to output the positive supply voltage for the source driver through the V_{OUT2} pin.

The output voltage setting for the V_{OUT2} pin should be Typ. +5.0V (TBD).

Since it is necessary to let the V_{OUT1} satisfy the correlation of " $V_{OUT1} > V_{OUT2} + 0.1V$ " in order to obtain normal output voltage value through the V_{OUT2} pin, use the IC within the range of the max. load current (7.3).

The circuit configuration · connection diagram for the voltage stabilizing circuit is as follows:

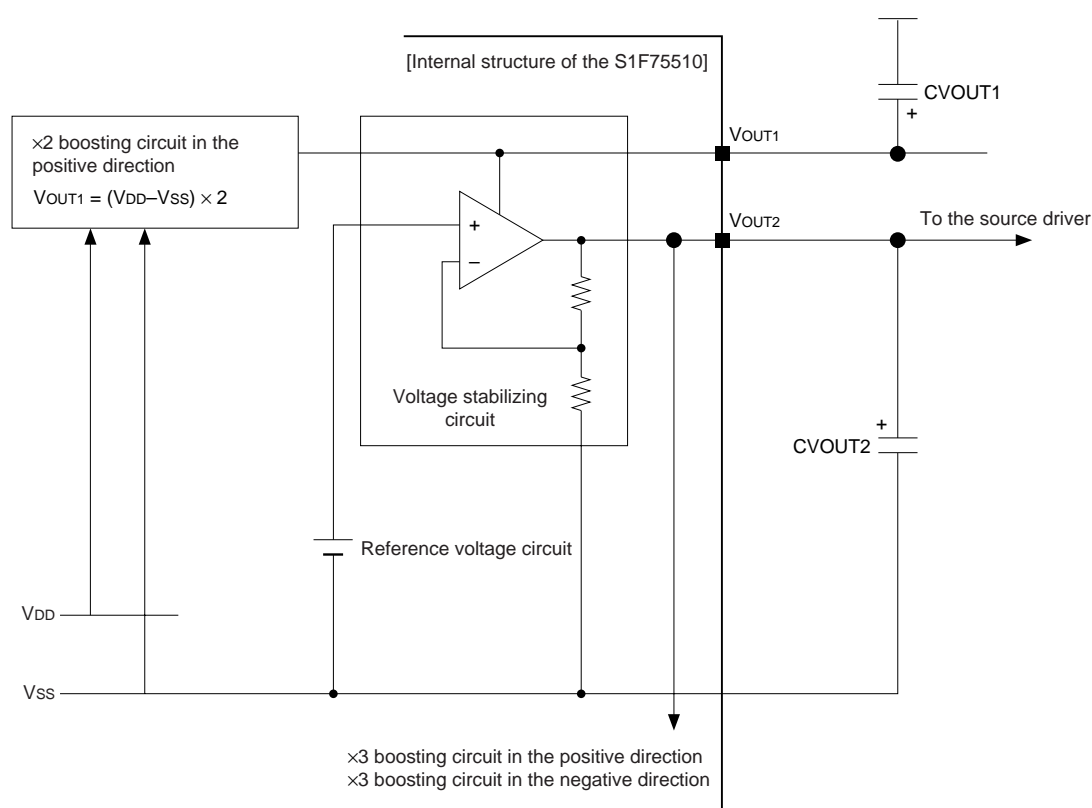


Fig. 4 Configuration diagram of the voltage stabilizing circuit

● X3 boosting circuit in the positive direction

The X3 boosting circuit in the positive direction generates the VOUT3 output voltage, means the positive supply voltage for the gate driver. It makes X3 boosting in the positive direction of the potential difference occurring between the VOUT2 – VSS using the VSS potential as the reference voltage, by charge pump boosting, to output through the VOUT3 pin.

The theoretical equation (output voltage value under the idealistic non-load state) for the VOUT3 becomes as follows:

$$V_{OUT3} = (V_{OUT2} - V_{SS}) \times 3$$

Actually, when a load is connected to the VOUT3, the output voltage will drop to the value represented by the equation indicated below.

$$V_{OUT3} = (V_{OUT2} - V_{SS}) \times 3 - (R_{VOUT3} \times I_{VOUT3})$$

R_{VOUT3} : Output impedance of the X3 boosting circuit in the positive direction

I_{VOUT3} : Load current

It means that the VOUT3 voltage will drop by the load.

To acquire desired output voltage, use the IC within the range of the specified load (7.3).

● X3 boosting circuit in the negative direction

The X3 boosting circuit in the negative direction generates the VOUT3 output voltage, means the negative supply voltage for the gate driver. It makes X3 boosting in the negative direction of the potential difference occurring between the VOUT2 – VSS using the VOUT2 potential as the reference voltage, by charge pump boosting, to output through the VOUT4 pin.

The theoretical equation (output voltage value under the idealistic non-load state) for the VOUT4 becomes as follows:

$$V_{OUT4} = (V_{OUT2} - V_{SS}) \times (-2) \quad (\text{The voltage value using the VSS potential as the reference voltage})$$

Actually, when a load is connected to the VOUT4, the output voltage will drop to the value represented by the equation indicated below.

$$V_{OUT4} = (V_{OUT2} - V_{SS}) \times (-2) - (R_{VOUT4} \times I_{VOUT4})$$

R_{VOUT4} : Output impedance of the X3 boosting circuit in the negative direction

I_{VOUT4} : Load current

It means that the VOUT4 voltage will drop by the load.

To acquire desired output voltage, use the IC within the range of the specified load (7.3).

● Electric charge discharging circuit

The electric charge discharging circuit discharges the electric charge remaining in the VOUT3 pin and VOUT4 pin to the VSS level.

This circuit starts operation when the POFFX pin is set to the VSS level.

The discharging sequence and the discharging impedance are according to the (TBD).

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating		Unit	Applicable pin	Remarks
		Min.	Max.			
Input supply voltage	VDD	- 0.3	4.0	V	VDD	—
Output voltage 1	VOUT1	- 0.3	7.5	V	VOUT1	—
Output voltage 2	VOUT2	- 0.3	7.5	V	VOUT2	—
Output voltage 3	VOUT3	- 0.3	22.5	V	VOUT3	—
Output voltage 4	VOUT4	- 15.0	0.3	V	VOUT4	—
Input pin voltage 1	VIN	- 0.3	VDD + 0.3	V	<Note 1>	—
Input current	IVDD	—	(TBD)	mA	VDD	
Output current 1	IVOUT1	—	(TBD)	mA	VOUT1	—
Output current 2	IVOUT2	—	(TBD)	mA	VOUT2	—
Output current 3	IVOUT3	—	(TBD)	mA	VOUT3	—
Output current 4	IVOUT4	—	(TBD)	mA	VOUT4	—
Allowable dissipation	PD	—	(TBD)	mW	—	Ta ≤ 55°C
Operating temperature	Topr	- 30	85	°C	—	—
Storage temperature	Tstg	- 55	150	°C	—	—
Soldering temperature and time	Tsol	—	260·10	°C·s	—	At leads

<Note 1> The applicable pins are POFFX, OSC1, CL, MODE and OSCSEL.

<Note 2> Do not apply external voltage to the output pins and the pin connecting to the capacitor.

<Note 3> Use of the IC under any conditions exceeding the above absolute maximum ratings may cause malfunctioning or permanent breakdown. Or, even if the IC may operate normally temporarily, the reliability may greatly drop.

S1F75510

■ ELECTRICAL CHARACTERISTICS

● DC characteristics

In case particular designations are not made (Note 1): Ta = -10 to +70°C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Input supply voltage	VDD	Applicable pin: VDD	(TBD)	3.0	3.6	V	—
High level input voltage	VIH	—	0.8VDD	—	VDD	V	2
Low level input voltage	VIL	—	0	—	0.2VDD	V	2
Input leak current 1	ILKI1	VSS ≤ VI ≤ VDD, VDD = (TBD) to 3.6V	-0.5	—	0.5	μA	2
Current consumption 1	IOPR1	VDD = 3.0V, no load Under the normal mode	—	(TBD) (300)	(TBD)	μA	—
Current consumption 2	IOPR2	VDD = 3.0V, no load Under the blank mode CL = (TBD) kHz	—	(TBD) (30)	(TBD)	μA	—
Power conversion efficiency 1 (Overall efficiency including the stabilized outputs)	Peff1	VDD = 3.0V Under the normal mode	(TBD)	(TBD)	(TBD)	%	3
Power conversion efficiency 2 (Overall efficiency including the stabilized outputs)	Peff2	VDD = 3.0V Under the blank mode CL = (TBD) kHz	(TBD)	(TBD)	(TBD)	%	4
Resting current	IQ	VDD = 3.6V POFFX = LOW	—	—	(TBD) (1.0)	μA	—

<Note 1> Conditions on the operation mode, external parts constant, pins, etc. in case particular designations are not made are as follows.

Connection and parts constant : Standard connection 1, 10.1

MODE pin : MODE = HIGH (Normal mode)

CL pin : CL = LOW (Fixed voltage)

<Note 2> The applicable pins are XDIS, SSLP, PCK1 and CNT

<Note 3> Load conditions: IVOUT2 = (TBD)mA, IVOUT3 = (TBD)μA, IVOUT4 = (TBD)μA

Conversion efficiency = $[(V_{OUT2} \times I_{VOUT2}) + (V_{OUT3} \times I_{VOUT3}) + (V_{OUT4} \times I_{VOUT4})] / (V_{DD} \times I_{VDD}) \times 100$

<Note 4> Load conditions: IVOUT2 = (TBD)μA, IVOUT3 = (TBD)μA, IVOUT4 = (TBD)μA

Conversion efficiency = $[(V_{OUT2} \times I_{VOUT2}) + (V_{OUT3} \times I_{VOUT3}) + (V_{OUT4} \times I_{VOUT4})] / (V_{DD} \times I_{VDD}) \times 100$

● Characteristics of X2 boosting in the positive direction + stabilized output

Ta = -10 to +70°C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
VOUT1 output impedance (Normal mode)	RVOUT1-1	Applicable pin: VOUT1	—	(TBD)	(TBD)	Ω	5
VOUT1 output impedance (Blank mode)	RVOUT1-2	Applicable pin: VOUT1	—	(TBD)	(TBD)	Ω	6
VOUT2 Stabilized output voltage	VOUT2	Applicable pin: VOUT2	(TBD) (4.90)	(TBD) (5.00)	(TBD) (5.20)	V	7
VOUT2 Stabilized output saturated resistance	RVOUT2	Applicable pin: VOUT2	—	—	10	Ω	8

<Note 5> VDD = (TBD)V to 3.6V, Load condition: IVOUT1 = (TBD)mA

<Note 6> VDD = (TBD)V to 3.6V, Load condition: IVOUT1 = (TBD)mA

<Note 7> VDD = (TBD)V to 3.6V, Load condition: IVOUT2 = (TBD)mA

<Note 8> VDD = (TBD)V to 3.6V, Load condition: IVOUT2 = (TBD)mA

● Characteristics of X3 boosting in the positive direction and X3 boosting in the negative direction

Ta = -10 to +70°C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
VOUT3 output impedance (Normal mode)	RVOUT3-1	Applicable pin: VOUT3	—	(TBD)	(TBD)	Ω	9
VOUT3 output impedance (Blank mode)	RVOUT3-2	Applicable pin: VOUT3	—	(TBD)	(TBD)	Ω	10
VOUT4 output impedance (Normal mode)	RVOUT4-1	Applicable pin: VOUT4	—	(TBD)	(TBD)	Ω	11
VOUT4 output impedance (Blank mode)	RVOUT4-2	Applicable pin: VOUT4	—	(TBD)	(TBD)	Ω	12

<Note 9> VDD = (TBD)V to 3.6V, Load condition: IVOUT3 = (TBD)μA

<Note 10> VDD = (TBD)V to 3.6V, Load condition: IVOUT3 = (TBD)μA

<Note 11> VDD = (TBD)V to 3.6V, Load condition: IVOUT4 = (TBD)μA

<Note 12> VDD = (TBD)V to 3.6V, Load condition: IVOUT4 = (TBD)μA

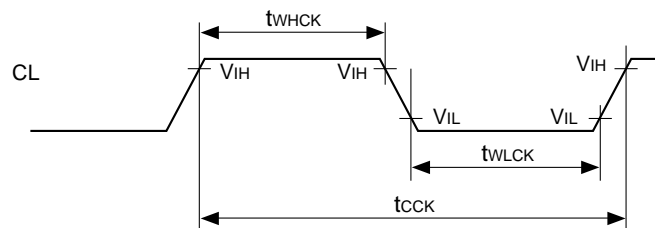
S1F75510

● AC characteristics

Measurement conditions for the AC characteristics

- Input signal level $V_{IH} = 0.8 V_{DD}$ (V)
 $V_{IL} = 0.2 V_{DD}$ (V)
- Input signal rise time $T_r = \text{Max. } 100\text{ns}$
- Input signal fall time $T_f = \text{Max. } 100\text{ns}$
- $V_{DD} = (\text{TBD}) \text{ to } 3.6\text{V}$, $V_{SS} = 0\text{V}$
- $T_a = -10 \text{ to } +70^\circ\text{C}$

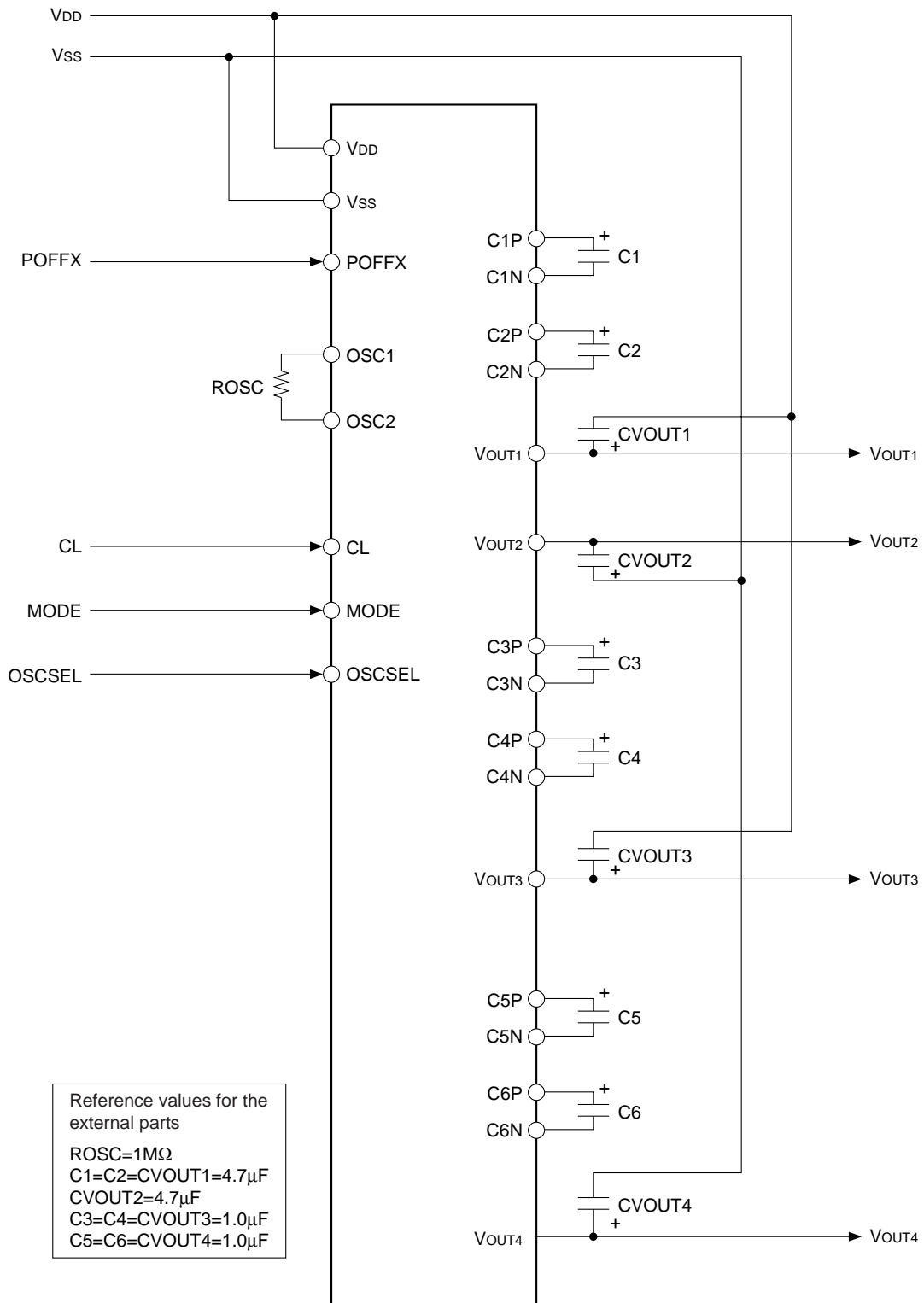
CL inputting timing



Item	Symbol	Rating			Unit	Applicable pin	Remarks
		Min.	Typ.	Max.			
CL cycle	t_{CCK}	(TBD)	(TBD)	(TBD)	μs	CL	—
CL High pulse duration	t_{WHCK}	(TBD)	—	—	ns		
CL Low pulse duration	t_{WLCK}	(TBD)	—	—	ns		

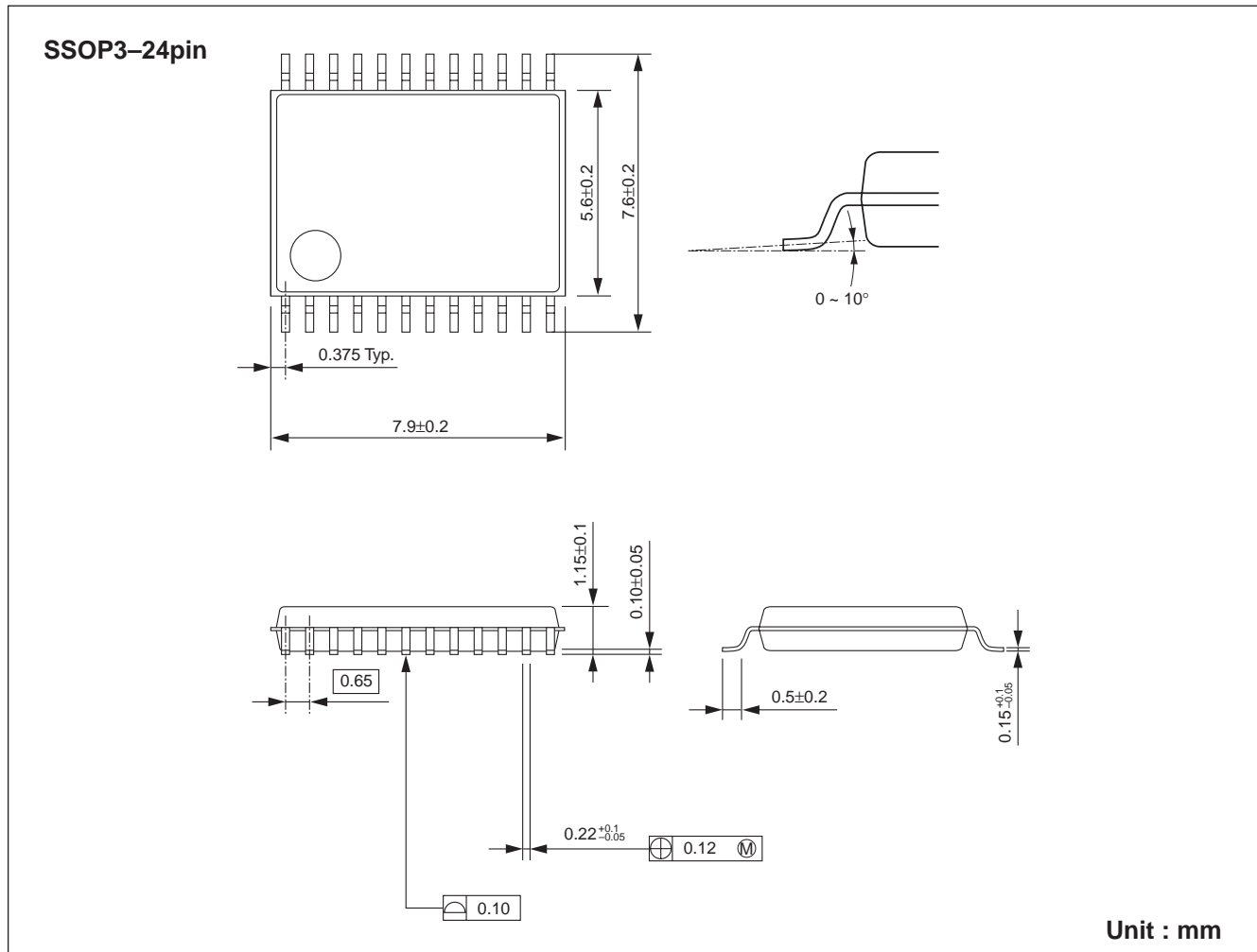
REFERENCE EXTERNAL CONNECTION (AN EXAMPLE)

Standard connection 1



S1F75510

■ DIMENSIONAL OUTLINE DRAWING



NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 2001, All rights reserved.

All other product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department Europe & U.S.A

421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5812 FAX: 042-587-5564

ED International Marketing Department Asia

421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5814 FAX: 042-587-5110

■ EPSON Electronic Devices Website

<http://www.epson.co.jp/device/>



First issue July, 2001

Printed in Japan ⊕

Rev. 1.0