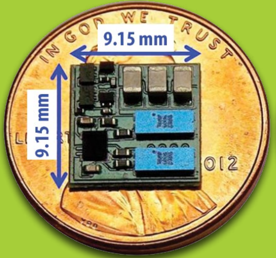
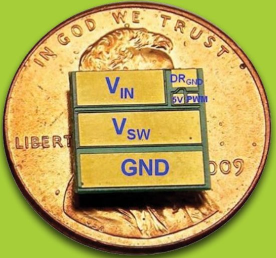
DrGaN*PLUS* Development Board - EPC9202
Quick Start Guide

Optimized Half-Bridge Circuit for eGaN® FETs



Single PWM Input



Optimized Half Bridge Circuit

EFFICIENT POWER CONVERSION

DESCRIPTION

This development board, measuring 0.36″ x 0.36″, contains two enhancement mode (*eGaN*®) field effect transistors (FETs) arranged in a half bridge configuration with an onboard Texas Instruments LM5113 gate drive and is driven by a single PWM input. The purpose of these development boards is to simplify the evaluation process by optimizing the layout and including all the critical components on a single board that can be easily connected into any existing converter. A complete block diagram of the circuit is given in Figure 1.

For more information on EPC's family of *eGaN* FETs, please refer to the datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		4.5	5	V
V_{IN}	Bus Input Voltage Range			70*	V
V_{OUT}	Switch Node Output Voltage			100	V
I_{OUT}	Switch Node Output Current			10*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	60		ns
	Minimum 'Low' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	200 #		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.

\# Limited by time needed to 'refresh' high side bootstrap supply voltage.

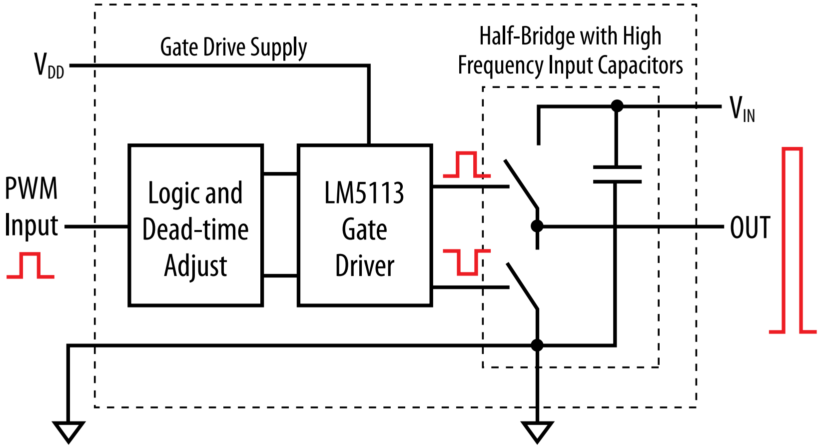


Figure 1: Block Diagram of Development Board

THERMAL CONSIDERATIONS

The development board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The development board does not have any current or thermal protection on board.

EPC9202

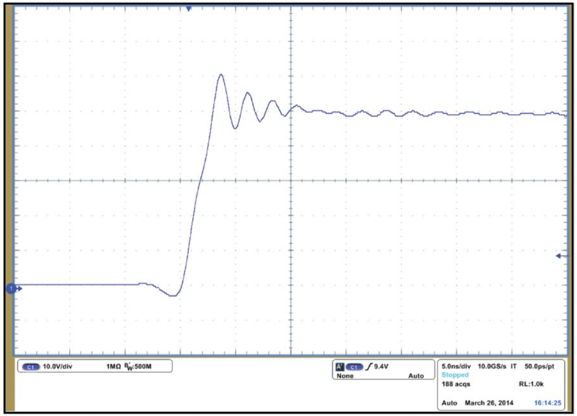


Figure 2: Typical switch node voltage rising waveform for V_{IN} = 48 V to V_{OUT} =12 V, I_{OUT} =10 A, f_{sw}=300 kHz buck converter

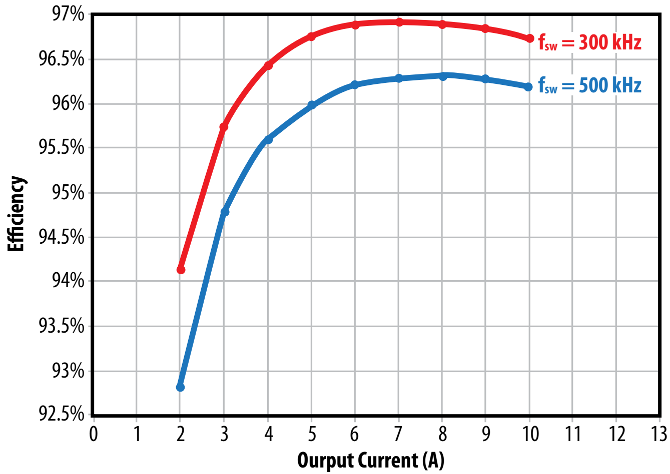


Figure 3: Typical efficiency for V_{IN}=48 V to V_{OUT} = 12 V buck converter with 100 V devices (Inductor: Coilcraft SER1390-103MLB)

DESIGN CONSIDERATIONS

To improve the electrical and thermal performance of the DrGaN*PLUS* development board some design considerations are recommended:

1. Large copper planes should be connected to the development board to improve thermal performance as shown in figures 4 through 6. If filled vias are used in the board design, thermal vias should be placed under the device as shown in figure 4 to better distribute heat through buried inner layers. For a design without filled vias, thermal vias should be located outside of the development board as shown in figure 6. Also, for a design without filled vias, the vias to make the V_{DD} connection should be tented and located outside of the V_{DD} pad.
2. To reduce conduction losses, the inductor and output capacitors should be located in close proximity to the development board.
3. The smaller IC ground connection (pin 6 in mechanical drawings), should be isolated from the power ground connection (pin 3 in mechanical drawings).
4. If additional input filter capacitance is required, it can be placed outside the module. Due to the internal on-board input capacitance, minimizing the distance of the additional input capacitors to the development board, while preferred, is not a design requirement.

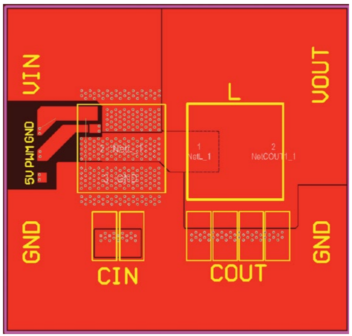


Figure 4: Top layer layout with filled thermal vias

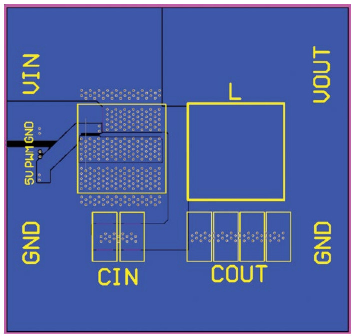


Figure 5: Bottom layer layout

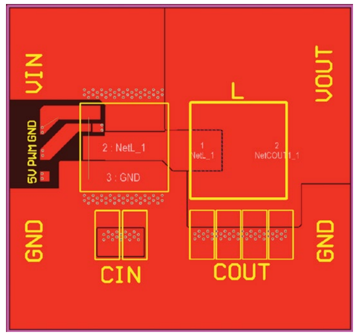
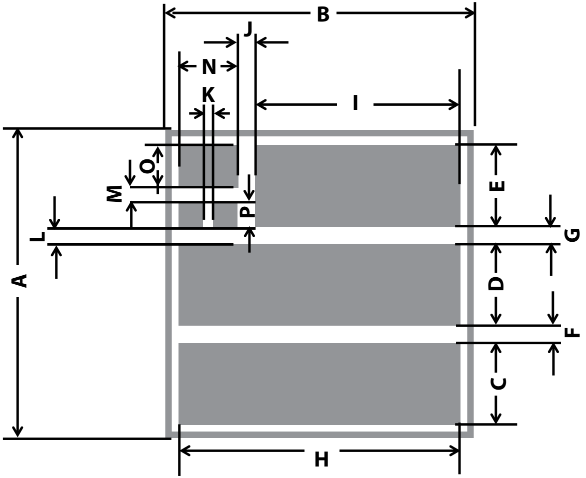
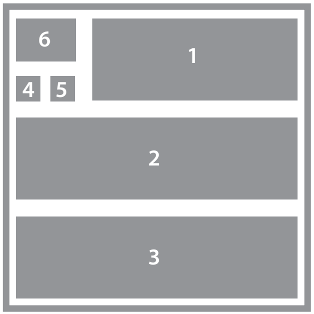


Figure 6: Top layer layout without filled thermal vias

MECHANICAL DATA





Pin 1: Input Voltage, V_{IN}

Pin 2: Switching Node, V_{SW}

Pin 3: Power Ground, P_{GND}

Pin 4: PWM Input, PWM

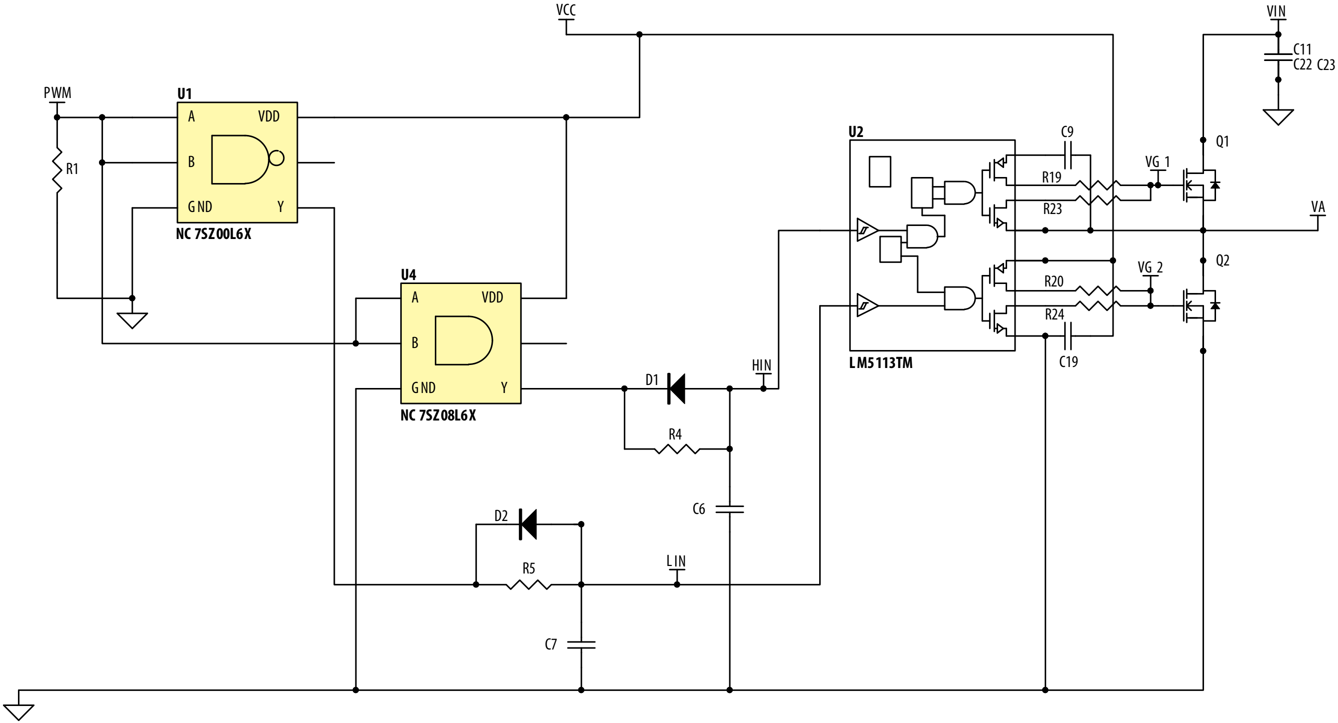
Pin 5: Driver Voltage, V_{DD}

Pin 6: IC Ground, A_{GND}

A	9.15 mm
B	9.15 mm
C	2.5 mm
D	2.5 mm
E	2.6 mm
F	0.525 mm
G	0.525 mm
H	8.475 mm
I	6.15 mm
J	0.525 mm
K	0.2 mm
L	0.475 mm
M	0.45 mm
N	1.8 mm
O	1.4 mm
P	0.8 mm

Table 2 : Bill of Materials

Item	Board Qty	Part Description	Manufacturer / Part #	Component
1	3	C11, C22, C23	Capacitor, 1uF, 20%, 100V, X7S, 0805	TDK, C2012X7S2A105M125AB
2	2	Q1, Q2	100 V 25 A eGaN FET	EPC, EPC2001
3	4	R19, R20, R23, R24	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00TR
4	1	C9	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K050BC
5	1	C19	Capacitor, 1uF, 10%, 16V, X5R	TDK, C1005X5R1C105K050BC
6	1	U2	I.C., Gate driver	Texas Instruments, LM5113
7	2	D1, D2	Diode Schottky 40 V 0.12A SOD882	NXP, BAS40L,315
8	1	U4	IC GATE AND UHS 2-INP 6-MICROPAK	Fairchild, NC7SZ08L6X
9	1	U1	IC GATE NAND UHS 2-INP 6MICROPAK	Fairchild, NC7SZ00L6X
10	1	R1	Resistor, 10K Ohm 1/20W 1% 0201	Stackpole, RMCF0201FT10K0
11	2	C6, C7	Capacitor, CER 100pF 25V 5% NP0 0201	TDK, C0603C0G1E101J030BA
12	1	R4	Resistor, 0 OHM 1/20W 0201 SMD	Panasonic, ERJ-1GN0R00C
13	1	R5	Resistor, 56 Ohm 1/20W 1% 0201 SMD	Panasonic, ERJ-1GEF56R0C



Development Board Schematic
Rev 0