Development Board EPC9065 Quick Start Guide

EPC2007C, EPC8010

6.78 MHz, High Power ZVS Class-D Development Board

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9065 is a high efficiency, Zero Voltage Switching (ZVS) differential mode Class-D amplifier development board that operates at, but is not limited to, 6.78 MHz (Lowest ISM band). The purpose of this development board is to simplify the evaluation process of a high power ZVS Class-D amplifier for use in applications such as A4WP wireless power using eGaN® FETs by including all the critical components on a single board that can be easily connected into an existing system. To support the increased power capability, two mounted heat sinks are included.

The amplifier board features the EPC2007C and the EPC8010, which are 100 V rated enhancement-mode gallium nitride FETs (eGaN® FET). The EPC2007C is used in the Class-D amplifier while the EPC8010 is used as a synchronous bootstrap FET. The amplifier can be set to operate in either differential mode or single ended mode and includes the gate drivers and 6.78 MHz oscillator.

For more information on the EPC2007C or EPC8010 eGaN FETs please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC9065

Symbol	Parameter	Conditions	Min	Max	Units
V_{DD}	Logic Input Voltage Range		7.5	12	V
V_{AMP}	Amp Input Voltage Range		0	80	V
V_{OUTA}	Switch Node Output Voltage			80	V
V_{OUTB}	Switch Node Output Voltage			80	V
I_{OUT}	Switch Node Output Current (each)			1.8*	A_{RMS}
V_{extosc}	External Oscillator Input Threshold	Input 'Low' Input 'High'	-0.3 3.5	0.8 5	V V
$V_{Osc\_Disable}$	Oscillator Disable Voltage Range	Open drain/ collector	-0.3	5	V
$I_{Osc\_Disable}$	Oscillator Disable Current	Open drain/ collector	-25	25	mA

** Maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.*

DETAILED DESCRIPTION

The EPC9065 consists of a differential mode ZVS Class-D amplifier, a 6.78 MHz oscillator, and a separate heat sink for each Class-D section. The power schematic of the EPC9065 is shown in figure 1.

For operating frequencies other than 6.78 MHz, the oscillator can be disabled by placing a jumper into J60 or can be externally shutdown using an externally controlled open collector / drain transistor on the terminals of J60 (note which is the ground connection). The oscillator disable switch needs to be capable of sinking at least 25 mA. The external oscillator can then be connected to J71.

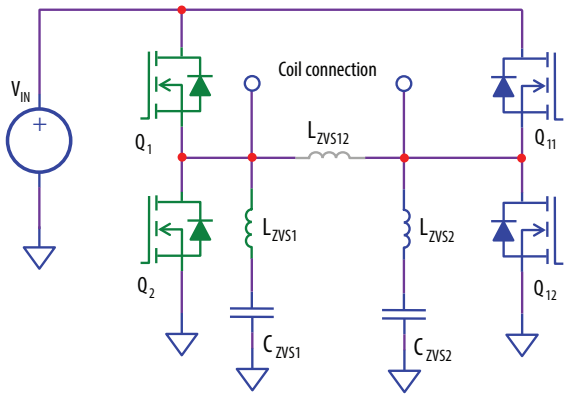


Figure 1: Power schematic of the EPC9065 differential mode ZVS amplifier

ZVS Timing Adjustment

Setting the correct time to establish ZVS transitions is critical to achieving high efficiency with the EPC9065 amplifier. This can be done by selecting the values for R71, R72, R73, and R74 respectively. This procedure is best performed using a potentiometer installed at the appropriate locations (P71, P72, P73, and P74) that is used to determine the fixed resistor values. The timing MUST initially be set without a load connected to the amplifier. The timing diagrams are given in figure 4 and should be referenced when following this procedure. Only perform these steps if changes have been made to the board as it is shipped preset. The steps are:

1. With power off, connect the logic input supply (7.5 - 12 V) to V_{DD} connector (J90). Note the polarity of the supply connector.
2. Connect a LOW capacitance oscilloscope probe to the probe-hole of the half-bridge to be set and lean it against the ground post as shown in figure 3.
3. Turn on the logic supply – make sure the supply is set to approximately 7.5 - 12 V.
4. Turn on the main supply voltage to 5 V to ensure that the switch node waveform looks similar to figure 4. If not, adjust the potentiometers. After verification, the main supply voltage can be set to the required predominant operating value (such as 24 V but NEVER exceed the absolute maximum voltage of 80 V).
5. While observing the oscilloscope, adjust the applicable potentiometers to achieve the green waveform of figure 4.
6. Repeat for the other half-bridge.
7. Replace the potentiometers with fixed value resistors if required.

Determining component values for L_{ZVS}

The ZVS tank circuit is not operated at resonance, and only provides the necessary negative device current for self-commutation of the output voltage at turn off. The capacitors C_{ZVS1} and C_{ZVS2} are chosen to have a very small ripple voltage component and are typically around 1 µF. The amplifier supply voltage, switch-node transition time will determine the value of inductance for L_{ZVSx} which needs to be sufficient to maintain ZVS operation over the DC device load resistance range and coupling between the device and source coil range and can be calculated using the following equation:

$$L_{ZVS} = \frac{\Delta t_{vt}}{8 \cdot f_{sw} \cdot (2 \cdot C_{OSSQ} + C_{well})} \quad (1)$$

Where:

Δt_{vt} = Voltage Transition Time [s]

f_{SW} = Operating Frequency [Hz]

C_{OSSQ} = Charge Equivalent Device Output Capacitance [F]

C_{well} = Gate Driver Well Capacitance [F]. For the LM5113, use 20 pF.

NOTE. The amplifier supply voltage V_{AMP} is absent from the equation as it is accounted for by the voltage transition time. The per device charge equivalent capacitance can be determined using the following equation:

$$C_{OSSQ} = \frac{1}{V_{AMP}} \cdot \int_0^{V_{AMP}} C_{OSS}(v) \cdot dv \quad (2)$$

To add additional immunity margin for shifts in load impedance, the value of L_{ZVS} can be decreased to increase the current at turn off of the devices (which will increase device losses). Typical voltage transition times range from 2 ns through 12 ns. For the differential case the voltage and charge (C_{OSSQ}) are doubled when calculating the ZVS inductance.

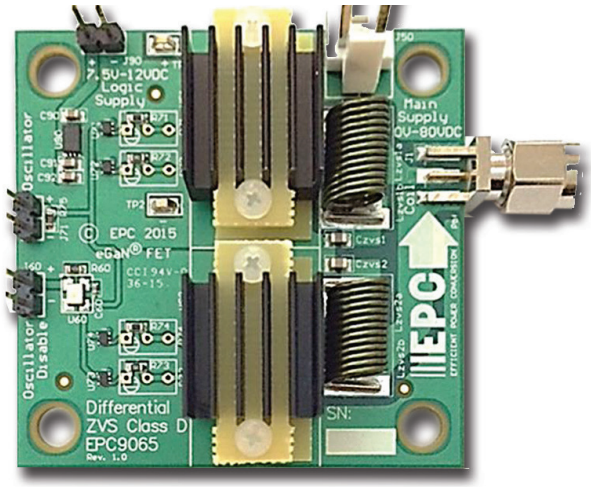
QUICK START PROCEDURE

The EPC9065 amplifier board is easy to set up and evaluate the performance of the eGaN FET in a wireless power transfer application.

Please note that main power is connected directly to the amplifier. Hence, there is no thermal or over-current protection to ensure the correct operating conditions for the eGaN FETs. If the main power is sourced from a benchtop DC power supply, it is highly advised to set a reasonable current limit of 500 – 800 mA during initial evaluation.

1. Make sure the entire system, including the heat sink assembly, is fully assembled prior to making electrical connections. This includes any load to be connected.
2. With power off, connect the main input power supply bus to the bottom pin of J50 and the ground to the ground connection of J50 as shown in figure 2.
3. With power off, connect the logic input power supply bus to $+V_{DD}$ (J90). Note the polarity of the supply connector. This is used to power the gate drivers and logic circuits.
4. Make sure all instrumentation is connected to the system.
5. Turn on the logic supply – make sure the supply is between 7.5 - 12 V.
6. Turn on the main supply voltage, starting at 0 V and increasing slowly to the required value (it is recommended to start at 5 V for dead time tuning purposes and do not exceed the absolute maximum voltage of 80 V).
7. Once operation has been confirmed, adjust the main supply voltage within the operating range and observe the output voltage, efficiency and other parameters on both the amplifier and device boards.
8. For shutdown, please follow steps in the reverse order. Start by reducing the main supply voltage to 0 V followed by steps 6 through 2.

NOTE. When measuring the high frequency content switch-node (Source Coil Voltage), care must be taken to avoid long ground leads. An oscilloscope probe connection (preferred method) has been built into the board to simplify the measurement of the Source Coil Voltage (shown in figure 3).



EPC9065 amplifier board with heat sink photo

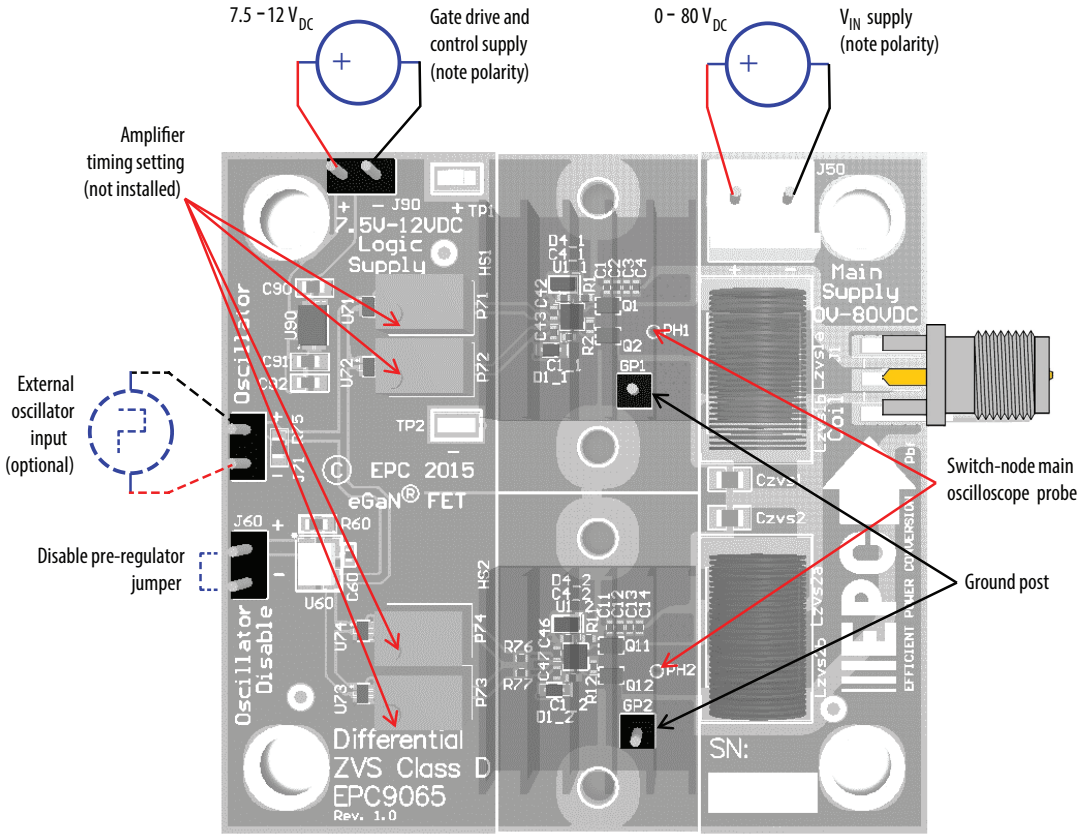


Figure 2: Proper connection and measurement setup for the amplifier board

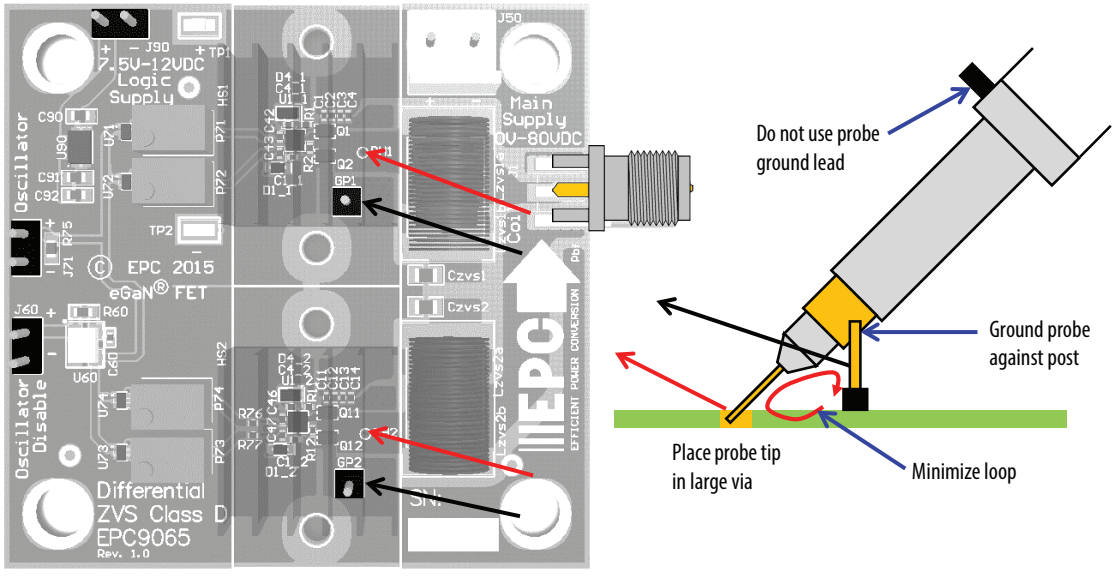


Figure 3: Proper measurement of the switch nodes using the hole and ground post

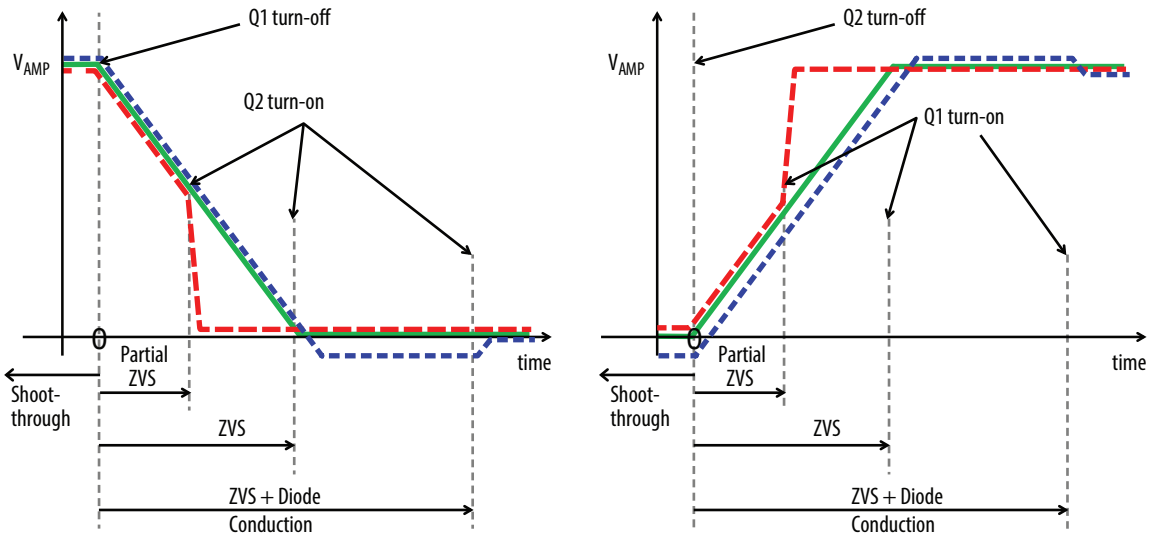


Figure 4: ZVS timing diagrams

THERMAL CONSIDERATIONS

The EPC9065 development board showcases the EPC2007C and EPC8010 eGaN FETs in a ZVS Class-D amplifier application. Although the electrical performance surpasses that of traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The operator must observe the temperature of the gate driver and eGaN FETs to ensure that both are operating within the thermal limits as per the datasheets.

A heat sink kit is mounted on each half bridge of the EPC9065 board. Figure 5 shows the assembly order for the heat sink kit.

NOTE. The EPC9065 development board has no current protection on board and care must be exercised not to over-current or over-temperature the devices. Excessively wide coil coupling and load range variations can lead to increased losses in the devices.

Precautions

The EPC9065 development board has no controller or enhanced protection systems and therefore should be operated with caution. Some specific precautions are:

1. It is highly advised to set a reasonable current limit of 500 - 800 mA during initial evaluation.
2. Ensure that the gap pad included in the heat sink assembly is firmly compressed on the eGaN FETs prior to full power operation. Be careful not to damage the die by over-tightening of the bolts.
3. Please contact EPC at info@epc-co.com should there be questions regarding specific load range impedance requirements.

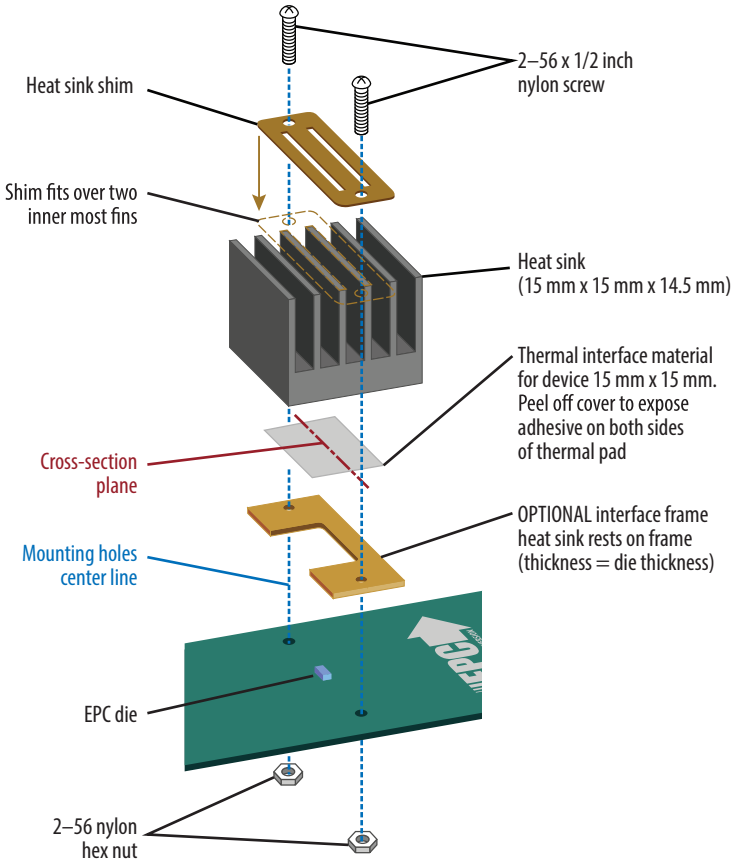


Figure 5: Heat sink kit assembly

Table 2: Bill of Materials - Amplifier Board				
Item	**Qty**	**Reference**	**Part Description**	**Manufacturer, Part Number**
1	2	C1_1, C1_2	Capacitor, Ceramic, 4.7 µF, 10 V, ±20%, X5R	Samsung, CL05A475MP5NRNC
2	4	C5, C6, C15, C16	Capacitor, Ceramic, 2.2 µF 100 V, ±10%, X7R	Taiyo Yuden, HMK325B7225KN-T
3	2	Czvs1, Czvs2	Capacitor, Ceramic, 1.0 µF, 50 V, ±10%, X7R	Taiyo Yuden, C2012X7R1H105K125AB
4	3	C90, C91, C92	Capacitor, Ceramic, 1.0 µF, 25 V, ±10%, X7R	TDK, C1608X7R1E105K
5	11	C71, C72, C73, C74, C2_1, C2_2, C4_1, C4_2, C5_1, C5_2, C60	Capacitor, Ceramic, 100 nF, 25 V, ±10%, X5R	TDK, C1005X5R1E104K050BC
6	8	C1, C2, C3, C4, C11, C12, C13, C14	Capacitor, Ceramic, 10 nF, 100 V, ±10%, X7S	TDK, C1005X7S2A103K050BB
7	2	C3_1, C3_2	Capacitor, Ceramic, 22 nF, 25 V, ±10%, X7R	TDK, C1005X7R1E223K050BB
8	4	C42, C43, C46, C47	Capacitor, Ceramic, 22 pF, 50 V, ±5%, NPO	TDK, C1005C0G1H220J050BA
9	1	R60	Resistor, 47 KΩ, ±5%, 1/10 W	Stackpole, RMCF0603JT47K0
10	1	R75	Resistor, 10 KΩ, ±5%, 1/10 W	Stackpole, RMCF0603FT10K0
11	2	R3_1, R3_2	Resistor, 2.74 KΩ, ±1%, 1/16 W	Panasonic, ERJ-2RKF2741X
12	2	R71, R74	Resistor, 470 Ω, ±1%, 1/16 W	Stackpole, RMCF0603FT470R
13	2	R72, R73	Resistor, 390 Ω, ±1%, 1/16 W	Stackpole, RMCF0603FT390R
14	2	R2_1, R2_2	Resistor, 20 Ω, ±5%, 1/16 W	Stackpole, RMCF0402FT20R0
15	2	R4_1, R4_2	Resistor, 6.8 Ω, ±5%, 1/10 W	Panasonic, ERJ-2GEJ6R8X
16	4	R1, R2, R11, R12	Resistor, 2.2 Ω, ±5%, 1/16 W	Yageo, RC0402JR-072R2L
17	2	R76, R77	Resistor, 0 Ω, 1/16 W, Jumper	Yageo, RC0402JR-070RL
18	2	Lzvs1b, Lzvs2b	Inductor, 390 nH, ±5%, ±2%, Q=180 I_{RMS}=4.4 A, 14.5 mΩ, Resonance=590 MHz	Coilcraft, 2929SQ-391JEB
19	8	D2_1, D2_2, D3_1, D3_2, D71, D72, D73, D74	Diode, Schottky Diode, 30 V, V_F=370 mV at 1 mA, 30 mA	Diodes Inc, SDM03U40-7
20	2	D4_1, D4_2	Diode, Zener, 5.1 V, 150 mW ±5%	Bourns Inc., BZT52C5V1T-7
21	2	D1_1, D1_2	Diode, Schottky, 40 V, 300 mA, V_F=900 mV at 100 mA	ST Microelectronics, BAT54KFILM
22	4	Q1, Q2, Q11, Q12	eGaN® FET, 100 V, 6 A, $R_{DS(on)}$=30 mΩ at 6 A, 5 V	EPC, EPC2007C
23	2	Q4_1, Q4_2	eGaN® FET, 100 V, 3.4 A, $R_{DS(on)}$=160 mΩ at 500 mA	EPC, EPC8010
24	1	U90	IC's, 5 V LDO, 250 mA, up to 16 V_{IN}, $V_{dropout}$=0.33 V at 250 mA	Microchip, MCP1703T-5002E/MC
25	2	U1_1, U1_2	IC's, Gate Driver, 5.2 VDC, 1.2 A, 4.5 V to 5.5 V	Texas Instruments, LM5113TME/NOPB
26	2	U72, U74	IC's, Logic 2 NAND Gate, 1.65 V to 5.5 V, ± 24 mA	Fairchild, NC7SZ00L6X
27	2	U71, U73	IC's, 2 Input NAND Gate, Tiny Logic, 1.65 V to 5.5 V, ± 32 mA	Fairchild, NC7SZ08L6X
28	1	U60	IC's, Programmable Oscilator 1.5 to 60 MHz, V_{IN}=1.8 V/2.5 V/2.8 V/3.0 V/3.3 V/5.0 V	Daishinku, DSO221SHF 6.780
29	2	TP1, TP2	Test Point, Test Point Subminiature	Keystone, 5015
30	3	J60, J71, J90	Header, Male Vertical, 36 Pin. 230" Contact Height, .1" Center Pitch	FCI, 68001-236HLF
31	1	J1	Connector, RP-SMA Plug, 50 Ω	Linx, CONREVSMA013.062
32	1	J50	Connector, Header 2 Pin .156 Pitch Vertical Gold	Molex Inc, 26614020
33	1	PCB1	PCB, EPC9065 REV 1	CCI, EPC9065 REV 1
34	1	C75	Capacitor, DNP, 100 pF, 25 V	Generic
35	4	P71, P72, P73, P74	Potentiometer, DNP, Multi Turn Potentiometer, 1 kΩ, ±10%, 1/4 W, 12 Turn Top Adjustment Small	Murata, PV37Y102C01B00
36	2	Lzvs1a, Lzvs2a	Inductor, DNP, 270 nH, ±5%, Q= 150, DCR= 12.5, F=50 MHz	CoilCraft, 2222SQ-271JEB
37	1	C44	IC's, DNP, Programmable Oscillator 3.3 V, OE, Demo is pre-programmed to 6.78 MHz	EPSON, SG-8002CE-PHB, or KDS Daishinku America, DSO221SHF 6.780/1XSF006780EH
38	2	GP1, GP2	Header, DNP .1" Male Vert.	Tyco, 4-103185-0-01

EPC would like to acknowledge Coilcraft (www.coilcraft.com) and KDS Daishinku America (www.kdsamerica.com) for their support of this project.

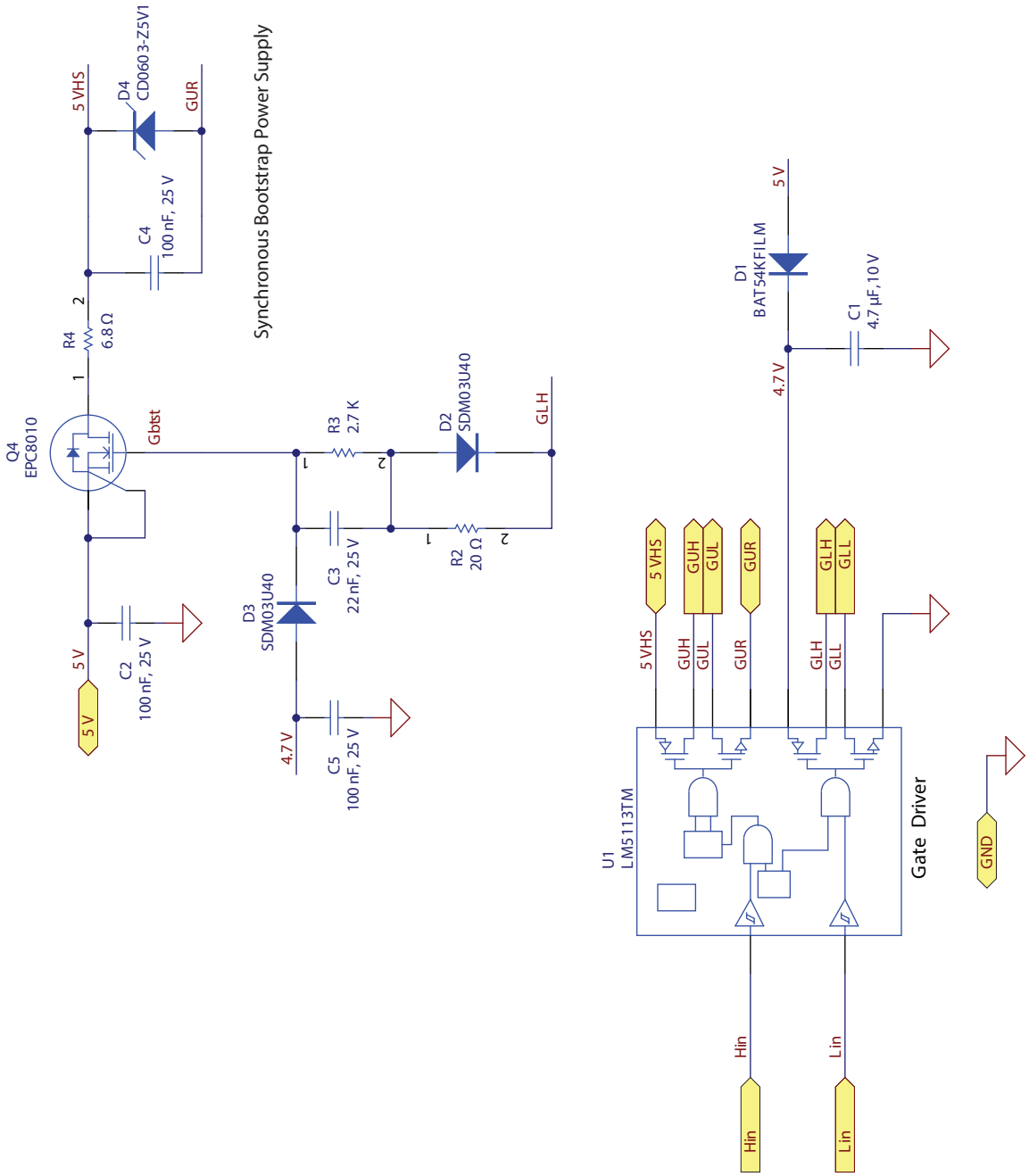


Figure 6: EPC9065 - Gate Driver Schematic

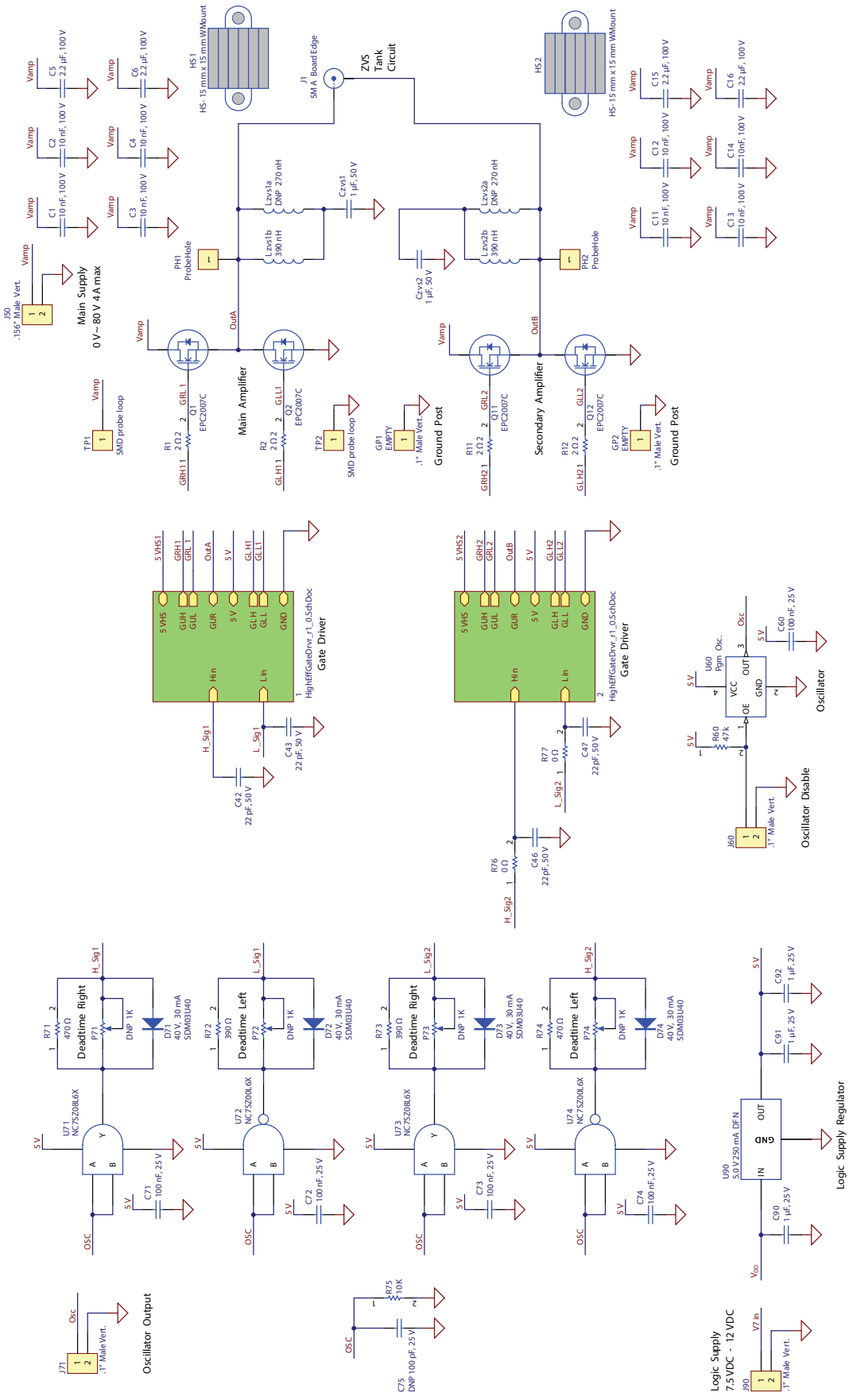


Figure 7: EPC9065 – ZVS Class D Schematic

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