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Datasheet
EC19D01
(Preliminary)

econais
Powers the Internet of Things

Revision History

Rev	Date	Comments
1	21-Oct-2013	Initial document release

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1 Module Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

2 List of Acronyms

Acronym	Description
802.11™	WLAN specification defined by a working group within the IEEE
AP	WLAN Access Point
BOM	Bill of Material
BPSK	Binary Phase Shift Keying
BT	Bluetooth
CCK	Complementary Code Keying
COB	Chip on Board
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DTIM1	Delivery Traffic Indication Message – 100ms beacon interval
DTIM3	Delivery Traffic Indication Message – 300ms beacon interval
FW	Firmware
HFC	WLAN, High Frequency Clock, 26 or 40 MHz
I/O	Input/Output
IC	Integrated Circuit
LDO	Low-dropout regulator
LFC	Low Frequency Clock, 32.768 kHz Real Time Clock
LNA	Low Noise Amplifier
MIB	Management Information Base
MIMO	Multiple-In, Multiple-Out
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PLL	Phase Locked Loop
POR	Power On Reset
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature phase-shift keying
RAM	Random Access Memory
RF	Radio Frequency
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
STBC	Space-Time Block Coding
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator

3 Device details, block diagram and schematics

General Description

EC19D01 is an 802.11bgn WLAN module including RF frontend circuitry, baseband, MAC, Clock Management and Power Management for direct battery operation. It also incorporates the balun and low pass filter and a 40MHz crystal. EC19D01 supports Bluetooth coexistence with the major Bluetooth chips available on the market.

EC19D01 is designed for direct PCB attach without under-fill and a low BOM cost for the total solution.

Key Features

- Compliant with 802.11b/g/n
- Supports direct attach to Li-Ion battery. Supports VBAT 2.7-4.5V with on-module power management.
- Class D stereo headphone drivers
- Digital Microphone input
- I2S and PCM external codec interface
- On-module IP stack and web server
- WiFi Direct Group Owner (GO and Client)
- Support for 802.11n up to MCS7, SGI 0.4us, STBC (Rx), L-SIG TXOP Protection, PSMP.
- BT ePTA/PTA Co-existence support.
- 802.1x, 802.11i, WEP, WPA, WPA2 (PSK/Enterprise, EAP), WPS security support, WAPI HW accelerator support.
- 802.11e including WMM/WMM-PS QoS support.
- 802.11d/h support
- Support of SDIO 2.0 (52 MHz) host interface.
- TX output power pre-calibrated in production.
- High integration level
    - External clock reference 26, 38.4, 40, 52 MHz support (tolerance +/- 20 ppm).
    - Integrated TX/RX switches
    - Fully integrated power management (DCDC).
    - Support external Power Management.
    - Integrated PA and LNA.

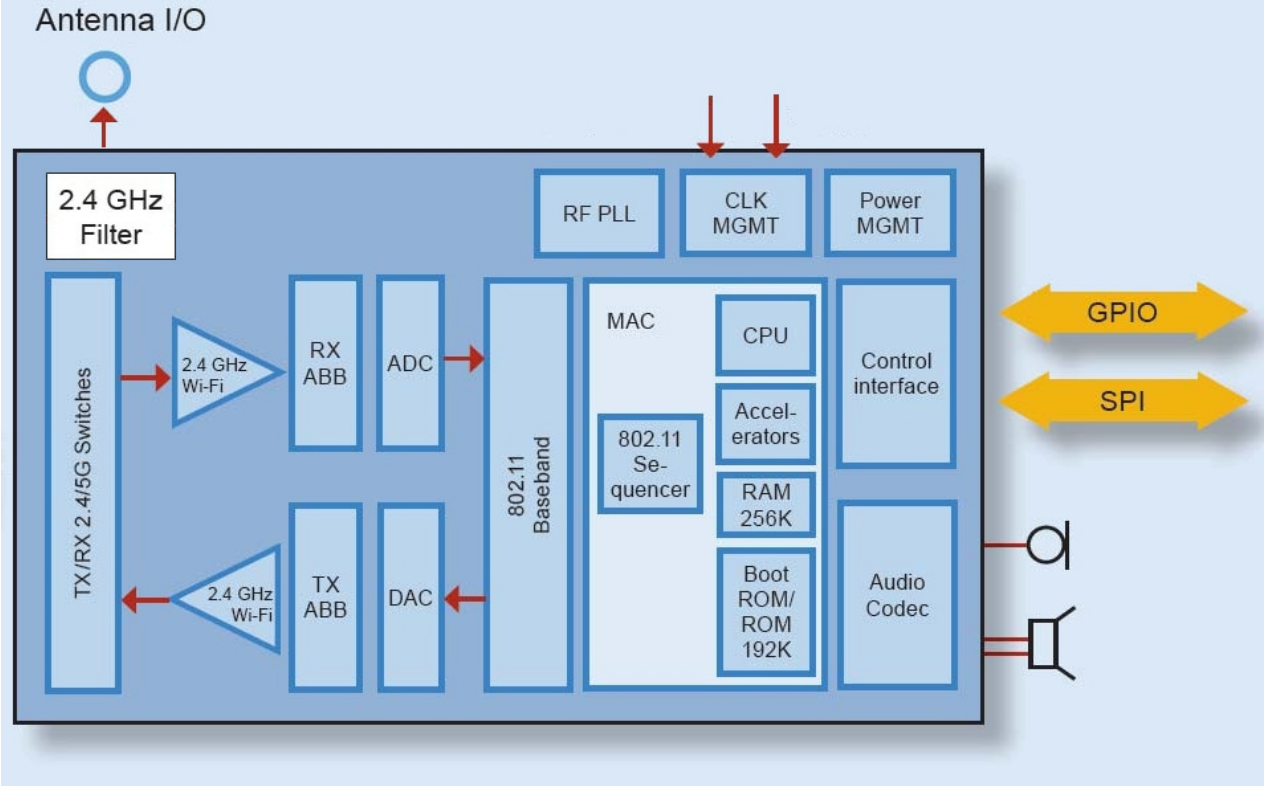
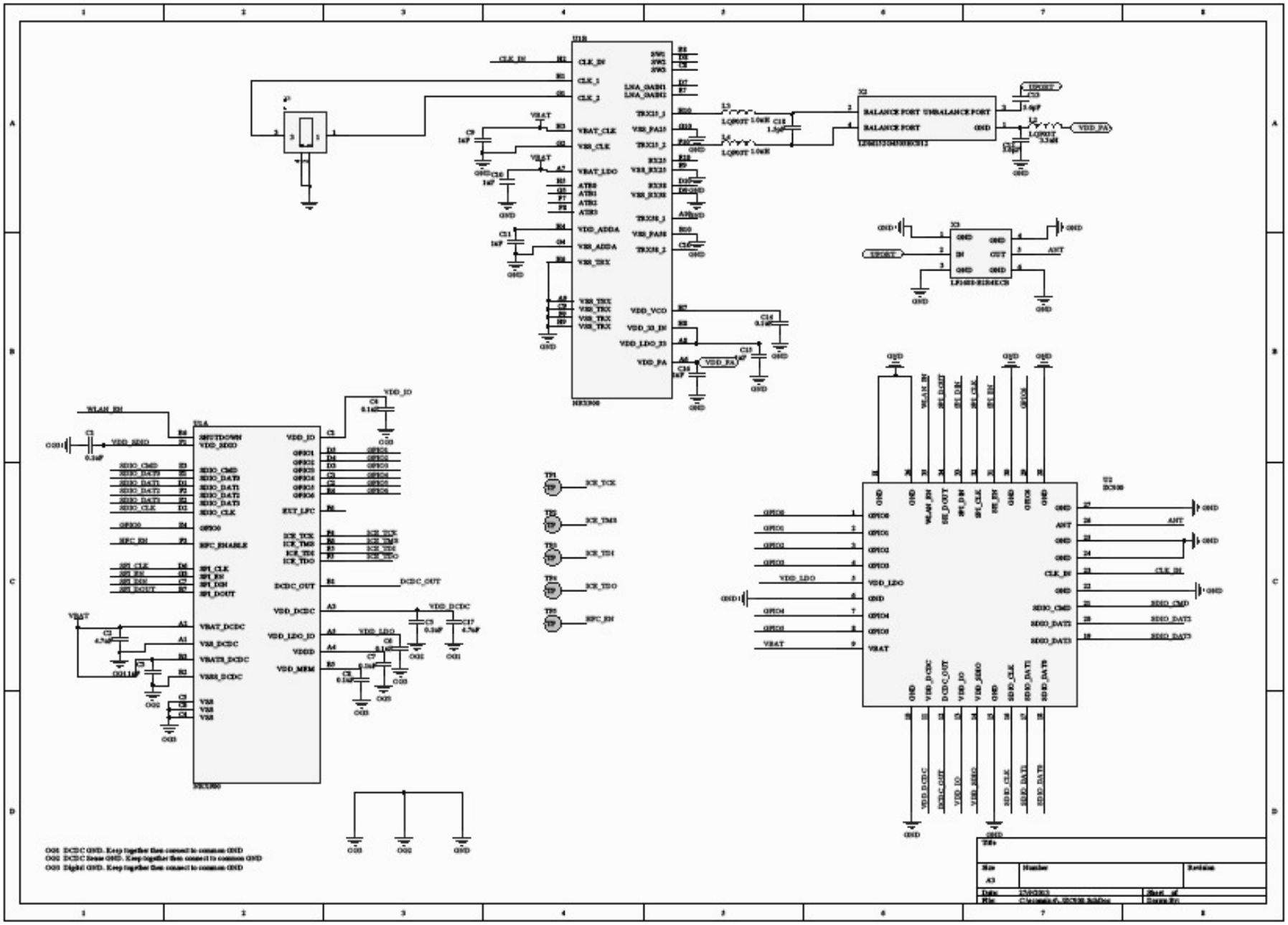


Figure 1: EC19D0x Block diagram



4 Electrical Data

4.1 Absolute Maximum Ratings

The absolute maximum ratings specify the values beyond which the device may be damaged permanently. Exposure to absolute maximum ratings conditions for extended periods of time may affect reliability. Each condition is applied with all other values kept within the recommended operating condition.

Symbol	Parameter	Min.	Max.	Unit
VBAT	Direct battery connect Supply voltage	0	4.8[1]	V
VDD_DCDC	Digital Supply voltage	-0.3		V
VDD_IO, VDD_SDIO	Supply voltage I/O	-0.3	3.6	V
Vin	Input voltage on any digital pin	-0.3	VDD_IO+0.3, VDD_SDIO+0.3	V
Vssdiff	Maximum voltage difference between different types of Vss pins			V
Tstg	Storage temperature	-65	125	°C

Table 1: Absolute maximum ratings

[1]: 5.5V acceptable for duration less than 2 ms

[2]: No Pb (Solder 40sec); Refer to the IPC/JEDEC J-STD-020C, July 2004.

4.2 Recommended Operating Conditions

The recommended operating conditions specify the values in which region the device is operational meeting specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tamb	Operating ambient temperature	-30		70	°C
VBAT	Direct battery connect Supply voltage. - All specs guaranteed. - All specs guaranteed with output power back-off - Device functional with reduced performance	2.7	3.6	4.5	V
VDD_DCDC,	Supply voltage		1.5		V
VDD_IO, VDD_SDIO	I/O supply voltage	1.62		3.6	V

Table 2: Recommended operating condition

4.3 Current Consumption

VBAT current consumption. RF power, Pout, is referenced to IC interface.

Conditions: VBAT= 3.6 V, Tamb = 25°C, internal DCDC for 1.5 Volt

Mode	Condition	Min	Typ	Max	Unit
Transmit 802.11b	CCK 11Mbps, Pout=21 dBm		220		mA
Transmit 802.11g	OFDM 54 Mbps, Pout=18 dBm		215		mA
Transmit 802.11n	OFDM 72.2 Mbps, Pout=17 dBm (2.4 GHz)		185		mA
Receive 802.11b	Normal mode – Max sensitivity		40		mA
Receive 802.11g/n	Normal mode – Max sensitivity		42		mA
P0 (Sleep Mode)			39		µA
Power Save DTIM1	Beacon interval 100ms		0.8		mA
Power Save DTIM3	Beacon interval 300ms		0.11		mA
Shutdown			10		µA

Table 3: Typical power consumption values in different modes

4.4 RF Performance

All data is referenced to the IC interface.

4.5 Channel Frequencies

Supported 2.4 GHz channels and frequencies according to IEEE802.11 b/g/n standard.

Channel no.	Frequency MHz	Note	Channel no.	Frequency MHz	Note
1	2412		8	2447	
2	2417		9	2452	
3	2422		10	2457	
4	2427		11	2462	
5	2432		12	2467	
6	2437		13	2472	
7	2442		14	2484	

Table 4: Channel and frequency table

4.6 Receiver Performance

Conditions: VBAT = 3.6 V. Tamb = 25°C.

Mode	Condition	Min	Typ	Max	Unit
Input level	All data rates, CCK FER < 8%, OFDM PER < 10%			-20	dBm
Adjacent channel rejection	11 Mbit/s, Pwanted = - 70 dBm	35			dB
	6 Mbit/s, Pwanted = - 79 dBm	16			dB
	54 Mbit/s, Pwanted = - 62 dBm	-1			dB
	72.2 Mbit/s, Pwanted = - 64 dBm	-2			dB

Table 5: Receiver performance

4.7 Receiver sensitivity

Conditions: VBAT = 3.6 V, Tamb = 25°C.

Band	Standard	Rate Mbps	Modulation/Coding Rate		Conditions	Module Port Specification			Units
						Min	Typ	Max	
2.4GHz	802.11b/g	1	DSSS		@ FER<8%, 1024 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-99,5		dBm
		2	DSSS				-97,0		dBm
		5,5	CCK				-94,5		dBm
		11	CCK				-91,0		dBm
		6	BPSK 1/2				-95,0		dBm
		9	BPSK 3/4				-93,5		dBm
		12	QPSK 1/2				-92,0		dBm
		18	QPSK 3/4				-90,0		dBm
		24	16QAM 1/2				-87,5		dBm
		36	16QAM 3/4				-84,0		dBm
		48	64QAM 2/3				-79,5		dBm
		54	64QAM 3/4				-78,0		dBm
	11n (OFDM, 20 MHz, Nss = 1)	7,2	MCS0	BPSK 1/2	@ PER<10%, 4096 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-93,5		dBm
		14,4	MCS1	QPSK 1/2			-90,5		dBm
		21,7	MCS2	QPSK 3/4			-88,5		dBm
		28,9	MCS3	16QAM 1/2			-85,5		dBm
		43,3	MCS4	16QAM 3/4			-82,0		dBm
		57,8	MCS5	64QAM 2/3			-78,0		dBm
		65	MCS6	64QAM 3/4			-76,5		dBm

		72,2	MCS7	64QAM 5/6			-74,5		dBm
	11n (OFDM, 40 MHz, Nss = 1)	15	MCS0	BPSK 1/2	@ PER<10%, 4096 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-90,5		dBm
		30	MCS1	QPSK 1/2			-87,5		dBm
		45	MCS2	QPSK 3/4			-85,5		dBm
		60	MCS3	16QAM 1/2			-82,5		dBm
		90	MCS4	16QAM 3/4			-79,0		dBm
		120	MCS5	64QAM 2/3			-75,0		dBm
		135	MCS6	64QAM 3/4			-73,5		dBm
		150	MCS7	64QAM 5/6			-71,5		dBm

Table 6:2.4 GHz Sensitivity (minimum input level)

4.8 Transmitter Performance

Conditions: VBAT = 3.6 V. Tamb = 25°C.

Fulfilled spectrum mask according to the IEEE 802.11b/g/n specification, calibrated.

Band	Std	BW	MCS	Conditions	Output Power (2.4 GHz) Mosule Port Specification				EVM	
					Min	Typ	Max	Units	Max	Units
2.4 GHz	11b/g	20	DSSS/CCK	Requirements at T=25 degrees and VBAT >= 3.3V; Load Z: 50 Ohms; Meeting spectral mask and regulatory requirements		21		dBm	15.0	%
			BPSK 1/2			21		dBm	13,00	%
			BPSK 3/4			21		dBm	13,00	%
			QPSK 1/2			21		dBm	13,00	%
			QPSK 3/4			21		dBm	13,00	%
			16QAM 1/2			20		dBm	9,00	%
			16QAM 3/4			19		dBm	7,00	%
			64QAM 2/3			18		dBm	5.6	%
			64QAM 3/4			18		dBm	5.6	%
	11n	20	MCS7			17		dBm	4.0	%

Table 7:Coding Rate dependent Output power vs. EVM for 2.4 GHz

4.9 Output Power vs. Supply Voltage

The figure below shows the allowed output power variations dependent of the VBAT_LDO supply voltage. This is controlled by FW and MIB settings.

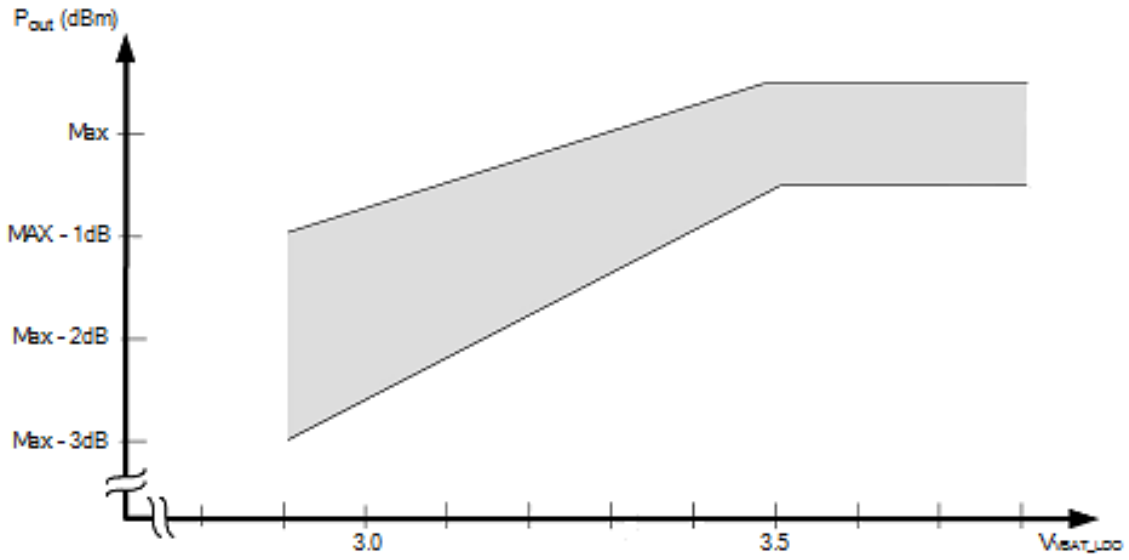


Figure 2: Output Power vs. Supply Voltage

4.10 Output Power vs. Temperature

The figure below shows the allowed variation of the output power versus temperature. The output power is controlled by FW in order to maximize the performance of the circuit without jeopardizing quality and function. Tested with the radio mounted on a PCB with the thermal resistance Tj-pin=40 deg/W.

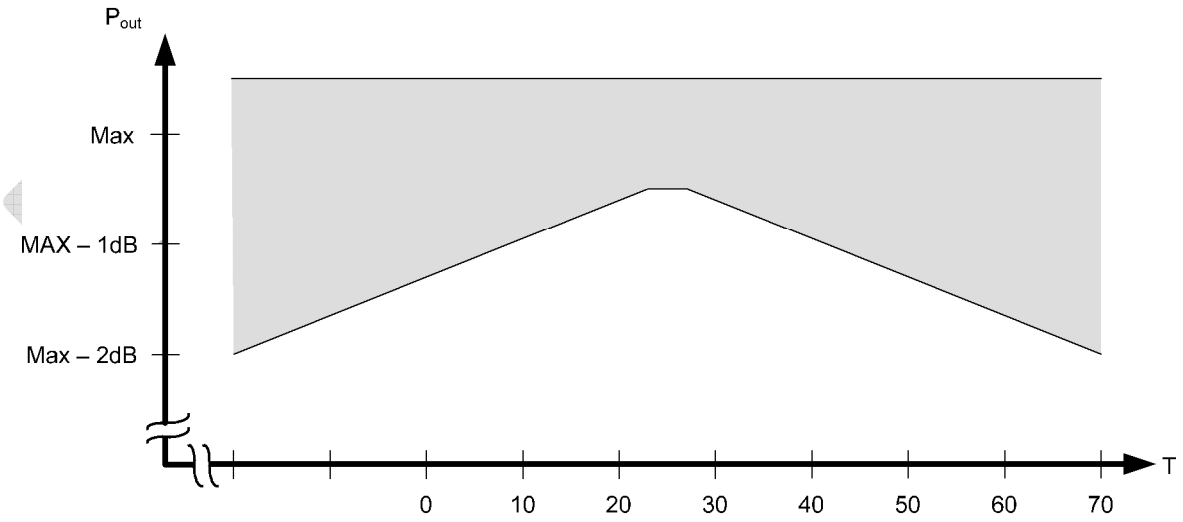


Figure 3: Output Power vs. Temperature

5 I/O Characteristics

5.1 SDIO timing characteristics

The SDIO/SPI-interface can run in three different modes, SDIO 1-bit mode, SDIO 4-bit mode or in SDIO/SPI 1-bit mode. Timing can be set for Default speed mode or High speed mode.

SDIO 1-bit Default speed mode is selected at Power On Reset. The host can change mode by sending the corresponding command over the SDIO-interface.

The Default mode is showed in Figure 1) and Table 8). For the high speed mode see Figure 2) and Table 9). Condition: VDDIO_SDIO= 1.7 – 3.6 V, Tamb= -20 – +70°C

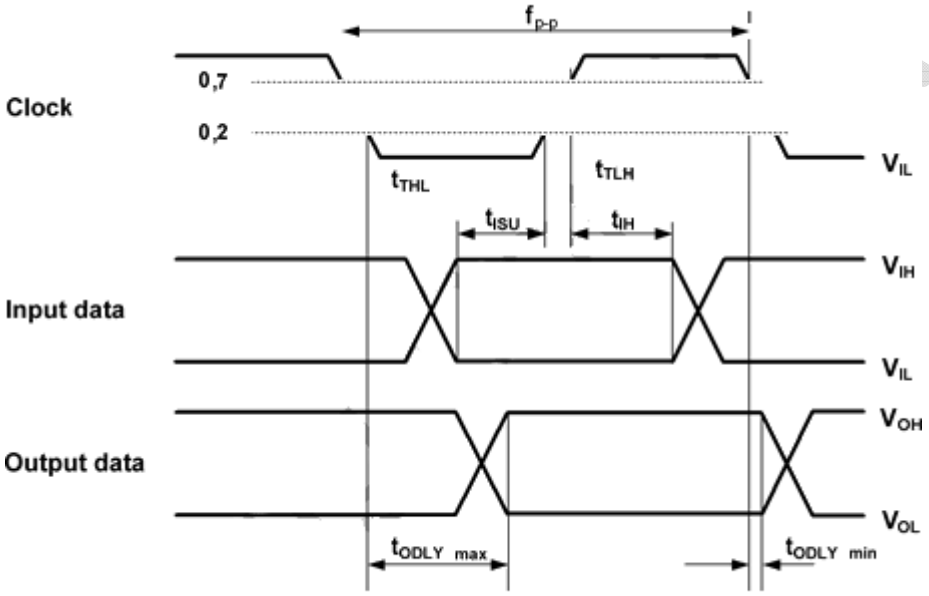


Figure 4: SDIO/SPI timing diagram (default mode)

Parameter	Symbol	Min	Max	Unit	Comment
Input set-up time	t_{ISU}	5		ns	
Input hold time	t_{IH}	5		ns	
Clock fall time	t_{THL}		10	ns	
Clock rise time	t_{TLH}		10	ns	
Output delay time	t_{ODLY}	0	14	ns	
Clock Frequency	f_{SDIO_CL}		25	MHz	

Table 8: SDIO timing parameter values (default mode)

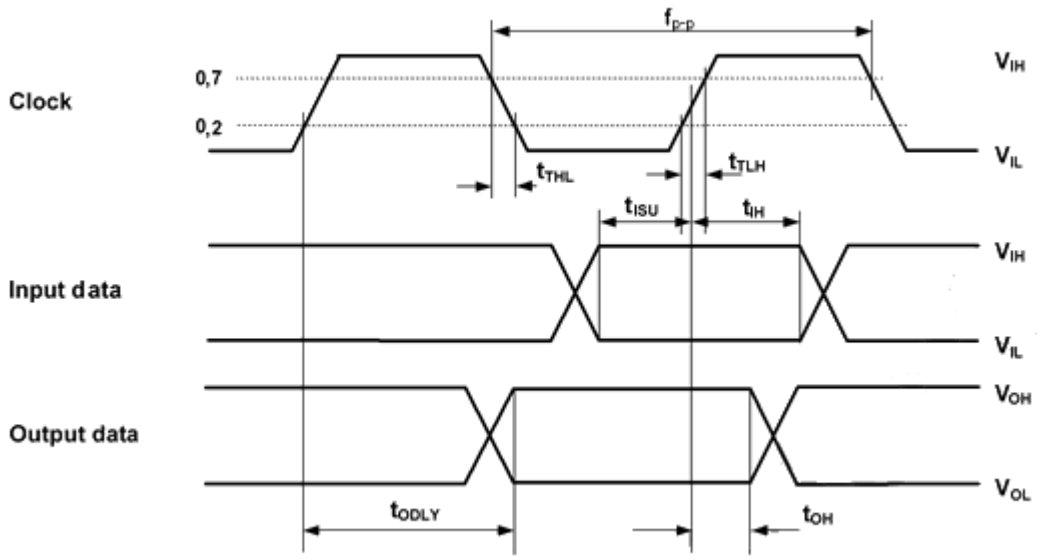


Figure 5: SDIO timing diagram (high speed mode)

Parameter	Symbol	Min	Max	Unit	Comment
Input set-up time	t_{ISU}	6		ns	
Input hold time	t_{IH}	2		ns	
Clock fall time	t_{THL}		3	ns	
Clock rise time	t_{TLH}		3	ns	
Output delay time	t_{ODLY}	2.5	14	ns	
Output hold time	t_{OH}	2.5		ns	
Clock Frequency	f_{SDIO_CL}		52	MHz	

Table 9: SDIO timing diagram (high speed mode)

5.2 SPI timing characteristics

The SPI interface is intended to be used for application specific purposes, like communicating with an external memory, display or codec. Note that this interface cannot be used as a host interface. The timing characteristics are shown in Figure 6 and Table 10.

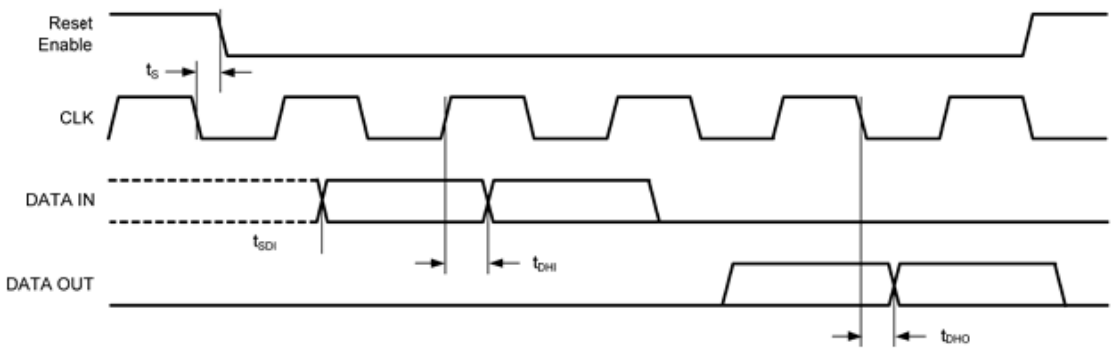


Figure 6: SPI timing diagram

Parameter	Symbol	Min	Max	Unit	Comment
SPI Clock Frequency	f_{SPI}		10	MHz	
Enable delay time	t_S		15	ns	
Input setup time	t_{SDI}	11		ns	
Input hold time	t_{DHI}	0		ns	
Output delay time	t_{DHO}		15	ns	

Table 10: SPI timing parameter values

5.3 Digital I/O pad

The digital I/O pads are of type none inverting three-state driver/receiver. The I/O pin functional schematic is shown in Figure 7. It includes an LVCMOS/LVTTL compatible input buffer and an output buffer with enable/disable control inputs. It also includes a programmable Pull up, Pull down and Hold-function. When the I/O is neither driven by the internal nor by an external circuitry, the hold function holds the latest state of the I/O. This is the case for example when Shutdown is activated, then the Hold function is set and the Output Enable-signal is set low

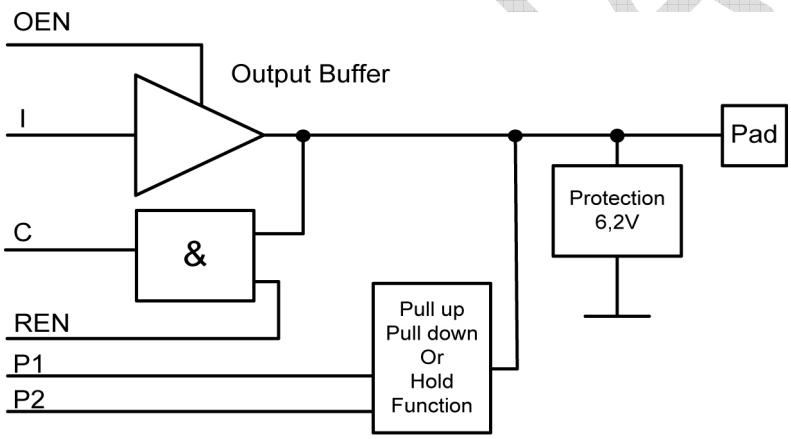


Figure 7: Functional schematic of the I/O pad

The hold-function resists a change of state on the pad. Therefore, an external driver that feeds the pad must overpower the hold function. The needed drive strength is low, typically less than 1 uA. The hold function resists a change of state on the pad only at the first part of the transition. In the last part, it assists the change of the state.

In addition to the above Digital I/O-pads there are five Output Only pads, SW1, SW2, SW3, LNA_GAIN1 and LNA_GAIN2. These I/O-cells consists of a non-inverting driver. They are connected to the VDD_IO-domain. During SHUTDOWN SW1 is set high and SW2 is set low.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Input low voltage	V_{IL}	-0.3		0.3* V_{IO}	V	
Input high voltage	V_{IH}	0.7* V_{IO}		V_{IO} +0.3	V	
Input leakage current	I_{IL}			50	nA	IO in High Z state
Output sink current, V_{OL} = 0.4 Volt	I_{OL}	4	7		mA	V_{IO}=1.8 Volt,
		5	8		mA	V_{IO}=3.3 Volt

Output drive current, V_{OH}= V_{IO}-0.4 Volt	I_{OH}	4	6		mA	V_{IO}=1.8 Volt,
		5	7		mA	V_{IO}=3.3 Volt
Weak Pull Down current	I_{PD}	15	37	97	uA	V_{IO}=1.8 Volt
		17	43	162		V_{IO}=3.3 Volt
Weak Pull Up current	I_{PU}	17	30	54	uA	V_{IO}=1.8 Volt
		39	65	105		V_{IO}=3.3 Volt
VDD_IO, VDD_SDIO	V_{IO}	1.62		3.6	V	
Input pin capacitance	C_{IP}	0	5.5		pF	
Output sink current, Output Only pads, V_{OL} = 0.4 Volt	I_{OLOO}		TBD		mA	V_{IO}=1.8 Volt
			3		mA	V_{IO}=3.3 Volt
Output drive current, Output Only pads, V_{OH}= V_{IO}-0.4 Volt	I_{OHOO}		TBD		mA	V_{IO}=1.8 Volt,
			3		mA	V_{IO}=3.3 Volt

5.4 Protection digital pins

All digital pins are protected against over-voltage with a “snap-back” circuit connected between the pad and GND. The “snap-back” voltage is 6.2 V and the holding voltage is 6 V. This provides a satisfying protection against over voltages and ESD.

Also there is a diode included to protect against reversed voltages.

5.5 Shutdown

The Shutdown input uses an analog pad type A1 with a high impedance resistor in series with a diode to GND. Set the pin low or open to put NRX901 in shutdown mode.

Pull the pin high to initialize EC19D01. If a pull up resistor is used, connect it to VBAT, recommended value is 1Mohm.

6 PIN Configuration

6.1 Device Pin Out

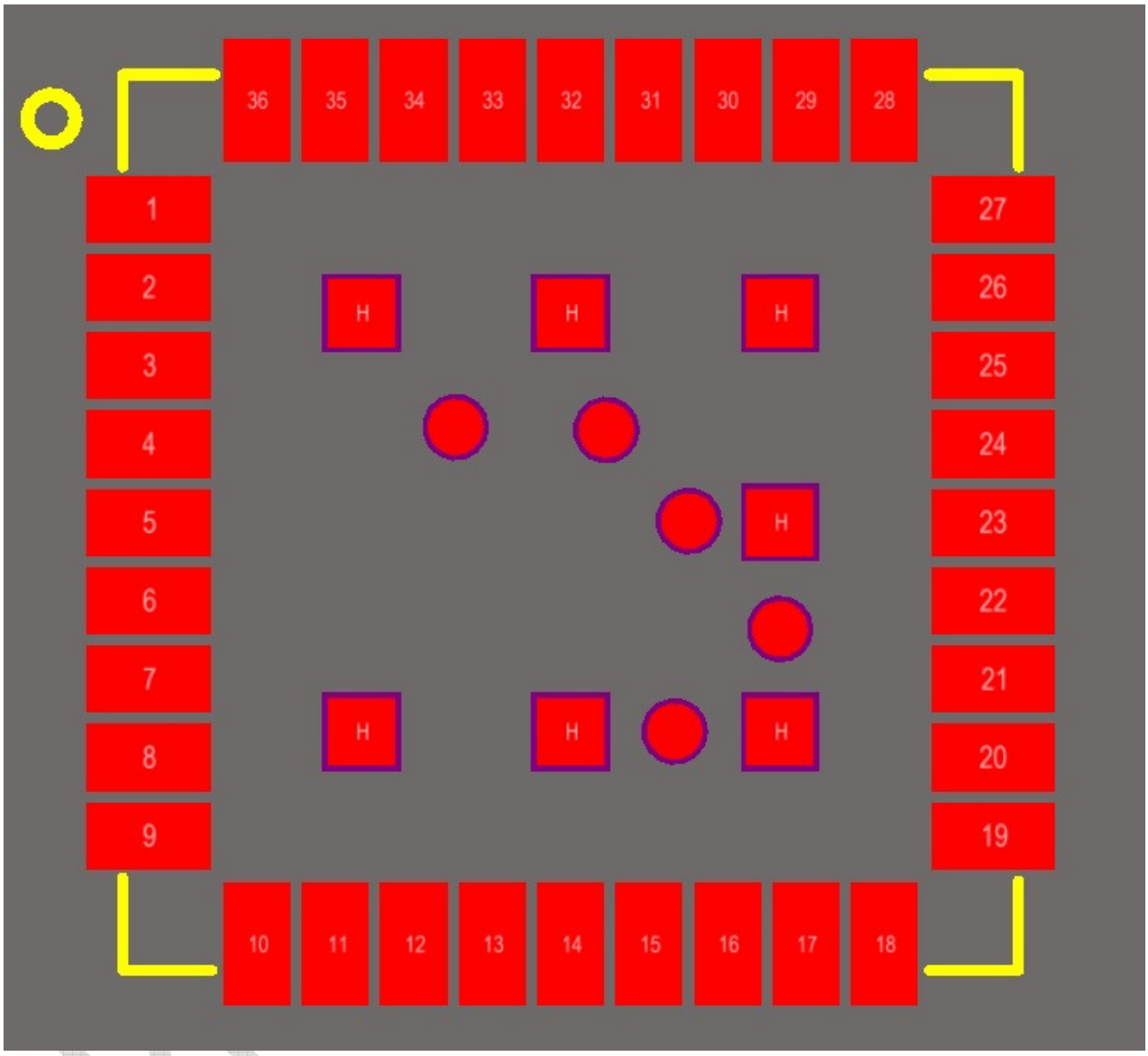


Figure 8: EC19D01 package perimeter pin-out (top view)

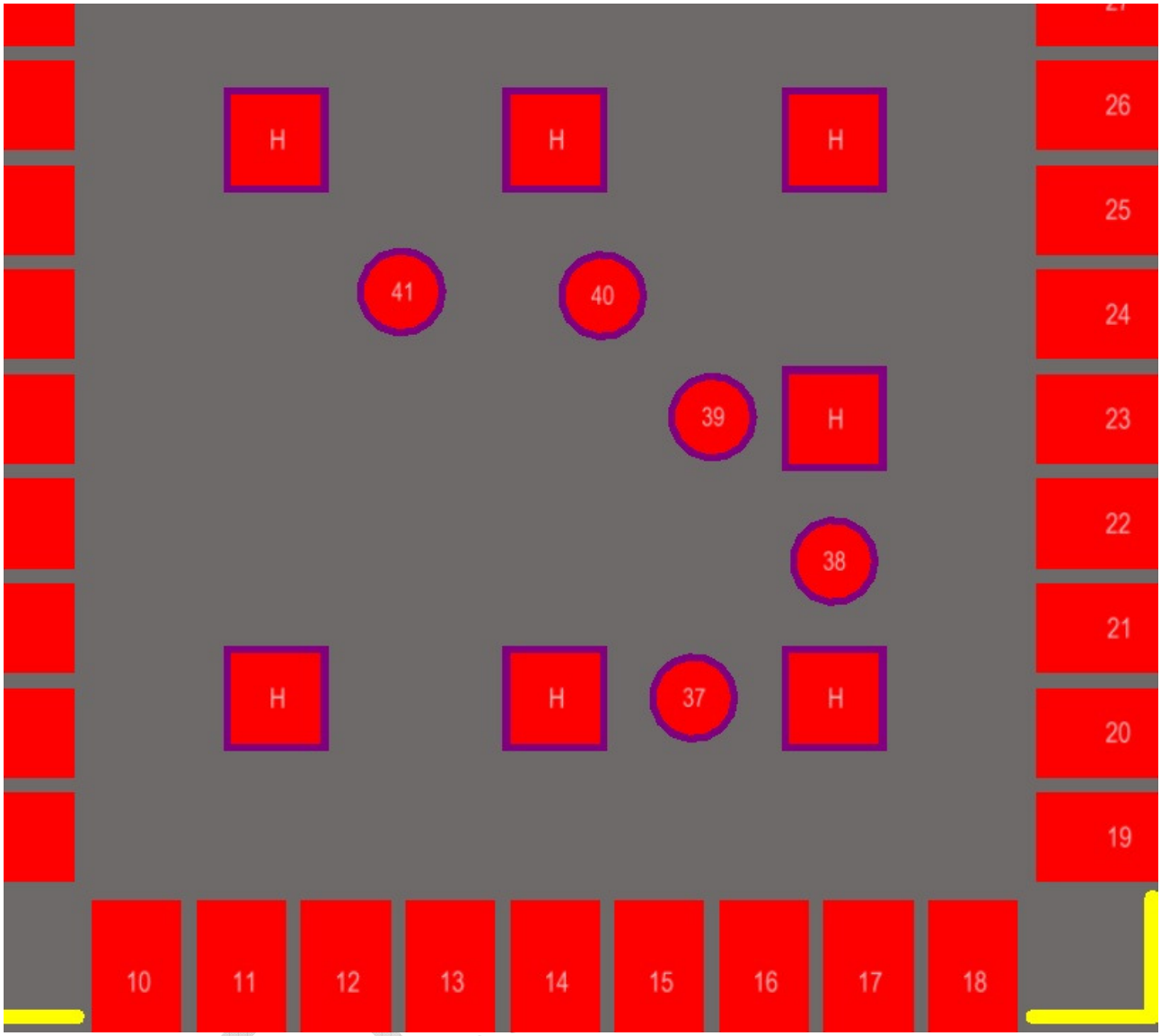


Figure 9: EC19D01 package central area pin out (top view)

6.2 Pin assignment

Pin #	Assignment	Pin #	Assignment	Pin #	Assignment
1	GPIO0	16	SDIO_CLK	31	SPI_EN
2	GPIO1	17	SDIO_DAT1	32	SPI_CLK
3	GPIO2	18	SDIO_DAT0	33	SPI_DIN
4	GPIO3	19	SDIO_DAT3	34	SPI_DOUT
5	VDD_LDO	20	SDIO_DAT2	35	WLAN_EN
6	GND	21	SDIO_CMD	36	GND
7	GPIO4	22	GND	37	HFC_EN
8	GPIO5	23	CLK_IN	38	ICE_TCK
9	VBAT	24	GND	39	ICE_TDO
10	GND	25	GND	40	ICE_TDI
11	VDD_DCDC	26	ANTENNA	41	ICE_TMS
12	DCDC_OUT	27	GND		
13	VDD_IO	28	GND		
14	VDD_SDIO	29	GPIO6		
15	GND	30	GND	H	GND

Table 11: Pin assignment list

6.3 Pin Functions and Configurations

Pin Name	Pin	Description	Pin Type	Pin state in Shutdown	Power Domain
Power					
VBAT	9	Main supply (battery) for DC/DC converter	S	ON	VBAT
VDD_IO	13	I/O supply voltage for GPIO1-GPIO6.	S	ON	VDD_IO
VDD_SDIO	14	I/O supply voltage for SDIO, ICE and SPI-buses	S	ON	VDD_SDIO
DCDC_OUT	12	DC/DC converter pulsing output.	S	OFF	VBAT
VDD_DCDC	11	DC/DC Voltage Sense. Connect to filtered side of inductor or to external VDD if DCDC is not used.	S	OFF	VDD_DCDC
VDD_LDO	5	1.8 – 3.6 Volt LDO Output. For use as I/O-voltage.	S	OFF	VBAT
Ground					
	6		GND	GND	
	10		GND	GND	
	15		GND	GND	
	22		GND	GND	
	24		GND	GND	
	25		GND	GND	
	27		GND	GND	
	28		GND	GND	

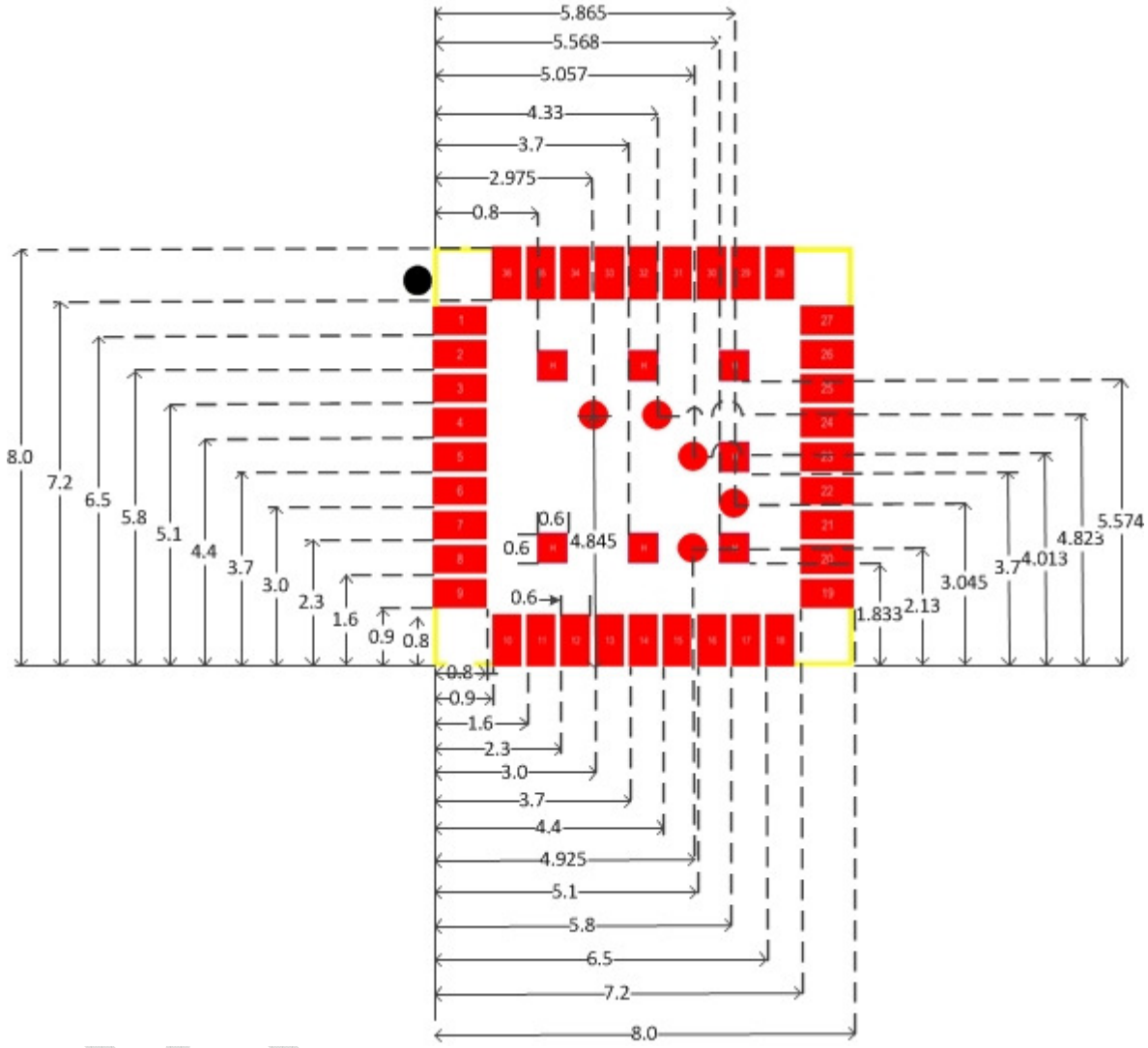
	30		GND	GND	
	36		GND	GND	
SDIO/Host Interface					
SDIO_CLK	16	SDIO Clock, SDIO/SPI CLK	I/O	Hold	VDD_SDIO
SDIO_DAT0	18	SDIO Data 0, SDIO/SPI MISO, UART RxD	I/O	Hold	VDD_SDIO
SDIO_DAT1	17	SDIO Data 1, SDIO/SPI IRQ, UART CTS	I/O	Hold	VDD_SDIO
SDIO_DAT2	20	SDIO Data 2, SDIO/SPI N/A, UART RTS	I/O	Hold	VDD_SDIO
SDIO_DAT3	19	SDIO Data 3, SDIO/SPI CS, UART TxD	I/O	Hold	VDD_SDIO
SDIO_CMD	21	SDIO Command, SDIO/SPI MOSI	I/O	Hold	VDD_SDIO
SPI Interface					
SPI_EN	31	SPI Enable output. Active low	I/O	Hold	VDD_SDIO
SPI_DIN	33	SPI Data input pin	I/O	Hold	VDD_SDIO
SPI_DOUT	34	SPI Data output pin	I/O	Hold	VDD_SDIO
SPI_CLK	32	SPI_Clock output	I/O	Hold	VDD_SDIO
General Interfaces					
HFC_EN	37	External clock request	I/O	Low	VDD_SDIO
GPIO0	1	Host Wakeup or General purpose I/O	I/O	Hold	VDD_SDIO
WLAN_EN	35	Shutdown input, Active low	A	LOW	VBAT
Debug/Test Interface					
ICE_TDO	39	ICE Test Data Output	I/O	Hold	VDD_SDIO
ICE_TDI	40	ICE Test Data Input	I/O	Hold	VDD_SDIO
ICE_TCK	38	ICE Test CLK	I/O	Hold	VDD_SDIO
ICE_TMS	41	ICE Test Mode Select	I/O	Hold	VDD_SDIO
General Purpose I/O					
GPIO1	2	General purpose I/O 1 Class D Head Phone Driver Left P AUD_CLK Audio I2S and PCM clock General purpose I/O 2	I/O	Hold	VDD_IO
GPIO2	3	Class D Head Phone Driver Left N AUD_LR/SYNC Audio I2S LR or PCM Sync	I/O	Hold	VDD_IO
GPIO3	4	General purpose I/O 3 Class D Head Phone Driver Right P AUD_DOUT Audio Data Out	I/O	Hold	VDD_IO
GPIO4	7	General purpose I/O 4 Class D Head Phone Driver Right N AUD_DIN Audio Data In	I/O	Hold	VDD_IO
GPIO5	8	General purpose I/O 5 Digital Microphone Clock Output	I/O	Hold	VDD_IO
GPIO6	29	General purpose I/O 6 Digital Microphone PDM Data Input	I/O	Hold	VDD_IO
Clock					
CLK_IN	23	External Clock input	A		VBAT

Table 12: Pin functions and configurations for EC19D01

Pad types Legend:

A	Analog
GND	Ground
I	Input
O	Output
RF	Radio Frequency driver, receiver
S	Supply Voltage
Hold	Week keeper state, keeps the previous state

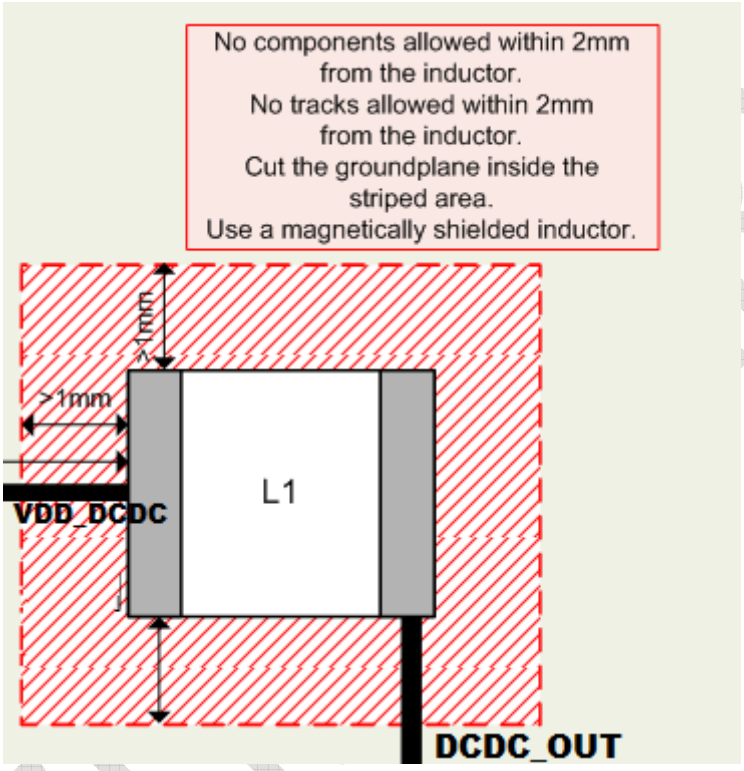
7 Mechanical dimensions, footprint



8 Layout considerations

8.1 DC-DC converter

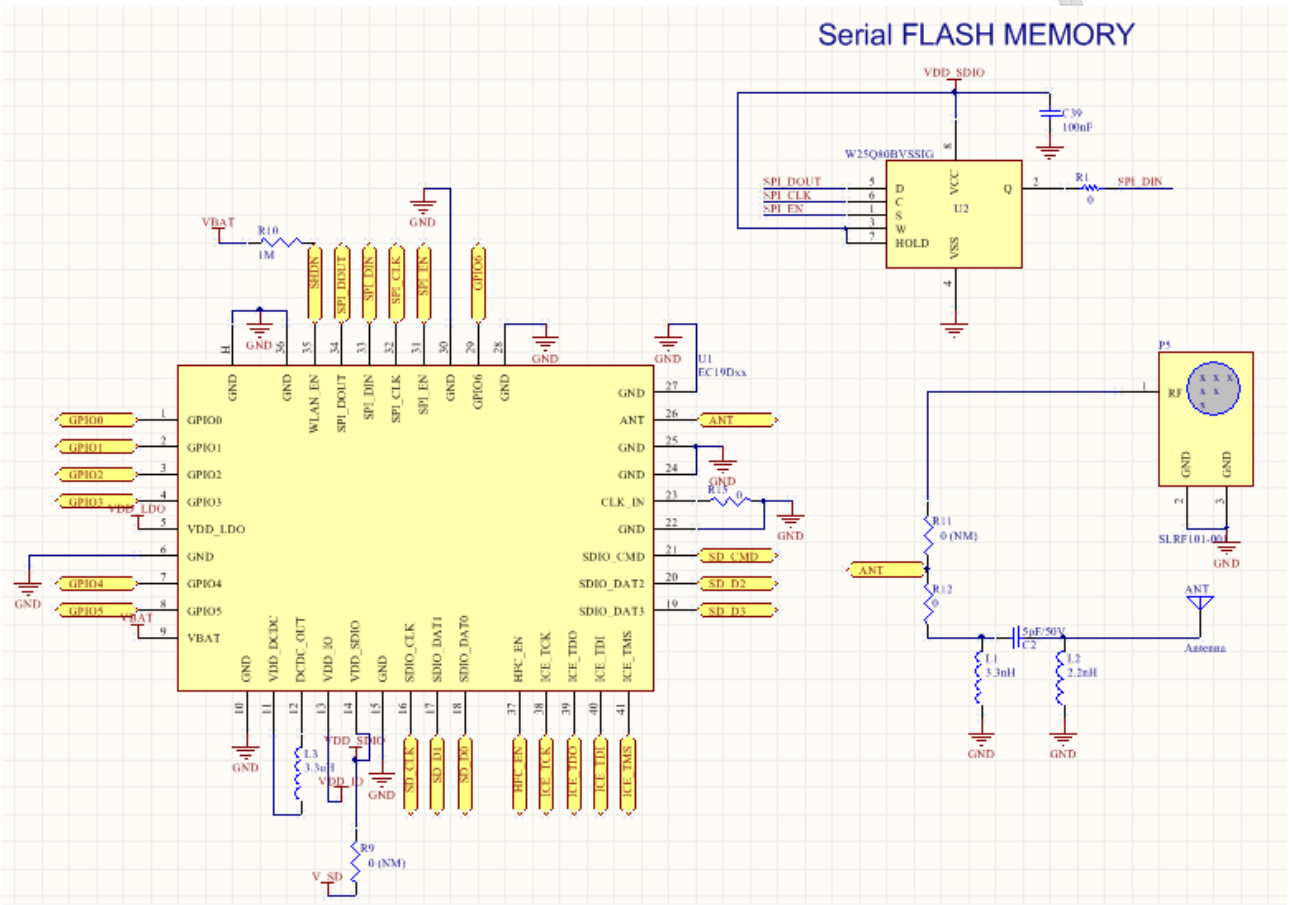
For the inductor connected to the VDD_DCDC and DCDC_OUT (pins 11 & 12 respectively) please follow the reference design below:



9 Reference Design

The EC19D01 should have some external components in order to function properly:

- Inductor for DC-DC functionality
- Serial Flash
- Antenna / Matching circuit



Inductor's characteristics: 3.3uH 20% LQM2HP (Murata LQM2HPN3R3MG0)

Recommended Flash Chips for storing patch and application code:

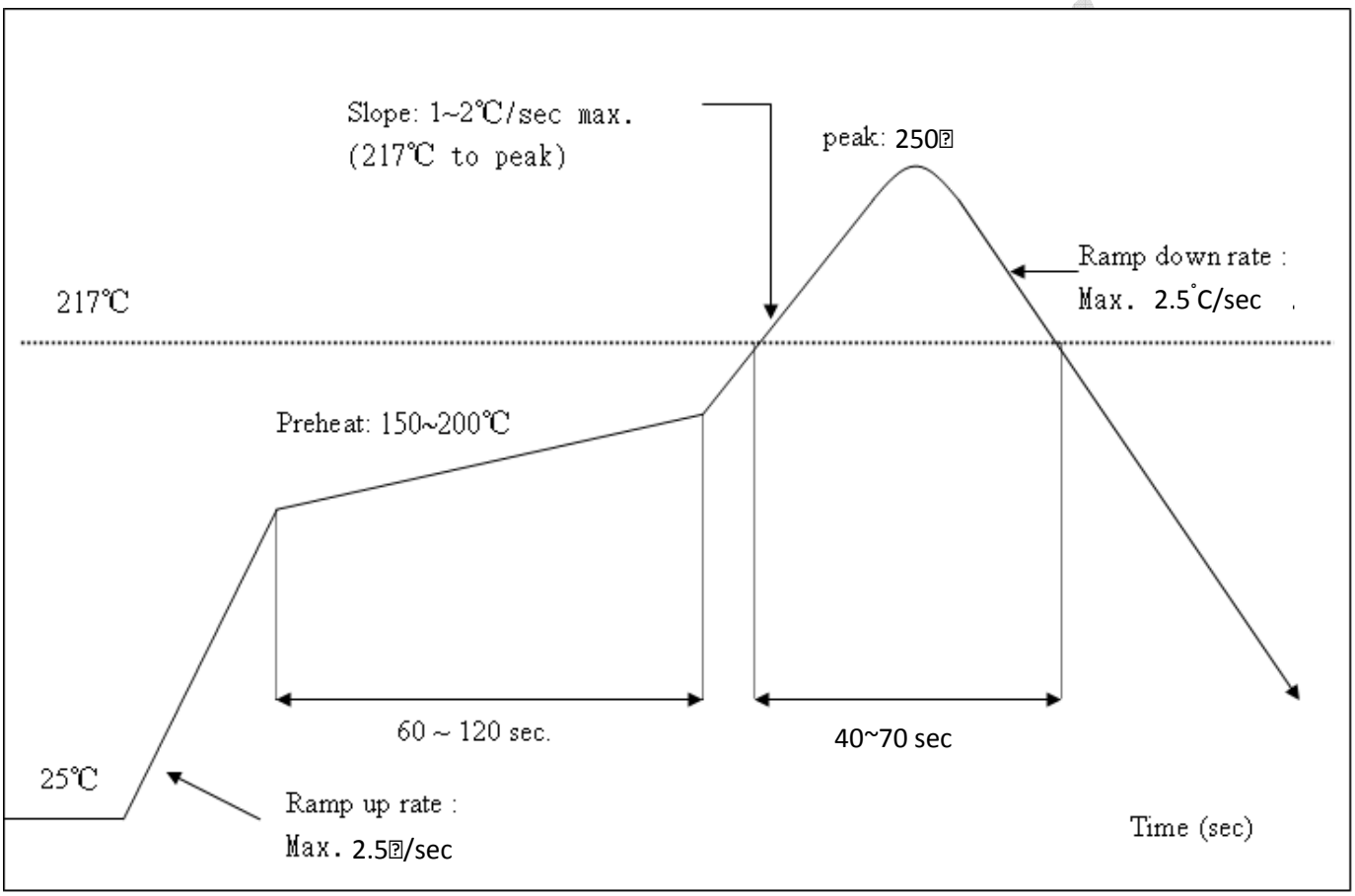
Vendor	Product	Size
STMicroelectronics	STM25P40	4 Mbit
Numonyx	M25P80 M25P16	8 Mbit 16 Mbit
Atmel	AT45DB011B	1 Mbit
Eon Silicon Solutions	EN25Q40 EN25Q80	4 Mbit 8 Mbit
Winbond	W25Q80	8 Mbit

10 Reflow profile

Refer to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of times : ≤2 times



11 Device Operation Description

11.1 WLAN Radio

EC19D01 contains a WLAN Radio. It is a fully integrated RF transceiver with a Zero-IF architecture, operating in the 2.4-2.5 GHz ISM band. The design uses differential RF-input/output to optimize the RF performance. A Transmit/Receive switch is integrated on module preventing signal leakage into the receiver path during RF transmit time.

11.1.1 WLAN RF Receiver

The receive section is designed to work well in a radio noisy environment such as a cellular phone. The RF signal is received and amplified by the on module WLAN LNA.

In addition a separate Receive input is available to enable the use of an external RF front end.

11.1.2 RF Transmitter

The EC19D01 WLAN Radio provides an on module high efficient RF Power amplifier to minimize overall solution cost. Output Power can be trimmed to meet IEEE standard requirements. Trim values can be stored in an on module fuse memory which will be available throughout the application life time.

The ISM band radio also includes a low output power mode, in the 0 dBm range, for lower power consumption in close range etc.

11.2 WLAN Baseband and MAC

11.2.1 Operational Modes

11.2.1.1 ShutDown

EC19D01 can use two shutdown modes HW SHUTDOWN and Soft SHUTDOWN.

11.2.1.1.1 HW Shutdown

SHUTDOWN_N shall be set high during normal operation. Pulling the SHUTDOWN_N pin low sets EC19D01 in HW Shutdown mode. This turns OFF most parts of the circuit and minimizes current consumption. All I/O interface pins keep their states with the I/O hold function when in Shutdown mode. In shutdown, keep the VBAT_DCDC, VBATS_DCDC, VBAT_LDO and VBAT_CLK supplies ON (the battery). EC19D01 will automatically turn OFF all generated power supplies, incl VDD_DCDC.

If the internal DCDC-converter for 1.5 Volt is not used, the externally supplied 1.5 Volt should be turned OFF while in HW Shutdown mode.

To end HW Shutdown mode set SHUTDOWN_N pin high and reload FW and MIB.

11.2.1.1.2 Soft Shutdown

Soft Shutdown is a FW function that stops all functions and sets HW in a deep sleep state. All I/O-pins are set to predefined states, FW defaults, or according to a Soft Shutdown MIB-setting.

During Soft Shutdown keep all power supplies ON and pin SHUTDOWN_N high.

To end Soft Shutdown mode toggle the SHUTDOWN_N pin low-high and reload FW and MIB.

11.2.1.2 Power Save

Power save is an energy saving mode where EC19D01 is only listening at regular intervals for the beacons transmitted from an access point and is set in sleep mode in between. During sleep mode, FW patches are kept in RAM with all not needed functions turned off. Since the receive time is very short compared to the listening interval the average current consumption is reduced significantly.

The timing of the listening interval is based on the LFC (32 kHz) clock. The LFC is implemented internally but can also be fed externally.

11.2.1.3 Power ON Sequence internal DCDC

Figure below shows a typical Power ON sequence used for the EC1901 module. VDD, 1.5 V is supplied from the internal DCDC converter and a 40MHz crystal is used. The FW patches and the MIB data are loaded from an external flash memory connected to the SPI interface. See timing diagram Figure 6) and Table 16).

VBAT should not be applied with a faster rise time than according to table below.

VDDIO should be turned ON after VBAT or at the same time as VBAT if rise time of VDDIO is the same or slower than VBAT rise time.

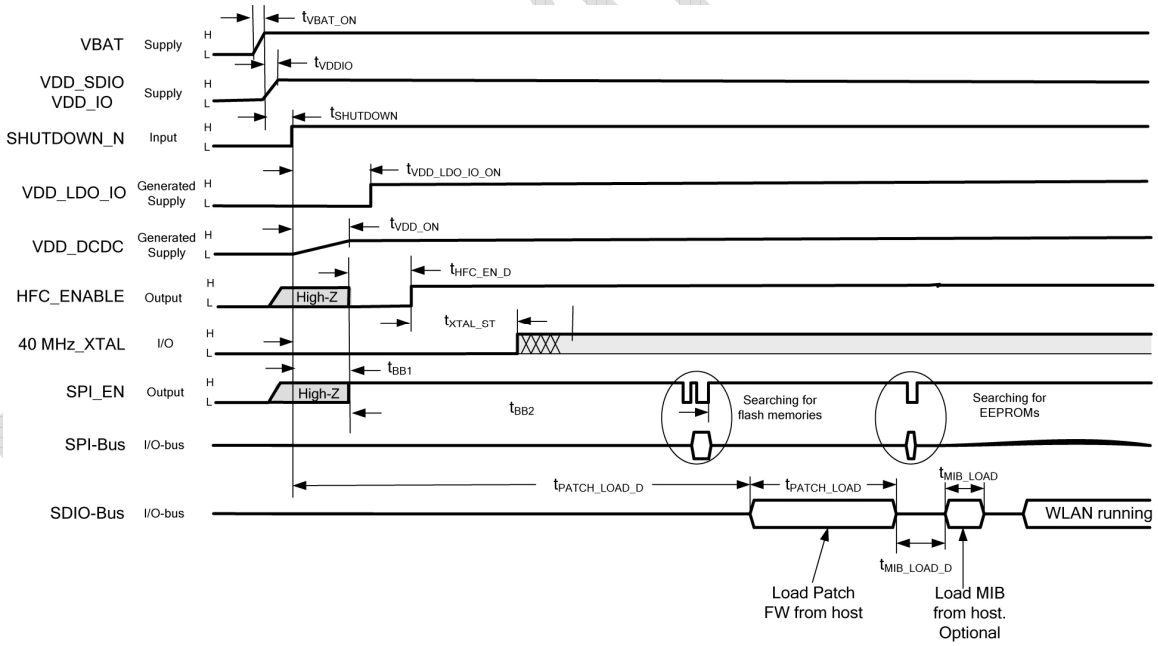


Figure 10: Timing diagram Power ON sequence

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VBAT rise time	t_{VBAT_ON}	2			µs	
VDDIO turn on time	t_{VDDIO}	0			µs	
Ctrl shutdown time	$t_{SHUTDOWN}$	1			ms	
Digital supply ramp time	t_{VDD_ON}		150		µs	
IO Supply ramp time	$t_{VDD\_LDO\_IO\_ON}$		360		µs	
40MHz OSC start-up time	t_{XTAL_ST}		1.5	1.8	ms	
BB1 startup time	t_{BB1}		0.1		ms	
BB2 startup time	t_{BB2}		2.6		ms	
HFC_ENABLE delay time	$t_{HFC\_EN\_D}$		0,17		ms	
Patch load delay	$t_{PATCH\_LOAD\_D}$	10			ms	
Patch loading time	t_{PATCH_LOAD}					Patch size dependent
IB load delay	$t_{MIB\_LOAD\_D}$	10			ms	Patch dependent
MIB load time	t_{MIB_LOAD}					MIB size dependent

Table 13: Timing parameters Power ON sequence

11.3 Power ON Sequence with external 1.5 Volt Supply

Turn ON external 1.5 Volt, VDD_DCDC, supply at time indicated in fig above.

11.3.1 Shutdown Sequence

The following figure shows a typical shutdown sequence for the EC19D01 module, when VDD_DCDC 1.5 V, is supplied from the internal DCDC converter and a 40MHz crystal is used.

End Shutdown mode with a Power ON Sequence described above.

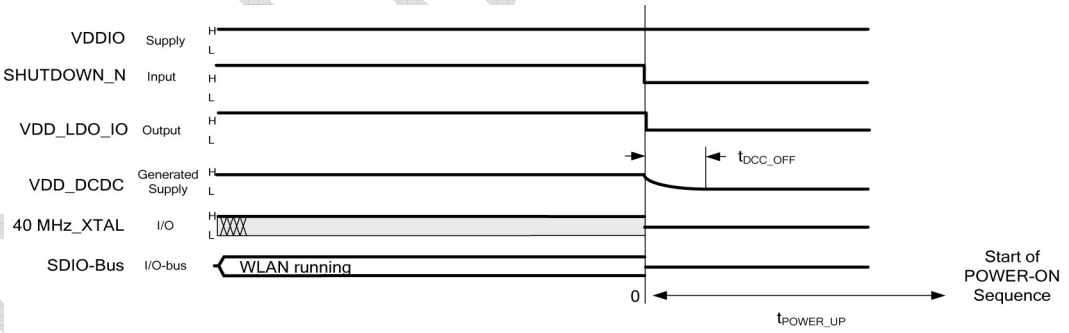


Figure 11: Shutdown Sequence

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DCDC turn off time	t_{DCDC_OFF}	0	2		ms	
Power-up after Shutdown time	t_{POWER_UP}	1			ms	

11.3.1.1 Power OFF Sequence

All power supplies can be turned OFF at the same time or in sequence as below.

1. Enter Shutdown, this will automatically turn OFF the internal DCDC converter
2. Turn OFF VDD_SDIO and VDD_IO
3. Turn OFF all VBAT

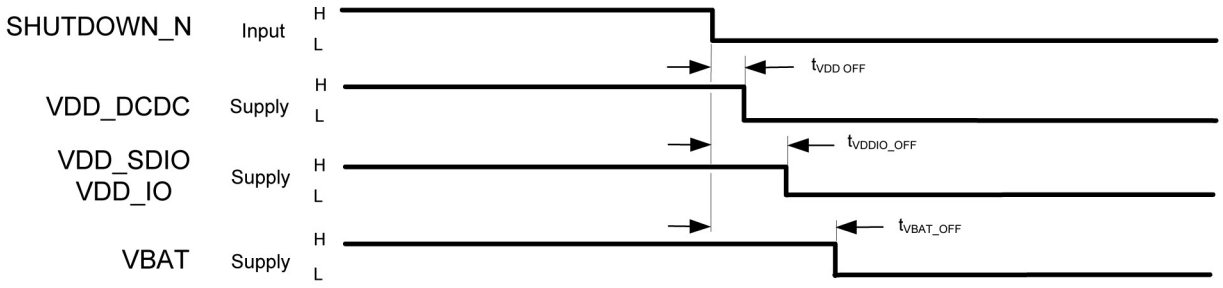


Figure 12: Power Off Sequence

Parameter	Symbol	Min	Typ	Max	Unit	Comment
VDD 1.5V supply off time	t_{VDD_OFF}	0			ms	
VDDIO supply off time	t_{VDDIO_OFF}	t_{VDD_OFF}		t_{VBAT_OFF}	ms	
VBAT supply off time	t_{VBAT_OFF}	t_{VDDIO_OFF}			ms	

Table 14: Timing parameters Power OFF sequence

11.3.2 Interfaces

The EC19D01 is equipped with a number of interfaces that can be set up in various ways.

11.3.2.1 External Interface (SDIO, SDIO/SPI, UART)

These I/O pins can be set in two different modes SDIO/SPI or UART.

For SDIO mode the default after Power ON Reset is 1-bit mode with default speed. FW can select SDIO 4-bit mode or SDIO-SPI at initialization time.

For UART mode, the default speed is 115200bps, 8 bits, no parity, 1 stop bit.

External interface mode selection is done by FW after Power ON Reset and/or after SHUTDOWN_N going high.

All unused interface pins shall be left open.

11.3.2.2 SPI Interface

The SPI interface It is set up as a standard master SPI device.

SPI_EN is used as an enable signal to a serial flash memory for downloading application/patch code and/or MIBdata to the baseband in an embedded application.

SPI_EN is active low, it shall be left open if not used.

Table below states the supported flash memories for storing patch and application code.

Vendor	Product	Size
STMicroelectronics	STM25P40	4 Mbit
Numonyx	M25P80	8 Mbit
	M25P16	16 Mbit
Atmel	AT45DB011B	1 Mbit

EEPROMs with I2C interface are supported by using SPI_CLK as SCL and SPI_EN as SDA-signal. EEPROMs are typically used for MIB-data in hosted applications.

Table below states the supported EEPROM memories, additional types can be supported by patch FW.

Vendor	EEPROM	Interface	Size
Seiko Instruments	S-24CS16A	I2C	16kbit
Seiko Instruments	S-25C080A	SPI	8kbit
Seiko Instruments	S-25C160A	SPI	16kbit
AKM	AK6506C	SPI	8kbit
STMicroelectronics	M24C08-F	I2C	8kbit
STMicroelectronics	M95160	SPI	16kbit

11.3.2.3 Host Wakeup

The Wake Up command via the SDIO interface is the normal wake up and is implemented in the FW.

If a dedicated pin is needed to wake up the host, use GPIO0. It belongs to the VDD_SDIO domain.

11.3.2.4 General Purpose I/O (GPIO)

There are six pins designated as a General Purpose I/O pins GPIO1 to GPIO6.

They belong to the VDD_IO domain and can be assigned to various functions by the FW.

These GPIOs can be used as Head Phone drivers, class D, and digital microphone interface signals or for BT coexistence handshake. Shall be left open if not used.

11.3.2.5 Test Interface

An In Circuit Emulator test bus (ICE_TMS, ICE_TDI, ICE_TDO and ICE_TCK) is available. It is a standard JTAG IEEE 1149 test access port.

11.3.3 Memory

11.3.3.1 System ROM

FW resides in three 64kB ROM banks.

11.3.3.2 System RAM

There are four 64kB SRAM banks used to store data and FW patches.

11.3.4 Bluetooth Coexistence

The pins GPIO1-4 are pre-assigned to be used as interface to a Bluetooth system to facilitate traffic

arbitration between the two systems. The control system is implemented in firmware and can be adapted for other free GPIOs and for various standards or proprietary coexistence protocols.

11.4 Audio Subsystem

The on module audio subsystem includes support for I2S/PCM interfaces, Class D stereo Head Phone drivers and two digital microphones.

These functions use pins GPIO1-6, selection of interface type is done by FW.

11.4.1 I2S/PCM

This is a 16-bit the I2S/PCM interface, mapped on pins GPIO1-4, for connections to an external codec. All standard sampling rates are supported, custom sampling rates can be provided by FW.

Both Master and Slave modes are supported.

Can not simultaneously use the digital microphone interface.

11.4.2 Class D

GPIO1-4 are class-D drivers for direct connection to stereo speakers/headphones.

GPIO 1-2 are differential drivers for the left channel.

GPIO 3-4 are differential drivers for the right channel.

For single ended head phones use GPIO1 for the left channel, GPIO3 for the right channel and GPIO4 as the common pin, emulated GND.

External filtering can be added to adapt to the particular head phones used in an application.

A Digital Microphone interface, compatible with Analog Devices ADMP421, is implemented on pins GPIO5-6. This interface supports two microphones, for stereo applications, by clocking data on both the positive and negative clock edges.

11.5 Power Management

The EC19D01 is a true single chip Wi-Fi module solution with fully integrated power management. The module is intended to be fed directly from a Lithium Ion-type battery. It's also possible to supply the module via external power management.

I/O supply is fed externally supporting a custom I/O supply set-up.

11.5.1 IO Supply

There are two main IO domains:

VDD_IO	IO supply voltage for pins GPIO1-6
VDD_SDIO	IO supply voltage for all other pins

Note that IO-supplies must never be higher than VBAT. Damage to the module will occur if any IO-supply exceeds VBAT with more than an internal diode drop.

11.5.2 Ground

The module has one common ground connection for the different power domains, see Typical Applications. There are several digital ground bumps, VSS, they should be treated as equal and all joined together on the PCB. Equal to the digital grounds, the I/O ground bump, VSS_IO, should all be connected to GND on the PCB.

The main ESD ground in the module is the digital ground VSS.

11.6 Clock Management

11.6.1 High Frequency Clock, HFC

The high frequency clock on the EC19D01 is used as general clock reference in the module. It supports both to the RF PLL and the Digital PLL with a reference frequency. The RF PLL generates the Radio VCO frequency and the Digital PLL generates frequencies to the Digital Baseband, MAC and I/Q ADC and DAC.

The High Frequency Clock can either be generated internally with just a crystal connected to CLK_1 and CLK_2 or introduced to the chip from an external source on pin CLK_IN.

The CLK_IN pin supports clock frequencies of 26, 38.4, 40 or 52 MHz.

EC19D01 contains an oscillator that only needs an external 40 MHz crystal to generate the clock signal. The crystal is connected between the pins CLK_1 and CLK_2. The crystal should be placed as close as possible to the circuit pins. Stray capacitances to GND for crystal interconnect traces should be as small as possible. Do not connect any capacitors to GND on the crystal pins. The requirements for the crystal are given in the table below.

Connect CLK_IN to GND when not used.

Parameter	Condition	Min	Typ	Max	Unit
Frequency			40		MHz
CL			8		pF
Cm		3.5		6.0	fF
C0 (shunt cap)		0.5		2.0	pF
Equiv Rs		0		60	ohm
Frequency tolerance	T_{amb}=25°C	-15		15	ppm
Freq vs temp	T_{amb}= -20 - +70°C	-15		15	ppm

Table 15: Recommended crystal parameters

11.6.2 External reference requirements

For an externally generated reference clock, the frequency 26, 38.4, 40 or 52 MHz should be used. Connect the external clock to pin CLK_IN.

The requirements on the external reference clock are stated in below table.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
AC-level		0.2		2.5	Vpp	Assuming the DC- level is between 0V and 2.6V
External clock accuracy		-15		15	ppm	
Resistive load		10k		1M	ohm	External reference should be able to drive this load while fulfilling the other requirements
Capacitive load		1		10	pF	
Phase Noise						
Frequency offset ±1kHz			-121		dBc/Hz	
Frequency offset ±10kHz			-137		dBc/Hz	
Frequency offset ±100kHz			-143		dBc/Hz	
Frequency offset 40 MHz reference ±1kHz			-117		dBc/Hz	
Frequency offset 40 MHz reference ±10kHz			-133		dBc/Hz	
Frequency offset 40 MHz reference ±100kHz			-139		dBc/Hz	

11.6.3 Low Frequency Clock, LFC

The EC19D01 has an internal 32 kHz Low Frequency Clock oscillator, LFC, that is used at chip start-up and during the Power Save scheme. NRX901 can also utilize an external 32 kHz clock, connected to the EXT_LFC pin. The chip will always initiate from Power ON Reset with the internal LFC, and then use external LFC if so configured via a setting in the MIB file. For timing calculations the LFC frequency is calibrated against the more accurate HFC frequency by FW.

The EXT_LFC pin uses the standard type of GPIO-cell, signal swing should comply with the VDD_SDIO supply. The EXT_LFC pin can be set as an ouput by FW for external use of the 32 kHz clock.

The external reference shall comply with the requirements outlined in below table.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
LFC frequency	f_{LFC}	30	32	34	kHz	
Clock accuracy		-2000		2000	ppm	
Duty Cycle		30	50	70	%	

Table 16: External LFC requirements

11.7 WLAN Firmware

The firmware is executed in on-module ROM. Firmware patches are downloaded from host at Power On Reset, or loaded into RAM from a serial Flash Memory connected to the SPI interface. The firmware implements the full IEEE 802.11b/g/n wireless LAN MAC protocol, an embedded IP stack together with a few commonly used applications that can be easily configured and controlled via the chip interface.

The wireless LAN MAC stack supports basic service set (BSS), Mobile AP and WiFi Direct. Low-level protocol functions such as RTS/CTS, acknowledgement, fragmentation, defragmentation, frame encapsulation (802.11h/RFC1042) and automatic beacon monitoring / scanning are handled by the NRX901 baseband MAC without host intervention. Passive or active scanning is performed autonomously once initiated by a host command.

The IP stack supports TCP, UDP, RTP, and ICMP over IPv4. On top of the IP stack there is web server with support for Server-Side Includes (SSI) and Common Gateway Interface (CGI) available. The web pages can be customized via the serial interface.

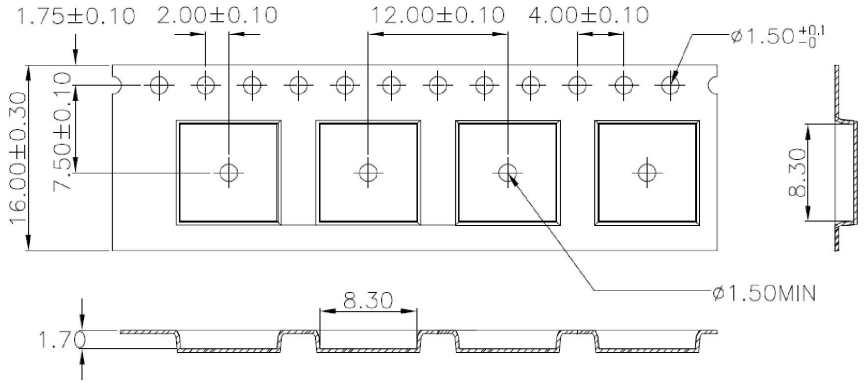
Power management is handled with minimum host interaction to minimize active duty periods.

11.7.1 Features

- 802.11 b/g/n/d/e/i/support
- Infrastructure mode support.
- Supports WiFi Direct, Group Owner (GO) and Client
- Supports Mobile AP and Mobile router functionality (Soft AP mode) supporting WPA/WPA2 AES + TKIP and 802.11 legacy power save for the clients
- IPv4 stack with TCP, UDP, RTP and ICMP support
- Web server with Server-Side Includes (SSI) and Common Gateway Interface (CGI)
- Zeroconfig support through support of the mDNS protocol
- Hardware accelerators (software managed hardware) for CCM (CBC-MAC, Counter Mode), TKIP (MIC, RC4), WAPI (SMS4) and WEP(RC4) along with CRC.
- Supports WPA/WPA2, PSK and Enterprise
- Supports WPS 2.0
- Additional security features according to 802.11i such as pre-authentication and TSN.
- Supports 802.11n up to MCS7 (Tx/Rx). Supporting MIMO 1x1 & 2X1, STBC, A-MPDU aggregation and 0.4us guard interval.
- WMM Power Save U-APSD
- Multiple queue management to fully utilize traffic prioritization defined by the 802.11e standard.
- 802.1h/RFC1042 Frame encapsulation.
- Scattered DMA for optimal CPU off load on Zero Copy data transfers operations.

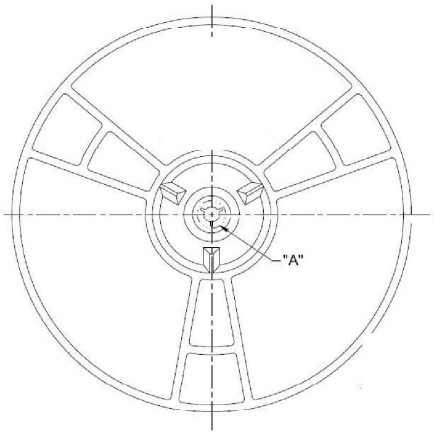
- Antenna diversity and selection (software-managed hardware).
- Clock/Power gating combined with 802.11-compliant power management dynamically adapted to the current connection condition providing minimal power consumption.
- Adaptive rate fallback algorithm that sets the optimum transmission rate and TX power based on actual signal-to-noise ratio and packet-loss information.
- Over-the-air downlink back-pressure to avoid packet discarding on slow host environment.
- Advanced seamless scanning support for optimal host CPU offload
- Seamless roaming support
- Configurable Packet Traffic Arbitration (PTA) with dedicated slave processor based design provides flexible and exact timing Bluetooth co-existence support for a wide range of Bluetooth Chip vendors.
- Dual and single antenna Bluetooth Coexistence support with optional simultaneous receive (WiFi/Bluetooth) capability

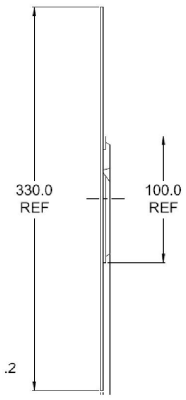
12 Pick and Place and Packing information

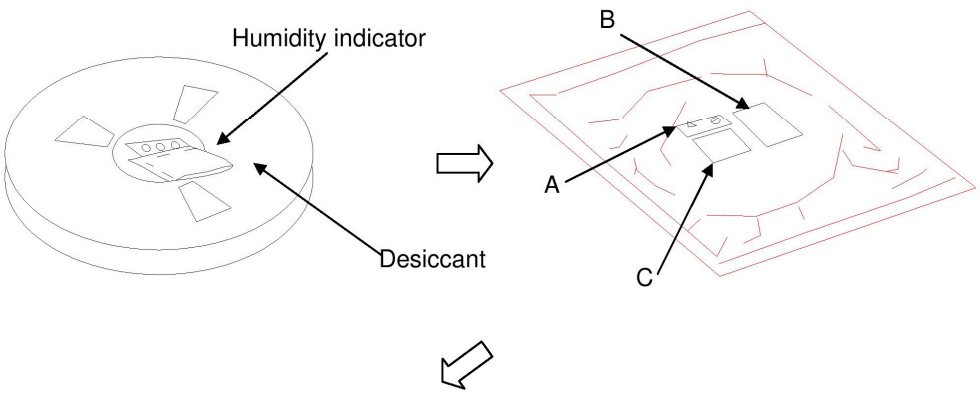


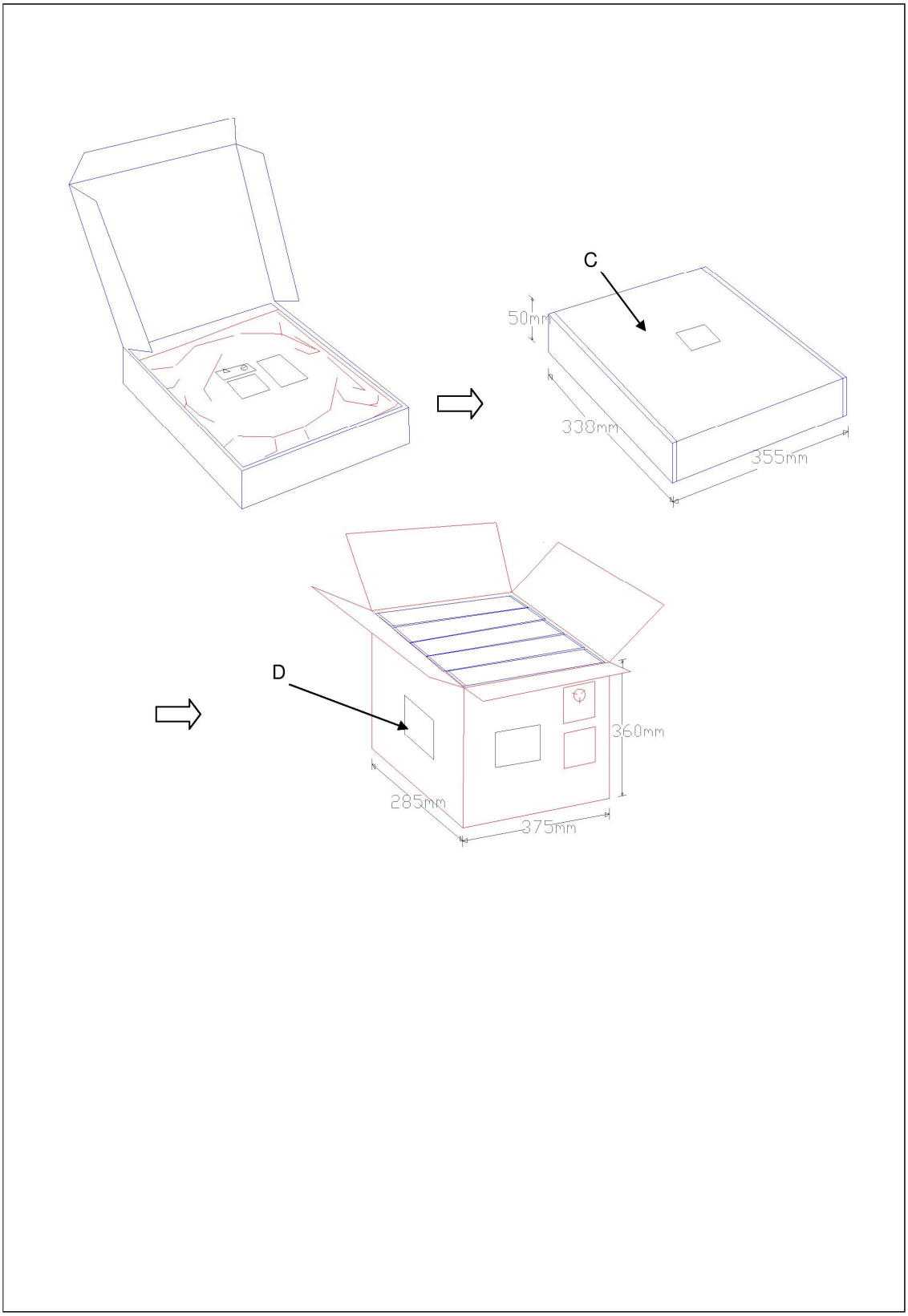
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Component load per 13" reel : 2500 pcs.

W	16.00±0.30
A0	8.30±0.10
B0	8.30±0.10
K0	1.70±0.10








C
50mm
338mm
355mm
D
360mm
285mm
375mm

13 Contact Information

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