

## **PIR Sensor Light Switch Controller Description**

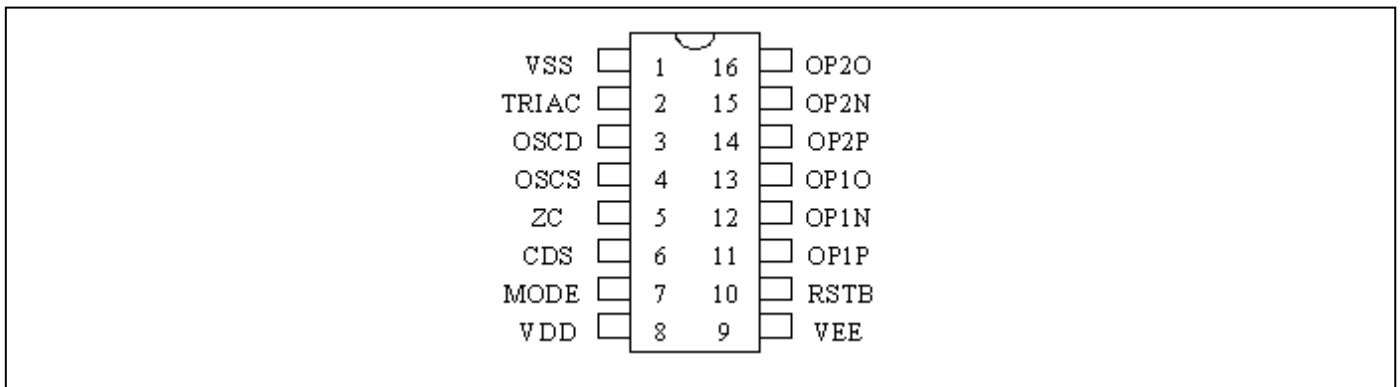
### **Features**

- Operating voltage: 5V (Typical)
- Average supply current: 120µA (Typical)
- On-chip regulator
- Build-in noise rejection circuit
- 16KHz system oscillator
- Adjustable output duration
- Override function
- ON/AUTO/OFF selectable by MODE pin
- Auto-reset with ZC signal disappearing over 3 seconds
- Output positive pulses to drive triac
- CDS to enable/disable output
- 40 second warm-up
- Quick check mode for installation
- Low cost SOIC-16 package

The PT8A2651 is a CMOS LSI chip designed for automatic PIR lamp control. The chip is equipped with operational amplifiers, a comparator, timer, a zero crossing detector, control circuit, a voltage regulator, a system oscillator, and an output timing oscillator.

Its PIR sensor detects infrared power variations induced by the motion of a human body and transforms it to a voltage variation. If the PIR output voltage variation conforms to the criteria (refer to the functional description), the lamp is turned on with an adjustable duration. The PT8A2651 offers three operating modes (ON, AUTO, OFF) which can be set through the MODE pin. While the chip is working in the AUTO mode the user can override it and switch to the quickly install mode or manual ON mode or return to the AUTO mode by switching the power switch. The chip is enclosed in a 16 pin SOIC.

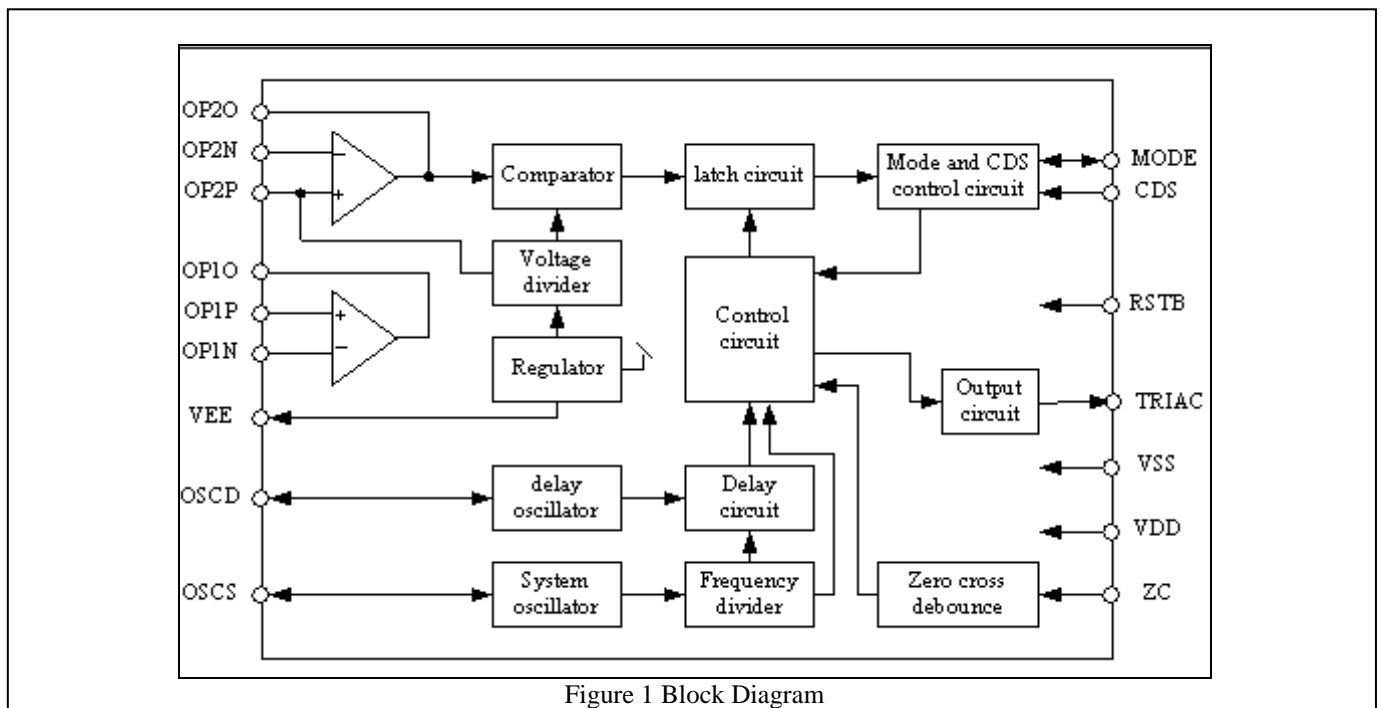
### **Pin Configuration**



### Pin Description

| Pin No. | Pin Name | I/O | Pin Description  |
|---------|----------|-----|--|
| 1       | VSS      | I   | Ground   |
| 2       | TRIAC    | O   | TRIAC drive to output two pulses, active positive pulse.   |
| 3       | OSCD     | I/O | Output timing oscillator. with an external RC to adjust output duration.   |
| 4       | OSCS     | I/O | System oscillator. with an external RC to set the system frequency. The system frequency =16KHz for normal application.  |
| 5       | ZC       | I   | Schmitt input for AC zero crossing detection   |
| 6       | CDS      | I   | CDS is connected to a CDS voltage divider for daytime/night auto-detection. Low input to this pin can disable the PIR input. CDS is a schmitt trigger input with 5-second input debounce time. |
| 7       | MODE     | I/O | Operating mode selection input:<br>VDD: TRIAC is always ON<br>VSS: TRIAC is always OFF<br>Open: Auto detection, outputs 31.25Hz square wave  |
| 8       | VDD      | I   | Positive power supply  |
| 9       | VEE      | O   | Regulated voltage output The output voltage is about 3.6V with respect to VSS.   |
| 10      | RSTB     | I   | Chip reset input, active low   |
| 11      | OP1P     | I   | Non-inverting input of OP1   |
| 12      | OP1N     | I   | Inverting input of OP1   |
| 13      | OP1O     | O   | Output of OP1  |
| 14      | OP2P     | I   | Non-inverting input of OP2, internal 1.8V default.   |
| 15      | OP2N     | I   | Inverting input of OP2   |
| 16      | OP2O     | O   | Output of OP2  |

### Block Diagram



## Maximum Ratings

|  |                      |
|--|----------------------|
| Storage Temperature .....  | -40°C to +125°C      |
| Ambient Temperature with Power applied .....                           | -20°C to +70°C       |
| Supply Voltage to Ground Potential (Input & V <sub>CC</sub> Only)..... | VSS-0.5V to VDD+0.5V |
| Supply Voltage to Ground Potential (Onput & D/O Only)..                | VSS-0.5V to VDD+0.5V |
| DC Input Voltage .....   | -0.5V to +6.0V       |
| DC Output Current .....  | 20mA                 |
| Power Dissipation .....  | 500mW                |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended operation conditions

| Sym              | Parameter                   | Test Conditions |                          | Min  | Typ | Max  | Unit |
|------------------|-----------------------------|-----------------|--------------------------|------|-----|------|------|
|                  |                             | VDD             | Conditions               |      |     |      |      |
| VDD              | Operating Voltage           | -               | -                        | 4.75 | 5.0 | 6.0  | V    |
| V <sub>IH</sub>  | “H” Input Voltage           | -               | -                        | 0.8  | -   | -    | VDD  |
| V <sub>IL</sub>  | “L” Input Voltage           | -               | -                        | -    | -   | 0.2  | VDD  |
| F <sub>SYS</sub> | System Oscillator Frequency | 5V              | ROSCS=430K<br>COSCS=180P | 12.8 | 16  | 19.2 | KHz  |
| T <sub>A</sub>   | Operating temperature       | -               | -                        | -20  | 25  | 70   | °C   |

## Electrical Characteristics

| Sym                 | Parameter                           | Test Conditions |                       | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-----------------|-----------------------|-----|-----|-----|------|
|                     |                                     | VDD             | Conditions            |     |     |     |      |
| V <sub>TH1</sub>    | CDS “H” Transfer Voltage            | 5V              | -                     | 3.0 | 3.3 | 3.6 | V    |
| V <sub>TL1</sub>    | CDS “L” Transfer Voltage            | 5V              |                       | 0.9 | 1.2 | 1.5 | V    |
| V <sub>TH2</sub>    | ZC “H” Transfer Voltage             | 5V              | -                     | 2.6 | 2.9 | 3.2 | V    |
| V <sub>TL2</sub>    | ZC “L” Transfer Voltage             | 5V              |                       | 1.1 | 1.4 | 1.7 | V    |
| V <sub>TH3</sub>    | OSCS “H” Transfer Voltage           | 5V              | -                     | 2.7 | 3   | 3.3 | V    |
| V <sub>TL3</sub>    | OSCS “L” Transfer Voltage           | 5V              |                       | 0.8 | 1   | 1.2 | V    |
| V <sub>TH4</sub>    | OSCD “H” Transfer Voltage           | 5V              | -                     | 2.7 | 3   | 3.3 | V    |
| V <sub>TL4</sub>    | OSCD “L” Transfer Voltage           | 5V              |                       | 0.8 | 1   | 1.2 | V    |
| I <sub>IH</sub>     | High level leakage current (ZC,CDS) | 5V              | V <sub>IH</sub> =4.5V | -1  | -   | 1   | μA   |
| I <sub>IL</sub>     | Low level leakage current (ZC,CDS)  | 5V              | V <sub>IL</sub> =0.5V | -1  | -   | 1   | μA   |
| I <sub>IHRSTB</sub> | RSTB Input high level current       | 5V              | V <sub>IH</sub> =4.5V | -1  | -   | -5  | μA   |
| I <sub>OH</sub>     | Output source current( TRIAC)       | 5V              | V <sub>OH</sub> =4.0V | -18 | -   | -   | mA   |
| I <sub>OL</sub>     | Output sink current(TRIAC)          | 5V              | V <sub>OL</sub> =0.5V | 3   | -   | -   | mA   |

## Voltage regulation circuit

| Sym               | Parameter                  | Test Conditions |                                      | Min  | Typ | Max  | Unit |
|-------------------|----------------------------|-----------------|--------------------------------------|------|-----|------|------|
|                   |                            | VDD             | Conditions                           |      |     |      |      |
| VEE               | Regulator Output Voltage   | 5V              | No load                              | 3.24 | 3.6 | 3.96 | V    |
| OP2P              | Non-inverting input of OP2 | 5V              | No load                              | 1.62 | 1.8 | 1.98 | V    |
| ΔV <sub>O</sub>   | Line regulation            | -               | 4.5≤VDD≤5.5V, I <sub>L</sub><br>=1mA | -    | 30  | 50   | mV   |
| ΔV <sub>LDR</sub> | Load regulation            | 5V              | 0.5mA ≤ I <sub>L</sub> ≤ 2mA         | -    | 60  | 100  | mV   |

**Operational amplifier and windows comparator**

| Parameter      | Description                     | Test conditions | Min | Typ  | Max | Unit |
|----------------|---------------------------------|-----------------|-----|------|-----|------|
| BW             | 3dB band width                  | -               | 10  | -    | -   | KHz  |
| V <sub>H</sub> | Threshold of windows comparator | VDD=5V          | 2.2 | 2.52 | 2.8 | V    |
| V <sub>L</sub> |                                 | VDD=5V          | 0.8 | 1.08 | 1.3 | V    |

**Frequency of oscillator and timing of ZC and trigger output**

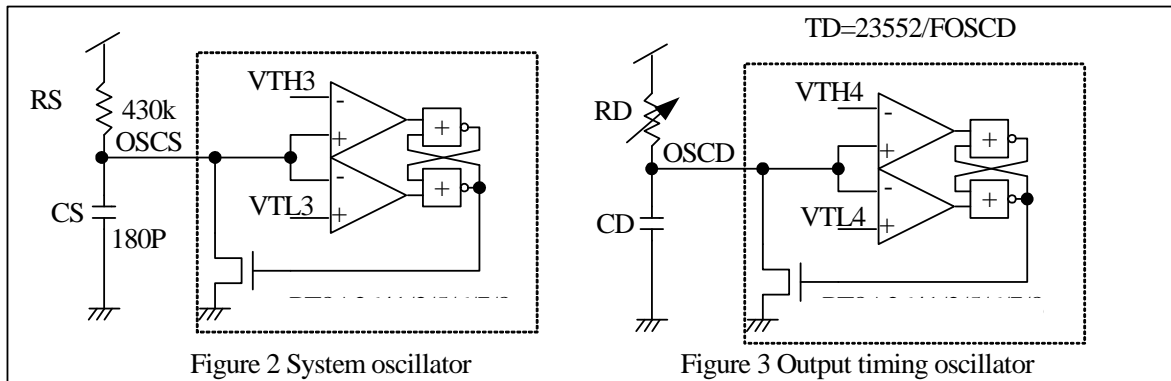
| Parameter         | Description                 | Test conditions              | Min  | Typ   | Max  | Unit |
|-------------------|-----------------------------|------------------------------|------|-------|------|------|
| F <sub>MODE</sub> | Oscillator frequency/512    | VDD=5V,<br>RS=430KΩ ,CS=180P | 25   | 31.25 | 37.5 | Hz   |
| T <sub>DZT</sub>  | Delay time from ZC to TRIAC |                              | 1.16 | 1.45  | 1.74 | ms   |
| T <sub>TPW</sub>  | TRIAC Pulse Width           |                              | 50   | 62.5  | 75   | μs   |

**Power Dissipation**

| Sym             | Description          | Test Conditions   | Min | Typ | Max | Unit |
|-----------------|----------------------|---|-----|-----|-----|------|
| I <sub>CC</sub> | Power supply current | VDD=5V, R <sub>S</sub> =430KΩ ,C <sub>S</sub> =180P,<br>R <sub>D</sub> =2MΩ, C <sub>D</sub> =104, other Input Pins=VSS,<br>all outputs float. | -   | 120 | 200 | μA   |

## Functional Description

- VEE**  
VEE supplies power to the analog front end circuit, it is about a stable 3.6V with respect to VSS normally.
- OSCS**  
OSCS is a system oscillator input pin. System frequency of 16KHz can be generated when connecting to an external RC, see figure 2 (R=430K, C=180pf).



- OSCD**  
OSCD is input pin of timing oscillator. It's connected to an external RC to obtain the desired output timer. Variable output turn-on duration can be achieved by selecting various values of RC or using a variable resistor, see figure 3.

**Note:** The minimum resistor should be low enough to 2K in order to provide adjustable range about 1000 times between min and max timer.

Formula for timer calculation as below (VH=3/5VCC, VL=1/5VCC)

Charging time of Capacitor:  $T_c = R * C * \ln[(VCC - VL) / (VCC - VH)] = 0.6931 * R * C$

Ideal calculation formula:  $TD = 23552 * T_c$ .

|                                 |      |                 |
|---------------------------------|------|-----------------|
|                                 | 5s   | 12minutes(720s) |
| R (C=223)                       | 15K  | 2000K           |
| Error compared to ideal formula | ±15% | ±5%             |

|                                 |       |      |      |       |
|---------------------------------|-------|------|------|-------|
|                                 | 3s    | 5s   | 25s  | 5000s |
| R (C=104)                       | 2K    | 3K   | 15K  | 3000K |
| Error compared to ideal formula | ±100% | ±80% | ±15% | ±5%   |

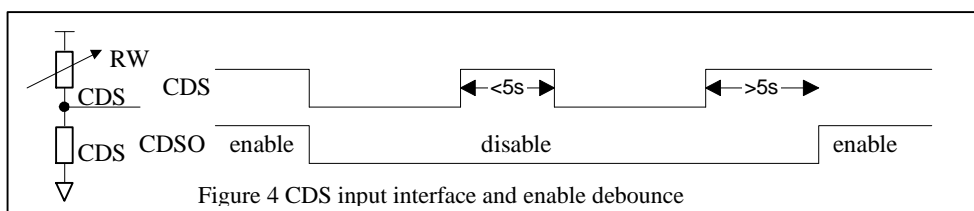
**Note:** It is recommended that C is more than 103 in order to guarantee not too bad linearity.

## TRIAC

TRIAC to drive (active positive pulse) TRIAC. The output active duration is controlled by the OSCD oscillating period.

- CDS**  
With a schmitt trigger input structure, CDS is used to distinguish lightness. Putting a cds component in a resistor divider, if light is weak enough, CDS is high the PIR input is active. Oppositely, the CDSO will be inactive when CDS is low. The input debounce time from inactive to active is 5 seconds. CDS should be pulled high without using this function. The input of CDS will be ignored once the output is active.

| CDS  | Status   | CDSO     |
|------|----------|----------|
| LOW  | Day Time | inactive |
| HIGH | Night    | active   |



**RSTB**

RSTB is used to reset the chip. It is internal pull-high and active low. The use of CRST can extend the power-on initial time. If the RSTB pin is an open circuit (without CRST), the initial time is the default (40 secs).

**Power on initial**

Because the band-pass filter and amplifier require a warm up period to reach a stable state after power-on so any inputs should be ignored during this period.

In the AUTO mode within the first 10 seconds of power-on initialization, the system allows override control to access the quickly install mode. However, after 40 seconds of the initial time the system allows override control between ON and AUTO. It will remain in the warm up period if the total initial time has not elapsed after returning to AUTO.

In case that the ZC signal disappears more than 3 seconds, the chip will restart the initialization operation. However, the restart initial time is always 40 seconds and cannot be extended by adding CRST to the RSTB pin as shown in Fig.5.

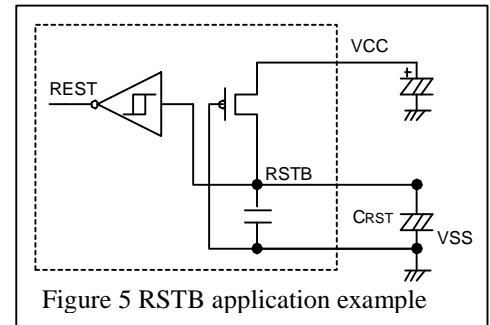


Figure 5 RSTB application example

**MODE**

MODE is a tri-state input pin used to select the operating mode.

| MODE | Operating Mode    | Description   |
|------|-------------------|---|
| VDD  | Output always ON  | TRIAC outputs positive pulse train with synchronizing to ZC   |
| VSS  | Output always OFF | TRIAC outputs low   |
| Open | AUTO              | Outputs remain off state until activated by a valid PIR trigger signal. When working in the AUTO mode, the chip allows override control by switching the ZC signal. MODE outputs square wave with frequency of 31.25Hz. |

**ZC**

ZC samples AC signal and generates zero crossing pulses to synchronize the TRIAC driver. With an effective ZC signal switching (switch OFF/ON 2 times within 3 seconds), the system provides the following additional functions:

Quickly install mode: Within 10 seconds after power-on, effective ZC switching will force the chip to enter the quickly install mode. During the mode, the outputs will be active for a duration of 1.3 seconds each time a valid PIR trigger signal is received. If a time interval exceeds 32 seconds without a valid trigger input, the chip will enter the AUTO mode automatically.

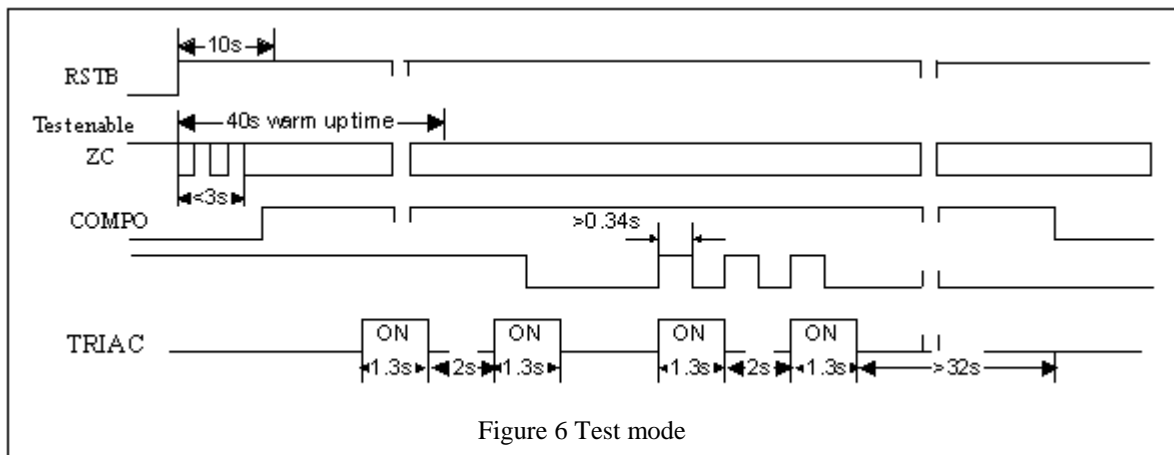


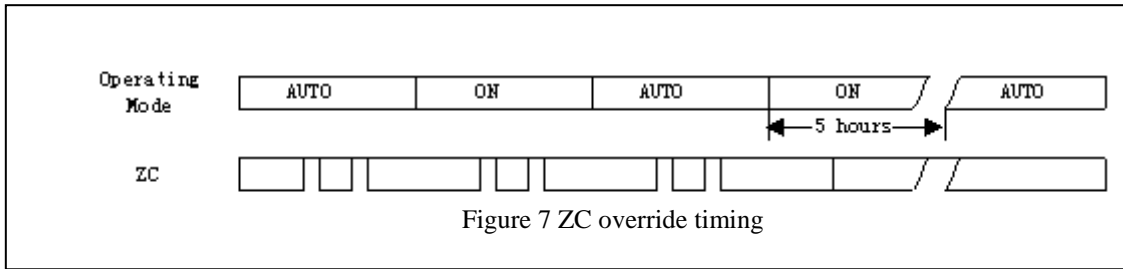
Figure 6 Test mode

**Override control**

When the chip is working in the AUTO mode (MODE= open), the output is activated by a valid PIR trigger signal and the active output duration is controlled by the OSCD oscillating period. The lamp can be switched always to "ON" from the AUTO mode by either switching the MODE pin to VDD or switching the ZC signal by an OFF/ON operation of the power switch (OFF/ON twice within 3 seconds). The term "override" refers to the change of operating mode by switching the power switch. The chip can be toggled from ON to AUTO by an override operation. Shows as Fig.7.

If the chip is overridden to ON and there is no further override operation, it will return to AUTO automatically after an internal preset ON time duration has elapsed. This override ON time duration is set to 5 hours.

During any operation (including override and the end of warm up as well as quick install mode), output will not flash.

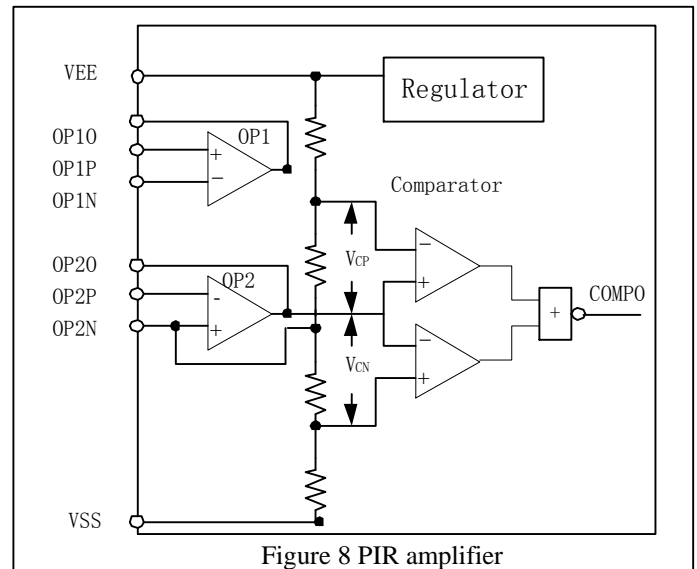


**PIR amplifier**

Refer to the following diagram for details on the front end amplifier of PIR.

In Fig.8 there are 2 op-amps with different applications. OP1 can be used independently as a first stage inverting or non-inverting amplifier for the PIR.

As the output of OP2 is directly connected to a comparator. The non-inverting input of OP2 is connected to the comparator's window center point and can be used to check this voltage and provide a bias voltage that is equal to the center point voltage of the comparator. In Fig.8 the comparator can have window width  $V_{CP}=V_{CN}=(1/5) V_{EE}$ .

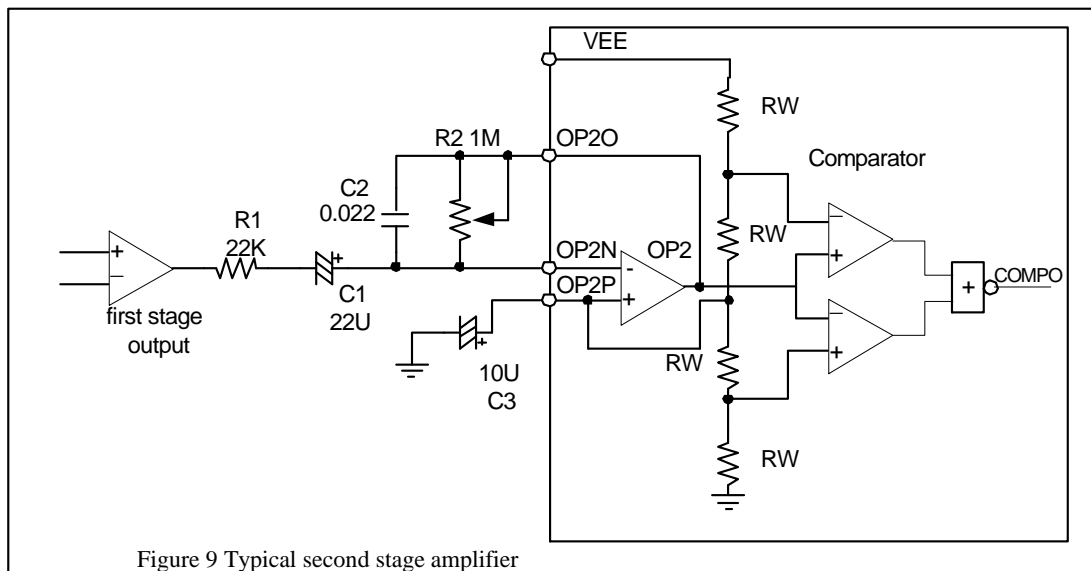


**Second stage amplifier**

Usually the second stage PIR amplifier OP2 is a simple capacitively coupled inverting amplifier with a band pass configuration. The non-inverting input terminal is biased to the center point of the comparator window and the output of OP2 is directly coupled to the comparator center point.

In Fig.9, OP2P is directly connected to the comparator window center, and with the C3 filter it can act as the bias for OP2. For this configuration  $A_V = R_2/R_1$ , low cutoff frequency  $f_L = 1/2\pi R_1 C_1$ , high cutoff frequency  $f_H = 1/2\pi R_2 C_2$ . By changing the value of R2 the sensitivity can be varied. C1 and C3 should be of low leakage types to prevent the DC operating point from change due to current leakage.

Each op-amp current consumption is approximately 15µA with the op-amps and comparator's working voltage all provided by the regulator. Refer to the following diagrams for typical PIR front end circuit.

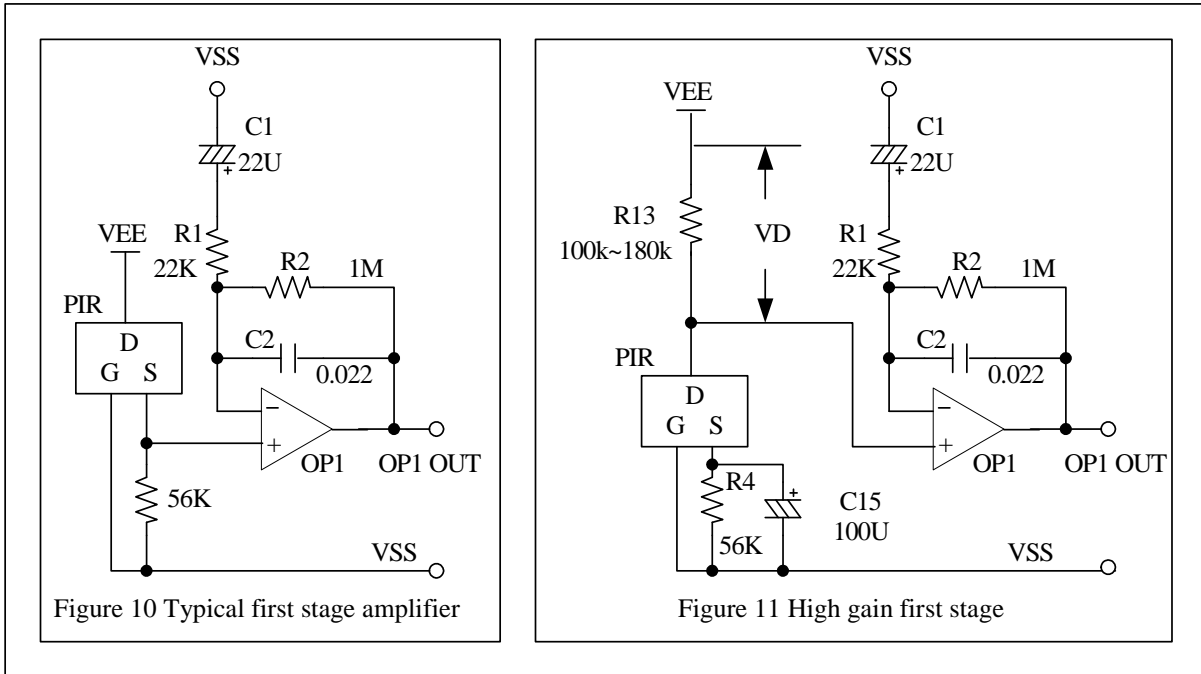


**First stage of PIR amplifier**

Fig.10 shows a typical first stage amplifier. C2 and R2 form a simple low pass filter with cut off frequency at 7Hz. The low frequency response is governed by R1 and C1 with cut-off frequency at 0.33Hz. The formula to calculate the gain shows as below.

$$AV = (R1+R2)/R1$$

Fig.10 and Fig.11 are similar but in Fig.10 the input signal of amplifier is taken from the drain of the PIR. This has higher gain than that in Fig.10. Since OP1 is a PMOS input, VD has to be greater than 1.2V for adequate operation.



**COMPO**

COMPO is output from comparator, it can be output at pin 10 if needed.

Signal from two-stage opamp outputs to a window comparator as pre-operation, COMPO outputs active positive pulses with various width once signal beyond window level. Whether an active PIR signal is detected, see figure 12 for detail.

**Trigger timing**

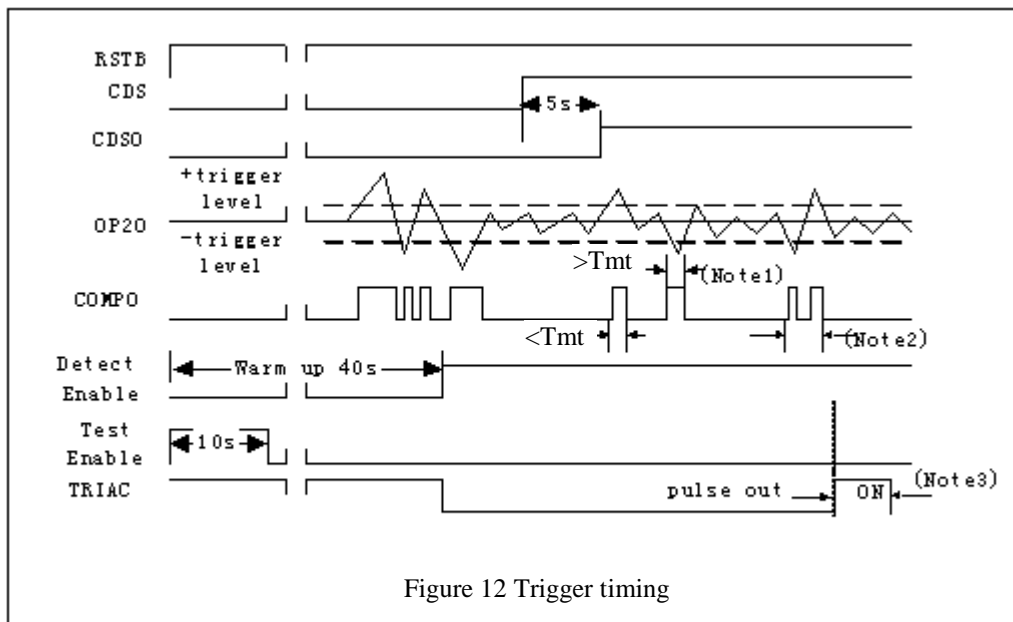


Figure 12 Trigger timing



Referring to Figure 12

**Note:** 1. One measurable trigger width ( $T_{mt}$ ) from comparator output is 24ms~ 32ms which varies with frequency of system oscillator (typical system frequency=16KHz ).

2. The output is activated if the trigger signal conforms to the following criteria:

- A trigger signal sustains duration: 0.34 seconds.
- 2 trigger signals within 2 seconds with one of the trigger signal sustain:0.16 seconds.
- More than 3 measurable triggers within 2 seconds.

3. The output duration is set by an external RC that is connected to the OSCD pin.

**Retrigger**

If another signal is attained in trigger hold time, the circuit will be retriggered, and the trigger hold time will be started from this time.

**Timing Diagram**

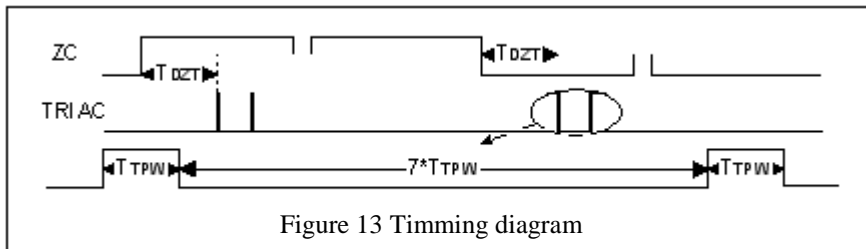
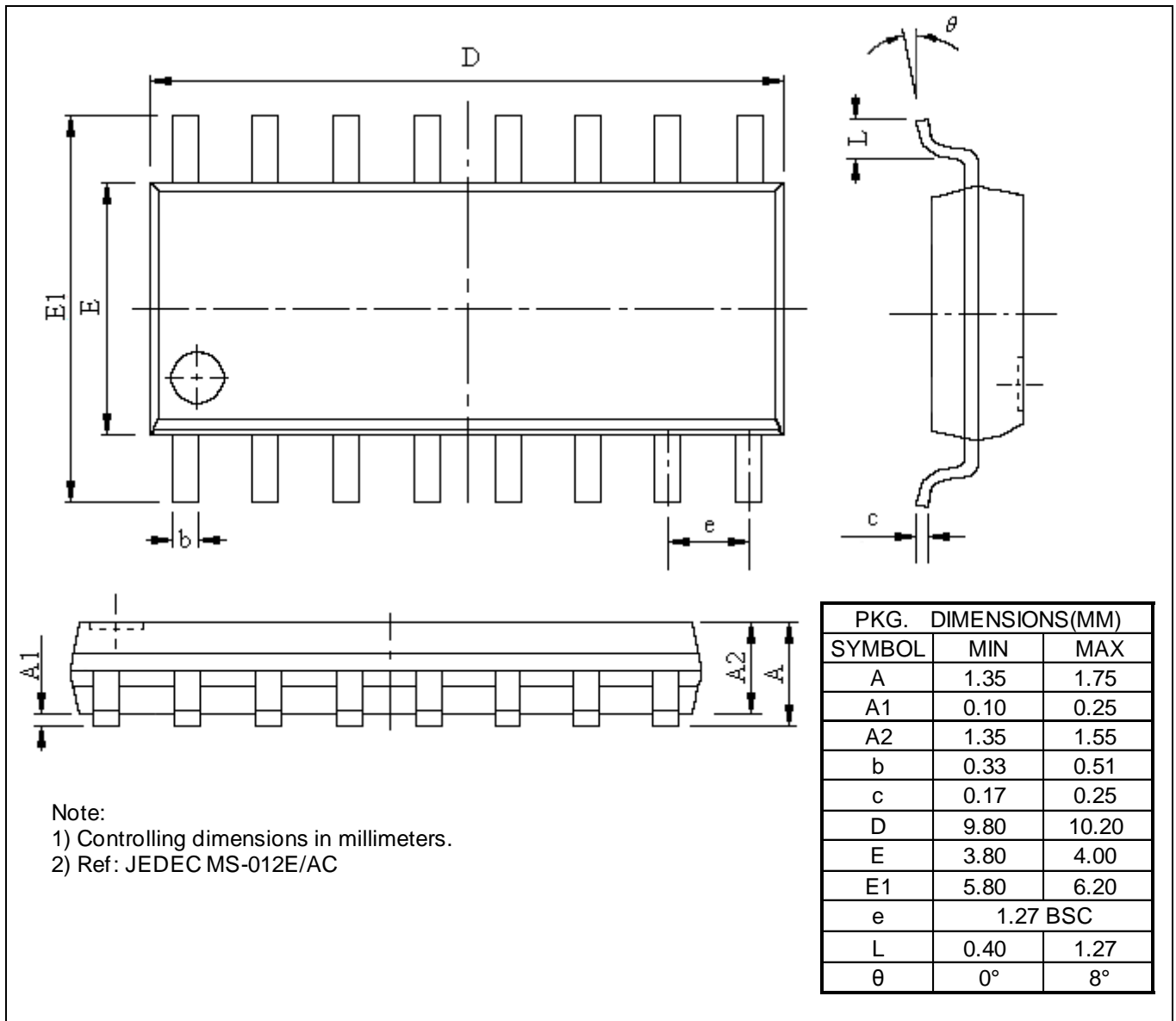


Figure 13 Timing diagram

### Mechanical Information

WE (SOIC-16)



### Ordering Information

| Ordering No. | Package Code | Package           |
|--------------|--------------|-------------------|
| PT8A2651WE   | W            | Lead free SOIC-16 |

**Note:**

- E = Pb-free
- Adding X Suffix= Tape/Reel

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