

Features

- Highly precision: $\pm 1.5\%$ (25 °C); $\pm 2.5\%$ (-40 °C to +85 °C);
- Low power consumption: 1.0 μ A @ 3.6V V_{CC}
- Detect voltage range: 1.8 to 5V in 100mV increments
- Operating voltage range: 1.2V ~ 5.5V
- Output configuration: N-channel open drain or CMOS
- Special threshold voltage product according to customer need
- Operating temperature range: -40 °C to + 85 °C
- Detect voltage temperature characteristics: $\pm 2.5\%$ \times TYP

Description

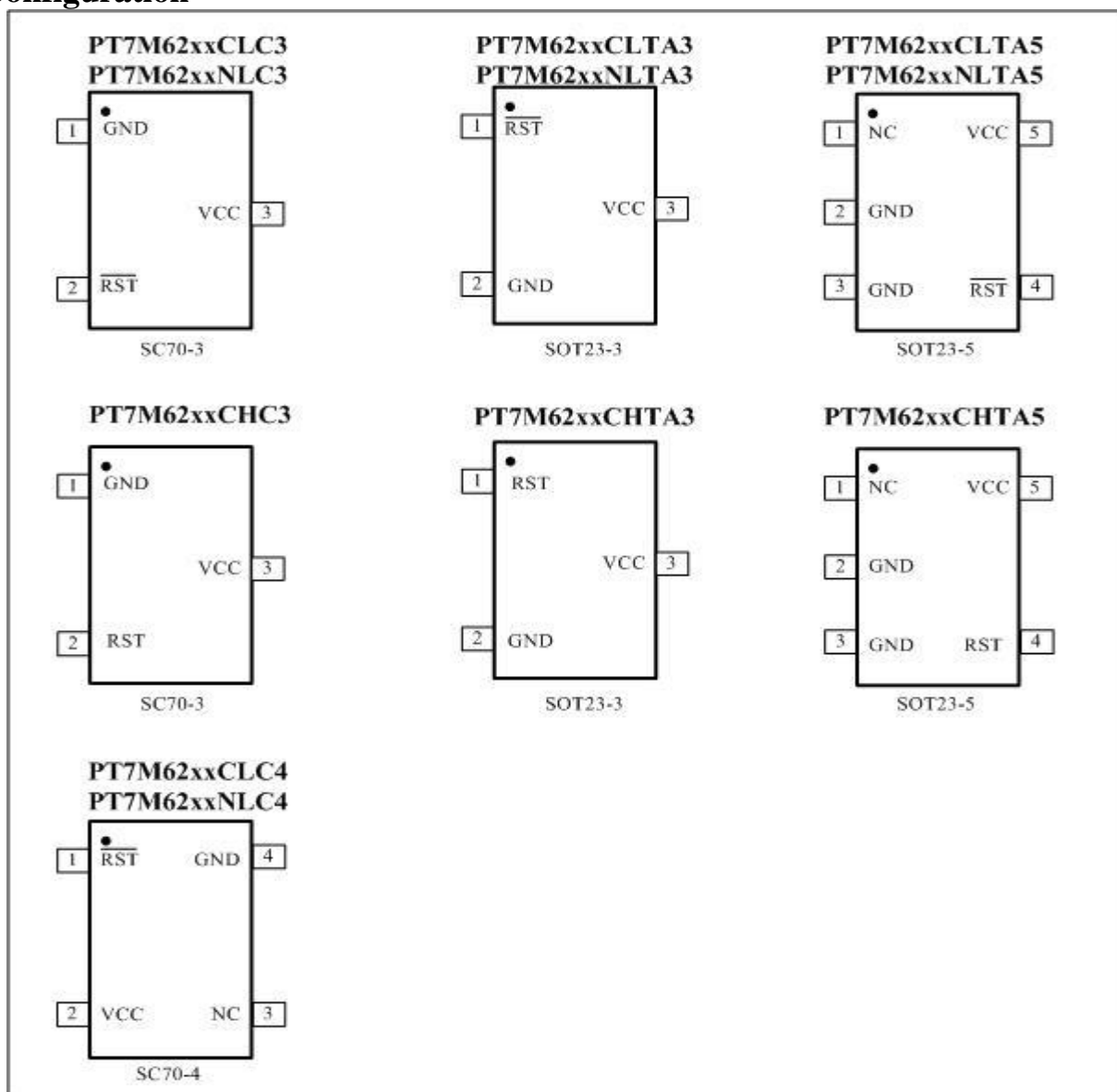
The PT7M62xx series of ultra-low-power voltage detectors monitor battery, power-supply and system voltages. Each circuit includes a precision bandgap reference, a comparator, internally trimmed resistor networks that set specified trip thresholds, and an internal 5% threshold hysteresis circuit. Output is asserted when V_{CC} rises above V_{TH+} ($V_{TH+} = V_{TH-} \times 1.05$) and remains asserted until V_{CC} falls below the internal V_{TH-}. These devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltages from +1.8V to +5V in 100mV increments. The series are voltage detectors with a propagation delay of 20 μ s(V_{CC} rise).

The family is available with three output stage options: push-pull with active-low output, push-pull with active-high output, and open drain with active-low output.

Function Comparison Table

Item	Part No.	Reset Output				Threshold
		Open-Drain		Push-Pull		
		Active high	Active low	Active high	Active low	
1	PT7M62xxCL	-	-	-	√	1.8V to 5.0V in 100mV increments
2	PT7M62xxCH	-	-	√	-	
3	PT7M62xxNL	-	√	-	-	

Pin Configuration

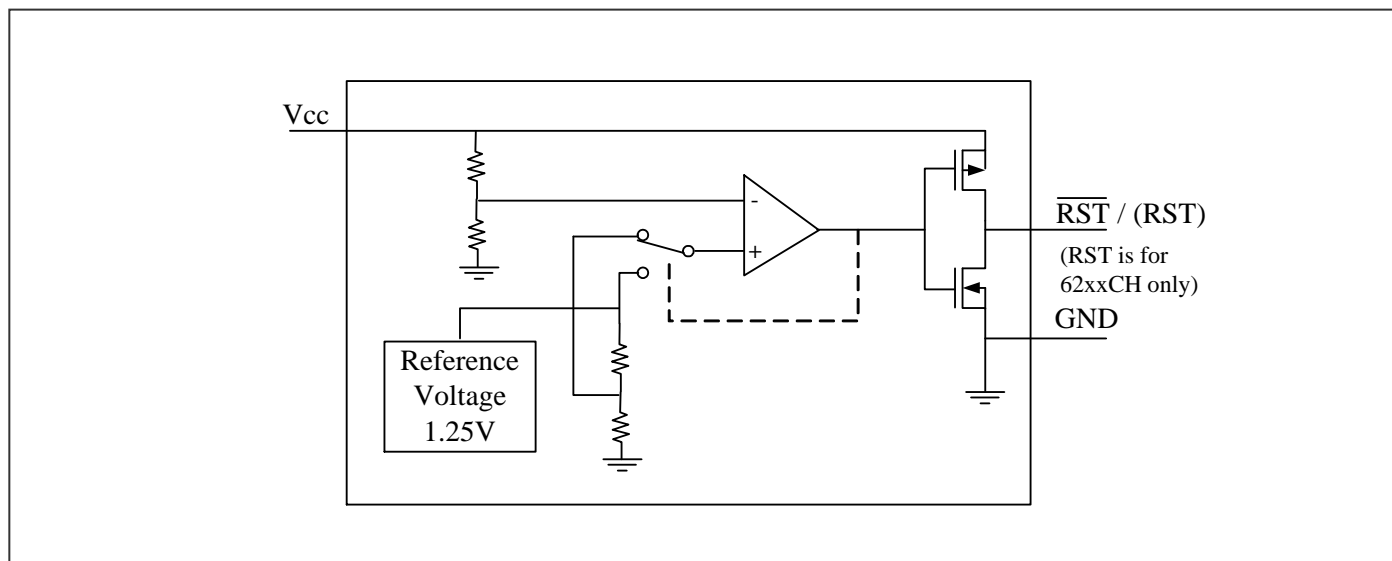


Pin Description

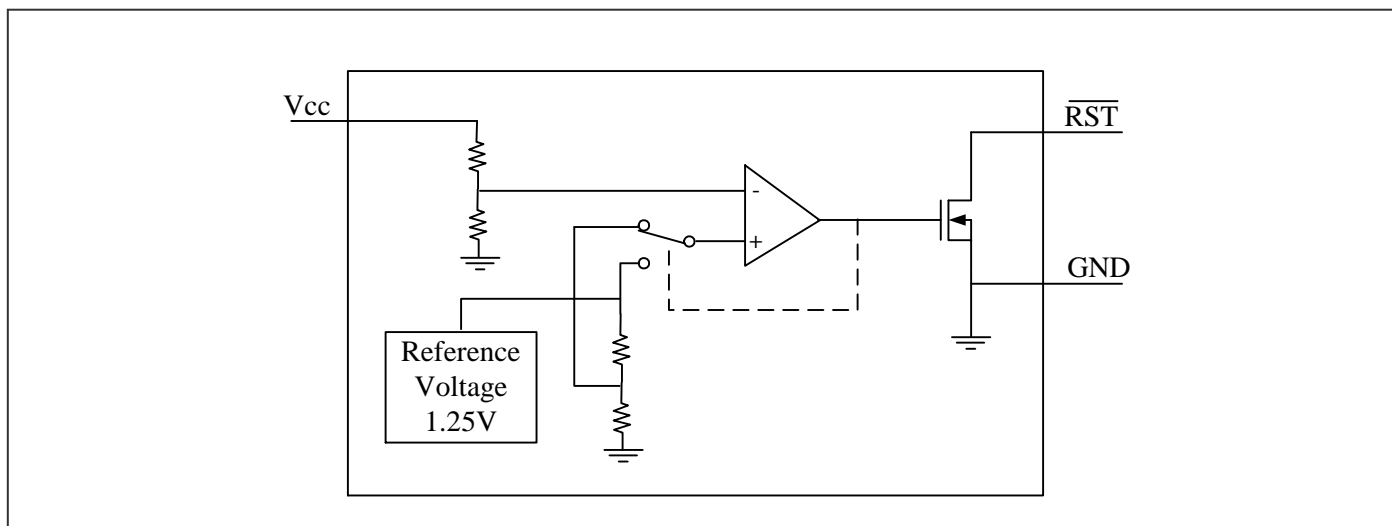
Name	Type	Description
$\overline{\text{RST}}$	O	Reset Output (PT7M62xxCL/NL): $\overline{\text{RST}}$ is asserted when V_{CC} drops below voltage threshold V_{TH} . Active low.
RST	O	Reset Output (PT7M62xxCH): RST is asserted when V_{CC} drops below voltage threshold V_{TH} . Active high.
GND	P	Ground
VCC	P	Supply Voltage.

Block Diagram

Block Diagram of PT7M62xxCL/CH



Block Diagram of PT7M62xxNL



Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND)	-0.3V to +6.0V
DC Input Voltage (All inputs except V _{CC} and GND).....	-0.3V to V _{CC} +0.3V
DC Output Current (All outputs)	20mA
Power Dissipation	320mW (Depend on package)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

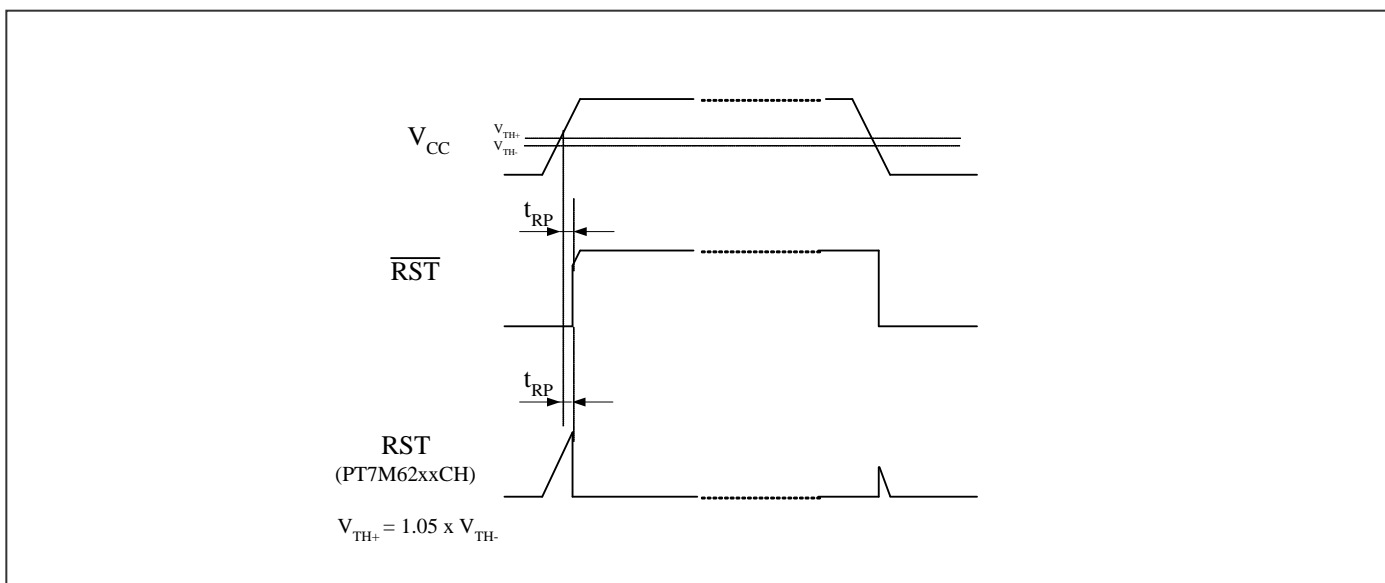
(V_{CC} = 1.2V to 5.5V, T_A = -40~85 °C, unless otherwise noted. Typical values are at T_A = +25 °C)

Description		Sym.	Test Conditions	Min	Typ	Max	Unit
Supply Voltage		V _{CC}	T _A = 0~70 ℃	1.0	-	5.5	V
			T _A = -40~85 ℃	1.2	-	5.5	
Supply Current		I _{CC}	V _{CC} = 3V. No load.	-	0.9	3.0	μA
			V _{CC} = 5V. No load.	-	1.3	3.6	μA
Output Driving	Output high	V _{OH}	V _{CC} ≥ 1.8V, I _{source} = 1mA	0.8×V _{CC}	-	-	V
			V _{CC} ≥ 2.5V, I _{source} = 3mA	0.8×V _{CC}	-	-	
			V _{CC} ≥ 4.5V, I _{source} = 8mA	0.8×V _{CC}	-	-	
	Output low	V _{OL}	V _{CC} ≥ 1.2V, I _{sink} = 1mA	-	-	0.3	V
			V _{CC} ≥ 2.5V, I _{sink} = 4mA	-	-	0.3	
			V _{CC} ≥ 4.5V, I _{sink} = 9mA	-	-	0.4	
Open-Drain Output Leakage Current		I _{LKG}	-	-	-	1	μA
Voltage Threshold		V _{TH+}	+25℃	(V _{TH+}) ×0.985	V _{TH+}	(V _{TH+}) ×1.015	V
			-40℃~85℃	(V _{TH+}) ×0.975	V _{TH+}	(V _{TH+}) ×1.025	
voltage threshold Hysteresis		V _{HYST}	V _{HYST} = [(V _{TH+})-(V _{TH-})]/(V _{TH-}) ×100%	3	5	6	%

Note: V_{TH-} = V_{TH+} / 1.045. V_{TH-} is voltage threshold when V_{CC} falls from high to low. V_{TH+} is voltage threshold when V_{CC} rises from low to high.

AC Electrical Characteristics

Timing diagram

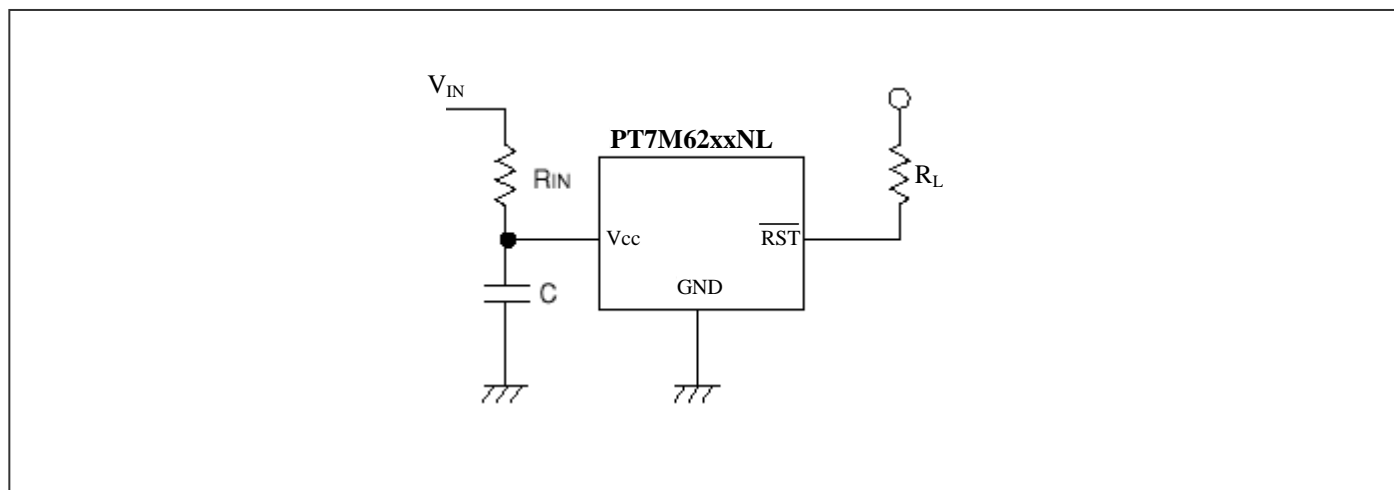


($V_{CC} = 1.2V$ to $5.5V$, $T_A = -40 \sim 85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$)

Sym.	Description	Test Conditions	Min	Typ	Max	Unit
t_{RP}	Timeout Period	-	-	-	200	μs
t_p	Delay	-	-	50	-	μs

Typical Operation Circuit

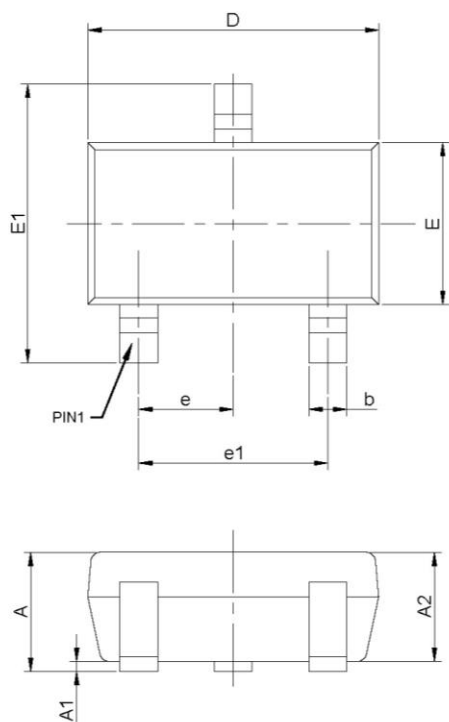
PT7M62xxNL Application Example



Please use N-ch open drains configuration, when a resistor R_{IN} is connected between the V_{CC} pin and power source V_{IN} . In such cases, please ensure that R_{IN} is less than $10k\Omega$ and that C is more than $0.1\mu F$. R_L could be $1k\Omega$ to $510k\Omega$.

Mechanical Information

TA3 (SOT23)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.75	3.10
E	1.45	1.75
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
θ	0°	8°

Note:

1. Comply with MO-178C, except D Max.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 3-Pin, Small Outline Transistor Plastic Package (SOT23)

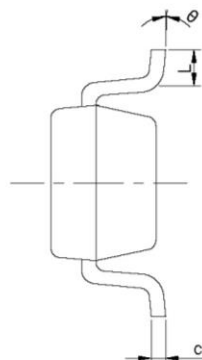
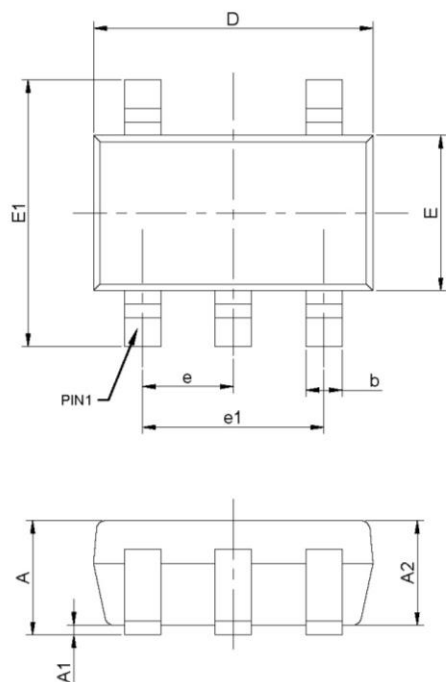
PACKAGE CODE: TA (TA3)

DOCUMENT CONTROL #: PD-2143

REVISION: A

16-0080

TA5 (SOT23)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.75	3.05
E	1.45	1.75
E1	2.60	3.00
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
θ	0°	8°

Note:

1. Ref: JEDEC MO-178C/AA
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BUR



DATE: 03/29/16

DESCRIPTION: 5-Pin, Small Outline Transistor Plastic Package (SOT23)

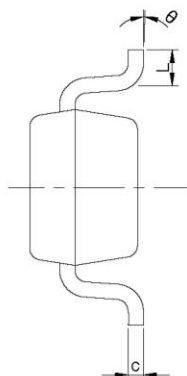
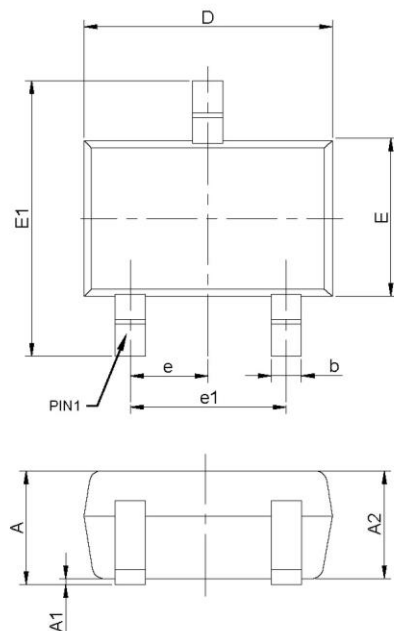
PACKAGE CODE: TA (TA5)

DOCUMENT CONTROL #: PD-2144

REVISION: A

16-0081

C3 (SC70)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.15	0.40
c	0.08	0.22
D	1.80	2.20
E	1.10	1.40
E1	1.75	2.45
e	0.65 BSC	
e1	1.30 BSC	
L	0.26	0.46
θ	0°	8°

Note:

1. Comply with MO-203C, except b Max, D Min, D Max, E1 Min and E1 Max.
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR



DATE: 03/29/16

DESCRIPTION: 3-Pin, SOT323 (SC70)

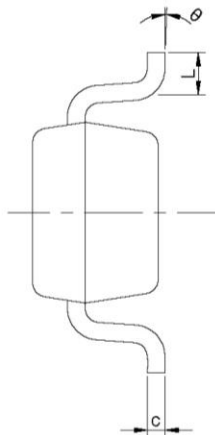
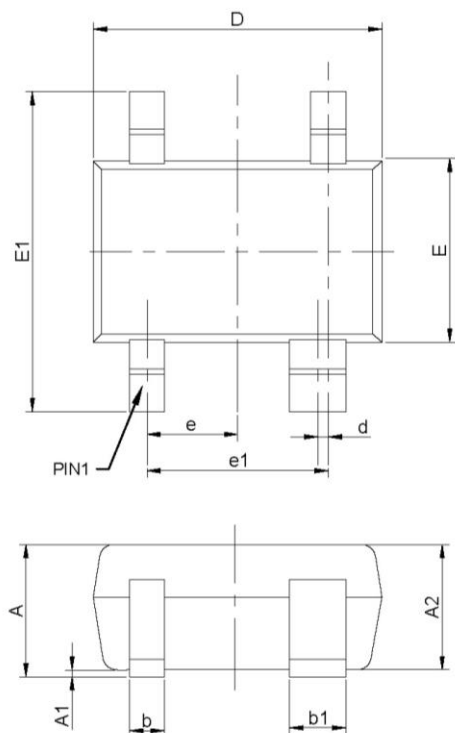
PACKAGE CODE: C (C3)

DOCUMENT CONTROL#: PD-2147

REVISION: A

16-0077

C4 (SC70)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.25	0.40
b1	0.35	0.50
c	0.08	0.15
D	2.00	2.20
d	0.05 TYP	
E	1.15	1.35
E1	2.15	2.45
e	0.65 TYP	
e1	1.20	1.40
L	0.26	0.46
θ	0°	8°

Notes:

1. Ref. JEDEC MO-203B



DATE: 06/18/13

DESCRIPTION: 4-Pin, SOT343 (SC70)

PACKAGE CODE: C (C4)

DOCUMENT CONTROL#: PD-2148

REVISION: --

13-0187

SOT23/SC70/SOT143 Package Top Marking Instruction

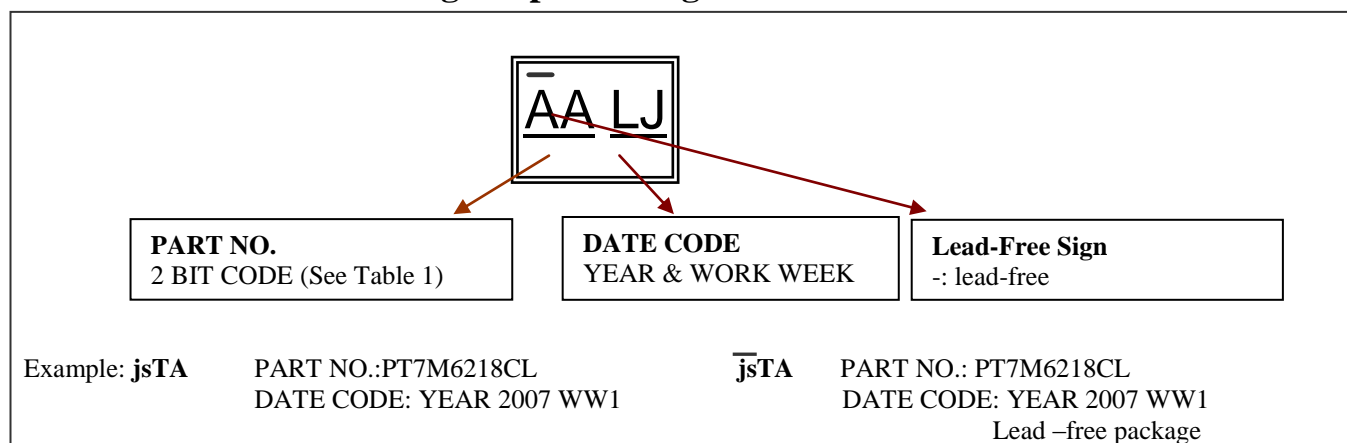


Table 1 Part No code comparison table

No.	Part No.	Code	No.	Part No.	Code	No.	Part No.	Code
1	PT7M6218CL	js	34	PT7M6229CL	kz	67	PT7M6240CL	mg
2	PT7M6218CH	jt	35	PT7M6229CH	la	68	PT7M6240CH	mh
3	PT7M6218NL	ju	36	PT7M6229NL	lb	69	PT7M6240NL	mi
4	PT7M6219CL	jv	37	PT7M6230CL	lc	70	PT7M6241CL	mj
5	PT7M6219CH	jw	38	PT7M6230CH	ld	71	PT7M6241CH	mk
6	PT7M6219NL	jx	39	PT7M6230NL	le	72	PT7M6241NL	ml
7	PT7M6220CL	jy	40	PT7M6231CL	lf	73	PT7M6242CL	mm
8	PT7M6220CH	jz	41	PT7M6231CH	lg	74	PT7M6242CH	mn
9	PT7M6220NL	ka	42	PT7M6231NL	lh	75	PT7M6242NL	mo
10	PT7M6221CL	kb	43	PT7M6232CL	li	76	PT7M6243CL	mp
11	PT7M6221CH	kc	44	PT7M6232CH	lj	77	PT7M6243CH	mq
12	PT7M6221NL	kd	45	PT7M6232NL	lk	78	PT7M6243NL	mr
13	PT7M6222CL	ke	46	PT7M6233CL	ll	79	PT7M6244CL	ms
14	PT7M6222CH	kf	47	PT7M6233CH	lm	80	PT7M6244CH	mt
15	PT7M6222NL	kg	48	PT7M6233NL	ln	81	PT7M6244NL	mu
16	PT7M6223CL	kh	49	PT7M6234CL	lo	82	PT7M6245CL	mv
17	PT7M6223CH	ki	50	PT7M6234CH	lp	83	PT7M6245CH	mw
18	PT7M6223NL	kj	51	PT7M6234NL	lq	84	PT7M6245NL	mx
19	PT7M6224CL	kk	52	PT7M6235CL	lr	85	PT7M6246CL	my
20	PT7M6224CH	kl	53	PT7M6235CH	ls	86	PT7M6246CH	mz
21	PT7M6224NL	km	54	PT7M6235NL	lt	87	PT7M6246NL	na
22	PT7M6225CL	kn	55	PT7M6236CL	lu	88	PT7M6247CL	nb
23	PT7M6225CH	ko	56	PT7M6236CH	lv	89	PT7M6247CH	nc
24	PT7M6225NL	kp	57	PT7M6236NL	lw	90	PT7M6247NL	nd
25	PT7M6226CL	kq	58	PT7M6237CL	lx	91	PT7M6248CL	ne
26	PT7M6226CH	kr	59	PT7M6237CH	ly	92	PT7M6248CH	nf
27	PT7M6226NL	ks	60	PT7M6237NL	lz	93	PT7M6248NL	ng
28	PT7M6227CL	kt	61	PT7M6238CL	ma	94	PT7M6249CL	nh
29	PT7M6227CH	ku	62	PT7M6238CH	mb	95	PT7M6249CH	ni
30	PT7M6227NL	63	PT7M6238NL	mc	96	PT7M6249NL	nj	
31	PT7M6228CL	kw	64	PT7M6239CL	md	97	PT7M6250CL	nk
32	PT7M6228CH	kx	65	PT7M6239CH	me	98	PT7M6250CH	nl
33	PT7M6228NL	ky	66	PT7M6239NL	mf	99	PT7M6250NL	nm

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Part Number	Package Code	Package
PT7M62xxCLTA3E	TA	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M62xxCLTA5E	TA	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M62xxCLC3E	C	3-Pin, SOT323 (SC70)
PT7M62xxCLC4E	C	4-Pin, SOT343 (SC70)
*PT7M62xxCHTA3E	TA	3-Pin, Small Outline Transistor Plastic Package (SOT23)
*PT7M62xxCHTA5E	TA	5-Pin, Small Outline Transistor Plastic Package (SOT23)
*PT7M62xxCHC3E	C	3-Pin, SOT323 (SC70)
PT7M62xxNLTA3E	TA	3-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M62xxNLTA5E	TA	5-Pin, Small Outline Transistor Plastic Package (SOT23)
PT7M62xxNLC3E	C	3-Pin, SOT323 (SC70)
PT7M62xxNLC4E	C	4-Pin, SOT343 (SC70)

Note 1:

- “xx” refer to voltage range, see below table 1.
- E = Pb-free or Pb-free & Green
- Adding X Suffix= Tape/Reel
- Contact Pericom for availability.
- “*” for CH part, please check the storage with related sales.

Table 1 Suffix “xx” definition of PT7M62xx

Suffix xx	V _{TH+} (V)	Suffix xx	V _{TH+} (V)	Suffix xx	V _{TH+} (V)	Suffix xx	V _{TH+} (V)	Suffix xx	V _{TH+} (V)
18	1.8	25	2.5	32	3.2	39	3.9	46	4.6
19	1.9	26	2.6	33	3.3	40	4.0	47	4.7
20	2.0	27	2.7	34	3.4	41	4.1	48	4.8
21	2.1	28	2.8	35	3.5	42	4.2	49	4.9
22	2.2	29	2.9	36	3.6	43	4.3	50	5.0
23	2.3	30	3.0	37	3.7	44	4.4		
24	2.4	31	3.1	38	3.8	45	4.5		

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