PI3A3160

3.3V, SOTiny™ 0.4Ω Dual SPDT Analog Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.4Ω (+2.7V Supply)
- Wide V_{DD} Range: +1.5V to +4.2V
- Low Power Consumption : 5µW
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 20ns max. at 3.3V
- High Off Isolation: –27dB at 100 kHz
- –41dB (100 kHz) Crosstalk Rejection Reduces Signal Distortion
- Extended Industrial Temperature Range: –40°C to 85°C
- Packaging:
  – Pb-free & Green, 12-pin TDFN (ZE)

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals

Pin Description

Pin Number	Name	Description
8, 11	NOx	Data Port (Normally Open)
3, 6	GND	Ground
2, 5	NCx	Data Port (Normally Closed)
1, 4	COMx	Common Output/Data Port
9, 12	V_{DD}x	Postive Power Supply(2)
7, 10	INx	Logic Control

Notes:
1. x = 0 or 1
2. V_{DD0} ad V_{DD1} are not internally connected. Each must be powered seperately.

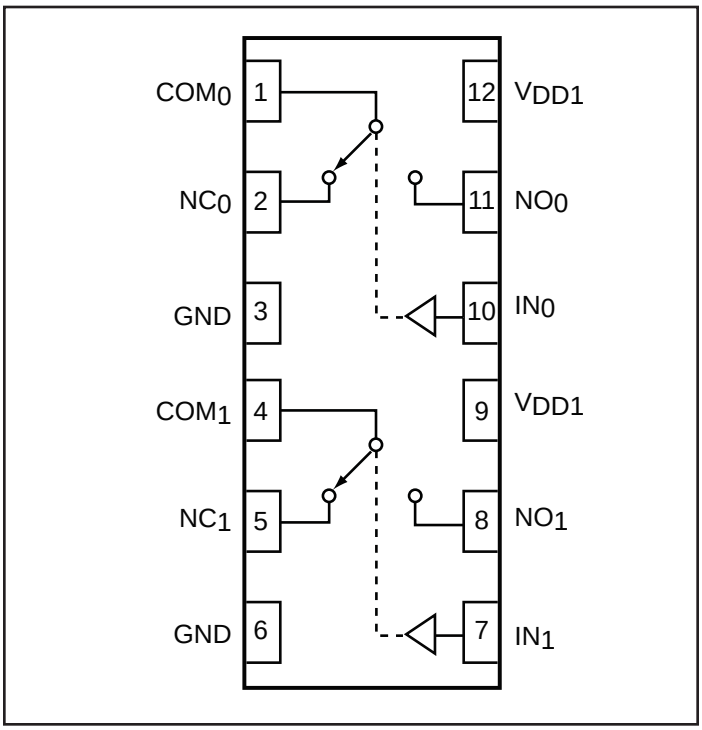
Description

The PI3A3160 is a fast Dual single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, +1.5V to +4.2V, the switch has an On-Resistance of 0.4Ω at 3.0V.

Control inputs, IN, tolerates input drive signals up to 3.3V, independent of supply voltage.

PI3A3160 is a lower voltage and On-Resistance replacement for the PI5A3158.

Block Diagram / Pin Configuration



Function Table

Logic Input	Function
0	NCx Connected to COMx
1	NOx Connected to COMx

Absolute Maximum Ratings

Voltages Referenced to GND

V_{DD} ..... –0.5V to +4.4V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (1)..... –0.5V to V_+ +0.3V
or 30mA, whichever occurs first

Current (any terminal)..... ±200mA

Peak Current, COM, NO, NC
(Pulsed at 1ms, 10% duty cycle)..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT23 (derate 7.1mW/ºC above +70ºC)..... 0.5W

Storage Temperature ..... –65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note 1: Signals on NC, NO, COM, or IN exceeding V_{DD} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +4.2V Supply

(V_{DD} = +4.2V ± 5%, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range (3)	V_{ANALOG}		Full	0		V_{DD}	V
On Resistance	R_{ON}	V_{DD} = 4.0V, I_{COM} = 99mA, V_{IN} = 0V to V_{DD}	25		0.4	0.45	Ω
			Full			0.6	
On-Resistance Match Between Channels(4)	ΔR_{ON}		25			0.08	
			Full			0.09	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{DD} = 4.0V, I_{COM} = 100mA	25			0.1	
			Full			0.1	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_{DD} =4.2V	25	-100		100	nA
			Full	-400		400	
COM On Leakage Current(6)	$I_{COM(ON)}$	V_{DD} = 4.2V	25	-200		200	
			Full	-400		400	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
8. Between any two switches. See Figure 5.

Electrical Specifications - Single +3.3V Supply

(V_{DD} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range (3)	V_{ANALOG}		Full	0		V_{DD}	V
On Resistance	R_{ON}	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = +1.5V	25		0.4	0.45	Ω
			Full			0.6	
On-Resistance Match Between Channels(4)	ΔR_{ON}		25			0.08	
			Full			0.09	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0.8V, 2.0V	25			0.1	
			Full			0.1	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_{DD} = 3.3V, V_{COM} = 0V, V_{NO} or V_{NC} = +2.0V	25	-100		100	nA
			Full	-400		400	
COM On Leakage Current(6)	$I_{COM(ON)}$	V_{DD} = 3.3V, V_{COM} = +2.0V, V_{NO} or V_{NC} = +2.0V	25	-200		200	
			Full	-400		400	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
8. Between any two switches. See Figure 5.

Electrical Specifications - Single +4.2V Supply

(V_{DD} = +4.2V ± 5%, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V)

Description	Parameters	Test Conditions	Temp (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed logic High Level	Full	1.6			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level				0.7	
Input Current with Voltage High	I_{INH}	V_{IN} = 1.4V, all others = 0.5V		–1		1	µA
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.5V, all other = 1.4V		–1		1	
Dynamic							
Turn-On Time	t_{ON}	V_{DD} = 4.2V, V_{NO} or V_{NC} = 2.0V, Figure 1	25			20	ns
			Full			25	
Turn-Off Time	t_{OFF}		25			12	
			Full			15	
Break-Before-Make	t_{BBM}	V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 8	25	1	12		
			Full	1			
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	25		100		pC
Off Isolation(7)	O_{IRR}	R_L = 50Ω, f = 100kHz, Figure 3			-27		dB
Cross Talk(8)	X_{TALK}	R_L = 50Ω, f = 100kHz, Figure 4			-41		
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 5			56		pF
COM Off Capacitance	$C_{COM(OFF)}$				56		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6			160		
Supply							
Power-Supply Range	V_{DD}		Full	1.5		3.6	V
Positve Supply Current	I_{CC}	V_{DD} = 3.6V, V_{IN} = 0V or V_{DD}	25			0.3	µA

Notes:

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3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
8. Between any two switches. See Figure 5.

Electrical Specifications - Single +3.3V Supply

(V_{DD} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Description	Parameters	Test Conditions	Temp (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed logic Low Level				0.5	
Input Current with Voltage High	I_{INH}	V_{IN} = 1.4V, all others = 0.5V		–1		1	µA
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.5V, all other = 1.4V		–1		1	
Dynamic							
Turn-On Time	t_{ON}	V_{DD} = 3.3V, V_{NO} or V_{NC} = 2.0V, Figure 1	25			20	ns
			Full			25	
Turn-Off Time	t_{OFF}		25			12	
			Full			15	
Break-Before-Make	t_{BBM}	V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 8	25	1	12		
			Full	1			
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	25		100		pC
Off Isolation(7)	O_{IRR}	R_L = 50Ω, f = 100kHz, Figure 3			-27		dB
Cross Talk(8)	X_{TALK}	R_L = 50Ω, f = 100kHz, Figure 4			-41		
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 5			56		pF
COM Off Capacitance	$C_{COM(OFF)}$				56		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6			160		
Supply							
Power-Supply Range	V_{DD}		Full	1.5		3.6	V
Positve Supply Current	I_{CC}	V_{DD} = 3.6V, V_{IN} = 0V or V_{DD}	25			0.3	µA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
8. Between any two switches. See Figure 5.

Electrical Specifications - Single +2.5V Supply

(V_{DD} = +2.5V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Description	Parameters	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V_{DD}	V
On Resistance	R_{ON}	V_{DD} = 2.5V, I_{COM} = 80mA, V_{NO} or V_{NC} = 1.8V	25			0.5	Ω
			Full			0.55	
On-Resistance Match Between Channels (4)	ΔR_{ON}		25			0.09	
			Full			0.09	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{DD} = 2.5V, I_{COM} = 80mA, V_{NO} or V_{NC} = 0.8V 1.8V	25			0.1	
			Full			0.1	
Dynamic							
Turn-On Time	t_{ON}	V_{DD} = 2.5V, V_{NO} or V_{NC} = 1.8V, Figure 1	25			20	ns
			Full			30	
Turn-Off Time	t_{OFF}		25			12	
			Full			15	
Break-Before-Make	t_{BBM}	V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 8	25	1	15		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		60		pC
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	1.4			V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.5	
Input HIGH Current	I_{INH}	V_{IN} = 1.4V, all others = 0.5V	Full	–1		1	µA
Input HIGH Current	I_{INL}	V_{IN} = 0.5V, all others = 1.4V	Full	–1		1	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Electrical Specifications - Single +1.8V Supply

(V_{DD} = +1.8V ± 10%, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V)

Description	Parameters	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V_{DD}	V
On-Resistance	R_{ON}	V_{DD} = 1.8V, I_{COM} = 60mA, V_{NO} or V_{NC} = 1.5V	25			0.55	Ω
			Full			0.7	
On-Resistance Match Between Channels (4)	ΔR_{ON}		25			0.03	
			Full			0.03	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{DD} = 1.8V, I_{COM} = 60mA, V_{NO} or V_{NC} = 0.8V, 1.5V	25			0.9	
			Full			1.1	
Dynamic							
Turn-On Time	t_{ON}	V_{DD} = 1.8V, V_{NO} or V_{NC} = 1.5V, Figure 1	25			40	ns
			Full			50	
Turn-Off Time	t_{OFF}		25			12	
			Full			15	
Break-Before-Make	t_{BBM}	V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 8	25	1	30		
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		40		pC
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	1.4			V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.5	
Input HIGH Current	I_{INH}	V_{IN} = 1.4V, all others = 0.5V	Full	–1		1	µA
Input HIGH Current	I_{INL}	V_{IN} = 0.5V, all others =1.4V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Test Circuits/Timing Diagrams

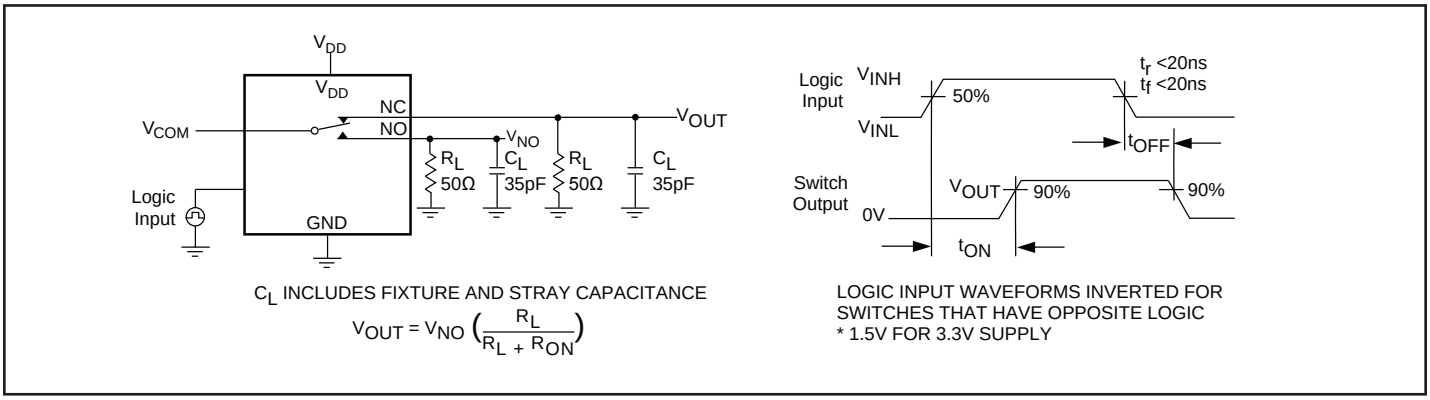


Figure 1. Switching Time

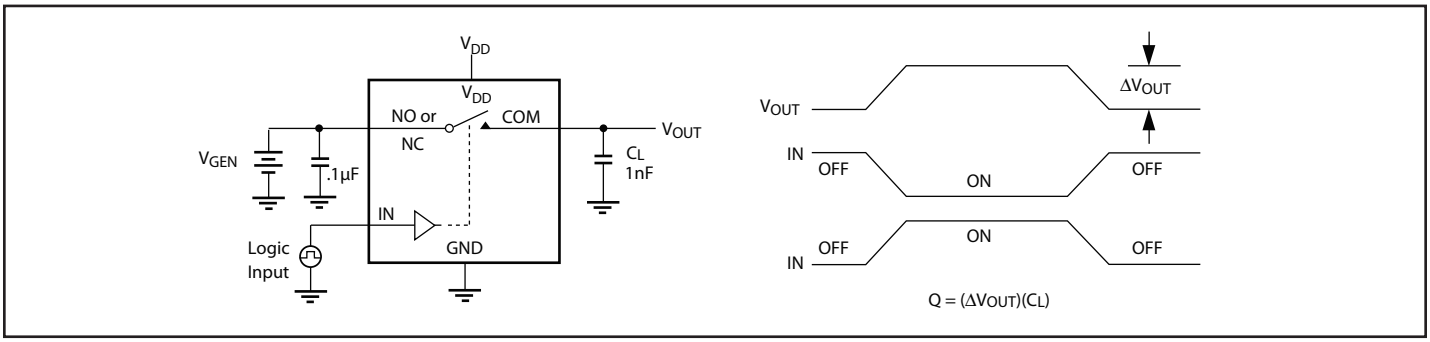


Figure 2. Charge Injection

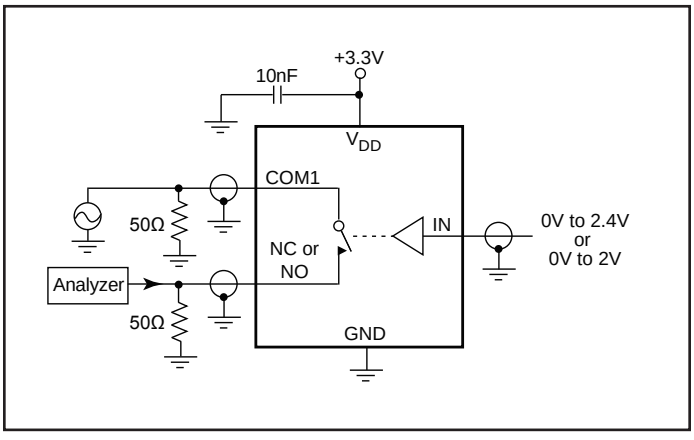


Figure 3. Off Isolation

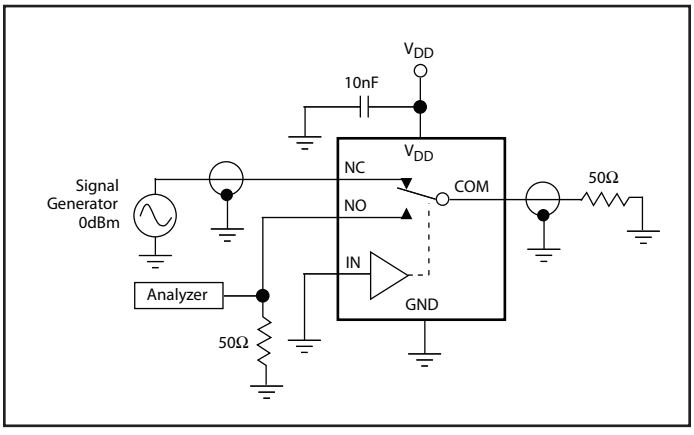


Figure 4. Crosstalk

Test Circuits/Timing Diagrams (continued)

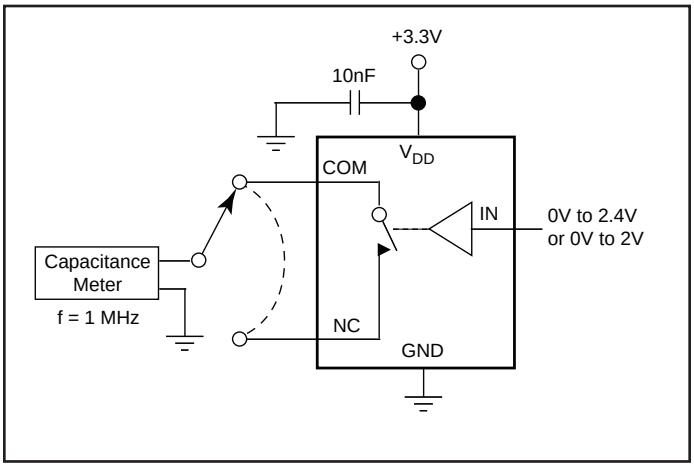


Figure 5. Channel-Off Capacitance

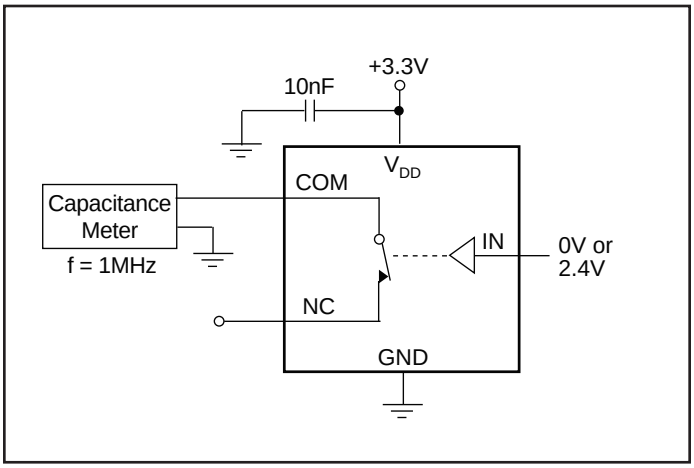


Figure 6. Channel-On Capacitance

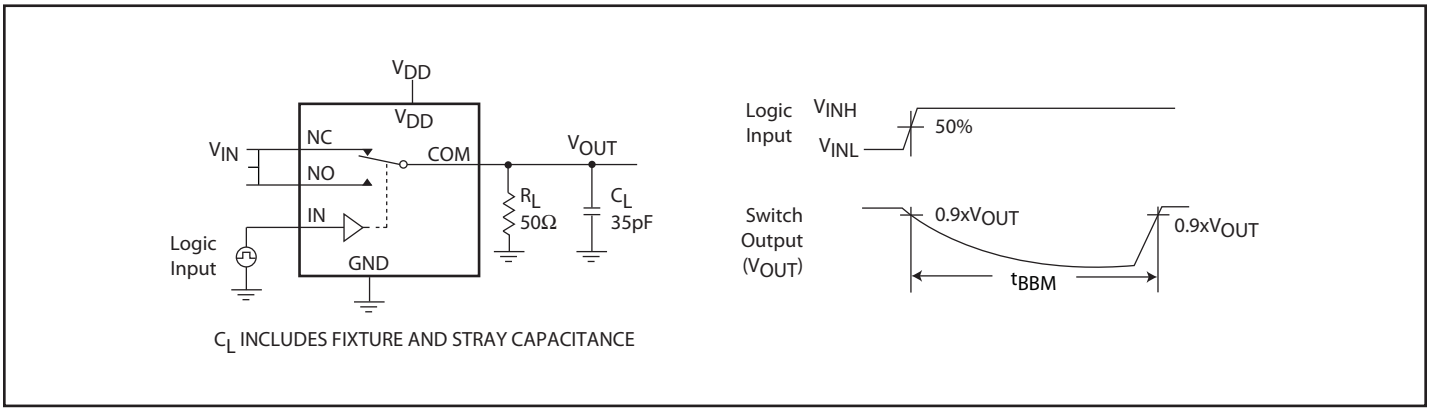
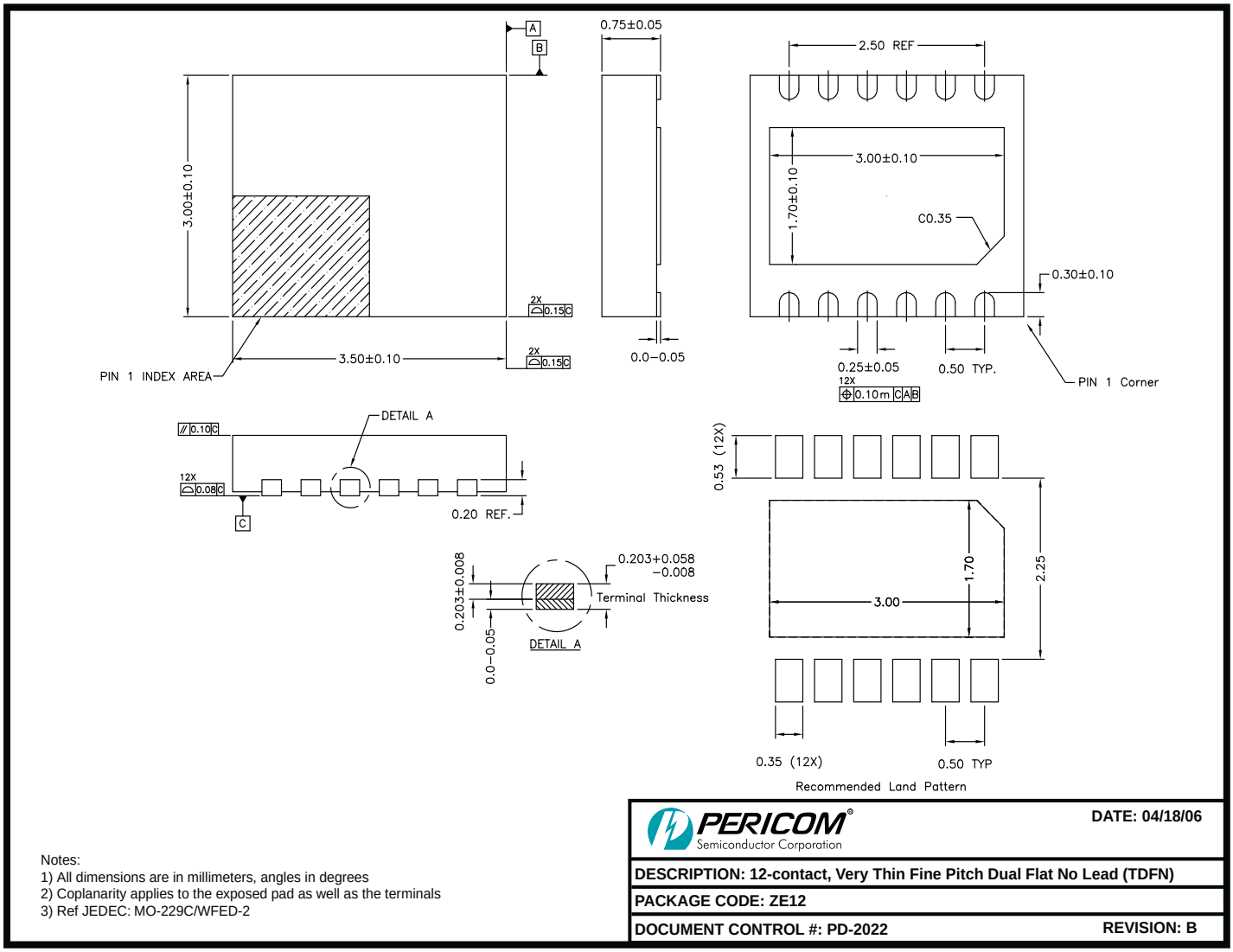


Figure 8. Break Before Make Diagram

Packaging Mechanical: 12-Contact TDFN (ZE)



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Note:

- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3A3160ZEEX	ZE	Pb-free & Green, 12-contact TDFN	YI

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape/Reel
3. Number of transistors = TBD