

Features

- CMOS Technology for Bus and Analog Applications
- Low ON-Resistance: 0.4Ω (+2.7V Supply)
- Wide V_{DD} Range: +1.5V to +3.6V
- Low Power Consumption : 5μW
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 20ns max. at 3.3V
- High Off Isolation: -27dB at 100 kHz
- -41dB (100kHz) Crosstalk Rejection Reduces Signal Distortion
- Extended Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green available):
 - 6-pin Small Compact SOT23 (T)

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals

Pin Description

Pin Number	Name	Description
1	NO	Data Port (Normally Open)
2	GND	Ground
3	NC	Data Port (Normally Closed)
4	COM	Common Output/Data Port
5	V _{DD}	Positive Power Supply
6	IN	Logic Control

Function Table

Logic Input	Function
0	NC Connected to COM
1	NO Connected to COM

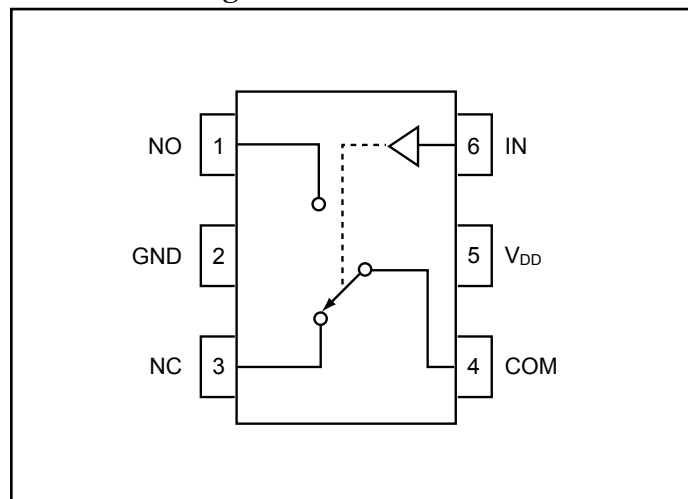
Description

The PI3A3159 is a, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, +1.5V to +3.6V, the PI3A3159 has an On-Resistance of 0.4Ω at 3.0V.

Control input, IN, tolerates input drive signals up to 3.3V, independent of supply voltage.

PI3A3159 is a lower voltage and On-Resistance replacement for the PI5A3159.

Connection Diagram



Absolute Maximum Ratings

Voltages Referenced to GND

V_{DD} -0.5V to +3.6V

V_{IN} , V_{COM} , V_{NC} , V_{NO} (Note 1) -0.5V to $V_{DD} + 0.3V$
or 30mA, whichever occurs first

Current (any terminal)..... ±200mA

Peak Current, COM, NO, NC

(Pulsed at 1ms, 10% duty cycle)..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT23-6 (derate 7.1mW/°C above +70°C)..... 0.5W

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note:

1. Signals on NC, NO, COM, or IN exceeding V_{DD} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +3.3V Supply

($V_{DD} = +3.3V \pm 10\%$, $GND = 0V$, $V_{IH} = 1.4V$, $V_{IL} = 0.5V$)

Parameter	Symbol	Conditions	Package	Temp. (°C)	Min. (1)	Typ. (2)	Max. (1)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	0		V_{DD}	V
On Resistance	R_{ON}	$V_{DD} = 2.7V$, $I_{COM} = 100mA$, V_{NO} or $V_{NC} = +1.5V$	SOT23	25			0.4	Ω
			TDFN	Full			0.5	
On-Resistance Match Between Channels(4)	ΔR_{ON}		25			0.08		
			Full			0.09		
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	$V_{DD} = 2.7V$, $I_{COM} = 100mA$, V_{NO} or $V_{NC} = 0.8V, 2.0V$	25			0.1		
			Full			0.1		
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$		25		-1	1	nA	
			Full		-10	10		
COM On Leakage Current(6)	$I_{COM(ON)}$	25		-2	2			
		Full		-20	20			

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON} \text{ max.} - R_{ON} \text{ min.}$
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.

Electrical Specifications - Single +3.3V Supply (continued)

(V_{DD} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input							
Input High Voltage	V _{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V _{IL}	Guaranteed Logic LowLevel				0.5	
Input Current with Voltage High	I _{INH}	V _{IN} = 1.4V, all others = 0.5V		-1		1	μA
Input Current with Voltage Low	I _{INL}	V _{IN} = 0.5V, all others = 1.4V		-1		1	
Dynamic							
Turn-On-Time	t _{ON}	V _{DD} = 3.3V, V _{NO} or V _{NC} = 2.0V, Figure 1	25			20	ns
			Full			20	
Turn-Off-Time	t _{OFF}		25			10	
			Full			15	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 2	25		40		pC
Off Isolation ⁽⁴⁾	O _{IRR}	R _L = 50Ω, f = 100 KHz, Figure 3			-27		dB
CrossTalk ⁽⁵⁾	X _{TALK}	R _L = 50Ω f = 100 KHz, Figure 4			-41		
NC or NO Capacitance	C _{NC/NO (OFF)}	f = 1MHz, Figure 5			90		pF
COM Off Capacitance	C _{COM(OFF)}				90		
COM On Capacitance	C _{COM(ON)}		f = 1MHz, Figure 6			240	
Supply							
Power-Supply Range	V _{DD}		Full	1.5		3.6	V
Positive Supply Current	I _{CC}	V _{DD} = 3.6V, V _{IN} = 0V or V _{DD}					100

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. Off Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 3.
5. Between any two switches. See Figure 4.

Electrical Specifications - Single +2.5V Supply ($V_{DD} = +2.5V \pm 10\%$, $GND = 0V$, $V_{IH} = 1.4V$, $V_{IL} = 0.5V$)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V_{ANALOG}			0		V_{DD}	V
On-Resistance	R_{ON}	$V_{DD} = 2.5V$, $I_{COM} = -8mA$, V_{NO} or $V_{NC} = 1.8V$	25			0.5	Ω
			Full			0.55	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}	$V_{DD} = 2.5V$, $I_{COM} = -8mA$, V_{NO} or $V_{NC} = 0.8V, 1.8V$	25			0.09	
			Full			0.09	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$	$V_{DD} = 2.5V$, $I_{COM} = -8mA$, V_{NO} or $V_{NC} = 0.8V, 1.8V$	25			0.02	
			Full			0.02	
Dynamic							
Turn-On-Time	t_{ON}	$V_{DD} = 2.5V$, V_{NO} or $V_{NC} = 1.8V$, Figure 1	25			30	ns
			Full			30	
Turn-Off-Time	t_{OFF}		25			15	
			Full			15	
Charge Injection ⁽³⁾	Q	$C_L = 1nF$, $V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, Figure 2	25		40		pC
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.5	
Input High Current	I_{INH}	$V_{IN} = 1.4V$, all others = 0.5V	Full	-1		1	μA
Input Low Current	I_{INL}	$V_{IN} = 0.5V$, all others = 1.4V	Full	-1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON} \text{ max.} - R_{ON} \text{ min.}$
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Electrical Specifications - Single +1.8V Supply
($V_{DD} = +1.8V \pm 10\%$, $GND = 0V$, $V_{IH} = 1.4V$, $V_{IL} = 0.5V$)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V_{ANALOG}			0		V_{DD}	V
On-Resistance	R_{ON}	$V_{DD} = 1.8V$, $I_{COM} = -4mA$, V_{NO} or $V_{NC} = 1.5V$	25			0.6	Ω
			Full			0.6	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}	$V_{DD} = 1.8V$, $I_{COM} = -4mA$, V_{NO} or $V_{NC} = 0.8V, 1.5V$	25			0.07	
			Full			0.09	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$	$V_{DD} = 1.8V$, $I_{COM} = -4mA$, V_{NO} or $V_{NC} = 0.8V, 1.5V$	25			0.8	
			Full			0.8	
Dynamic							
Turn-On-Time	t_{ON}	$V_{DD} = 1.8V$, V_{NO} or $V_{NC} = 1.5V$, Figure 1	25			50	ns
			Full			50	
Turn-Off-Time	t_{OFF}		25			25	
			Full			25	
Charge Injection ⁽³⁾	Q	$C_L = 1nF$, $V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, Figure 2	25		36		pC
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.5	
Input High Current	I_{INH}	$V_{IN} = 1.4V$, all others = 0.5V	Full	-1		1	μA
Input Low Current	I_{INL}	$V_{IN} = 0.5V$, all others = 1.4V	Full	-1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON} \text{ max.} - R_{ON} \text{ min.}$
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Test Circuits/Timing Diagrams

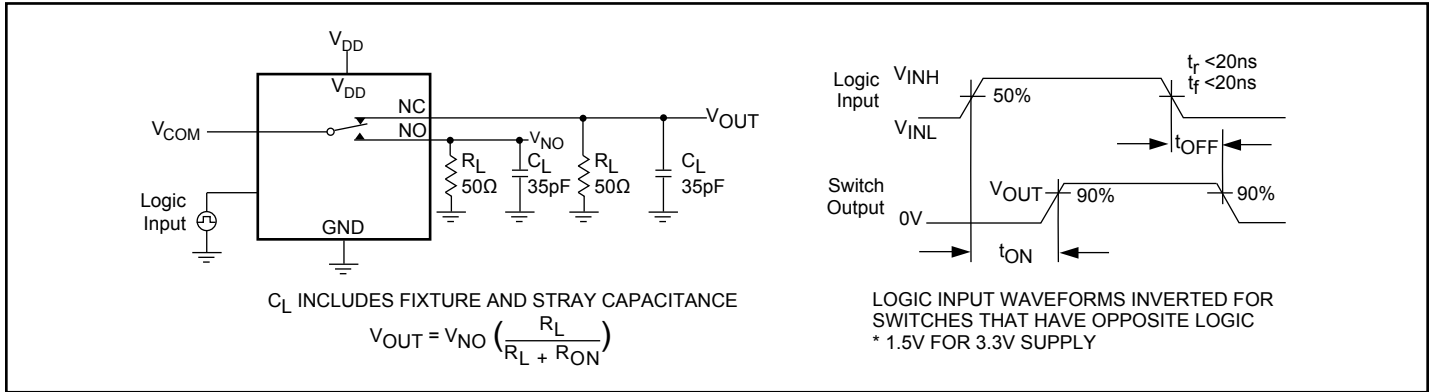


Figure 1. Switching Time

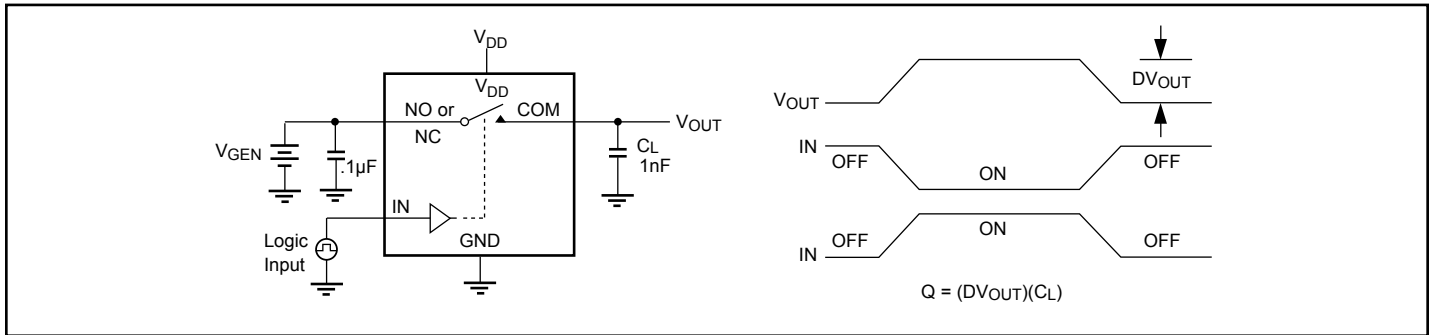


Figure 2. Charge Injection

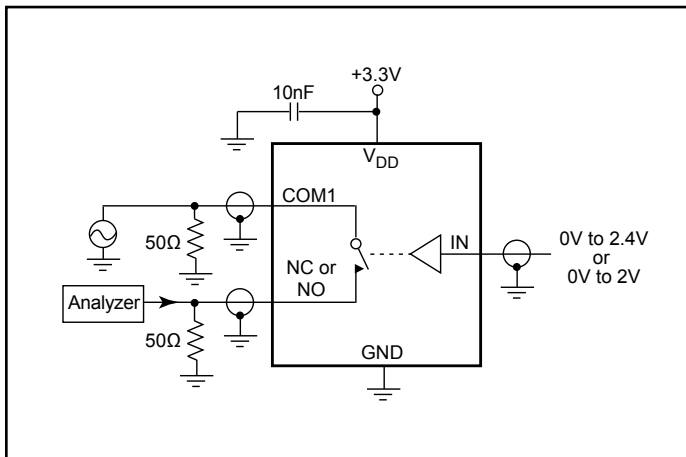


Figure 3. Off Isolation

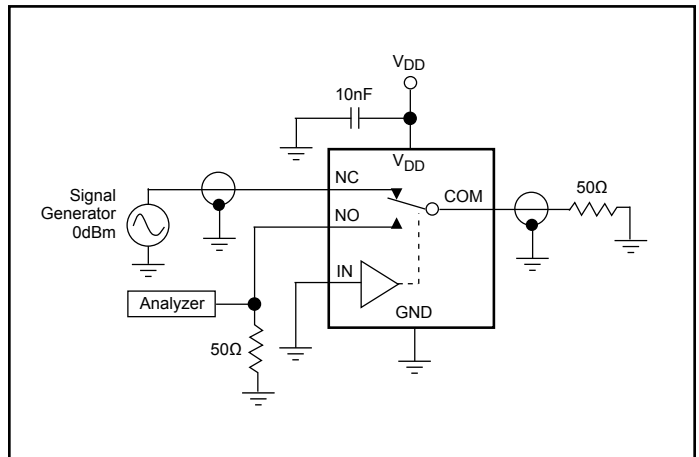


Figure 4. Crosstalk

Test Circuits/Timing Diagrams (continued)

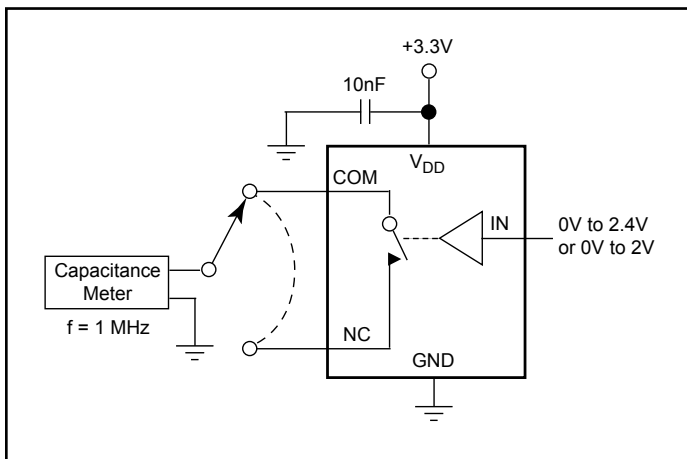


Figure 5. Channel-Off Capacitance

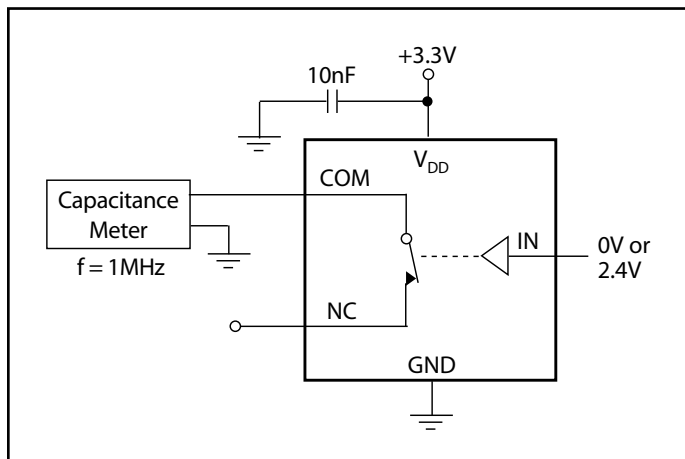
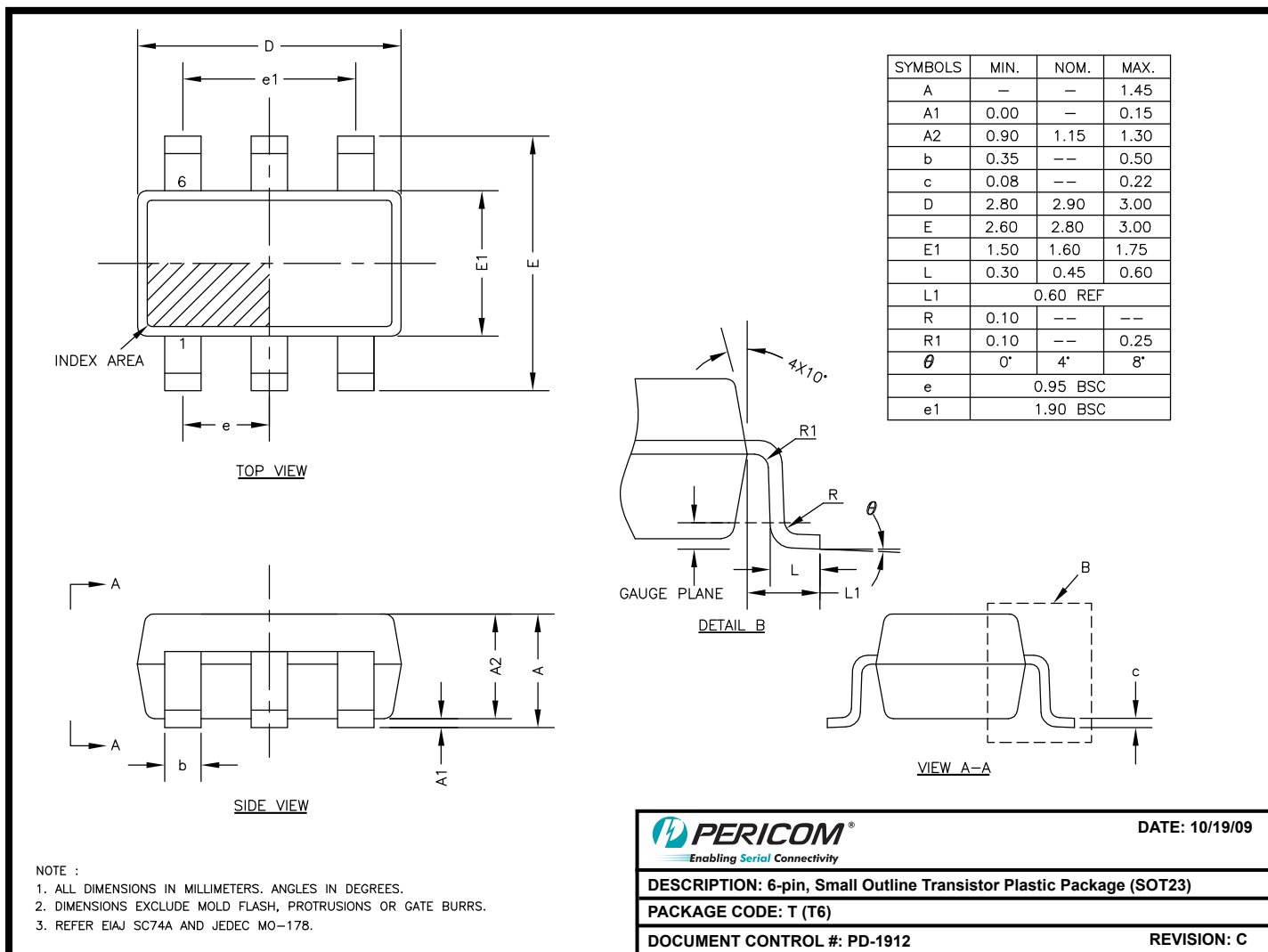


Figure 6. Channel-On Capacitance

Packaging Mechanical: 6-Pin SOT23 (T)



09-0131

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3A3159TEX	T	Pb-free & Green, 6-pin, SOT23	ZG

Notes:

Thermal characteristics can be found on the company web site at <http://www.pericom.com/packaging/>
 X = Tape/Reel