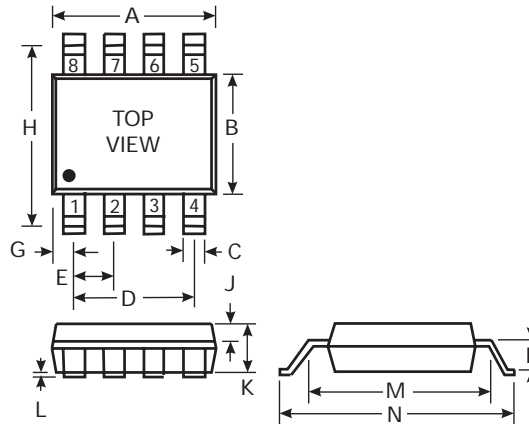
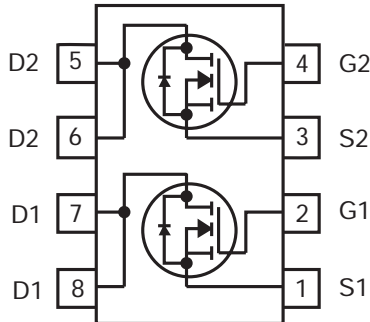


DUAL N-CANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- High Cell Density DMOS Technology
- Lower On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance



SO-8		
Dim	Min	Max
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

Mechanical Data

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	± 3.7 ± 15	A
Power Dissipation for:	P_d	Dual Operation (Note 1d)	2.0
		Single Operation (Note 1a)	1.6
		(Note 1b)	1.0
		(Note 1c)	0.9
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	$^\circ\text{C}$

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	78	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	40	$^\circ\text{C}/\text{W}$

- Notes:
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance ($R_{\theta JC} + R_{\theta CA}$) where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ in this instance is $40^\circ\text{C}/\text{W}$ but is dependent on the specific circuit board thermal design.
 - 1a. With 0.5 in^2 of 2 oz. copper mounting pad $R_{\theta JA} = 78^\circ\text{C}/\text{W}$.
 - 1b. With 0.02 in^2 of 2 oz. copper mounting pad $R_{\theta JA} = 125^\circ\text{C}/\text{W}$.
 - 1c. With 0.003 in^2 of 2 oz. copper mounting pad $R_{\theta JA} = 135^\circ\text{C}/\text{W}$.
 - 1d. With 1.0 in^2 of 2 oz. copper mounting pad, total power dissipation of up to 2W for dual operation can be achieved

Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _j = 55°C	I _{DSS}	—	—	2.0 25	μA	V _{DS} = 24V, V _{GS} = 0V
Gate-Body Leakage, Forward	I _{GSSF}	—	—	100	nA	V _{GS} = 20V, V _{DS} = 0V
Gate-Body Leakage, Reverse	I _{GSSR}	—	—	-100	nA	V _{GS} = -20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage T _j = 125°C	V _{GS(th)}	1.0 0.7	1.7 1.2	2.8 2.2	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance T _j = 125°C	R _{DS(ON)}	—	0.06 0.08 0.08 0.11	0.08 0.13 0.11 0.18	Ω	V _{GS} = 10V, I _D = 2.2A V _{GS} = 10V, I _D = 2.2A V _{GS} = 4.5V, I _D = 1.0A V _{GS} = 4.5V, I _D = 1.0A
On-State Drain Current	I _{D(ON)}	15 3.5	—	—	A	V _{GS} = 10V, V _{DS} = 10V V _{GS} = 4.5V, V _{DS} = 10V
Forward Transconductance	g _{FS}	—	6.0	—	∅	V _{DS} = 15V, I _D = 3.7A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	—	320	—	pF	V _{DS} = 10V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{OSS}	—	225	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	85	—	pF	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	t _{D(ON)}	—	10	20	ns	V _{DD} = 10V, I _D = 1.0A V _{GEN} = 10V, R _{GEN} = 6.0Ω
Turn-On Rise Time	t _r	—	13	20	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	21	50	ns	
Turn-Off Fall Time	t _f	—	5.0	50	ns	
Total Gate Charge	Q _g	—	9.5	27	nC	V _{DS} = 10V, I _D = 3.7A. V _{GS} = 10V
Gate-Source Charge	Q _{gs}	—	1.5	—	nC	
Gate-Drain Charge	Q _{gd}	—	3.3	—	nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Max Continuous Drain-Source Diode Forward Current	I _S	—	—	1.2	A	
Drain-Source Diode Forward Voltage	V _{SD}	—	0.8	1.3	V	V _{GS} = 0V, I _S = 1.25A (Note 2)
Reverse Recovery Time	t _{rr}	—	—	100	ns	V _{GS} = 0V, I _F = 1.25A, dI _F /dt = 100A/μs

Note: 2. Pulse Test: Pulse width ≤ 300 μs duty cycle ≤ 2%.

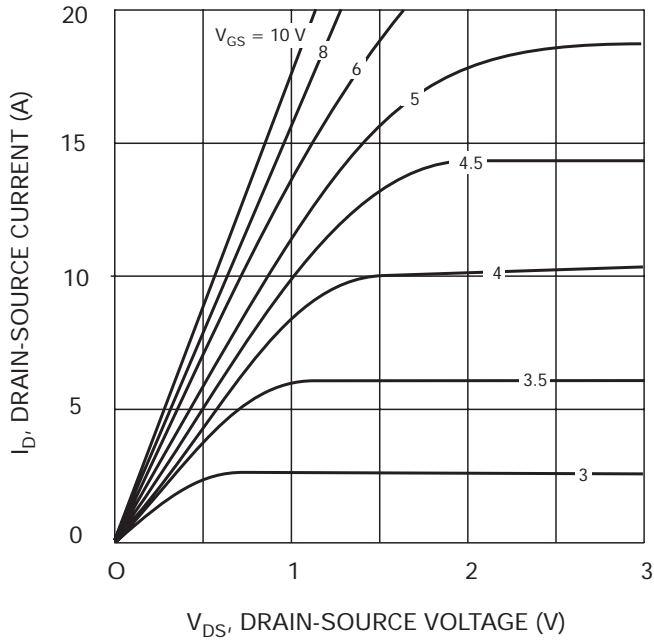


Fig. 1, On-Region Characteristics

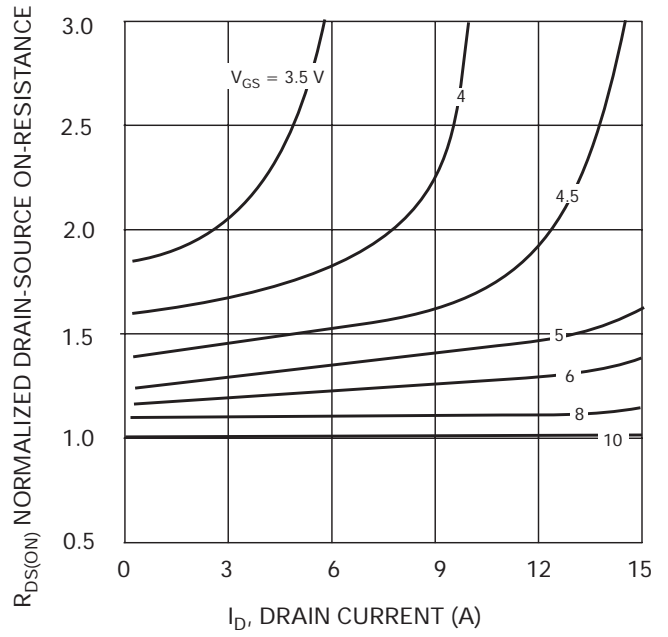


Fig. 2, On-Resistance vs Gate Voltage and Drain Current

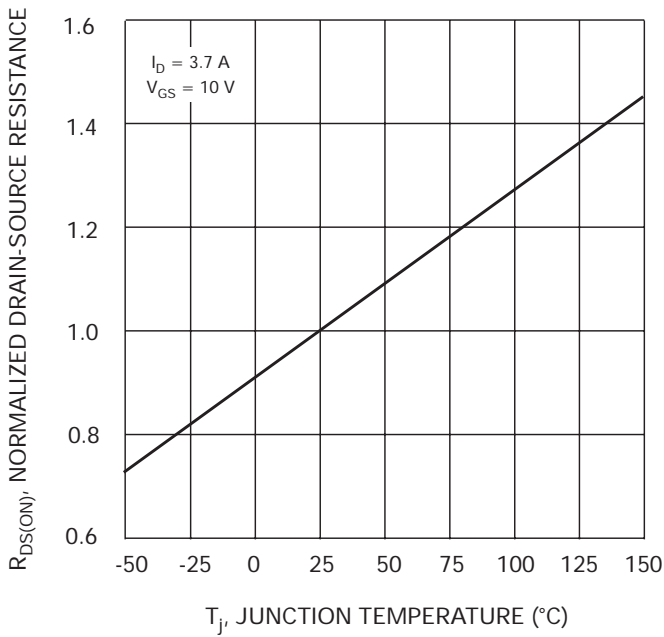


Fig. 3, On-Resistance vs Temperature

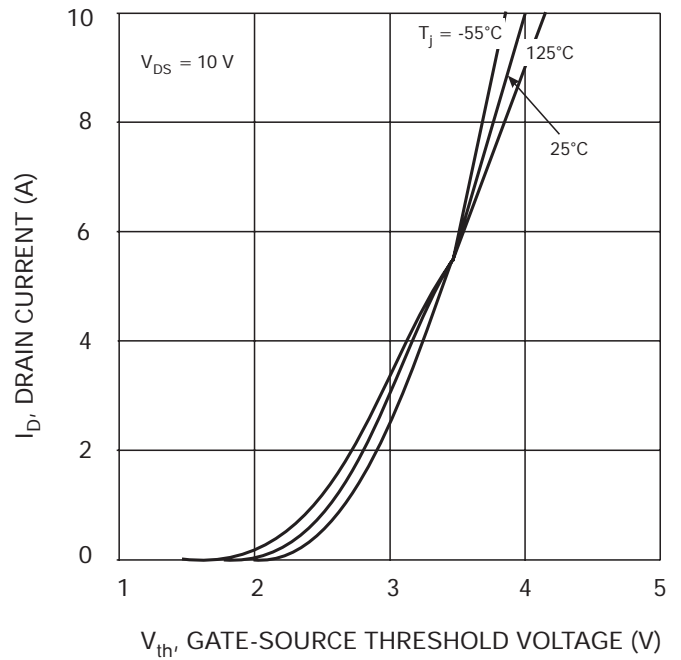


Fig. 4, Transfer Characteristics

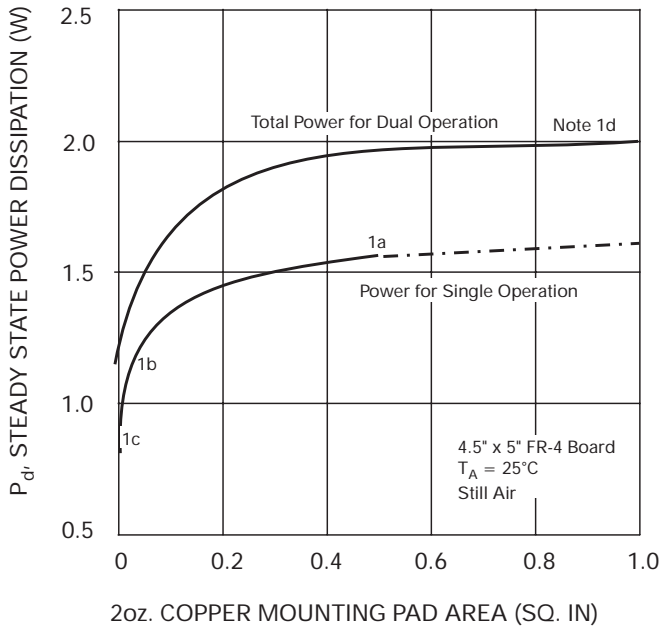


Fig. 5, Steady State Pwr Dissipation vs Copper Mtg Pad Area

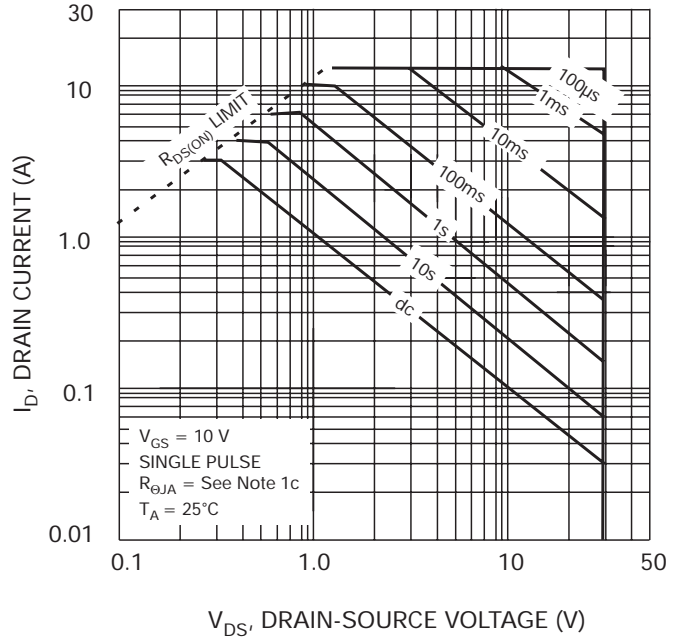


Fig. 6, Maximum Safe Operating Area

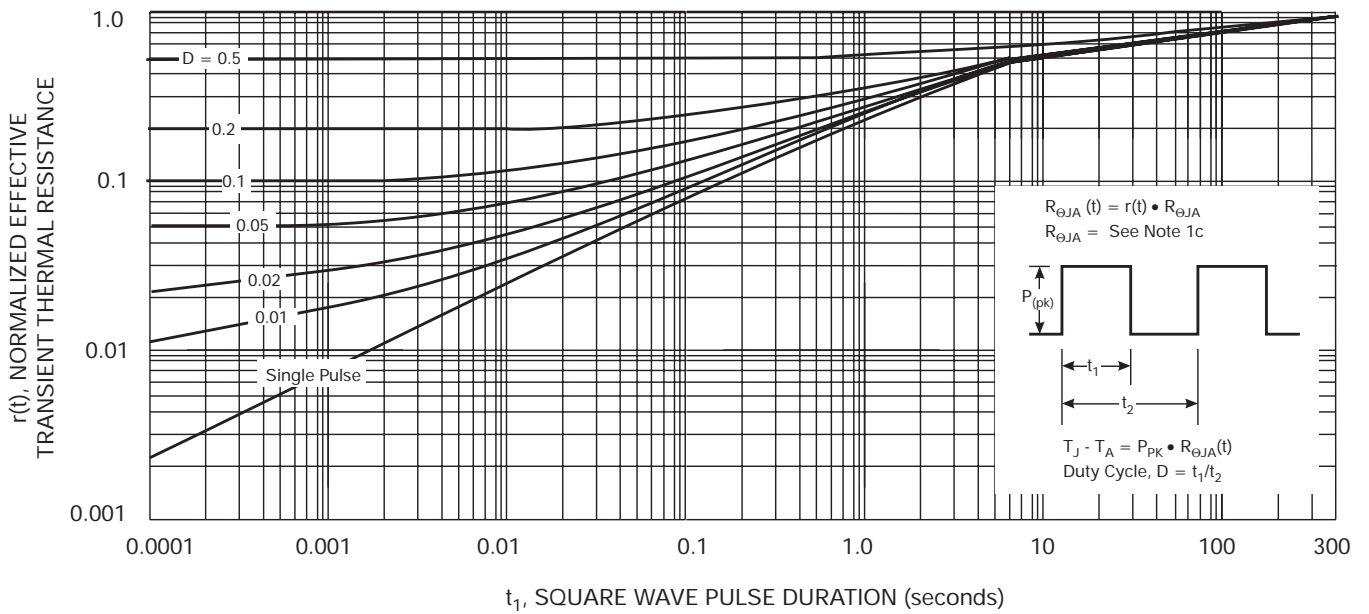


Fig. 7, Typical Normalized Transient Thermal Impedance Curves

Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower $R_{\theta JA}$ values and allow junction to reach thermal equilibrium sooner.