# AP7201

## DUAL 150mA LOW DROPOUT LINEAR REGULATOR

## Features

- Wide input voltage range: 1.9V – 5.5V
- Low dropout voltage: 100mV at 100mA output current
- Very low quiescent current (Iq): 25uA typical
- Fixed output voltage: 1.0V to 3.3V
- Up to 150mA per output channel
- Very fast transient response
- High PSRR: 78dB at 1kHz
- Accurate voltage regulation
- 300mA current limiting
- Thermal shutdown protection
- Ambient temperature range -40ºC to 85°C
- Package available: DFN2018-6 (USP-6B)
- DFN2018-6 (USP-6B): Available in “Green” Molding Compound (No Br, Sb)
- Lead Free Finish / RoHS Compliant (Note 1)

## General Description

The AP7201 is a dual low-dropout (LDO) CMOS linear regulator. The device operates from 1.9V to 5.5V input and delivers up to 150mA per output channel.

The AP7201 includes a pass element, voltage reference, error amplifier, current limit and built-in phase compensation. Key features include individual logic-compatible enable/shutdown control inputs, fold-back current limit and thermal shutdown protections.

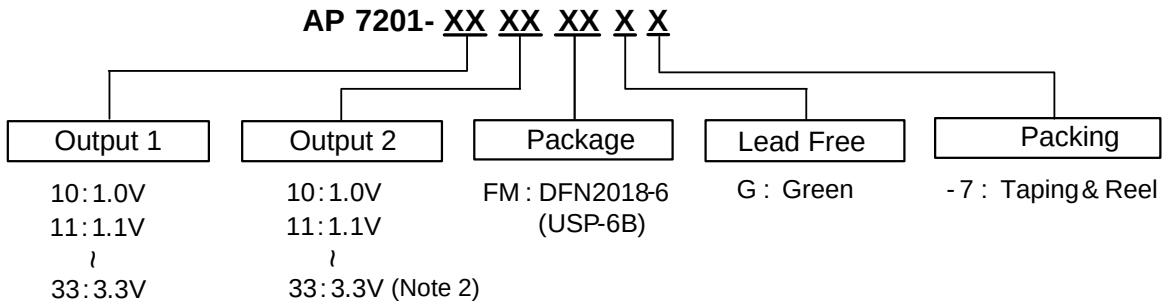
The AP7201 is fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. The fixed output voltage for each channel is set independently. Voltages are 100mV per step within a range of 1.0V to 3.3V.

The EN function allows the output of each channel to be turned off independently, resulting in greatly reduced power consumption. The AP7201 is available in the DFN2018-6 (USP-6B) package.

## Applications

- Cell Phones
- Smart Phones and PDA
- MP3/MP4
- PMP
- Bluetooth Headsets
- Digital Still Cameras
- GPS

## Ordering Information




| Device | Pb-Free or Green | Package Code | Packaging (Note 3) | 7” Tape and Reel | |
|---|---|---|---|---|---|
| | | | | Quantity | Part Number Suffix |
| AP7201-1818FMG-7 | Pb | FM | DFN2018-6 (USP-6B) | 3000/Tape & Reel | -7 |
| AP7201-1828FMG-7 | Pb | FM | DFN2018-6 (USP-6B) | 3000/Tape & Reel | -7 |
| AP7201-2828FMG-7 | Pb | FM | DFN2018-6 (USP-6B) | 3000/Tape & Reel | -7 |

Notes:
1. RoHS revision 13.2.2003. Glass and high temperature solder exemptions applied, see *EU Directive Annex Notes 5 and 7.*
2. Diodes, Inc. offers custom laser trimming for additional Fixed output voltage combinations from 1.0V to 3.3V. For output voltage availability, please contact your local Diodes, Inc. sales representative.
3. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.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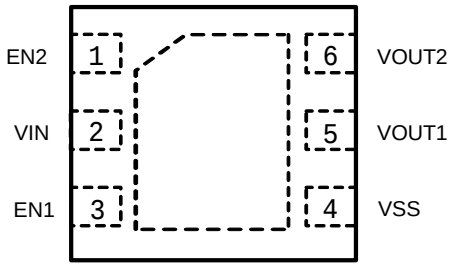
## Pin Assignments

( Top View )

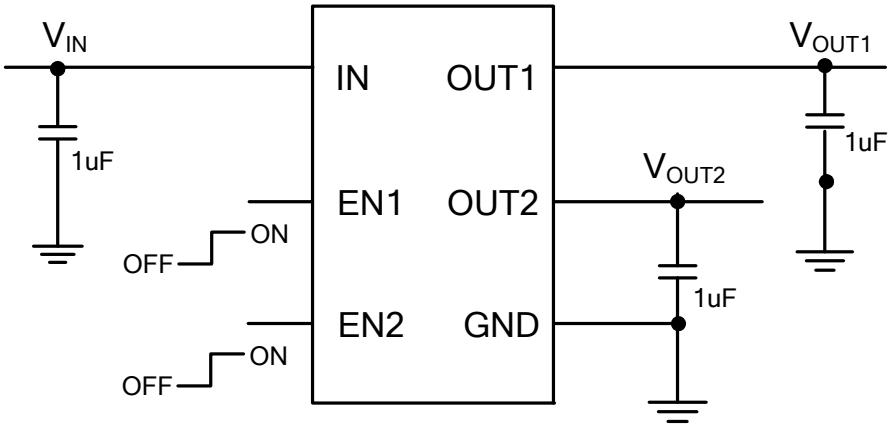



DFN2018-6 (USP-6B)

## Pin Descriptions

| Pin Name | Pin Number | Function |
|---|---|---|
| EN2 | 1 | Enable input 2 (Active High) |
| VIN | 2 | Voltage input pin.<br>Bypass to ground through at least 0.22µF ceramic capacitor. |
| EN1 | 3 | Enable input 1 (Active High) |
| GND (VSS) | 4 | Ground |
| OUT1 | 5 | Voltage output 1.<br>Bypass to ground through at least 0.22µF ceramic capacitor. |
| OUT2 | 6 | Voltage output 2.<br>Bypass to ground through at least 0.22µF ceramic capacitor. |

## Typical Application Circuits





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## Absolute Maximum Ratings

| Symbol | Description | | Rating | Unit |
|---|---|---|---|---|
| ESD HBM | Human Body Model ESD Protection | | 4 | KV |
| ESD MM | Machine Model ESD Protection | | 250 | V |
| $Ven1_{MAX}$ | Enable 1 Voltage | | $V_{IN}$ + 0.3 | V |
| $Ven2_{MAX}$ | Enable 2 Voltage | | $V_{IN}$ + 0.3 | V |
| $Vout1_{MAX}$ | Output 1 Voltage | | $V_{IN}$ + 0.3 | V |
| $Vout2_{MAX}$ | Output 2 Voltage | | $V_{IN}$ + 0.3 | V |
| $Vin_{MAX}$ | Input Voltage | | 6.5 | V |
| $I_{OUT\ MAX}$ | Continuous Load Current per Channel | | 150 | mA |
| $T_{LEAD}$ | Lead Temperature | | 260 | °C |
| $T_{ST}$ | Storage Temperature | | -65 to 150 | °C |
| $T_J$ | Maximum Junction Temperature | | 150 | °C |
| $P_{D\ MAX}$ | Power Dissipation (Notes 4, 5, 6) | DFN2018-6 (USP-6B) | 1700 | mW |

Notes: 4. $T_J$, max =150°C.
5. Ratings apply to ambient temperature at 25°C.

## Recommended Operating Conditions

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | 1.9 | 5.5 | V |
| $I_{OUT}$ | Output Current per Channel | 0 | 150 | mA |
| $T_A$ | Operating Ambient Temperature | -40 | 85 | °C |


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## Electrical Characteristics

( $T_A$ = 25°C, $V_{IN}$ = $V_{EN}$, $C_{IN}$ = 1uF, $C_{OUT}$ = 1uF unless otherwise stated )

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operation Input Voltage Range | | 1.9 | | 5.5 | V |
| $I_Q$ | Input Quiescent Current | $I_{OUT}$= 0 | — | 25 | 45 | uA |
| $I_{Q(OFF)}$ | Input Shutdown Current | $V_{EN}$ = 0V | — | | 1 | uA |
| $I_{LK(OFF)}$ | Input Leakage Current | $V_{EN}$ = 0V, OUT grounded | — | | 1 | uA |
| $V_{Dropout}$ | Dropout Voltage | $V_{OUT}$ = 1.8V, $I_{OUT}$= 100mA | | 170 | 220 | mV |
| $V_{Dropout}$ | | $V_{OUT}$ = 3.3V, $I_{OUT}$= 100mA | | 100 | 150 | mV |
| $V_{OUT}$ | Output Voltage Accuracy | | -2 | | 2 | % |
| $\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$ | Line Regulation | $V_{IN}$ = $V_{OUT}$+0.2V ($V_{IN}$ > 1.9V) to 5.0V, $I_{OUT}$= 1mA | | 0.01 | 0.2 | %/V |
| $\Delta V_{OUT}$ | Load Regulation | $I_{OUT}$ from 1mA to 100mA | | 5 | 30 | mV |
| $t_{ST}$ | Start-up Time | $V_{EN}$ = 0V to 2.0V, $I_{OUT}$= 150mA | | 50 | | us |
| PSRR | PSRR | 1kHz, $I_{OUT}$= 30mA | | 78 | | dB |
| $I_{SHORT}$ | Short-circuit Current | $V_{IN}$ = 5.0V, $V_{OUT}$ < 0.2V | | 40 | | mA |
| $I_{LIMIT}$ | Current Limit | $V_{IN}$ = $V_{OUT}$ + 1.0V | | 300 | | mA |
| $V_{IL}$ | EN Input Logic Low Voltage | | | | 0.25 | V |
| $V_{IH}$ | EN Input Logic High Voltage | | 1.6 | | | V |
| $I_{EN}$ | EN Input Leakage | $V_{EN}$ = 0V or Vin | — | | 0.1 | uA |
| $T_{SHDN}$ | Thermal Shutdown Threshold | | | 145 | | °C |
| $T_{HYS}$ | Thermal Shutdown Hysteresis | | | 15 | | °C |
| $\theta_{JA}$ | Thermal Resistance Junction-to-Ambient (Note 6) | DFN2018-6 | | 70 | | °C/W |

Notes: 6. Test condition for DFN2018-6: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer 1.0”x1.4” ground plane.


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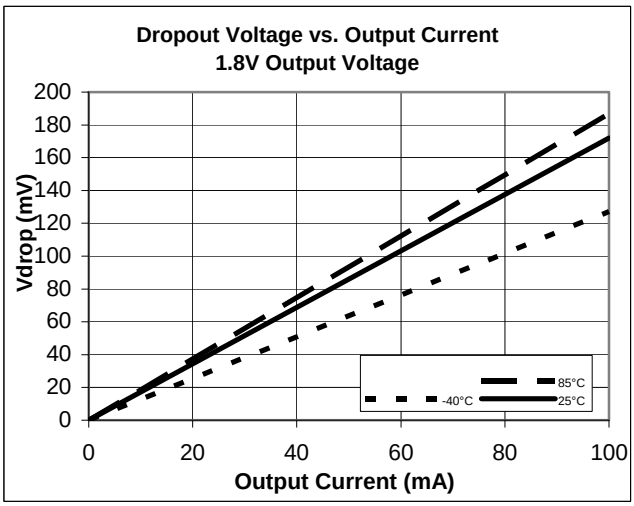
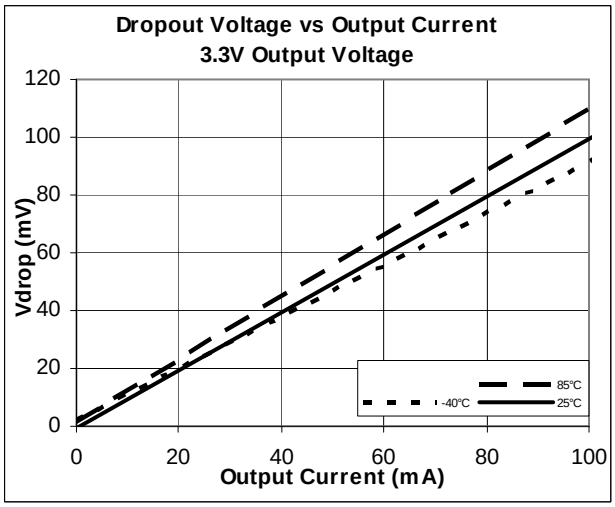
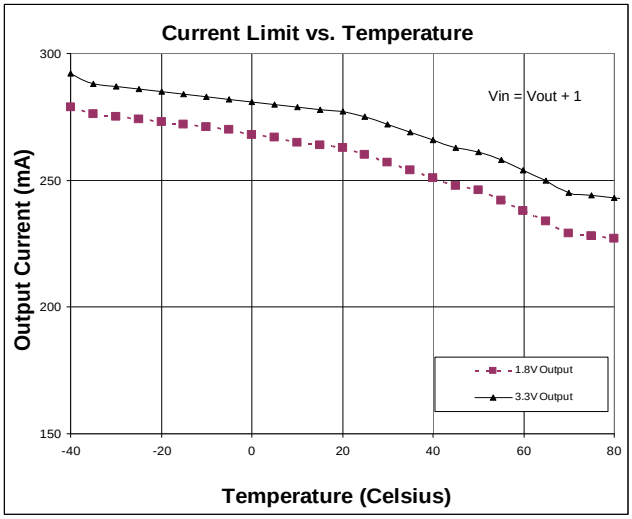
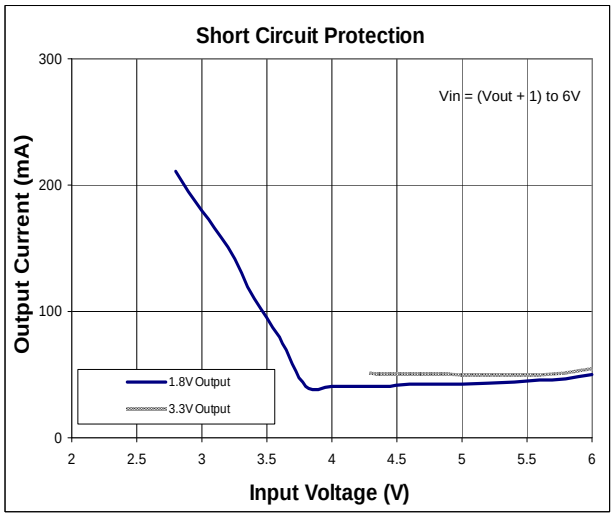
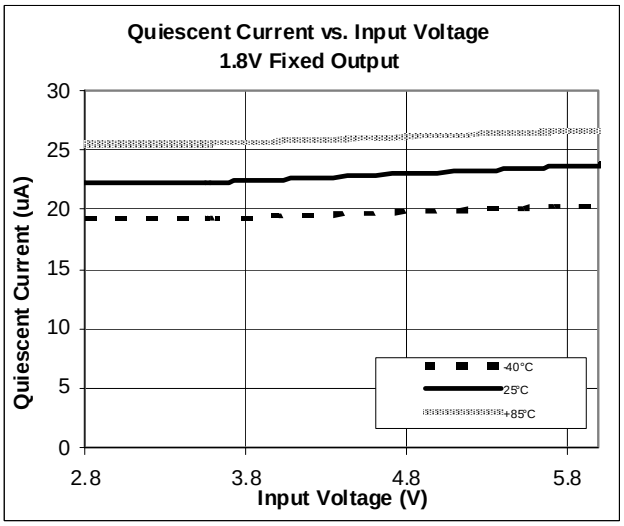
## Typical Performance Characteristics

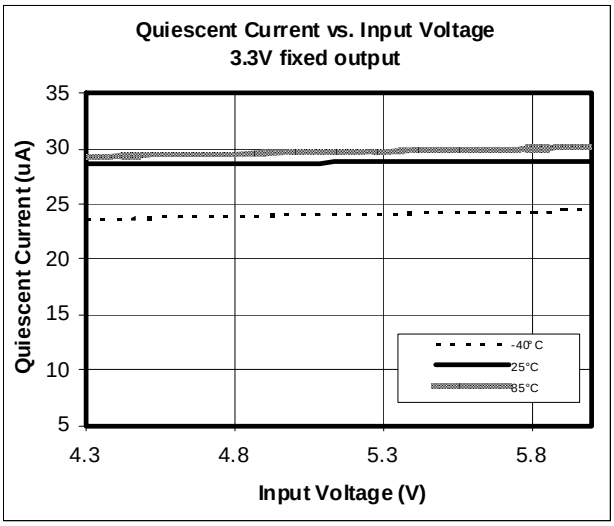




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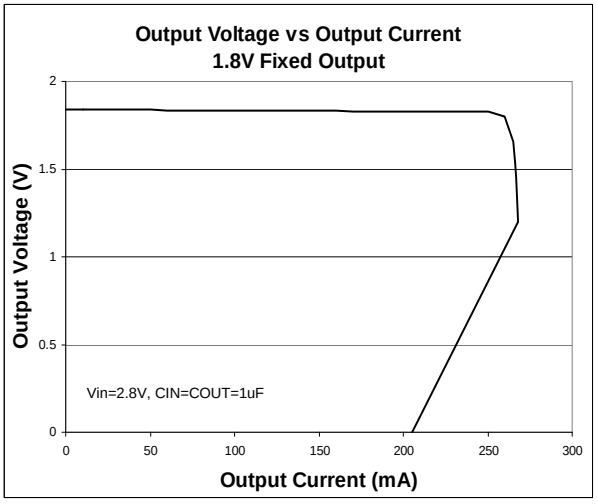
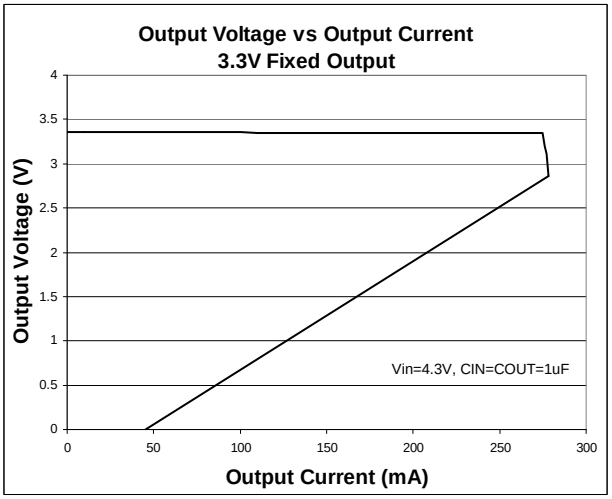
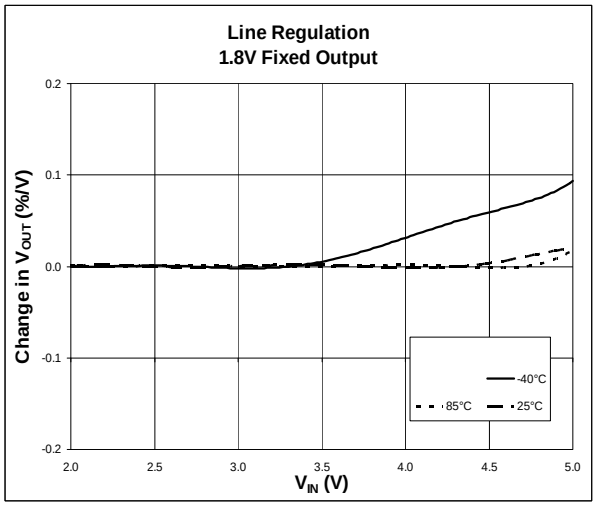
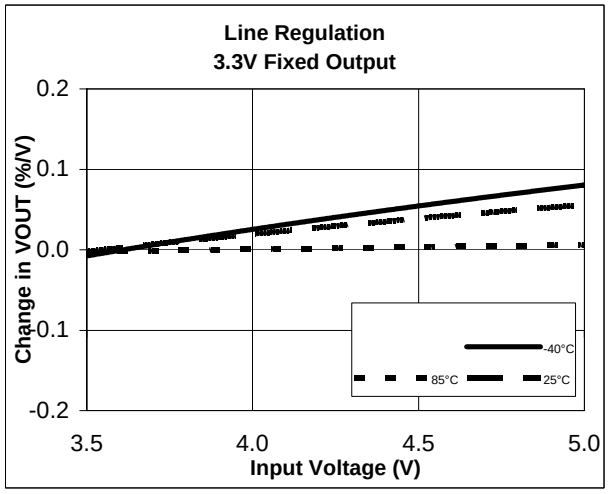
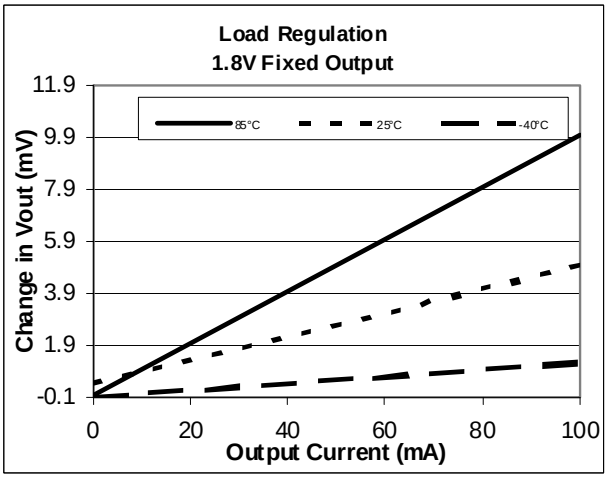
## Typical Performance Characteristics (Continued)

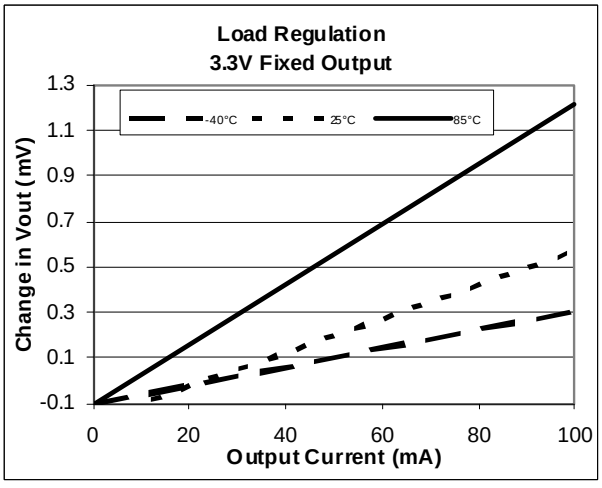




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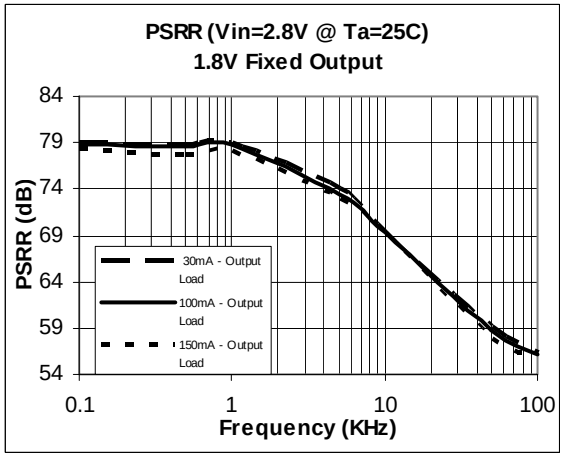
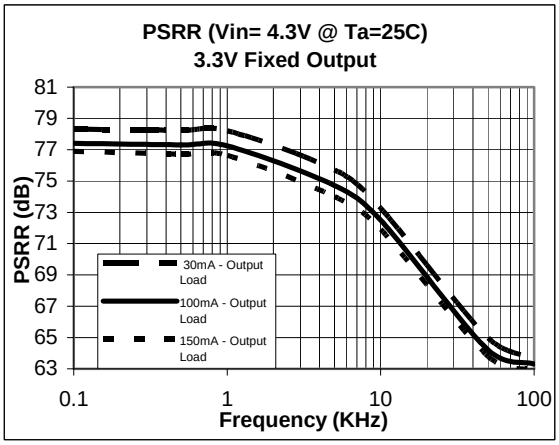
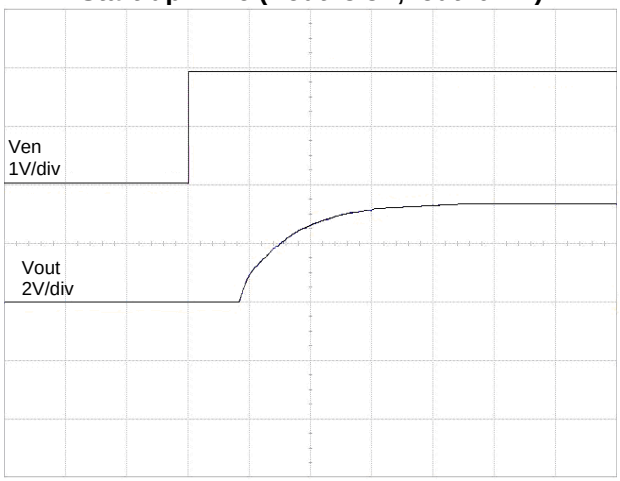


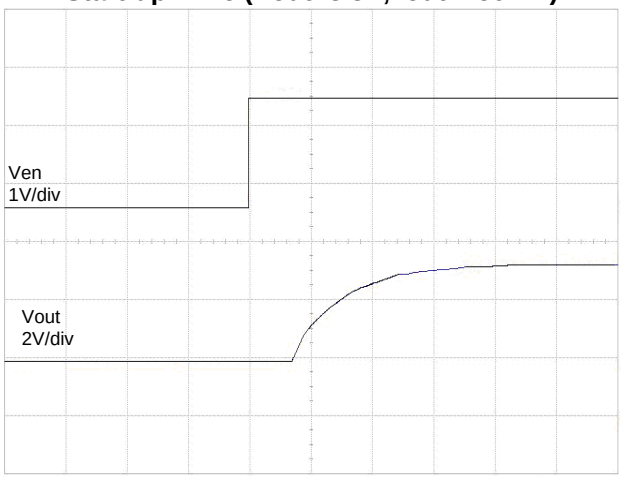




**Start-up Time (Vout=3.3V, Iout=0mA)**



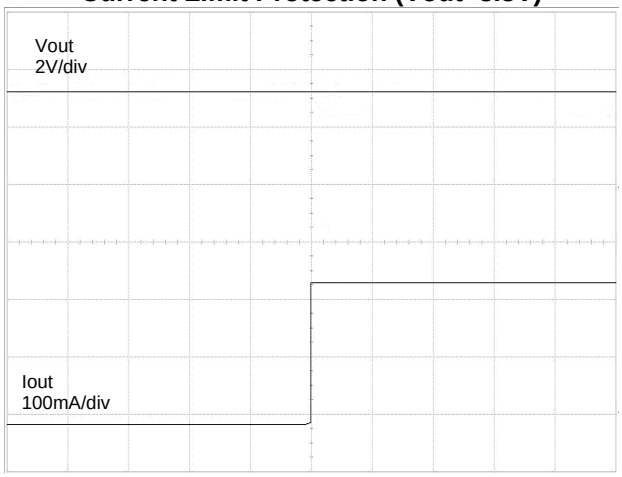

**Time (20us/div)**

**Start-up Time (Vout=3.3V, Iout=150mA)**



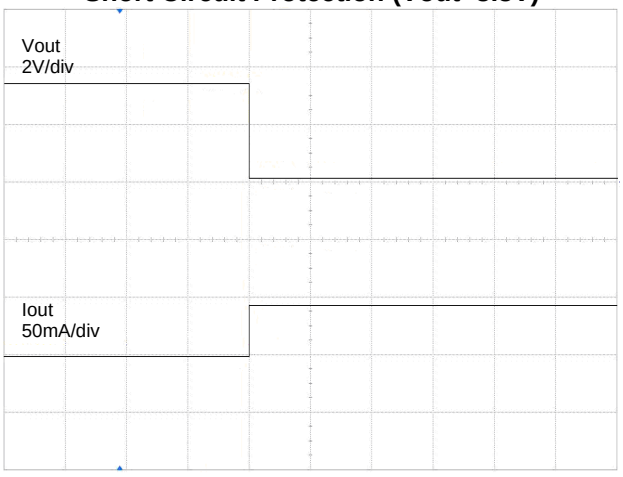

**Time (20us/div)**

**Current Limit Protection (Vout=3.3V)**




**Time (50us/div)**

**Short Circuit Protection (Vout=3.3V)**




**Time (1ms/div)**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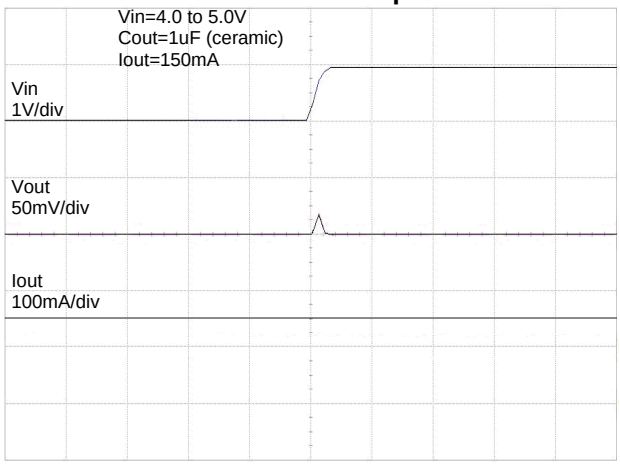
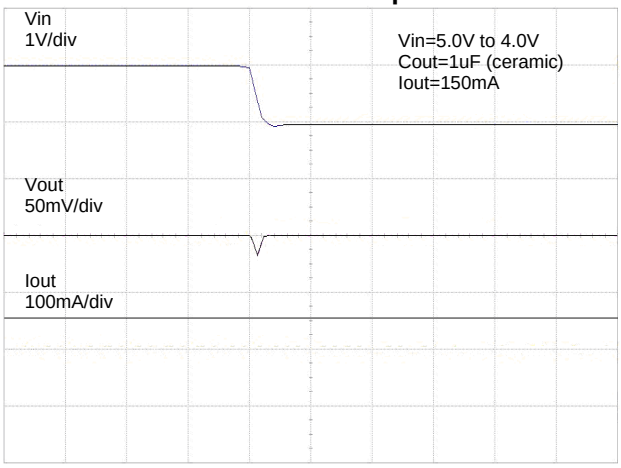
## Typical Performance Characteristics (Continued)

**Line Transient Response**



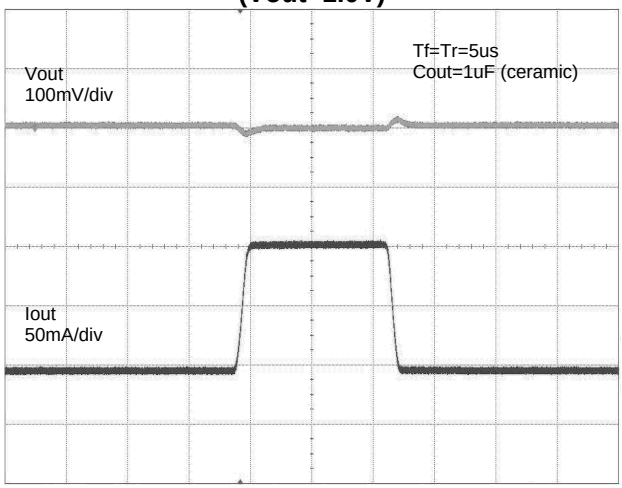

**Time (20us/div)**

**Line Transient Response**



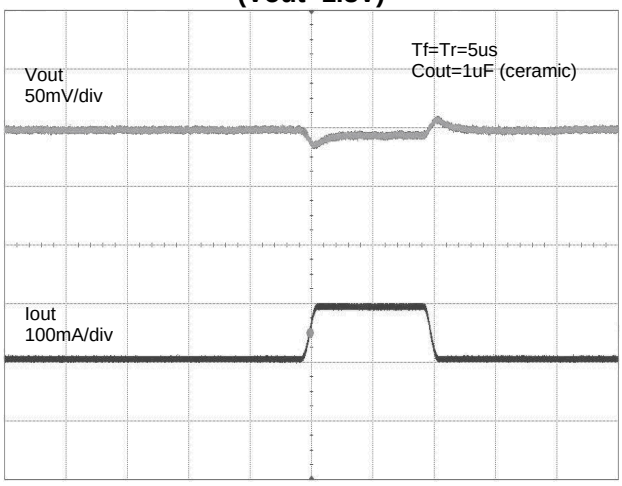

**Time (20us/div)**

**Output Load Transient Response (Vout=1.0V)**




**Time (40us/div)**

**Output Load Transient Response (Vout=1.8V)**




**Time (40us/div)**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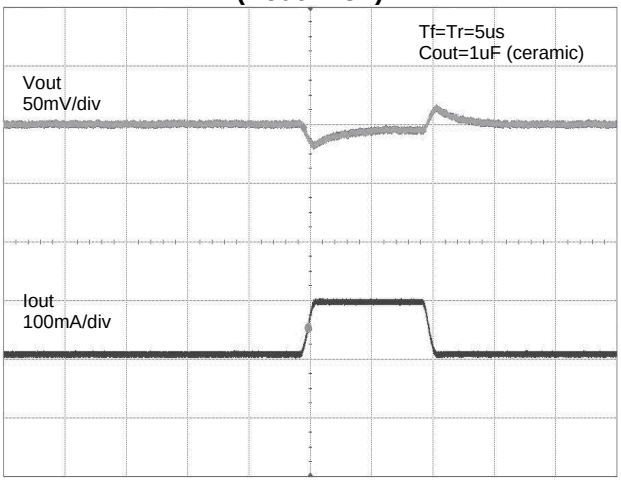
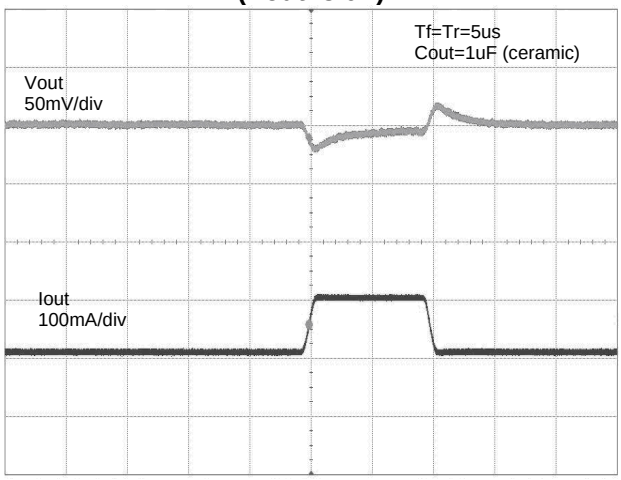
## Typical Performance Characteristics (Continued)

**Output Load Transient Response (Vout=2.8V)**



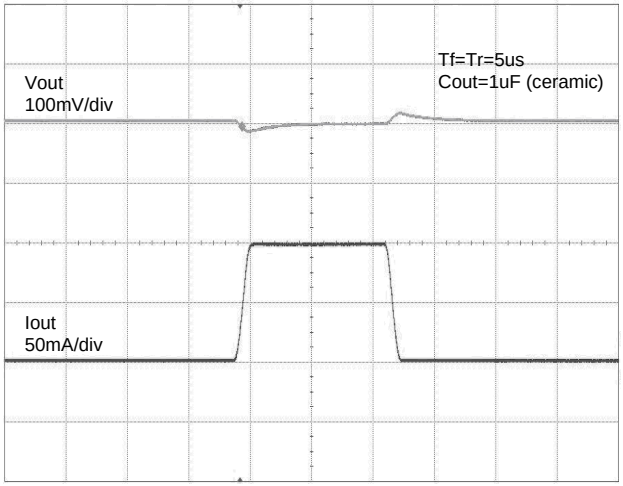

Time (40us/div)

**Output Load Transient Response (Vout=3.0V)**




Time (40us/div)

**Output Load Transient Response (Vout=3.3V)**




Time (40us/div)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## Application Note

**Input Capacitor**

AP7201 requires a minimum input capacitance of 0.22μF ceramic capacitor between VIN and GND pins to prevent any impedance interactions with the supply. This input capacitor should be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

**Output Capacitor**

AP7201 requires a minimum of 0.22μF capacitance on each output to stabilize the transient response of the LDO. The AP7201 is designed to have excellent transient response for most applications with a small amount of output capacitance. A ceramic capacitor is recommended on each channel to connect between OUT and GND pins. The device is also stable with multiple capacitors in parallel, which can be of any type of value. Larger capacitance helps to reduce undershoot and overshoot during transient and provides better stability and noise performance. This output capacitor should be placed as close as possible to OUT and GND pins for optimum performance.

**No Load Stability**

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

**ENABLE/SHUTDOWN Operation**

The AP7201 is turned on by setting the EN pin high by pulling to input voltage (VIN), and is turned off by pulling it low (GND). The EN function allows the output of each regulator to be turned off independently, resulting in greatly reduced power consumption. The EN pin should be tied to VIN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under $V_{IL}$ and $V_{IH}$.

**Current Limit Protection**

In the presence of a short or excessive load current condition, the AP7201 uses an internal short circuit fold-back mechanism that triggers the current limit protection and clamps the output current to approximately 300mA.

**Short Circuit Protection**

When OUT pin is short-circuited to GND or OUT pin voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 40mA typical. This feature protects the regulator from over-current and damage due to overheating.


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## Application Note (Continued)

**Wide Fixed Output Range**

The AP7201, with a wide fixed output range of 1V to 3.3V, provides a versatile solution for many portable and low power applications.

**Low Quiescent Current**

The AP7201, consuming only around 25µA for all input range, provides great power saving in portable and low power applications.

**Thermal Shutdown Protection**

Thermal protection disables both outputs when the junction temperature rises to approximately +145°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

**Power Dissipation**

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) x I_{OUT}$$

The AP7201 is available in the DFN2818-6 package with exposed pad, which is the primary conduction path for heat to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, to ensure the device will not overheat, it should be attached to an appropriate amount of copper PCB area.

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

$$P_D(max@T_A) = \frac{(+145°C - T_A)}{R_{\theta JA}}$$


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## Marking Information

**(1) DFN2018-6 (USP-6B)**

**( Top View )**

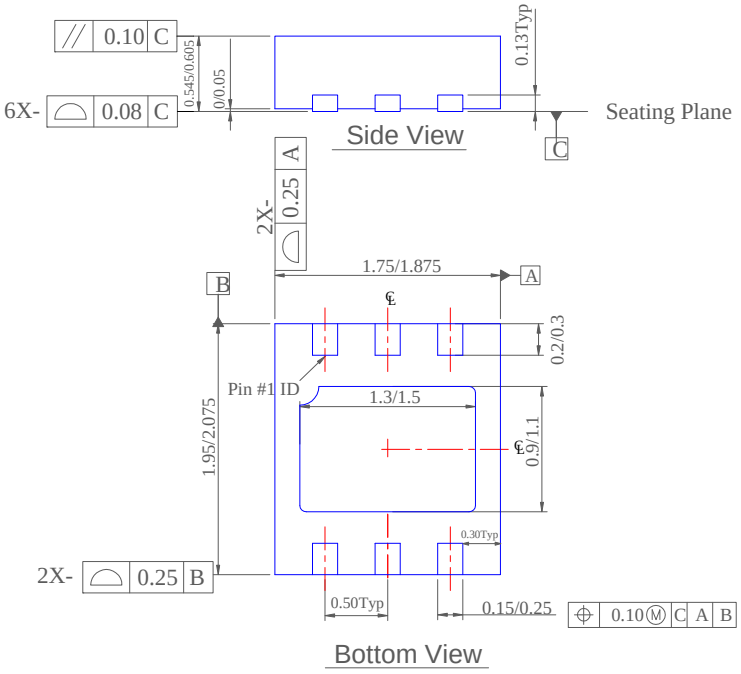

AA : Output 1
BB : Output 2
Y : Year "7" : 2007
"8" : 2008
WW : Month 01~52
X : G : Green

**Marking ID Code Table**

| Device | ID Code |
|---|---|
| AP7201-1818FM | 1818 |
| AP7201-1828FM | 1828 |
| AP7201-2828FM | 2828 |

## Package Information ( All Dimensions in mm )

**(1) DFN2018-6 (USP-6B)**





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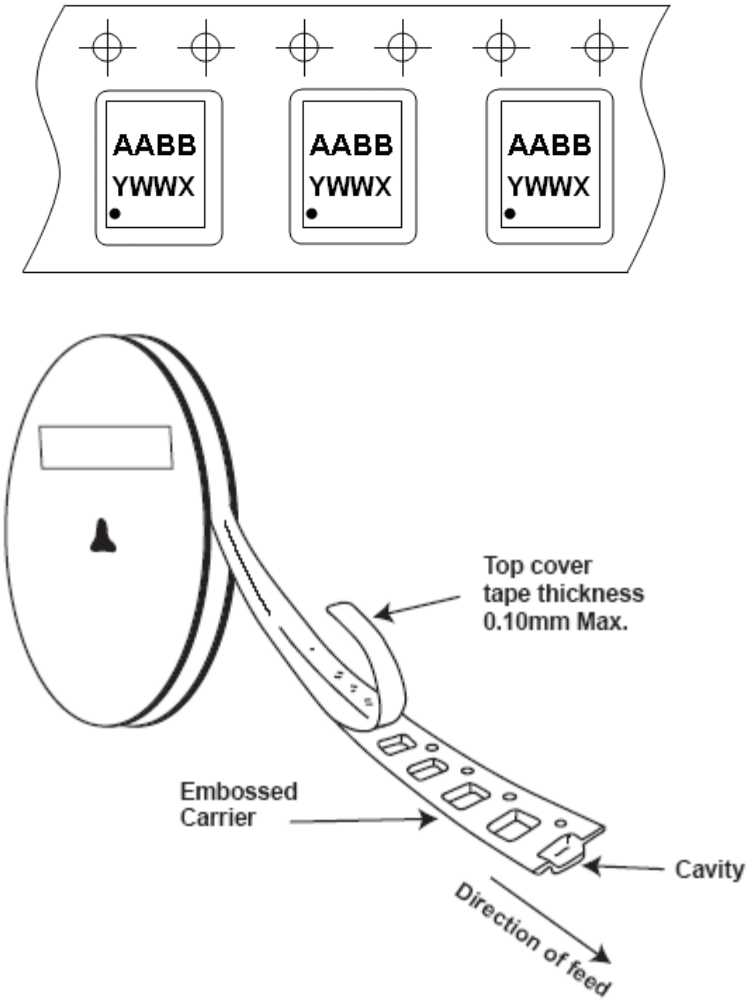
## Taping Orientation (Note 7)




Notes: 7. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf

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