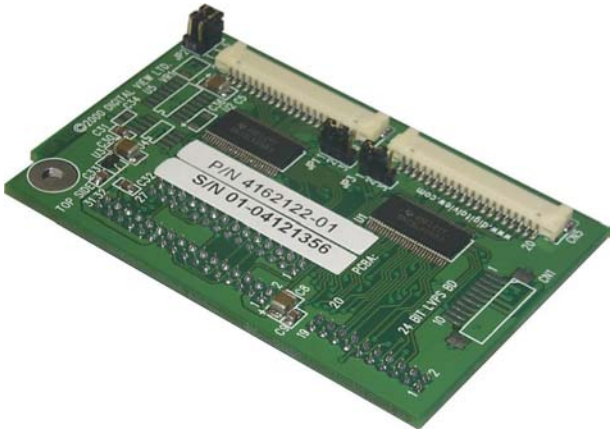
DIGITALVIEW®
visual communication specialists

LVDS Add On Board P/N 4162122-01

The LVDS add-on board P/N 4162122-01 design for dual pixel LVDS panels. It provides jumper setting to select the Data Enable (DE) signal on transmitter chips.



Jumper Settings :
JP1- Clock phase selection (Default 1-2 closed)
Change this setting to obtain best quality.

JP2 - Panel voltage selection
1-3, 2-4 closed : 12V panel
3-5, 4-6 closed : 3.3 / 5V panel (Default)

JP3 – Enable DE signal on signal or dual LVDS transmitter chip at even pixel side
1-2 closed : Enable DE signal on both LVDS transmitter chips (U1 & U2) (Default - Use for all panels)

2-3 closed : Enable DE signal on single LVDS transmitter chip (U1)
(Use for all panel except : Sharp LQ160E1LG08 and Sharp LQ181E1LW31)

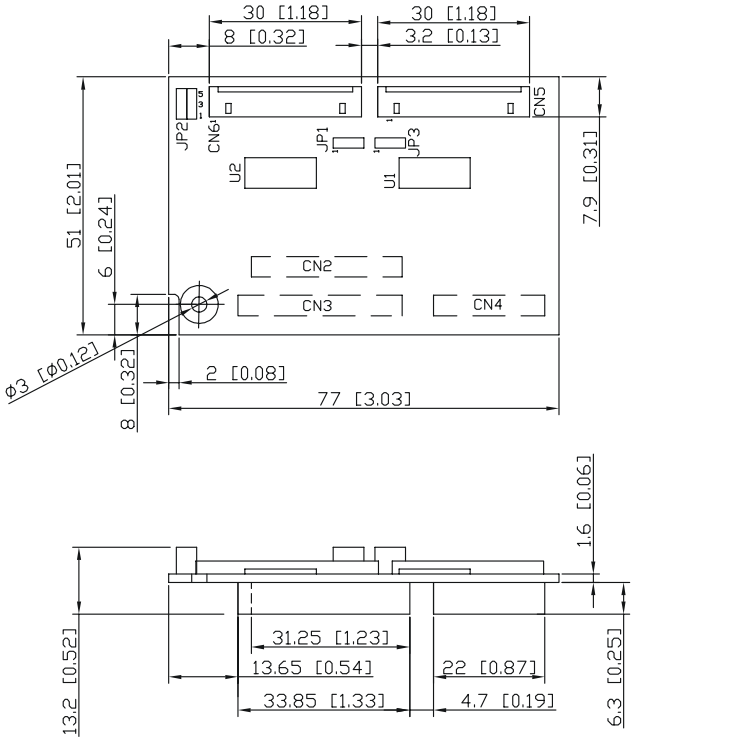
Compatible with LVDS board :

Old LVDS board	Jumper setting on LVDS board P/N 4162122-01
P/N 4162122-00	JP1 : 2-3 closed ; JP2 : 1-3,2-4 closed ; JP3 : 1-2 closed
P/N 4106886-64	JP1 : 2-3 closed ; JP2 : 3-5,4-6 closed ; JP3 : 2-3 closed
P/N 4162138-10	JP1 : 1-2 closed ; JP2 : 3-5,4-6 closed ; JP3 : 2-3 closed
P/N 4162140-10	JP1 : 1-2 closed ; JP2 : 3-5,4-6 closed ; JP3 : 1-2 closed (Connect with CN5 only)

Use of connectors :

Connector	Connector type
CN2	Hirose DF11-28DS-2DSA
CN3	Hirose DF11-32DS-2DSA
CN4	Hirose DF11-20DF-2DSA
CN5	Hirose DF14-20P-1.25P
CN6	Hirose DF14-20P-1.25P

Mechanical Drawing :



All dimensions are in MM [Inch]

Pin Assignments :

CN5 - Hirose DF14-20P-1.25P

PIN	SYMBOL	DESCRIPTION
1	VLCD	Panel power supply
2	VLCD	Panel power supply
3	GND	Ground
4	GND	Ground
5	/OUTO0	Negative differential LVDS data O0
6	OUTO0	Positive differential LVDS data O0
7	GND	Ground
8	/OUTO1	Negative differential LVDS data O1
9	OUTO1	Positive differential LVDS data O1
10	GND	Ground
11	/OUTO2	Negative differential LVDS data O2
12	OUTO2	Positive differential LVDS data O2
13	GND	Ground
14	/CLKOUTO	Negative LVDS clock O
15	CLKOUTO	Positive LVDS clock O
16	GND	GND
17	/OUTO3	Negative differential LVDS data O3
18	OUTO3	Positive differential LVDS data O3
19	GND	Ground
20	NC	No connection

CN6 - Hirose DF14-20P-1.25P

PIN	SYMBOL	DESCRIPTION
1	VLCD	Panel power supply
2	VLCD	Panel power supply
3	GND	Ground
4	GND	Ground
5	/OUTE0	Negative differential LVDS data E0
6	OUTE0	Positive differential LVDS data E0
7	GND	Ground
8	/OUTE1	Negative differential LVDS data E1
9	OUTE1	Positive differential LVDS data E1
10	GND	Ground
11	/OUTE2	Negative differential LVDS data E2
12	/OUTE2	Positive differential LVDS data E2
13	GND	Ground
14	/CLKOUTE	Negative LVDS clock E
15	CLKOUTE	Positive LVDS clock E
16	GND	Ground
17	/OUTE3	Negative differential LVDS data E3
18	OUTE3	Positive differential LVDS data E3
19	GND	Ground
20	NC	No connection