XAECK100 Automotive Evaluation Kit

Features

- **Quick and easy evaluation of Cypress's automotive imaging technology**
- **Up to 120 dB dynamic range**
- **Autobrite® intelligently adapts to lighting conditions perfect for extreme mixed lighting situations**
- **High sensitivity and near-infrared response**
- **Parallel and IEEE 1394 connections for high quality digital image capture**
- **Analog NTSC video**
- **Control settings through IEEE 1394 or I^2C**
- **8-and 12-bit image capture modes**
- **Multiple data formats**
- **Single frame, consecutive frame and AVI capture modes**
- **User-friendly Windows® software**
- **API for camera control and image capture through customer-built software**
- **Small and convenient form factor**
- **Monochrome, color, and stereo options available**

Functional Description

The XAECK100 is available in monochrome, color, and stereo versions

Monochrome XAECK10001

Figure 1 illustrates the contents of a monochrome XAECK10001 evaluation kit.

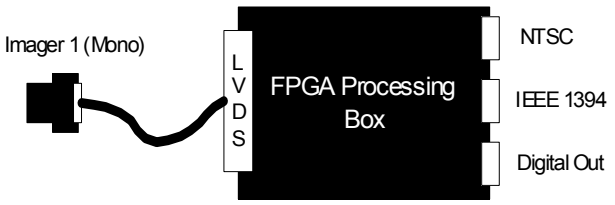

Figure 1. Monochrome System

Monochrome Processing Box Specifications

Processing Box	
Housing	
Processing Base	2 Million Gate Xilinx FPGA
Input Transport Medium	LVDS Serial I/F
Output Transport Medium	NTSC, IEEE 1394, Parallel Digital (Single Ended)
Serial Control	IEEE 1394, Digital Serial (I^2C)
Power Supply	6V (external source)

Monochrome Processing Block Diagram

Figure 2 illustrates the video processing and control algorithms implemented in the control box of the XAECK10001, monochrome camera kit.

The pipeline is broken up into three basic categories each of which is described in one of the following sections.

Input Control

The input control section of the pipeline controls how the imager captures the raw image. This includes control of parameters such as the frame rate, the integration period and the dynamic range of the camera. Autobrite® applies primarily to this section of the pipeline.

Noise Removal

The noise removal section of the pipeline corrects for non-ideal characteristics of the imager. This includes compensation for column fixed pattern noise, dark current subtraction, and a non-linear filter that eliminates stuck on or stuck off pixels.

Image Enhancement

The image enhancement section of the pipeline optimizes the video for display or 8-bit processing applications. In these applications, it is necessary to reduce the bit width of the video from 12 bits to 8 bits. The camera supports two options for accomplishing this.

The first option is called merge bins. Merge bins develops a non-linear, but monotonic mapping from the input video to the 8-bit output video. The degree to which merge bins affects the video can be controlled by specifying a threshold value. Higher threshold numbers will result in a larger affect. Setting the threshold to 0 will cause the algorithm to have no affect, and setting the threshold to values greater than 1000 will cause the algorithm to approximate histogram equalization.

The threshold may be fixed, or expressed as a function of the gray shade. Specifying the threshold as a function of gray shade allows the algorithm to affect bright, moderate, and dark portions of the image differently and is especially suitable for night applications.

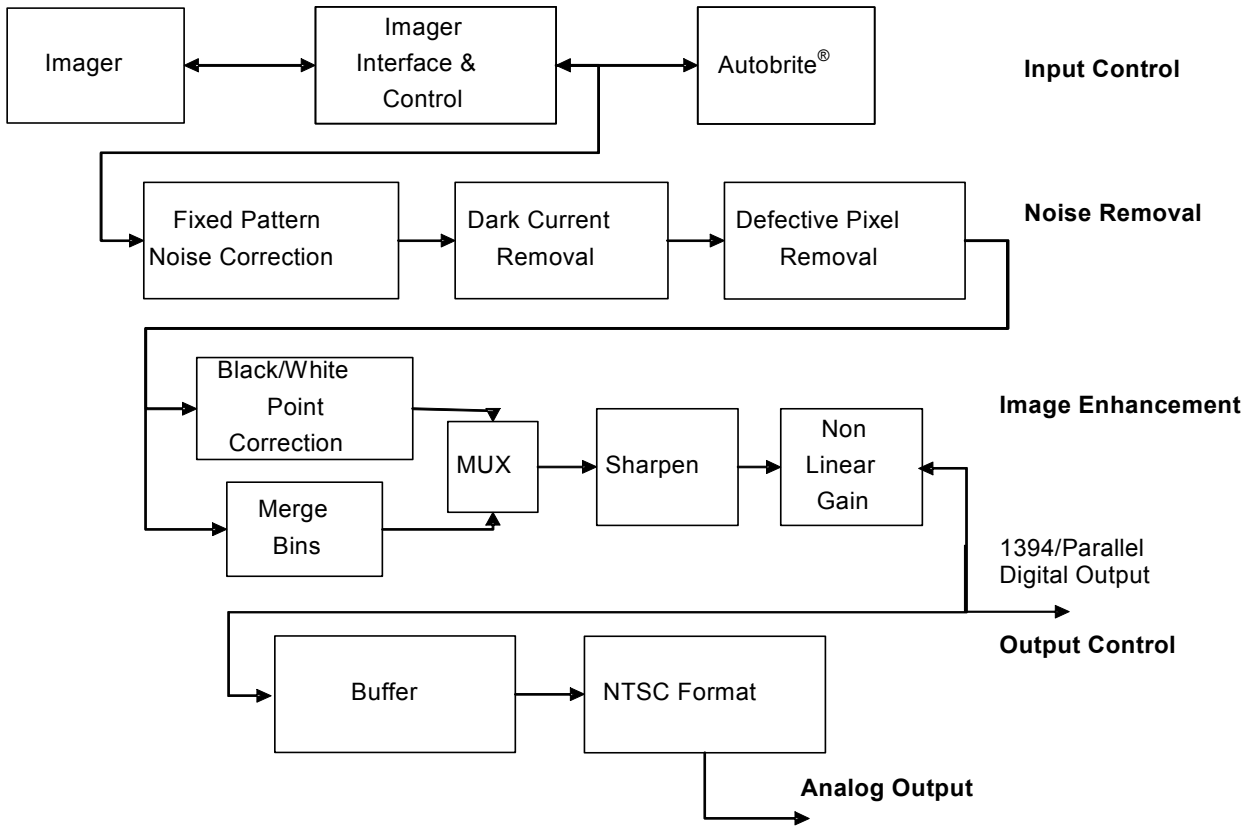

Figure 2. Monochrome Processing Pipeline

The second option (which may be selected by a dip switch setting) is to implement black/white point correction and then truncate the video to 8 bits. This algorithm calculates an offset that guarantees a programmable number of pixels in the image are at a gray code of zero. In a second step, a gain that insures a programmable number of pixels are saturated is applied to the video. This in effect stretches the histogram to cover the complete range. Once this has been accomplished, the 12-bit data is truncated to 8 bits

Color XAECK10003

Figure 3 illustrates the contents of a color XAECK10003 evaluation kit.

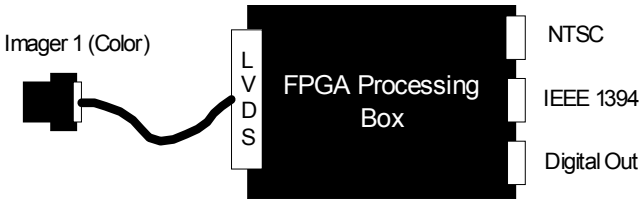

Figure 3. Color System

Color Processing Box Specifications

Processing Box	
Housing	
Processing Base	2 Million Gate Xilinx FPGA
Input Transport	LVDS Serial I/F
Output Transport	NTSC, IEEE 1394, Parallel Digital (Single Ended)
Serial Control	IEEE 1394,Digital Serial (I^2C)
Power Supply	6V (external source)

Color Block Diagram

Figure 2 illustrates the video processing and control algorithms implemented in the control box of the XAECK10001, monochrome camera kit. Some of the blocks are common with the monochrome processing pipeline. Please refer to that section for descriptions of those blocks. The following sections describe blocks unique to the color processing pipeline.

Dark Scene Median Filter

The color pipeline includes a 3-tap median filter that can be used to remove noise in dark scenes. The camera can be configured to automatically apply the filter as the image average drops.

Decompress

When operated in an extended dynamic range mode, the imager captures data using a non-linear response. To improve the accuracy of some of the processing steps it is necessary to first linearize the data. Since the gamma is known, the camera is able to apply a reverse gamma function to generate 20-bit linear data for further processing.

Crosstalk Compensation

The crosstalk compensation block applies a 3x3 matrix transform to the data to compensate for known electrical and optical crosstalk in the imager.

White Balance

The camera applies a modified “gray world” algorithm to balance the colors. The algorithm attempts to add gain to specific color channels to have the chrominance of the image to average to a gray value. It is modified from a typical value by the following.

The maximum tint that can be applied by this algorithm is limited. This prevents strongly colored scenes from generating color artifacts. In addition, the white balance is disabled as the scene darkens. The point at which the balance coefficients are frozen can be configured by the user.

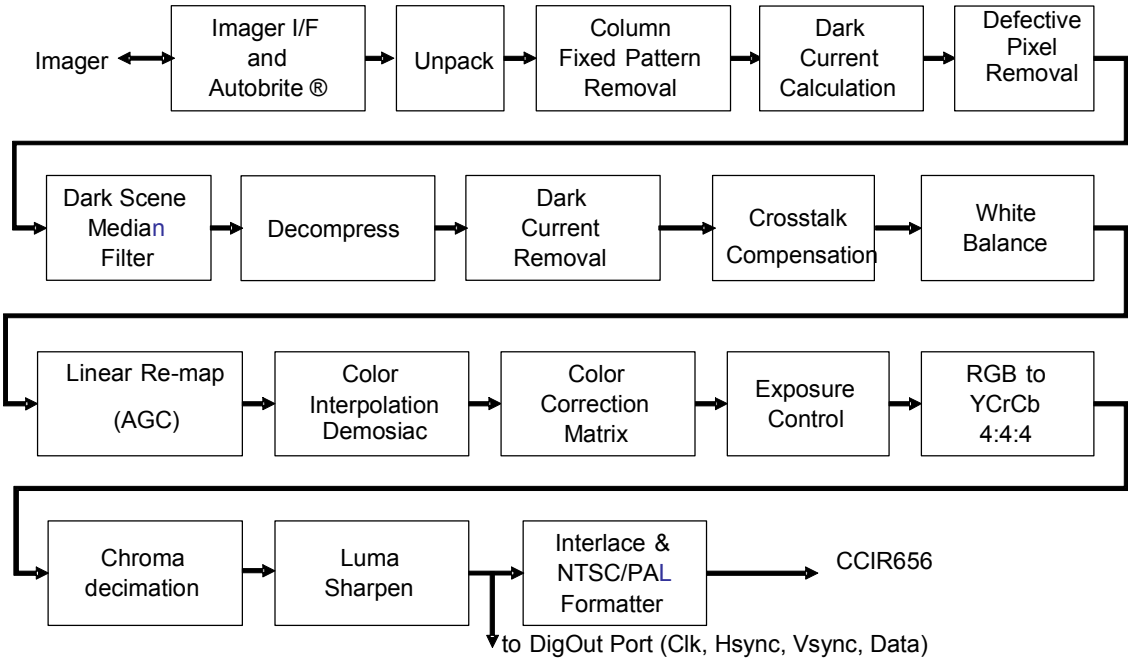

Figure 4. Color Processing Block Diagram

Linear Re-map

The linear remap block attempts to ensure the image histogram fills all values in the 8-bit space. It calculates an offset that ensures a programmable number of pixels are black—this is also referred to as black point correction. It also includes a gain stage that ensures a programmable number of pixels are at the saturated value—this is also referred to as white point correction

Color Interpolation

The color interpolation block applies a filter to the data to generate red, green, and blue values for all pixels.

Color Correction Matrix

The color correction matrix applies a color correction function to compensate for the known transmission of the color filters and IR blocking filter.

Exposure Control

The exposure control block applies a non-linear transfer function to the data to optimize it for display on 8-bit displays.

Luma Sharpen

The luma sharpen block in the color system functions similarly to the same block on the monochrome system with some exceptions.
The strength of the luminance sharpening filter has finer adjustments than in the monochrome system. In addition, the strength of the filter can be automatically scaled with the image average. This prevents the sharpening filter from adding noise to dark scenes. The behavior of this filter may be modified through either the IEEE 1394 or I^2C Interface.

Stereo XAECK10005

Figure 5 illustrates the contents of a stereo XAECK10005 evaluation kit.

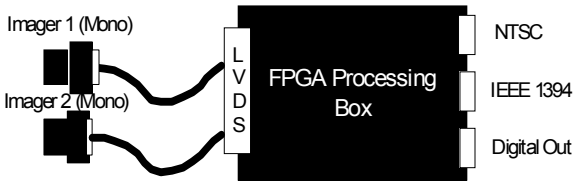

Figure 5. Stereo System

Stereo Processing Box Specifications

Processing Box	
Housing	
Processing Base	2 Million Gate Xilinx FPGA
Input Transport	LVDS Serial I/F
Output Transport	NTSC, IEEE 1394, Parallel Digital (Single Ended)
Serial Control	IEEE 1394, Digital Serial (I^2C)
Power Supply	6V (external source)

Stereo Processing Block Diagram

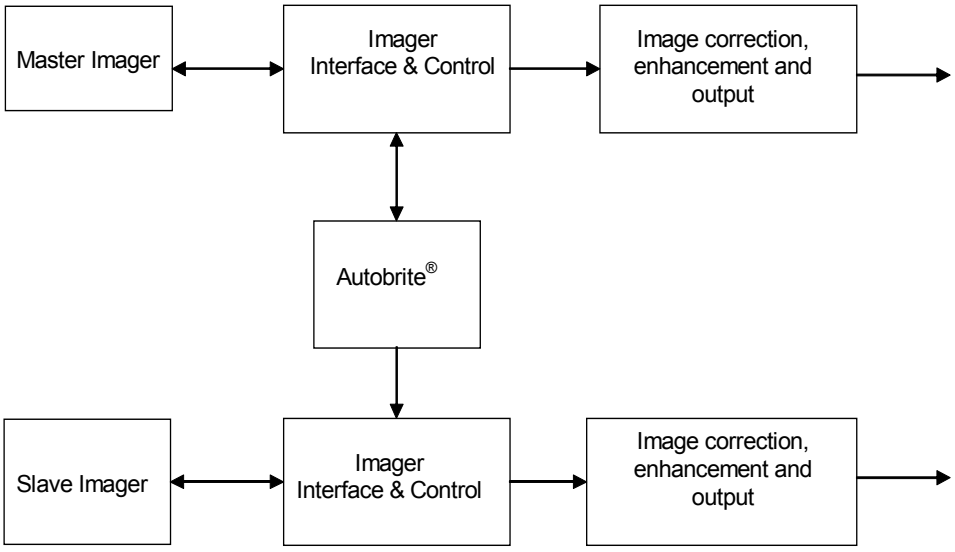

Figure 6. Stereo Block Diagram

Additional Stereo Features

The image correction, enhancement, and output portions of the pipeline are identical to the monochrome system. Please refer to the monochrome section for descriptions of these processing steps.

The stereo system differs in the calculation of Autobrite parameters. In the stereo system, the Autobrite parameters calculated for the master camera are fed to the slave camera to ensure the two imagers respond similarly to identical objects in the scene.

In addition to ensuring the settings match, the hardware ensures that the capture timing also matches. The exposure and read out time of the slave camera is locked to the master camera to ensure that images are taken at the same time. There is a register bit that indicates when the cameras have successfully synchronized. Note that the performance of the camera is not guaranteed should the imagers fail to synchronize for any reason.

Camera Head

All of the XAECK100 versions come with one or more camera head packages. The camera head is the portion of the XAECK100 that includes the imager, the lens, and sufficient electronics to transport the digital sensor data to the processing box. The functionality in the head is minimized to maximize the flexibility offered by the physically larger and more programmable processing box.

The standard module is referred to as the “evaluation” head. It provides flexible mounting and lens features and is intended to be used for technical evaluations of the camera. It provides a standard tripod thread and a CS-Mount lens. It comes standard with a CS-M12 adaptor and two M-12 lenses. The housing is made from aluminum, which provides a rugged, but not sealed package.

Figure 7 illustrates the shape of the evaluation head.

Interface Description

The Automotive Evaluation Kits are intended to support the evaluation of Cypress’s technology in a variety of applications, so it is designed to provide a number of options for control and video interface. Each of the interfaces is described in the following sections.

NTSC Interface

To support interoperability and easy integration of the camera with displays and other systems, the XAECK100 includes an NTSC or RS170 analog video interface. The quality of the video available over the analog interface is limited by the NTSC and RS170 standards, but this can provide a fast method of getting the camera to operate in a basic mode. Applications requiring maximum image fidelity should consider using one of the other interfaces.

The XAECK100 defaults to standard NTSC timing on the application of power. This allows users to directly connect the camera to a display without developing an interface to the serial control interface. Applications required additional adaptability and programmability should consider using one of the other interfaces.

Parallel Digital Interface

The evaluation kits offer a parallel digital video interface intended to allow customers to connect directly to the digital interface of DSP modules

Vertical Timing

Figure 8 defines the vertical timing of the digital video interface.

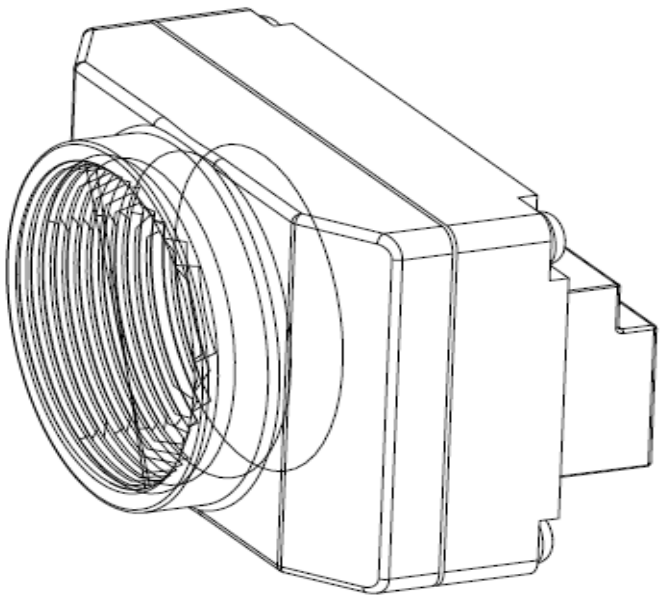

Figure 7. Evaluation Head Sketch

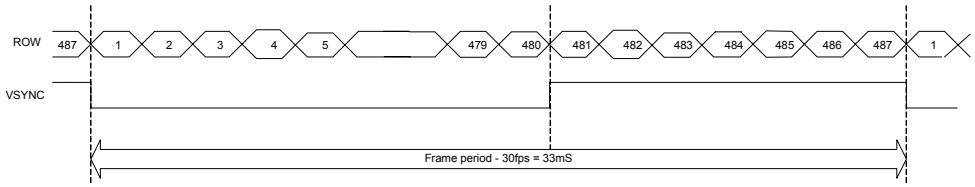

Figure 8. Vertical Timing Waveform

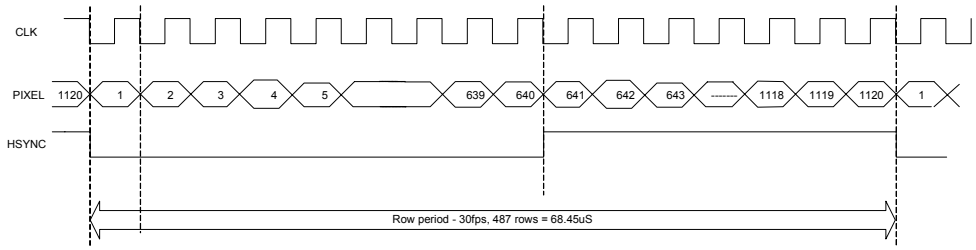

Figure 9. Horizontal Timing Waveform

All signals are generated synchronously to the pixel clock. The rising edge of the pixel clock should be used to latch the data.

Horizontal Timing

Figure 9 defines the horizontal timing of the digital video interface. All signals are generated synchronously to the pixel clock. The rising edge of the pixel clock should be used to latch the data.

IEEE 1394 Interface

The IEEE 1394 Interface provides both video transport from the camera to a PC and control of the camera using either a custom application developed by customers using Cypress's Image Capture API, or using the Video Capture application provided by Cypress.

The IEEE 1394 interface has been optimized to illustrate the performance of the camera rather than following a commercial video standard. This interface provides 12-bit video data at the sensor resolution as well as information on the status of the camera. In addition, this interface can be used to program or control the camera to adapt its behavior to fit the specific requirements of any application. The control settings available through the IEEE 1394 interface also affect the NTSC output, so this can be used in applications that require an analog output from the camera.

For further information on how to use either method to control the camera, please refer to one of the following application notes:

- Automotive Evaluation Kit–User's Manual (AN6001)

I²C Interface

The Automotive Evaluation Kit offers an I²C control interface intended to allow direct control of the camera. The read and write sequence is shown in the following diagram.

The I²C registers control various parameters of the image processing algorithms. The following section provides details on how various registers control the image processing algorithm.

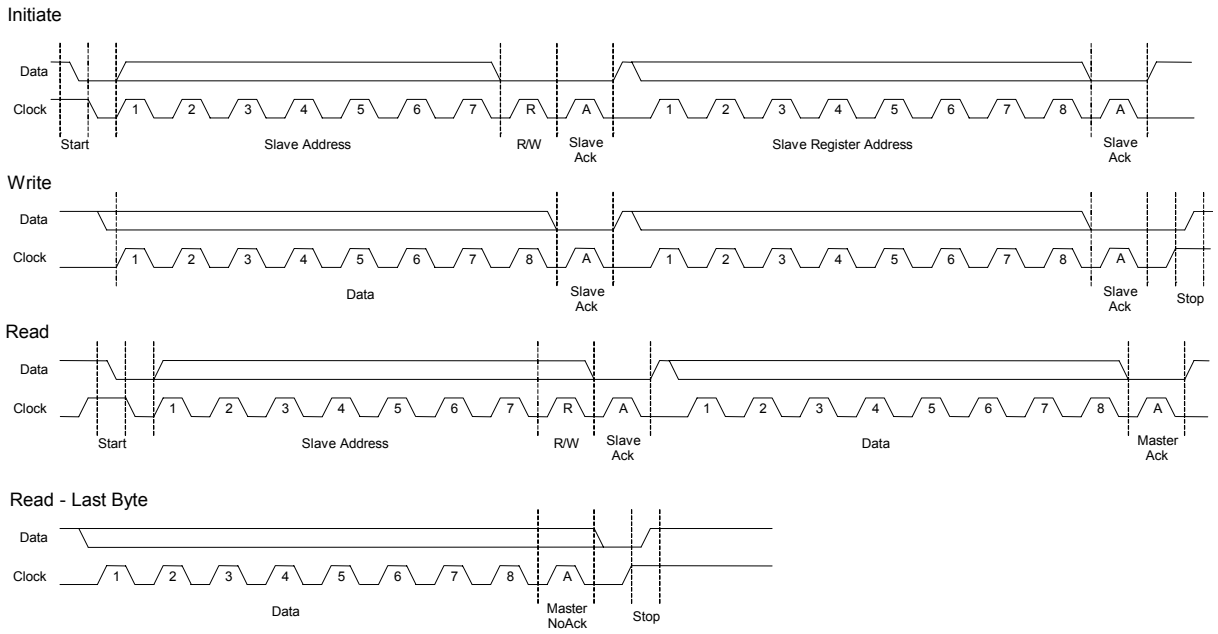

Figure 10. I²C Timing

Camera Head Interface

The Automotive Evaluation Kit units increases application flexibility by using a proprietary interface across a standard serialized LVDS. While the user is not expected to use this interface (nor is it expected to be incorporated into the final product design), it does conform to the following specifications.

Camera Head Interface Specification

Parameter	Specification
Cable Length	Up to 5 meters
Cable type	Cat-5
Connector	Standard Ethernet

Connector Definition

The parallel digital video and serial control interfaces are provided on a 40-pin header on the module. The header uses two rows of square pins on a 0.1” center. The function of the pins depends somewhat on the type of evaluation kit and is defined for each kit in the following sections.

The diagram below shows the location of each of the connectors on the ECK PCB. Note that the ECK cover has to be removed to access some of the connectors.

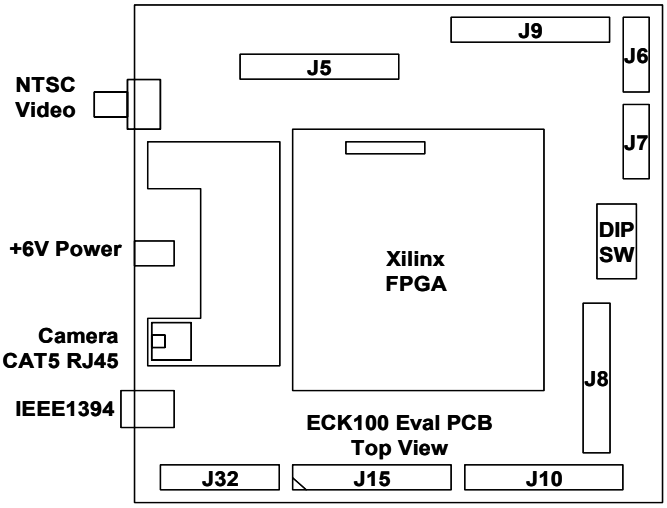

Figure 11. Mother Board Placement Diagram Of The ECK-100 Demo Kit

XAECK10001, Monochrome Camera J15

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	Data_0	4	Data_1
5	Data_2	6	Data_3
7	Data_4	8	Data_5
9	Data_6	10	Data_7
11	Data_8	12	Data_9
13	Data_10	14	Data_11
15	NC	16	No connect
17	Strobe	18	No connect
19	FOD (INPUT)	20	No connect
21	No connect	22	No connect
23	No connect	24	CLK
25	No connect	26	No connect
27	No connect	28	(0 = reset, 1 = run), nc if unused (INPUT)
29	No connect	30	HSYNC (0 = video, 1 = blank)
31	No connect	32	VSYNC (0 = video, 1 = blank)
33	No connect	34	FOD(INPUT)
35	No connect	36	SDA(BIDIR)
37	No connect	38	SCL(INPUT)
39	GND	40	GND

XAECK10003, Color Camera J15

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	Y_0	4	No connect
5	Y_1	6	No connect
7	Y_2	8	No connect
9	Y_3	10	No connect
11	Y_4	12	No connect
13	Y_5	14	No connect
15	Y_6	16	No connect
17	Y_7	18	No connect
19	Reserved	20	No connect
21	No connect	22	No connect
23	CbCr_0	24	CLK
25	CbCr_1	26	No connect
27	CbCr_2	28	(0 = reset, 1 = run), nc if unused (INPUT)
29	CbCr_3	30	HSYNC(0 = video, 1 = blank)
31	CbCr_4	32	VSYNC(0 = video, 1 = blank)
33	CbCr_5	34	FOD(INPUT)
35	CbCr_6	36	SDA(BIDIR)
37	CbCr_7	38	SCL(INPUT)
39	GND	40	GND

XAECK10005, Stereo Camera J15

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	Master_Data_0	4	Master_Data_1
5	Master_Data_2	6	Master_Data_3
7	Master_Data_4	8	Master_Data_5
9	Master_Data_6	10	Master_Data_7
11	Master_Data_8	12	Master_Data_9
13	Master_Data_10	14	Master_Data_11
15	Slave_Data_0	16	Slave_Data_1
17	Strobe	18	Slave_Data_2
19	FOD (INPUT)	20	No connect
21	No connect	22	No connect
23	Slave_Data_3	24	CLK
25	Slave_Data_4	26	No connect
27	Slave_Data_5	28	(0 = reset, 1 = run), nc if unused (INPUT)
29	Slave_Data_6	30	HSYNC (0 = video, 1 = blank)
31	Slave_Data_7	32	VSYNC (0 = video, 1 = blank)
33	Slave_Data_8	34	Slave_Data_11
35	Slave_Data_9	36	SDA(BIDIR)
37	Slave_Data_10	38	SCL(INPUT)
39	GND	40	GND

Note: For physical representation of J15 refer to diagram on page # 7.

DIP Switch Definition

The XAECK100 includes an eight-position DIP switch that can be used to configure some of the default settings of the camera. *Table 1* summarizes the functionality of this switch.The settings described in **bold** are the factory settings.

Table 1.DIP Switch Definitions (DIP Switch settings on Demo Kit)

DIP	XAECK10001-Mono		XAECK10003-Color		XAECK10005-Stereo	
	ON	OFF	ON	OFF	ON	OFF
1	ROI is enabled by default and cannot be disabled by register operations.	**ROI is disabled by default, but can be enabled by register operations**.	ROI is enabled by default and cannot be disabled by register operations.	**ROI is disabled by default, but can be enabled by register operations.**	ROI is enabled by default and cannot be disabled by register operations.	**ROI is disabled by default, but can be enabled by register operations**.
2	Reserved	**Reserved**	Reserved	**Reserved**	Reserved	**Reserved**
3	Linear Remap is selected as the AGC algorithm.	**Merge Bins is selected as the AGC algorithm**	Reserved	**Reserved**	Linear Remap is selected as the AGC algorithm.	**Merge Bins is selected as the AGC algorithm**
4	**AGC is enabled by default, but may be disabled by register operations.**	AGC is disabled by default and cannot be enabled by register operations.	Reserved	**Reserved**	AGC is enabled by default, but may be disabled by register operations.	**AGC is disabled by default and cannot be enabled by register operations.**
5	Reserved	**Reserved**	Reserved	**Reserved**	Reserved	**Reserved**
6	Reserved	**Reserved**	Reserved	**Reserved**	Reserved	**Reserved**
7	**Processing is enabled on the IEEE 1394 video**.	Raw sensor data is transmitted over the IEEE 1394 interface. Note the NTSC interface still transmits processed data	**Processing is enabled on the IEEE 1394 video**.	Raw sensor data is transmitted over the IEEE 1394 interface. Note the NTSC interface still transmits processed data	**Processing is enabled on the IEEE 1394 video.**	Raw sensor data is transmitted over the IEEE 1394 interface. Note the NTSC interface still transmits processed Data
8	A non-linear gain function is applied to the video after the AGC function.	**No additional non-linear gain is applied to the video after the AGC function.**	Reserved	**Reserved**	A non-linear gain function is applied to the video after the AGC function.	**No additional non-linear gain is applied to the video after the AGC function.**

Functional Specification

This section describes the general functional design specifications for the monochrome Automotive Evaluation Kit camera module.

Image Capture Features

The camera kit includes a number of features that allows the user to configure the mode by which images are captured. These features can be configured either using the Video-playback application or the serial control. The following sections describe these features and how they are intended to be used. For detailed information on their operation, please refer to one of the following application notes.

Control Interface	Document Title
Video-playback	Automotive Evaluation Kit–User's Manual (AN6001)

Free Running Mode

The default mode of operation for the camera is the free running mode. In this mode the camera requires no external stimulus in order to operate. When power is applied the camera will boot up and provide processed images at the default frame.

The camera generates a video signal at up to 30 fps with internally generated clocks and synchronization signals. These synchronization signals are output along with the processed image data. The frame timing is illustrated in *Figure 12*.

Frame on Demand Mode

The camera module offers a frame on demand mode. When this is enabled, the camera module will output one single frame in response to an external frame start pulse. The latency to the start of the output frame is variable, with a maximum of 1 frame between the frame start pulse and the falling edge of

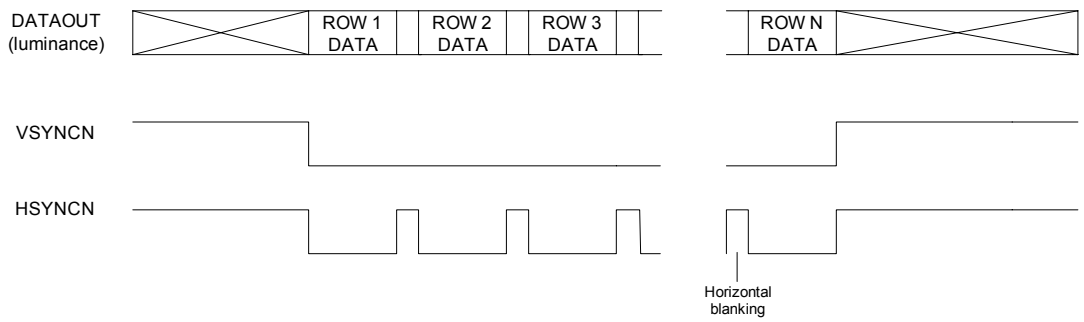

Figure 12. Free Running Timing

vsync to indicate the start of the output frame. The camera will internally be in a fully operational mode with the exception of the output drivers. This is necessary to ensure that the output frame is processed with all the correct parameters and any filters are settled.

In essence this mode of operation can be likened to a request to turn on the output drivers of the camera module for one frame. All other camera logic will be running as if in Free Running mode.

If the user's system drives the frame start line high at least one clock cycle before the falling edge of an internal vsync signal then the output drivers shall be switched on in time for that frame. If the frame start line is pulled High during a frame (while vsync is Low) then the next frame will be output. This is illustrated further in *Figure 13*.

Strobe Synchronization

The evaluation kit supports three methods for synchronizing externally generated lighting sources (strobes) to the camera's exposure:

Full Frame Strobe with FOD

This mode is used when the strobe is enabled for the entire frame. The strobe pin IS NOT USED in this mode. This mode is compatible with the use of Autobrite and/or less than full integration time. The imager exposure parameters are updated only when the FOD signal is asserted, and within frame boundaries. The strobe should be enabled at the same time that the FOD signal is asserted. The strobe should be disabled once the entire frame is read into the receiving system.

There may be a latency of several frames between the assertion of FOD and the actual readout of the frame. This time is used to allow the image exposure and filter settings to be correctly determined.

A maximum latency may be set by the user in integer number of frames. If this limit is reached then the frame will be read out regardless of whether the correct exposure is reached. If this operation is not desired then the maximum latency should be set to 0, which will result in there being no limit to the latency.

Full Frame Strobe without FOD

This mode is used when the strobe is enabled for the entire frame. The strobe may be turned on/off when the strobe pin is high. The strobe state should be maintained when the strobe pin is low. The strobe pin will be low when ANY imager row is integrating.

This mode is compatible with the use of Autobrite and less than full integration time. If Autobrite state is to be maintained between strobe applications then that mode should be enabled and the FOD pin used to communicate when the strobe is being fired, it is NOT used as a frame request pin.

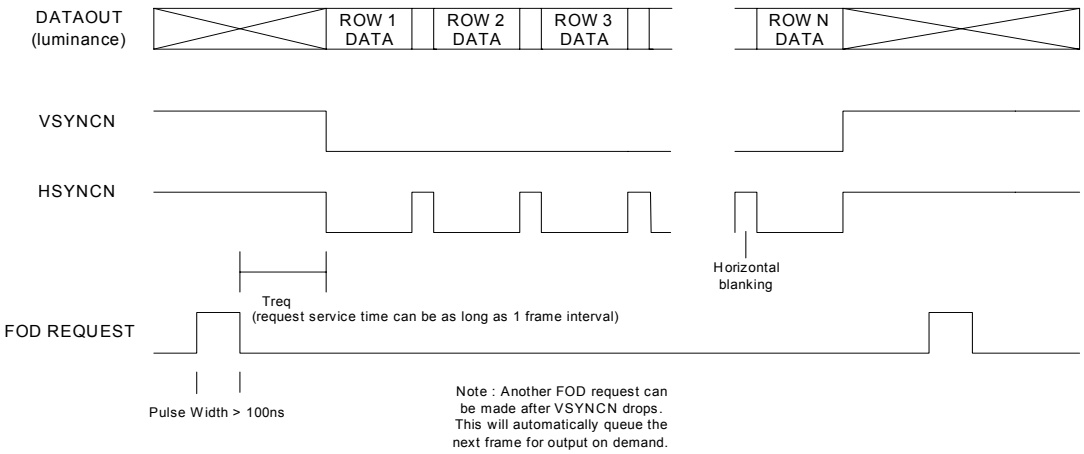

Figure 13. Frame on Demand Timing

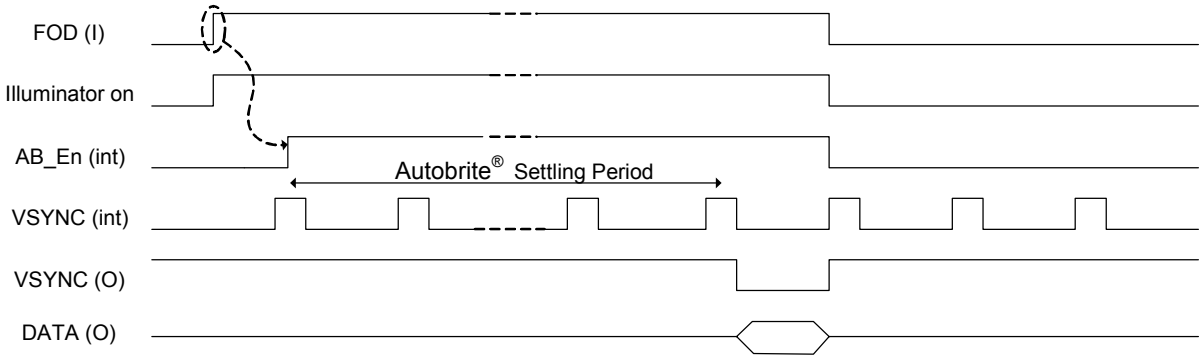

Figure 14. Full Frame Strobe with FOD Timing Diagram

Sub Frame Strobe

This mode is used when the strobe is enabled for less than the full frame. The strobe must start and finish within the period that the strobe output is High. The strobe must be off when the strobe output is Low.

The strobe pin will be high when ALL imager rows are integrating. This mode requires that Autobrite be set for linear, full integration time operation. This mode doesn't interact with FOD.

Autobrite®

The camera includes both automatic and manual control of image, or on a user specified region of interest. The following sections describe the control in more detail.

This is intended to be a general description of the features available in the XAECK100.

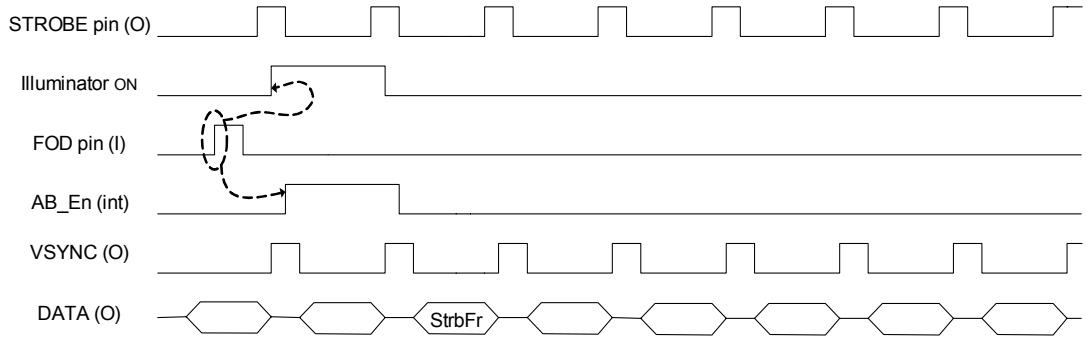

Figure 15. Full Frame Strobe without FOD Timing Diagram

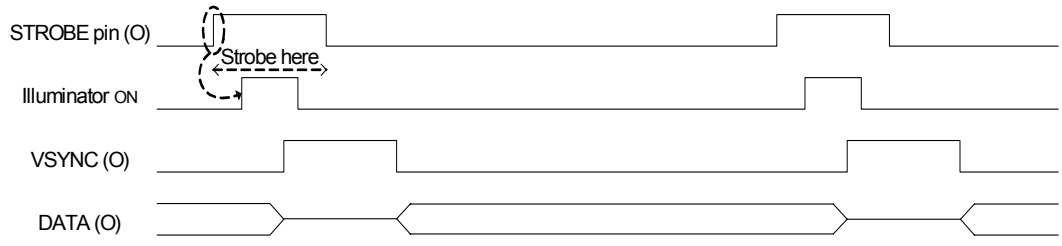

Figure 16. Partial Frame Strobe Timing

Region of Interest

The camera includes a region of interest feature that can be used to influence the automatic control of the dynamic range and the integration period. The user designates a region of interest (of any size and position) within the full frame. The camera automatically optimizes the exposure and dynamic range for this region (alternatively, the region can be ignored for exposure and dynamic range setting). The region is defined by specifying the upper left and lower right corners of a rectangle using pixel row and column numbers.

Tint Control

The camera provides for both automatic and manual control of the integration period. This can be specified independently of the gamma control—that is either can be fixed or set automatically. The Tint control algorithm attempts to set the camera to an integration period that places the average pixel value at a default or user specified level.

In addition to setting the desired image average, the user may bound the integration period that is available to the automatic control. This can prevent the integration from exceeding motion blur limits in dark environments.

Gamma Control

The camera provides for both automatic and manual control of the dynamic range by selecting one of 29 response, or gamma curves. This can be specified independently of the Tint control—that is either can be fixed or set automatically. The Gamma control algorithm attempts to select a gamma code that will result in a specific number of saturated pixels and top bin pixels. By default the top bin is set to the top 25% of available gray shades.

The algorithm works by increasing the dynamic range when the number of saturated pixels (max gray level) exceeds the saturation setting. The dynamic range is reduced when the number of pixels in the top bin of a histogram falls below a specified value.

In addition to setting the target values, the user may limit the maximum and minimum gamma settings available to the algorithm. This may be useful to applications that respond poorly to extremely high gamma values.

The user may set the number of saturated and top bin pixels desired. The choice of values for these parameters is limited to powers of 2.

Stereo Features

In the stereo version (XAECK10005) the gamma and Tint are controlled in a master/slave manner. Statistics are collected only from the master camera and the desired gamma and Tint are calculated in the same manner as in a regular monochrome camera. The desired gamma and Tint are then fed to the slave camera to ensure that both cameras are using identical settings for image capture

Image Processing Features

The camera includes a number of features that improve or remove artifacts from the image. These features are described in the following sections.

Dark Current Removal

The camera automatically senses the dark current using inactive, or dark, columns in the sensor. The current is measured for each row and subtracted from the image. This feature may be disabled by the user.

Column Fixed Pattern Noise Correction

During the vertical retrace period of scanning the imager, two fixed voltages are applied to all of the columns of the imager. These voltages are sampled by the ADC and used to calculate offset and gain errors on a column basis. These errors are then removed from the next frame. This feature may be disabled by the user.

Defective Pixel Correction

The camera includes a feature to compensate for defective pixels. A 3x3 non-linear filter is used to screen out defective pixels. The center pixel is compared against the average of its neighbors and if it is too high or low, the average is substituted for the defective pixel. This feature may be disabled by the user.

Sharpening Filter

The camera includes a 3x3 general sharpening filter. The user may disable or specify the strength of the filter.

Image Statistics

The current gamma, Tint, and image average parameters are available over the I^2C control interface.

Optical Specifications

Applications evaluating Cypress camera technology may have different Field Of View (FOV) requirements, so different lenses are available to support each application. The following table summarizes the general performance of the camera and later sections the specifications of each lens.

Table 2. Optical Specifications

Feature	Specifications
Color Response	Monochrome
Resolution	640 (H) x 480 (V) pixels
Frame Rate	60 fps maximum, full frame
Scan Mode	Progressive
Shutter	Rolling
Dynamic Range	>=120 dB
Spectral Range	400–1100 nm
Digital SNR	45 dB
Sensitivity	5V/lux sec
Format	1/3 inch
Fixed Pattern Noise	0.09%
Pixel Response Nonuniformity	1.2%

Standard Lenses

The standard kit comes with two lenses intended to support common field of view and aperture requirements. Other lenses are available, or the user may select his own lens to support additional requirements.

18° FOV Lens Specifications

The following specifications apply to the 18° field of view lens.

Specifications	Value
HFOV	18°
F/#	2.0
efl	16.0 mm
Lens element	All Glass, AR Coated
Barrel	M12x0.5, metal (aluminium)

50° FOV

The following specifications apply to the nominal 50° FOV lens.

Specifications	Value
HFOV	48.4°
F/#	2.0
efl	5.7 mm
Lens element	All Glass, AR Coated
Barrel	M12x0.5, metal (aluminium)

Optional Lenses

The following lens options have been tested with the XAECK100 kit and are available to support your application. Please contact either sales or customer support to inquire about the availability of one of more of these lenses.

30° FOV

Specifications	Value
HFOV	28.7°
F/#	2.8
efl	10 mm
Lens element	All Glass, AR Coated
Barrel	M12x0.5, metal (aluminium)

90° FOV

Specifications	Value
HFOV	82.9°
F/#	1.8
efl	2.9 mm
Lens element	All Glass, AR Coated
Barrel	M12x0.5, metal (aluminium)

Register Description

Table 3 defines the address map of the registers used to configure and control the evaluation kit. The addresses listed in the table refer to the Slave Register Address. The Slave address for the device is binary 1111011, which has a read/write bit appended to it to make an eight bit field. The function of each register is defined in a later section. All registers are not supported in every product. The table includes an indication of which products support each register.

Table 3. Register Description

Register Address	Description	XAECK10001	XAECK10003	XAECK10005
0	User Tint	Yes	Yes	Yes
1	Min Tint	Yes	Yes	Yes
2	Max Tint	Yes	Yes	Yes
3	Frame Rate	Yes	Yes	Yes
4	Gamma Control	Yes	Yes	Yes
5	White/Black Point Control	Yes	Partial	Yes
6	ROI 1	Yes	Yes	Yes
7	ROI 2	Yes	Yes	Yes
8	Video Control	Yes	Partial	Yes
9	Linear Remap (AGC) and ROI Control	Yes	Partial	Yes
A	Autobrite® Control	Yes	Yes	Yes
B	FOD Control	Yes	Yes	Yes
C	Dark Current (Read Only)	Yes	Yes	Yes
D	Video Status (Read Only)	Yes	Yes	Yes
E	Tint Status (Read Only)	Yes	Yes	Yes
F	Firmware version/Soft Reset	Yes	Yes	Yes
10				
11	Dip Switch Status (Read Only)	Yes	Yes	Yes
12				
13	MB Control 1	Yes	No	Yes
14	MB Control 2	Yes	No	Yes

Table 3. Register Description (continued)

Register Address	Description	XAECK10001	XAECK10003	XAECK10005
15	MB Table Load	Yes	No	Yes
16	MB step function start	Yes	Yes	Yes
17	MB step function end	Yes	Yes	Yes
18	MB step function control	Yes	Yes	Yes
19-1F				
20	Color Pipeline Control 1	No	Yes	No
21	Color Pipeline Control 2	No	Yes	No
22	Autoexposure/Decompress Control	No	Yes	No
23	Update Register	No	Yes	No
24	Recomp Control	No	Yes	No
25-2B				
2C	RedGain	No	Yes	No
2D	Green1Gain	No	Yes	No
2E	Green2Gain	No	Yes	No
2F	BlueGain	No	Yes	No
30	Stereo Lock Status	No	No	No
31-3F				
40	Manual Barrier Control Mode	Yes	No	Yes
41	Barrier Control Breakpoint 1	Yes	No	Yes
42	Barrier Control Breakpoint 2	Yes	No	Yes
43	Barrier Control Breakpoint 3	Yes	No	Yes
44	Barrier Control Breakpoint 4	Yes	No	Yes
45	Barrier Control Breakpoint 5	Yes	No	Yes
46	Barrier Control Breakpoint 6	Yes	No	Yes
47	Barrier Control Breakpoint 7	Yes	No	Yes
48	Barrier Control Breakpoint 8	Yes	No	Yes
49-FF				

0x00 User Tint

Bit Definition															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AB_K			**TINT_EN**	**TINT**											

The User Tint register is used when manual control of the integration period is required by the application. The bits are defined as follows:

[15:13] AB_K: This bit field can be used to slow down the response of the automatic The Integration Period is the amount of time (in row times) that the pixels accumulate light. This is basically the exposure time of the frame. The shorter the Integration Time, the darker the image will be. This may be desirable if smooth changes between camera settings are preferable to rapid response. New Tint values are calculated based on the assumption that the image average will scale linearly with the Tint setting. The algorithm works by calculating the difference between the current and target image average and then based on that difference calculating what change in Tint is required to attain the desired image average. The algorithm then multiplies the change in Tint by the AB_K value and then adds the result to the current Tint value. Therefore, smaller values of AB_K will cause the Tint value to adjust in smaller increments, although the size of the steps will remain proportional to the lighting change for a fixed AB_K.

The following table shows some examples of how AB_K affects the Tint calculations for a desired image average of 128. (Calculated Tint = Tint(128/Image Average))

Image Average	Tint	Calculated Tint	Tint Difference	AB_K	New Tint
50	100	256	156	1	256
50	100	256	156	0.5	178
50	100	256	156	0.25	139
150	250	213	–37	1	213
150	250	213	–37	0.5	231
150	250	213	–37	0.25	241

The operation of this field is defined by the following table. Other values are not defined and should not be used

AB_K	Description
4	Normal Response
3	75% of Normal Speed
2	50% of Normal Speed
1	25% of Normal Speed

[12] TINT_EN: Writing a ‘1’ to this bit will enable manual control of the integration period. When enabled, the TINT value specified in this register will be used and automatic control of the integration period is disabled. Writing a ‘0’ to this location will disable manual control and enable the automatic control of the integration period. Changes to this bit will take affect on the next full frame of video.

[11:0] TINT: This field specifies the integration period as a number of rows. The maximum integration is 486 rows. At a frame rate of 30 fps, writing a value of 0X1E6 would result in a 33 ms integration period. Changes to this parameter will take affect on the next full frame of video.

0x01 Min Tint

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TINT_SKIP				MIN_TINT											

The Min Tint register is used to specify the minimum integration period available to the algorithm controlling Autobrite® as well as controlling several other features. The bits are defined as follows:

[15:12] TINT_SKIP: This field specifies the frequency at which Tint updates made when automatic control of Tint is enabled. This field is set to a 2 frames by default to accommodate the one frame latency between calculation of a new Tint value and its taking effect. Note that the Tint will settle in the same number and size of steps, but will take longer to settle. To change the size of steps that Tint will use to adjust, use the AB_K parameter.

[11:0] MIN_TINT: This field is used to specify the minimum integration period that the Autobrite® algorithm will use to control the camera. It is only valid when manual control of the integration period is disabled. It is specified as the number of row periods you wish to have the sensor integrate. The maximum integration is 486 rows. Changes to this parameter will take affect on the next full frame of video.

0x02 Max Tint

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	BRIGHT			MAX_TINT											

The Max Tint register is used to specify the maximum integration period available to the algorithm controlling Autobrite® as well as controlling several other features. The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14:12] BRIGHT: The brightness field is used to control the target image average used to set the Tint parameter when in automatic mode. The image average is calculated based on the 8 MSBs of the video directly off of the sensor and can range from 0 to 255. The target image average is this field multiplied by 30. The default value for this field is “100”, which represents a value of 128 and targets an image average in the middle of the range. Setting the value to “101” would result in a target value of 160—which would result in a larger Tint and a brighter image average directly off of the sensor. Note that this does not influence the linear remap block which may apply a gain and offset—resulting on a change to the final image average.

[11:0] MAX_TINT: This field is used to specify the maximum integration period that the Autobrite® algorithm will use to control the camera. It is only valid when manual control of the integration period is disabled. It is specified as the number of row periods you wish to have the sensor integrate. Changes to this parameter will take affect on the next full frame of video.

0x03 Frame Rate

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PIX_RPLC		FRAME_RATE					

The Frame Rate register is used to specify the frame rate of both the scanning of the imager and the output video. The bits are defined as follows:

[15:8] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[7:6] PIX_RPLC: This field can be used to replace the active video with either all white or all black pixels. This is a feature that can be used to test/troubleshoot the camera. The field is defined by the following table:

PIX_RPLC	Description
00	Normal Video
01	Video is all black
10	Video is all White
11	Video is a counting value

[5:0] FRAME_RATE: This field represents an integer that specifies the number of frames to be taken per second.

0x04 Gain/Gamma Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	GAMMA_SKIP				MAX_GAMMA					GAMMA					GAMMA_EN

The Gain/Gamma Control register is used to specify parameters that affect the gamma control of the camera as well as the digital gain. The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14:11] GAMMA_SKIP: This field specifies the frequency at which gamma may be updated by the automatic control algorithm (when enabled.) The default is set to 2 to account for a one frame latency between the calculation of a new value and its effect. Lower values may result in an overshoot in the response to a step change in image lighting.

[10:6] MAX_GAMMA: These bits define the maximum gamma code that will be available to the algorithm controlling the dynamic range of the sensor. Changes to this parameter will take affect on the next full frame of video.

[5:1] GAMMA: These bits specify the value of gamma to be used when user gamma is enabled. Increasing values of gamma represent increasing amounts of signal compression—resulting in increased dynamic range. Values of 3 and below are linear and the maximum value of 31 represents the maximum dynamic range of the sensor. Changes to this field take affect immediately—even in the middle of a frame. This may result in a frame with the top and bottom portions of the image being taken with different gamma settings.

[0] GAMMA_EN: Writing a '1' to this bit will enable the use of the gamma value specified in the GAMMA field of this register to be used in place of the value calculated by the Autobrite® algorithm. This may result in a frame with the top and bottom portions of the image being taken with different gamma settings

0x05 Black/White Point Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP_PIX_CNT								WP_PIX_CNT							

The Black/White point control register is used to control how the offset and gain parameters are calculated in the linear remap block of the processing. Note that this register affects the linear remap function which must be both enabled and selected using the hardware DIP switches. Writing to this register when AGC is disabled, or Merge Bins is selected as the AGC algorithms will have no affect on the image. To enable both AGC and select white/black point control (linear remap) dip switches 3 and 4 must be set to the on position. The bits are defined as follows:

[15:8] BP_PIX_CNT: *[XAECK10001 Only]* This field specifies the number of black pixels to be included in the output image. The value entered into this field is multiplied by 64

[7:0] WP_PIX_CNT: *[XAECK10001/003 Only]* This field specifies the number of white pixels to be included in the output image. The value entered into this field is multiplied by 256. In the XAECK10003, additional precision is added in register 24.

0x06 ROI 1

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROI_XOFF[11:3]								ROI_XON[11:3]							

The ROI 1 register is used to specify the size and location of the region of interest box in the x axis (imager columns). The bits are defined as follows:

[15:8] ROI_XOFF: This field specifies the 8 most significant bits of the ending X coordinate. The least significant bits are fixed at "000". Therefore, the resolution of this coordinate is limited to multiples of 8.

[7:0] ROI_XON: This field specifies the 8 most significant bits of the starting X coordinate. The least significant bits are fixed at "000". Therefore, the resolution of this coordinate is limited to multiples of 8.

0x07 ROI 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROI_YOFF[15:8]								ROI_YON[7:0]							

The ROI 2 register is used to specify the size and location of the region of interest box in the y axis (imager rows). The bits are defined as follows:

[15:8] ROI_YOFF: This field specifies the 8 most significant bits of the ending Y coordinate. The least significant bits are fixed at "00". Therefore, the resolution of this coordinate is limited to multiples of 4.

[7:0] ROI_YON: This field specifies the 8 most significant bits of the starting Y coordinate. The least significant bits are fixed at "00". Therefore, the resolution of this coordinate is limited to multiples of 4.

0x08 Video Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_ROW0_EN	TINT_HYST	STALL_AB_DISABLE	DARK_OFFSET_EN	SHARP_STRENGTH	SHARP_EN	FPN_GAIN_EN	FPN_OFFSET_EN	FULL_FRAME_FPN	AGC_MODE	WP_EN	BP_EN	SK_EN	INVRT_SYNC	NTSC_TEST_ENABLE	Reserved

The Video control register is used to configure and enable various features of the camera control algorithms.

[15] CFG_ROW0_EN: Writing a '1' to this location enables configuration data to be used in place of the first row of data on the IEEE 1394 video output. This contains a variety of information about the capture parameters and processing behavior and tags each frame with it.

[14] TINT_HYST: Writing a '1' to this bit will cause the automatic control of the Tint settings to have additional hysteresis. This added hysteresis will cause changes of less than one line to be suppressed. This is useful in eliminating the appearance of flickering in very bright scenes where a change of one line of integration time represents a significant change in image brightness.

[13] STALL_AB_DISABLE: Writing a '1' to this location will cause the Autobrite control parameters to be fixed during the frames that are not enabled for transmission.

[12] DARK_OFFSET_EN: Writing a '1' to this location will enable dark current correction. Writing a '0' will disable dark current correction.

[11] SHARP_STRENGTH: Writing a '1' to this bit will cause the sharpening filter to be at the stronger setting. Writing a '0' to this bit will cause the sharpening filter to be at a weaker setting.

[10] SHARP_EN: Writing a '1' to this bit will enable the 3x3 FIR sharpening filter. This filter has two strengths.

[9] FPN_GAIN_EN: Writing a '1' to this location will enable the automatic correction of column fixed pattern gain errors in the hardware. FPN coefficients are calculated by placing known voltages on the columns when imager data is not being read. Writing a '0' to this location will disable FPN gain correction. Note that on power-up or after a system reset, this may require as much as two minutes to reach full performance. This is a result of filtering on the correction values to remove the affects of non-fixed pattern noise.

[8] FPN_OFFSET_EN: Writing a '1' to this location will enable the automatic correction of column fixed pattern offset errors in the hardware. FPN coefficients are calculated by placing known voltages on the columns when imager data is not being read. Writing a '0' to this location will disable FPN offset correction. Note that on power up or after a system reset, this may require as much as two minutes to reach full performance. This is a result of filtering on the correction values to remove the affects of non-fixed pattern noise.

[7] FULL_FRAME_FPN: Writing a '1' to this location will cause FPN data to be collected over the entire frame. This is a test feature and it will cause the video to be overwritten. Writing a '0' to this bit will enable normal operation.

[6] AGC_MODE: Writing a '0' to this bit will disable all gain stages in the processing pipeline including linear remap and user gain. This mode is intended to be used to measure the SNR of the imager. Writing a '1' to this bit will enable normal operation of the processing pipeline.

[5] WP_EN: *[XAECK10001 with Linear Remap Only]* Writing a '1' to this bit will enable the linear remap (or AGC) block in the processing pipeline. This block adds gain to the digital signal to ensure that the target number of pixels is at a saturated value. Writing a '0' to this bit will disable the block.

[4] BP_EN: *[XAECK10001 with Linear Remap Only]* Writing a '1' to this bit will enable black point correction in the linear remap (or AGC) block in the processing pipeline. This feature subtracts and offset from the pixel value in order to ensure that a target number of pixels is at a value of zero. WP_EN must be set in order for this feature to be active.

[3] SK_EN: Writing a '1' to this location will enable the starkiller, non-linear filter. This filter detects and corrects for single pixel defects in the imager.

[2] INVRT_SYNC: Writing a '1' to this location will change the vertical and horizontal sync pulses on the digital video output to be active low signals. They are active high by default.

[1] NTSC_TEST_ENABLE: Writing a '1' to this bit will cause the camera to generate a test pattern on the NTSC output. Writing a '0' will enable normal operation.

[0] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

0x09 Linear Remap (AGC) Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					ROI_WP_EN	ROI_WP_EN	WP_FIXED_EN	WP_FIXED_GAIN							

[XAECK100 Only] The Linear Remap Control register provides control over the Automatic Gain Control (AGC) block in the pixel processing pipeline. The block provides for both black level and white level correction and can be based either on the entire image or on a region of interest. Note that this register only functions if AGC is enabled and linear remap is selected using the hardware DIP switches. The bits are defined as follows:

[15:11] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[10] WP_ROI_EN: *[XAECK10001 with Linear Remap Only]* Writing a '1' to this bit will cause the white point correction in the linear remap block to depend only on pixels contained (or excluded by) the region of interest.

[9] BP_ROI_EN: *[XAECK10001 with Linear Remap Only]* Writing a '1' to this bit will cause the black point correction in the linear remap block to depend only on pixels contained (or excluded by) the region of interest.

[8] WP_FIXED_EN: Writing to this bit sets the mode of the linear remap block. Writing a '1' to this bit enables a fixed gain mode. When in fixed gain mode, bits [7:0] of this register are used to set the linear gain of this block. Writing a '0' to this bit enables automatic gain mode. In the automatic mode, bits [7:0] of this register specify the maximum gain that the block is permitted to use.

[7:0] WP_FIXED_GAIN_INT: If in automatic gain mode, this is the maximum gain that linear remap will allow. If in fixed gain mode, this is the gain that linear remap will apply to each pixel. The 8 bits are set up with 6 integer and 2 fractional bits, i.e., 8'h06 = 1.5x gain. The default value is 0X80.

0x0A Autobrite Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TRI_OUT	SHOW_ROI_BOX	ROI_EN	ROI_Polarity	Reserved		NO FLICK	WIDTH_SAT_COUNT				WIDTH_TOP_BIN			

The Autobrite Control register is used to specify parameters that influence the automatic selection of a gamma code (dynamic range control.) The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14] TRI_OUT: Writing a '1' to this bit will tri-state the video output buffers. This will reduce system power and noise when the digital video output is not in use.

[13] SHOW_ROI_BOX: Writing a '1' to this location will enable the generation of a line around the region of interest that has been defined using register 9. This is useful for checking to ensure the region of interest has been set correctly. Writing a '0' to this location will disable this feature.

[12] ROI_EN: Writing a ‘1’ to this location will enable the ROI feature. Writing a ‘0’ to this location will disable the feature and cause the entire frame to be used for automated control of the Tint and Gamma

[11] ROI_POLARITY: Writing a ‘1’ to this location will cause the area inside the region of interest to be used to calculate Gamma, Tint and linear remap settings. Writing a ‘0’ to this location will cause the area outside the region of interest to be used.

[10:9] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[8] NOFLICK: Writing a ‘1’ to this bit will enable a feature intended to reduce artifacts associated with 50-/60-Hz illumination. Note that this is only effective when gamma is set to three.

[7:4] WIDTH_SAT_COUNT: This bit field sets the width of the saturated pixel counter used to increase the gamma setting. The recommended value is B’1010”, other values can lead to oscillations in the image capture loop.

[3:0] WIDTH_TOP_BIN: This bit field sets the width of the histogram bin used to reduce the Autobrite® gamma curve. The recommended value is B’0111”, d = 7, other values can lead to oscillations in the image capture loop.

0x0B FOD Control

Bit Definition														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					FOD_MODE		FOD_BYPASS	FOD_AB_IGNORE	FOD_COUNT_LIM						FOD_REQ_LVL

The FOD Control register is used to specify the frame on demand mode desired for the application.

[15:11] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[10:9] FOD_MODE: These bits control the FOD mode of camera operation. They are defined in the following table.

FOD_MODE[15:14]	Description
00	FOD OFF
01	FULL FRAME STROBE WITH FOD
10	FULL FRAME STROBE WITHOUT FOD
11	RESERVED MODE

[8] FOD_BYPASS: Writing a ‘1’ to this bit will cause FOD to be bypassed and every frame will be visible at the digital port. This is in essence a video mode. Writing a ‘0’ to this bit will enable the FOD mode defined in register 0x02.

[7] FOD_AB_IGNORE: Writing a ‘1’ to this bit forces the FOD logic to wait for the FOD_COUNT_LIM number set below even if the Autobrite parameters settle in fewer frames.

[6:1] FOD_COUNT_LIM: This field specifies the maximum number of frames that the camera will be permitted to use to allow the Autobrite control settings to settle to the correct values. The requested frame may be delivered earlier, but will not be delivered later than this number of frames. Note that setting this value to zero will disable the limit—that is, setting it to zero provides an unlimited time for the camera Autobrite parameters to settle.

[0] FOD_REQ_LVL: Writing a ‘1’ to this bit allows level sensitive FOD frame queuing. If the FOD request line is held high the digital port will continue to send out frames without the need to drive the request line low first. Note that the first frame will have up to one frame time of latency in addition to the number of frames it required for the Autobrite algorithm to settle.

0x0C Dark Current (Read Only)

Bit Definition														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DARK_CURRENT											

The Dark Current register can be used to read back the average dark current correction value. The bits are defined as follows:

[15:12] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[11:0] DARK_CURRENT: The dark current correction.

0x0D Video Status (Read Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CUR GAMMA				IMAG AV							

The Video Status register is a read only register that provides the status of the current image. The bits are defined as follows:

[15:13] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[12:8] CUR_GAMMA: This bit field represents the current gamma code most recently calculated by the Autobrite algorithm. This value is updated as soon as the new value is calculated and there is a two frame latency before they take effect.

[7:0] IMAG_AV: This bit field represents the current image average most recently calculated by the Autobrite algorithm.

0x0E Tint Status (Read Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CUR_TINT											

The Tint Status register is a read only register that provides the most recent Tint value calculated by the Autobrite algorithm. The bits are defined as follows:

[15:12] Reserved: These bits are reserved for future use.

[11:0] CUR_TINT: This bit field represents the current Tint (integration period) most recently calculated by the Autobrite algorithm. This value is updated as soon as the new value is calculated and there is a two frame latency before they take effect. The Tint value is calculated by multiplying the number of row periods the sensor is to integrate by 8. The maximum integration is 486 rows, which yields a value of 0XF30. At a frame rate of 30 fps, a value of 0XF30 translates to a 33-ms integration period.

Note: Care must be taken when reading this register. There is a small possibility that the Tint value could be updated in the time between the I^2C transactions of reading the upper 8 bits and the lower 8-bits. It is recommended that this register be read twice and if the values are not the same, reread the register and the values should be the same. Note that Tint updates only once per frame.

0x0F Firmware Version/Soft Reset

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									Version						RST

The Firmware Version/Soft Reset register is used to either firmware version or to reset the camera to the power-on state. The bits are defined as follows:

[15:7] Reserved: These bits are reserved for future use.

[6:1] Version: This bit field identifies the version of the firmware in the evaluation camera. The version number increases as defects are corrected and features added to the evaluation kit.

[0] RST: Writing a '1' to this bit will return all registers to the power on state.

0x11Dip Switch Status (Read Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DIP[8:1]							

The Dip Switch Status register provides information on the current dip switch settings. Applications using features that can be overridden by the hardware dip switches should check this register. Information on the function of the dip switches can be found in section 8 of this document.

[15:3] Reserved: Reserved for future use.

[7:0] DIP: A '1' in each position indicated that the corresponding switch is in the on position. Refer to "DIP Switch Definition" on page 10 for information on the function of the dip switches.

0x13 Merge Bins Control 1

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Q_Slope			Max_Q											

[XAECK10001 Only] The Merge Bins Control register is used to enable and control the behavior of the merge bins contrast enhancement algorithm. The merge bins algorithm can be controlled by specifying a Q function that indicates how strongly gray levels should be affected by the algorithm. The Q function can be specified in one of two methods. The first method uses an internal drawing engine to generate the function. The alternative is to manually load a table which will specify a unique Q value for each gray level. The drawing engine operates in two modes, the first of which assumes that a maximum Q is specified for gray level zero and that this value is reduced for increasing gray levels at a specified slope until a minimum Q value is reached. This mode is controlled by register 0x13 and 0x14. For information on the second mode refer to register 0x16-0x18. The bits are defined as follows:

[15:3] Reserved: Reserved for future use.

[14:12] Q_Slope: The Q Slope field specifies the rate at which the Q value is reduced for increasing gray shades. This field is cumulatively subtracted from the initial, maximum value

[11:0] Max_Q: The Max Q field specifies the Q value for gray level zero. This forms the starting point for the Q function. Note: if the Min_Q value is set to be higher than the Max_Q value, the result will be a flat threshold at the Min_Q value.

0x14 Merge Bins Control 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MB_Enable	Reserved	User_Curve_En	Draw_Enable	Min_Q											

[XAECK10001 Only] This register is used in conjunction with register 0x13 to control the merge bins drawing engine. The bits are defined as follows:

[15] MB_Enable: Writing a '1' to this bit will enable the merge bins algorithm

[14] Reserved: Reserved for future use.

[13] User_Curve_En: Writing a '1' to this bit will enable the use of a user loaded curve. This must be loaded via register 0x15 prior to enabling this function.

[12] Draw_En: Writing a '1' to this bit will enable a Q function based on the parameters programmed in registers 0x13 and 0x14.

[11:0] Min_Q: The Min Q field specifies the Q value at which the function will level off. The Q value for gray shade zero is set to the max Q value and then decremented by the Q Slope until this value is reached. **Note**: If the Min_Q value is set to be higher than the Max_Q value, the result will be a flat threshold at the Min_Q value.

0x15 Merge Bins Table Load

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Q											

[XAECK10001 Only] The Q function can be specified in one of two methods. The first method uses an internal drawing engine to generate the function. The alternative is to manually load a table which will specify a unique Q value for each gray level. This register controls the manual loading of the table. The bits are defined as follows:

[15:12] Reserved: Reserved for future use.

[11:0] Q: The first time this field is written after a power-on or reset (including a soft reset initiated by writing to register 0xF) the Q value will be stored in the table at the location for gray code 0. The second write will store the Q value into location 1 and subsequent writes will continue to increment the storage location. The algorithm uses 512 locations.

0x16 Merge Bins Threshold Step Function Starting Value

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Q_start											

This register controls the second mode of operation for the merge bins drawing engine. This function assumes that the threshold starts at a specified value and is flat with increasing bin count and then changes to a second value at a specified transition point. Registers 0x16-0x18 control this mode of operation. This register is used to specify the starting threshold value. Note that the drawing engine must be enabled using register 0x13 for these register to take affect. The bits are defined as follows:

[15:12] Reserved: Reserved for future use.

[11:0] Q_start: The Q_start specifies the fixed threshold Q value from the step function until the transition gray level. The default value is 0x010.

0x17 Merge Bins Threshold Step Function Ending Value

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Q_end											

The Table Load register is used to load the ending Q value for the threshold step function.

[15:12] Reserved: Reserved for future use.

[11:0] Q_end: The Q_end specifies the fixed threshold Q value from the step function after the transition gray level. The default value is 0x020.

0x18 Merge Bins Threshold Step Function Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Step_ena	Step_transition								

The Table Load register is used to load the transition gray level value for the threshold step function and the enable signal for the function.

[15:10] Reserved: Reserved for future use.

[9] Step_ena: Step function enable signal. Writing a '1' will enable the MB threshold step function. The default value is '0'.

[11:0] Step_transition: The Step_transition specifies the gray level where the threshold Q value makes transition from Q_start to Q_end. The default value is 0X100.

0x20 Color Pipeline Control 1

Bit Definition														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BW Interp Bypass	Reserved		CMAT CSEL	Bypass Color	Display Gamma Enable	AE Enable	CMAT Enable	Reserved	Median Filter Disable	WB Enable	Crosstalk Enable	WB_Remap Enable	Recomp Enable	Decomp Enable	Median Enable

[XAECK10003 Only] The color control register is used to enable and disable various features in the color processing pipeline.

[15] BW Interp Bypass: Writing a '1' to this field will cause the color processing pipeline to bypass the color interpolation filter.

[14:13] Reserved: These bits are reserved for future use. To ensure compatibility with other systems these bits should not be modified.

[12] CMAT CSEL: Writing to this field will select which of two color correction filters is applied. This should be left at the default value.

[11] Bypass Color: Writing a '1' to this filed will cause the color processing pipeline to bypass all processing steps after the color interpolation filter.

[10] Display Gamma: Writing a '1' to this field applies a non-linear gain to enhance dark scenes.

[9] AE Enable: Writing a '1' to this field will enable the autoexposure algorithm.

[8] CMAT Enable: Writing a '1' to this field will enable a color filter that adjusts for the actual transmission of the IR and color filters.

[7] Reserved: This bit is reserved for future use. To ensure compatibility with other systems it should not be modified.

[6] Median Filter Disable: Writing a '1' to this field will disable Median filter: Writing a '1'

[5] WB Enable: Writing a '1' to this field will disable [5] WB Enable: Writing a '1'

[4] Crosstalk Enable: Writing a '1' to this field will enable a filter intended to reduce color artifacts resulting from cross talk between pixels in the imager.

[3] WB Remap Enable Sets white balance to the correct data positions for recomp/decomp settings. Incorrect use of this bit will cause overflow in the data path.

[2] Recomp Enable: Enable recompression of the data. Incorrect use of this bit will cause overflow in the data path.

[1] Decomp Enable: Enable decompression of the data before crosstalk reduction and white balancing. Incorrect use of this bit will cause overflow in the data path.

[0] Median Enable: Writing a '1' to this field will enable a three tap horizontal low pass filter that is used to reduce noise in dark images.

0x21 Color Pipeline Control 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Stop WB Update	WB4/WB3n	Reserved						WB_Img_Avg_Threshold							

[XAECK10003 Only] The color control register is used to enable and disable various features in the color processing pipeline.

[15] Stop WB Update: Writing a '1' to this field will freeze the current white balance correction coefficients.

[14] WB4/WB3n: Choose between 4-color white balance (R,G1, G2, B) or 3-color white balance

[13:8] Reserved: These bits are reserved for future use. To ensure compatibility with other systems these bits should not be modified.

[7:0] WB_Img_Avg_Threshold: This field specifies the image average at which the white point correction algorithm will cease calculating new correction coefficients. This is used to reduce artifacts in dark images that result for false white point calculations.

0x22 Autoexposure/Decompress Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			AE_User_Gamma_Enable	AE_User_Gamma						Decomp_gamma_Sel	Gamma_Decomp				

[XAECK10003 Only] The Autoexposure/Decompress control register allows the used to specify autoexposure and decompress gamma curves.

[15:13] Reserved: Reserved for future use. For proper behavior a Read-Modify-Write operation is recommended when writing to this register.

[12] AE_User_Gamma Enable: Writing a '1' to this field will enable the use of the user specified gamma curve for the autoexposure algorithm.

[11:6] AE_User_Gamma: This field allows the user to manually specify one of 32 pre-defined gamma curves for use in the autoexposure algorithm.

[5] Decomp_gamma_Sel: Writing a '1' to this field will enable the use of the user specified gamma curve for the decompress algorithm.

[4:0] Gamma_Decomp: This field allows the user to manually specify one of 32 pre-defined gamma curves for use in the decompress algorithm.

0x23 Force WB Update

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Force_Update	Reserved								

[XAECK10003 Only] The update register is used to force an update of the Automatic White Balance coefficients. Typically this is only used when White Balance has been frozen using register 0x20.

[15:10] Reserved: Reserved for future use.

[9] Force_Update: Writing a '1' to this register will force the white balance algorithm to update its parameters. This bit will always read back a '0'.

[8:0] Reserved: Reserved for future use. For proper behavior a Read-Modify-Write operation is recommended when writing to this register.

0x24 Recomp Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Recomp_WP_Num_Pix[7:0]							

[XAECK10003 Only] The recomp color register controls the recompression of the pixel after processing.

[15:8] Reserved: Reserved for future use.

[7:0] Recomp_WP_Num_Pix[7:0]: This field adds to the resolution of the number of white pixels targeted by the white point correction algorithm.

0x2C RedGain [XAECK10003 only]

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						RedGain									

[9:0] RedGain: Every Red pixel is multiplied by the value in this register. This feature is only active if BlueGain[15] is 1.

0x2D Green1Gain [XAECK10003 only]

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Green1Gain									

The gain factor is a 2.8 fractional number. Bits 9:8 represent an integer multiplication factor and 7:0 represent the fraction. A gain of unity is 0x0100. A gain of 1/2 is 0x0080. A gain of 2 1/4 is 0x0240. Generally this value should only be used to adjust the 4 color channels relative to each other depending on the lighting conditions. Adjusting the brightness of the image should be done with the WP_FIXED_GAIN in register 0x09.

[9:0] G1Gain: Every Green1 pixel is multiplied by the value in this register. This feature is only active if BlueGain[15] is 1.

0x2E Green2Gain [XAECK10003 only]

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Green2Gain									

Normally the 2 green colors are left at Unity gain (0x0100) which is the default and the Red and Blue channels are adjusted to get a flat response from all three colors.

[9:0] G2Gain: Every Green2 pixel is multiplied by the value in this register. This feature is only active if BlueGain[15] is 1.Note that if WB4/WB3n is 0, this value is ignored and the G1Gain value is used instead.

0x2F BlueGain [XAECK10003 only]

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WB	Reserved					BlueGain									

[15] Manual_WB: Writing a 1 to this bit enables manual White Balance. The Automatic White Balance coefficients are ignored and the values used in registers 0x2C-0x2F are used for white balance instead. Note that White Balance and the image processing pipeline must be enabled or these registers will be ignored.

[9:0] BlueGain: Every Blue pixel is multiplied by the value in this register. This feature is only active if Manual_WB (BlueGain[15]) is 1.

Note: When Manual_WB is 0, registers 0x2C-0x2F will read the current automatic white balance value. When Manual_WB is 1, then the value written to each of these registers will be read back. When the automatic white balance is enabled, each of the 4 registers should be read and written back, and then Manual_WB set to 1. This will put the ECK into manual White Balance mode with no visible changes in the output video. The values in the gain registers can then be incrementally updated to the desired White Balance levels.

0x30 Stereo Lock Status

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															Locked

The Stereo Lock Status register provides information about the status of the synchronization of the two cameras.

[15:1] Reserved: Reserved for future use.

[0] Locked: When this bit is set, the stereo imager timing has successfully locked. Should this bit read back a '0', correct camera operation is not guaranteed and the camera should be reset.

0x40 Manual Barrier Control Mode Register

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													User_bar_ready	Load_user_bar	User_bar_mode_en

[XAECK10001 Only] The Manual Barrier Control Mode register is used to load or enable the manual user barrier control feature. The bits are defined as follows:

[15:3] Reserved: Reserved for future use. For proper behavior a Read-Modify-Write operation is recommended when writing to this register.

[2] User bar ready: This bit indicates that the user barrier controller is ready to accept a new setting.

[1] Load user bar: Set this bit after loading registers 41-48 with the desired breakpoints. This bit should be cleared by the user only AFTER the user_bar_ready bit has returned to the high state.

[0] User_bar_mode_en: Setting this bit enables user barrier mode. Clearing this bit returns the camera to Autobrite® control.

0x41 to 0x48 Manual Barrier Control Breakpoint 1 to 8

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BARRIER LEVEL				ROWCOUNT											

[XAECK10001 Only] The Manual Barrier Breakpoint Control Breakpoint registers are used to set the row number at which that specific barrier is asserted.

[15:12] BARRIER LEVEL: Set the barrier level that should be asserted in these four bits. Valid values are 0–7. A value of 0 indicates the reset level, while a value of 7 indicates unhindered integration. Intermediate values can be used to hold the integration at a certain level.

[11:0] ROWCOUNT: This is a DOWN COUNTER that counts from the maximum number of rows down to 0. At row 0 the data is read off the sensor so this point is fixed.

The barrier level programmed above is asserted from the last change until the rowcount programmed here. From the next row on the next programmed barrier is used.

See ECK 100 Barrier Voltage Control for details on usage and examples.

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Document History Page

Document Title: XAECK100 Automotive Evaluation Kit Document Number: 001-04834				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	401656	See ECN	SYT	New Data Sheet
*A	410276	See ECN	SYT	Replaced the Cross reference from “Figure 4” to “Figure 2” in the Color Block Diagram section of Page 3. Changed “Star Killer” to “Defective Pixel Removal” in the block diagram of Fig 4. Added “Linear Re-map” explanations for Fig 4. Renamed “Imager Module Package” as “Camera Head” on Page 5. Corrected typo “1394” to “IEEE 1394” in the whole of the document Reversed the clock count in Fig 10 on Page 7. Changed “100 mil” to “.1 inch” in the Connector Definition on Page #7. Changed I2C to I^2C in the whole of the document Corrected typo “XAECK10001” to “XAECK10005” on Page # 8. Corrected typo in the DIP Switch Definitions column 3 from “XAECK10001” to “XAECK10005” on Page # 9. Added Barrel information for the 18° FOV Lens Specifications on Page # 13.
*B	436583	See ECN	QGS	In Features NTSC video changed to Analog NTSC video on page # 1. Added more explanation about I^2C interface on page # 6. Added Mother Board Placement Diagram Of The ECK-100 Demo Kit diagram on page # 7. XAECK10003, Color Camera J15 on page # 8. Expanded the abbreviation for FOV as Field Of View on page # 13. Added more explanation for Register Description on page # 14. Register address 2C to 2F added in Register Description table on page # 15. Added Register explanations on page # 26. Note added in 0x0E Tint Status bit definition[11:0]CUR_TINT on page # 27.