

32-bit Microcontrollers

CMOS

FR60 MB91470/480 Series

MB91482/F475/F478/F479/F482/F487/ MB91FV470

■ DESCRIPTION

The MB91470/480 series is Fujitsu's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed processing performance.

This series uses the FR60 CPU, which is compatible with the FR* family of CPUs.

* : FR is a line of products of FUJITSU MICROELECTRONICS Limited.

■ FEATURES

- FR60 CPU
 - 32-bit RISC, load/store architecture, five-stage pipeline
 - Operating frequency of 80 MHz (PLL clock multiplied)
 - 16-bit fixed-length instructions (basic instructions)
 - Instruction execution speed : one instruction per cycle
 - Memory-to-memory transfer, bit processing, barrel shift instructions, etc. : instructions suitable for embedded applications
 - Function entry and exit instructions, multi load/store instructions of register contents : instructions compatible with C language.
 - Register interlock function to facilitate assembly-language coding
 - Built-in multiplier/instruction-level support
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
 - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
 - Harvard architecture allowing program access and data access to be executed simultaneously
 - Instructions compatible with the FR family

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Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page
URL:<http://edevic.fujitsu.com/micom/en-support/>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

MB91470/480 Series

- Built-in Peripheral functions
 - Combinations of built-in Flash/ROM and RAM capacities

	MB91470 series		MB91480 series	
	144 pins		100 pins	
	Flash memory product	MASK ROM product	Flash memory product	MASK ROM product
256 Kbytes/16 Kbytes	MB91F475	—	MB91F482	MB91482
384 Kbytes/24 Kbytes	MB91F478	—	—	—
512 Kbytes/32 Kbytes	MB91F479	—	MB91F487	—

- I/O ports
- NMI (Non Maskable Interrupt)
- External interrupts
- Bit search module (for REALOS)

Function to search for the position of the first bit that has changed from 1 to 0 in a word starting from the MSB
- 16-bit reload timers
- Timing generator
- 8/16-bit PPG timers
- Multi-function timer
 - 16-bit free-run timer
 - Input capture (Linked to free-run timer)
 - Output compare (Linked to free-run timer)
 - A/D start up compare (Linked to free-run timer)
 - Wave form generator

Various wave forms are generated by using output compare output, 16-bit PPG timer and 16-bit dead timer.
- Base timer

Only one timer function can be selected from the 16-bit PWM timer, 16-bit PPG timer, 16/32-bit reload timer, and 16/32-bit PWC timer.
- 8/16-bit up/down counter
- Multi-function serial interface
 - Full-duplex double buffer
 - With 16-byte FIFO
 - Asynchronous (start-stop synchronization) communication, clock synchronous communication, I²C* standard mode (Max 100 kbps), I²C high-speed mode (selectable various modes at maximum of 400 kbps)
 - Selectable parity On/Off
 - Each channel has built-in baud rate generator
 - Error detection function for parity, frame and overrun errors
 - External clock can be used as transfer clock
 - With I²C function
- 8/10-bit A/D Converter (Successive comparison type)
 - Resolution : 8-bit or 10-bit resolution selectable
 - Conversion time : 1.2 μs (minimum conversion time for 33 MHz peripheral clock (CLKP))
1.2 μs (minimum conversion time for 40 MHz peripheral clock (CLKP))

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- 12-bit A/D Converter (successive approximation type)
 - Resolution : 12 bits
 - Conversion Time : 2.0 μ s (minimum conversion time for 33 MHz peripheral clock (CLKP))
2.2 μ s (minimum conversion time for 40 MHz peripheral clock (CLKP))
 - Differential input mode is available.
- Clock monitor
 - Peripheral clock (CLKP) divided by 2/4/8/16/32/64/128/256 can be output.
- Multiplication and Addition Calculator
 - RAM : Instruction RAM (I-RAM) 256 $\times$ 16-bit
Factor RAM (X-RAM) 64 $\times$ 32-bit
Variable RAM (Y-RAM) 64 $\times$ 32-bit
 - High-speed multiplication and addition (seven-stage pipeline processing)
 - Product addition (32-bit $\times$ 32-bit + 72-bit)
 - Operation result is extracted rounded from 72 bits to 32 bits or 72-bit result data reading.
- DMAC (DMA Controller)
 - Transfers can be started by software or by interrupts from the built-in peripherals.
- Wild register
 - Instructions or data located at a target address can be replaced (in the built-in Flash/ROM area only) .
- External bus interface
 - Maximum operating frequency of 40 MHz
 - 16-bit address full output (64 Kbytes space) capability
 - 8/16-bit data output
 - Use of unused data/address pins as general-purpose I/O ports
 - Totally independent 3-area chip select outputs that can be set at minimum of 64 Kbytes.
 - Support of interface for various memory (SRAM, ROM/Flash)
 - Basic bus cycle : 2 cycles
 - Automatic wait cycle generator that can be programmed for each area and can insert waits
 - External wait cycle using RDY input
- Other Features
 - Watchdog timer
 - Low-power consumption modes
 - Sleep/stop function
 - CMOS technologies : 0.18 μ m
 - Power supply : Single power supply (V_{CC} = 4.0 V to 5.5 V)

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

MB91470/480 Series

■ PRODUCT LINEUP

Characteristics	MB91470/480 series common EVA	MB91470 series			MB91480 series	
	MB91FV470	MB91F475	MB91F478	MB91F479	MB91F487	MB91F482 MB91482
Pin number	224 pins	144 pins			100 pins	
Built-in Flash/ROM capacity	512 Kbytes (Flash)	256 Kbytes (Flash)	384 Kbytes (Flash)	512 Kbytes (Flash)	512 Kbytes (Flash)	256 Kbytes (Flash/ROM)
Built-in RAM capacity	40 Kbytes	16 Kbytes	24 Kbytes	32 Kbytes	32 Kbytes	16 Kbytes
External bus	Yes	Yes			—	
I/O ports	160	113			77	
External interrupts	NMI 16 channels	NMI 10 channels			NMI 10 channels	
Reload timer	2 channels	2 channels			2 channels	
Timing generator	2 units	1 unit			2 units	
PPG	8-bit × 16 channels 16-bit × 8 channels	8-bit × 8 channels 16-bit × 4 channels			8-bit × 16 channels 16-bit × 8 channels	
Multi-function timer	2 units	1 unit			2 units	
Free-run timer	6 channels	3 channels			6 channels	
OCU	12 channels	6 channels			12 channels	
ICU	8 channels	4 channels			8 channels	
A/D activation compare	6 channels	3 channels			6 channels	
Wave form generator	12 channels	6 channels			12 channels	
Base timer	6 channels	4 channels			4 channels	
Up/down counter	2 channels	1 channel			—	
Multi-function serial interface	6 units	6 units			3 units	
8/10-bit A/D converter	4 channels × 2 units 16 channels × 1 unit	12 channels × 1 unit			4 channels × 2 units 10 channels × 1 unit	
12-bit A/D converter	4 channels × 2 units	4 channels × 2 units			—	
Clock monitor	1 unit	—			1 unit	
Multiplication and addition calculator	1 unit	1 unit			1 unit	
DMAC	5 channels	5 channels			5 channels	
Wild register	16 channels	16 channels			16 channels	
Debug function	DSU4	—			—	

MB91470/480 Series

■ PACKAGE AND CORRESPONDING PRODUCTS

Series name Package	MB91470 series	MB91480 series	
	MB91F475 MB91F478 MB91F479	MB91F482 MB91F487	MB91482
FPT-100P-M20 (LQFP-0.50 mm)	—	○	○
FPT-144P-M12 (LQFP-0.40 mm)	○	—	—
BGA-144P-M06 (PFBGA-0.80 mm)	○	—	—

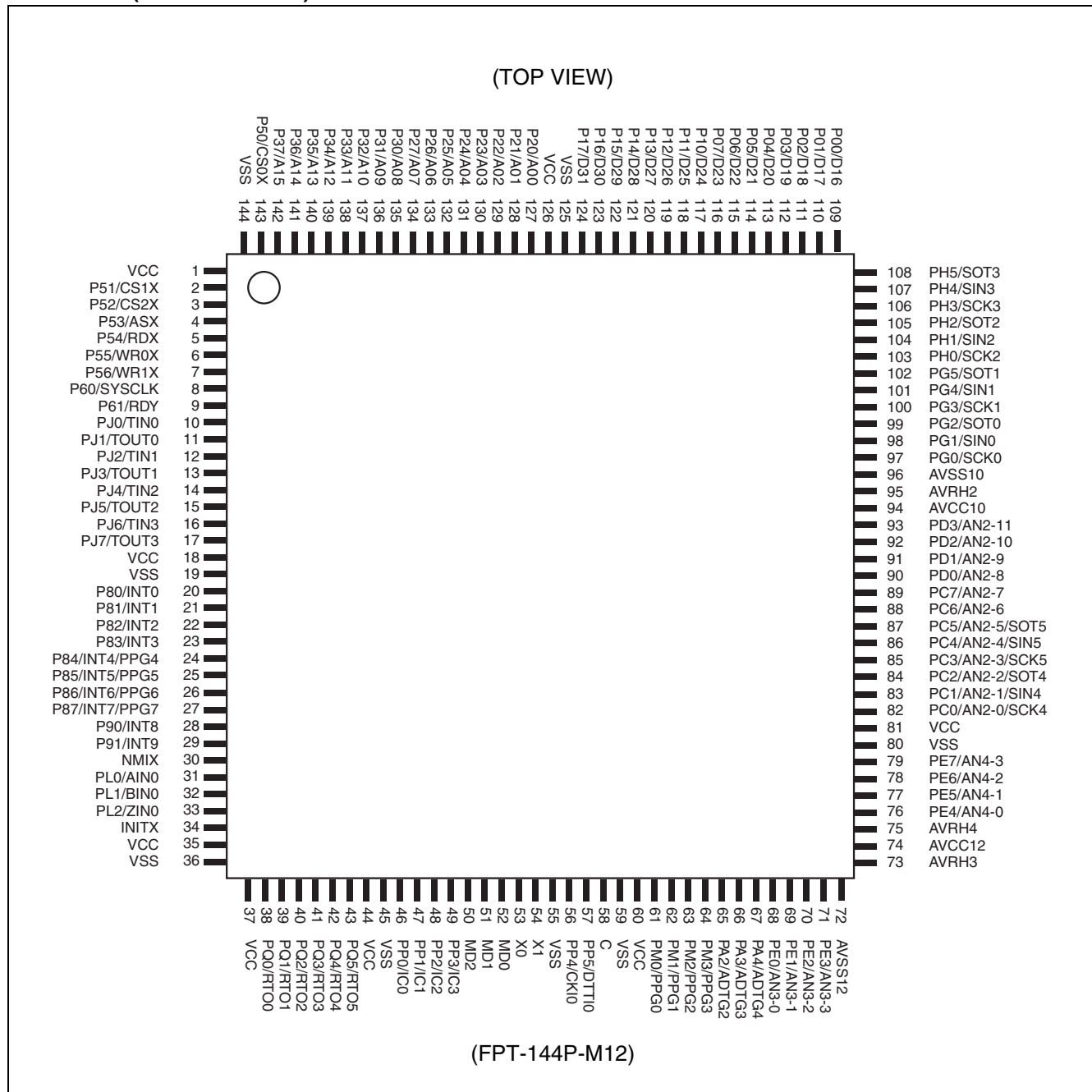
○ : Supported

Note : For details of each package, refer to “■ PACKAGE DIMENSIONS”.

MB91470/480 Series

■ PIN ASSIGNMENT

• LQFP-144 (MB91470 series)



MB91470/480 Series

• PFBGA-144 (MB91470 series)

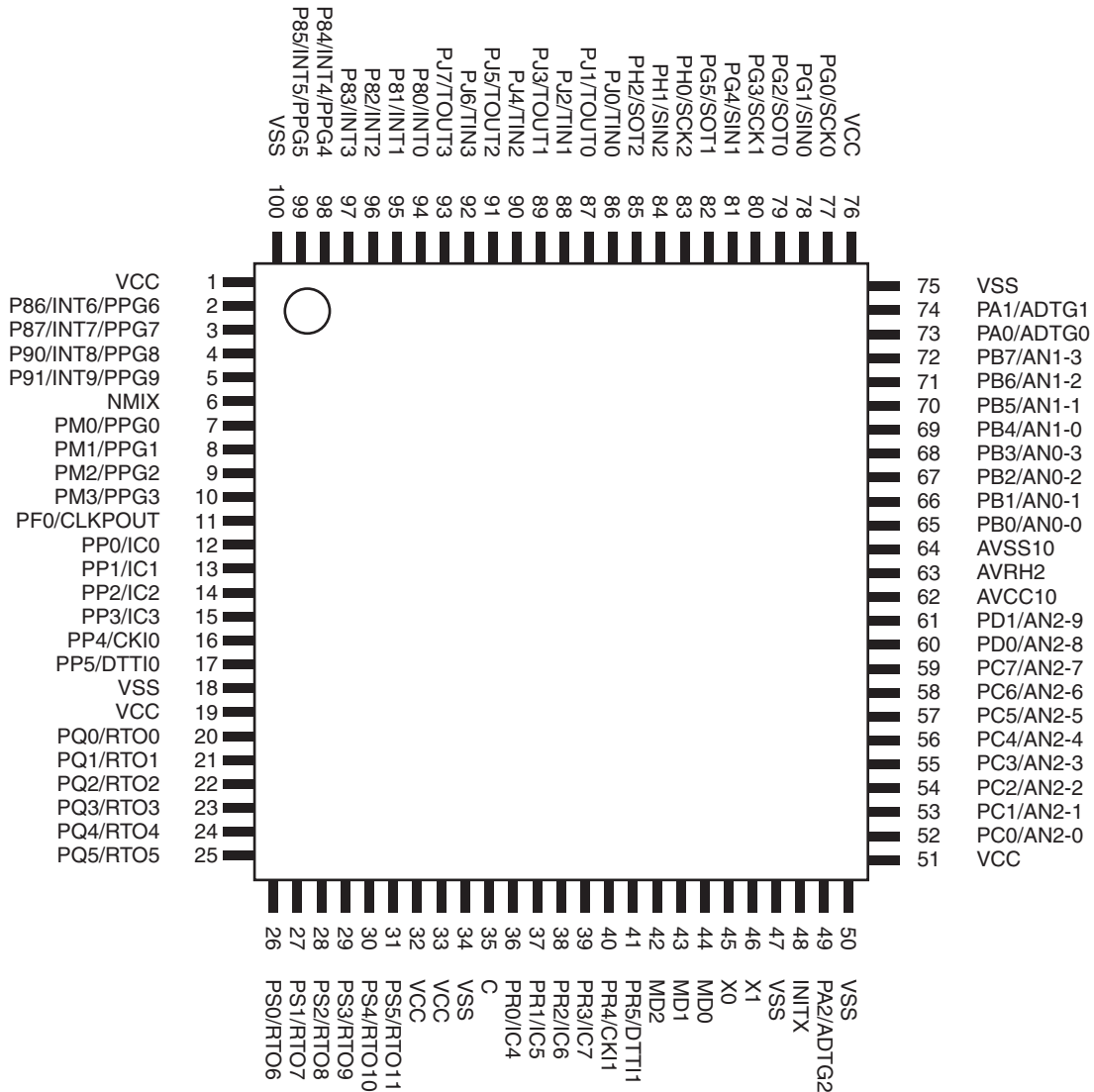
▼ Index	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	1	48	47	46	45	44	43	42	41	40	39	38	37	A
B	2	49	88	87	86	85	84	83	82	81	80	79	36	B
C	3	50	89	120	119	118	117	116	115	114	113	78	35	C
D	4	51	90	121	144	143	142	141	140	139	112	77	34	D
E	5	52	91	122						138	111	76	33	E
F	6	53	92	123						137	110	75	32	F
G	7	54	93	124						136	109	74	31	G
H	8	55	94	125						135	108	73	30	H
J	9	56	95	126						134	107	72	29	J
K	10	57	96	127	128	129	130	131	132	133	106	71	28	K
L	11	58	97	98	99	100	101	102	103	104	105	70	27	L
M	12	59	60	61	62	63	64	65	66	67	68	69	26	M
N	13	14	15	16	17	18	19	20	21	22	23	24	25	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

(BGA-144P-M06)

MB91470/480 Series

• LQFP-100 (MB91480 series)

(TOP VIEW)



(FPT-100P-M20)

MB91470/480 Series

■ PIN DESCRIPTIONS

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
50	M6	42	MD2	H, K	Mode pin 2 This pin sets the basic operating mode. Connect this pin to either VCC pin or VSS pin. Use circuit type K on the Flash memory model.
51	N6	43	MD1	H, K	Mode pin 1 This pin sets the basic operating mode. Connect this pin to either VCC pin or VSS pin. Use circuit type K on the Flash memory model.
52	K5	44	MD0	H, K	Mode pin 0 This pin sets the basic operating mode. Connect this pin to either VCC pin or VSS pin. Use circuit type K on the Flash memory model.
53	L6	45	X0	A	Clock (oscillation) input
54	K6	46	X1	A	Clock (oscillation) output
34	L1	48	INITX	I	External reset input
30	J4	6	NMIX	H	NMI (Non Maskable Interrupt) input
109	A12	—	D16	C	Bit 16 of external data bus I/O pin
			P00		General-purpose I/O port
110	B12	—	D17	C	Bit 17 of external data bus I/O pin
			P01		General-purpose I/O port
111	A11	—	D18	C	Bit 18 of external data bus I/O pin
			P02		General-purpose I/O port
112	B11	—	D19	C	Bit 19 of external data bus I/O pin
			P03		General-purpose I/O port
113	C12	—	D20	C	Bit 20 of external data bus I/O pin
			P04		General-purpose I/O port
114	B10	—	D21	C	Bit 21 of external data bus I/O pin
			P05		General-purpose I/O port
115	A10	—	D22	C	Bit 22 of external data bus I/O pin
			P06		General-purpose I/O port
116	C11	—	D23	C	Bit 23 of external data bus I/O pin
			P07		General-purpose I/O port
117	C10	—	D24	C	Bit 24 of external data bus I/O pin
			P10		General-purpose I/O port

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MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
118	B9	—	D25	C	Bit 25 of external data bus I/O pin
			P11		General-purpose I/O port
119	A9	—	D26	C	Bit 26 of external data bus I/O pin
			P12		General-purpose I/O port
120	D10	—	D27	C	Bit 27 of external data bus I/O pin
			P13		General-purpose I/O port
121	C9	—	D28	C	Bit 28 of external data bus I/O pin
			P14		General-purpose I/O port
122	B8	—	D29	C	Bit 29 of external data bus I/O pin
			P15		General-purpose I/O port
123	A8	—	D30	C	Bit 30 of external data bus I/O pin
			P16		General-purpose I/O port
124	D9	—	D31	C	Bit 31 of external data bus I/O pin
			P17		General-purpose I/O port
127	A7	—	A00	C	Bit 0 of external address bus output pin
			P20		General-purpose I/O port
128	B7	—	A01	C	Bit 1 of external address bus output pin
			P21		General-purpose I/O port
129	C7	—	A02	C	Bit 2 of external address bus output pin
			P22		General-purpose I/O port
130	D7	—	A03	C	Bit 3 of external address bus output pin
			P23		General-purpose I/O port
131	A6	—	A04	C	Bit 4 of external address bus output pin
			P24		General-purpose I/O port
132	B6	—	A05	C	Bit 5 of external address bus output pin
			P25		General-purpose I/O port
133	C6	—	A06	C	Bit 6 of external address bus output pin
			P26		General-purpose I/O port
134	D6	—	A07	C	Bit 7 of external address bus output pin
			P27		General-purpose I/O port
135	A5	—	A08	C	Bit 8 of external address bus output pin
			P30		General-purpose I/O port

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MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
136	B5	—	A09	C	Bit 9 of external address bus output pin
			P31		General-purpose I/O port
137	C5	—	A10	C	Bit 10 of external address bus output pin
			P32		General-purpose I/O port
138	D5	—	A11	C	Bit 11 of external address bus output pin
			P33		General-purpose I/O port
139	A4	—	A12	C	Bit 12 of external address bus output pin
			P34		General-purpose I/O port
140	B4	—	A13	C	Bit 13 of external address bus output pin
			P35		General-purpose I/O port
141	C4	—	A14	C	Bit 14 of external address bus output pin
			P36		General-purpose I/O port
142	A3	—	A15	C	Bit 15 of external address bus output pin
			P37		General-purpose I/O port
143	A2	—	CS0X	C	External chip select 0 output
			P50		General-purpose I/O port
2	B2	—	CS1X	C	External chip select 1 output
			P51		General-purpose I/O port
3	C1	—	CS2X	C	External chip select 2 output
			P52		General-purpose I/O port
4	C2	—	ASX	C	External address strobe output
			P53		General-purpose I/O port
5	B3	—	RDX	C	External read strobe output
			P54		General-purpose I/O port
6	D2	—	WR0X	C	External write strobe output Corresponding to bit 31 to bit 24 of external data bus I/O
			P55		General-purpose I/O port
7	D1	—	WR1X	C	External write strobe output Corresponding to bit 23 to bit 16 of external data bus I/O
			P56		General-purpose I/O port
8	C3	—	SYSCLK	C	External clock output
			P60		General-purpose I/O port

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MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
9	D3	—	RDY	C	External ready input
			P61		General-purpose I/O port
20	G2	94	INT0	D	External interrupt 0 input
			P80		General-purpose I/O port
21	G3	95	INT1	D	External interrupt 1 input
			P81		General-purpose I/O port
22	G4	96	INT2	D	External interrupt 2 input
			P82		General-purpose I/O port
23	H1	97	INT3	D	External interrupt 3 input
			P83		General-purpose I/O port
24	H2	98	INT4	D	External interrupt 4 input
			PPG4		Output of PPG timer 4
			P84		General-purpose I/O port
25	H3	99	INT5	D	External interrupt 5 input
			PPG5		Output of PPG timer 5
			P85		General-purpose I/O port
26	H4	2	INT6	D	External interrupt 6 input
			PPG6		Output of PPG timer 6
			P86		General-purpose I/O port
27	J1	3	INT7	D	External interrupt 7 input
			PPG7		Output of PPG timer 7
			P87		General-purpose I/O port
28	J2	4	INT8	D	External interrupt 8 input
			PPG8		Output of PPG timer 8
			P90		General-purpose I/O port
29	J3	5	INT9	D	External interrupt 9 input
			PPG9		Output of PPG timer 9
			P91		General-purpose I/O port
—	—	—	INT10	D	External interrupt 10 input
			PPG10		Output of PPG timer 10
			P92		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
—	—	—	INT11	D	External interrupt 11 input
			PPG11		Output of PPG timer 11
			P93		General-purpose I/O port
—	—	—	INT12	D	External interrupt 12 input
			PPG12		Output of PPG timer 12
			P94		General-purpose I/O port
—	—	—	INT13	D	External interrupt 13 input
			PPG13		Output of PPG timer 13
			P95		General-purpose I/O port
—	—	—	INT14	D	External interrupt 14 input
			PPG14		Output of PPG timer 14
			P96		General-purpose I/O port
—	—	—	INT15	D	External interrupt 15 input
			PPG15		Output of PPG timer 15
			P97		General-purpose I/O port
—	—	73	ADTG0	D	External trigger input of 8/10-bit A/D converter 0
			PA0		General-purpose I/O port
—	—	74	ADTG1	D	External trigger input of 8/10-bit A/D converter 1
			PA1		General-purpose I/O port
65	L9	49	ADTG2	D	External trigger input of 8/10-bit A/D converter 2
			PA2		General-purpose I/O port
66	K9	—	ADTG3	D	External trigger input of 12-bit A/D converter 3
			PA3		General-purpose I/O port
67	N10	—	ADTG4	D	External trigger input of 12-bit A/D converter 4
			PA4		General-purpose I/O port
—	—	65	AN0-0	G	Analog 0 input of 8/10-bit A/D converter 0
			PB0		General-purpose I/O port
—	—	66	AN0-1	G	Analog 1 input of 8/10-bit A/D converter 0
			PB1		General-purpose I/O port
—	—	67	AN0-2	G	Analog 2 input of 8/10-bit A/D converter 0
			PB2		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
—	—	68	AN0-3	G	Analog 3 input of 8/10-bit A/D converter 0
			PB3		General-purpose I/O port
—	—	69	AN1-0	G	Analog 0 input of 8/10-bit A/D converter 1
			PB4		General-purpose I/O port
—	—	70	AN1-1	G	Analog 1 input of 8/10-bit A/D converter 1
			PB5		General-purpose I/O port
—	—	71	AN1-2	G	Analog 2 input of 8/10-bit A/D converter 1
			PB6		General-purpose I/O port
—	—	72	AN1-3	G	Analog 3 input of 8/10-bit A/D converter 1
			PB7		General-purpose I/O port
82	J12	52	AN2-0	G	Analog 0 input of 8/10-bit A/D converter 2
			SCK4 (SCL4)		Clock I/O of multi-function serial interface 4 (used in I ² C mode, SCL4)
			PC0		General-purpose I/O port
83	J13	53	AN2-1	G	Analog 1 input of 8/10-bit A/D converter 2
			SIN4		Data input of multi-function serial interface 4 (not used in I ² C mode)
			PC1		General-purpose I/O port
84	K10	54	AN2-2	G	Analog 2 input of 8/10-bit A/D converter 2
			SOT4 (SDA4)		Data output of multi-function serial interface 4 (used in I ² C mode, SDA4)
			PC2		General-purpose I/O port
85	J11	55	AN2-3	G	Analog 3 input of 8/10-bit A/D converter 2
			SCK5 (SCL5)		Clock I/O of multi-function serial interface 5 (used in I ² C mode, SCL5)
			PC3		General-purpose I/O port
86	H12	56	AN2-4	G	Analog 4 input of 8/10-bit A/D converter 2
			SIN5		Data input of multi-function serial interface 5 (not used in I ² C mode)
			PC4		General-purpose I/O port
87	H13	57	AN2-5	G	Analog 5 input of 8/10-bit A/D converter 2
			SOT5 (SDA5)		Data output of multi-function serial interface 5 (used in I ² C mode, SDA5)
			PC5		General-purpose I/O port
88	J10	58	AN2-6	G	Analog 6 input of 8/10-bit A/D converter 2
			PC6		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
89	H11	59	AN2-7	G	Analog 7 input of 8/10-bit A/D converter 2
			PC7		General-purpose I/O port
90	H10	60	AN2-8	G	Analog 8 input of 8/10-bit A/D converter 2
			PD0		General-purpose I/O port
91	G13	61	AN2-9	G	Analog 9 input of 8/10-bit A/D converter 2
			PD1		General-purpose I/O port
92	G12	—	AN2-10	G	Analog 10 input of 8/10-bit A/D converter 2
			PD2		General-purpose I/O port
93	G11	—	AN2-11	G	Analog 11 input of 8/10-bit A/D converter 2
			PD3		General-purpose I/O port
68	M10	—	AN3-0/ AN3-0P	G	12-bit A/D converter 3 analog 0 input (in single input mode) 12-bit A/D converter 3 analog 0 (+) side input (in differential input mode)
			PE0		General-purpose I/O port
69	L10	—	AN3-1/ AN3-0N	G	12-bit A/D converter 3 analog 1 input (in single input mode) 12-bit A/D converter 3 analog 0 (–) side input (in differential input mode)
			PE1		General-purpose I/O port
70	N11	—	AN3-2/ AN3-1P	G	12-bit A/D converter 3 analog 2 input (in single input mode) 12-bit A/D converter 3 analog 1 (+) side input (in differential input mode)
			PE2		General-purpose I/O port
71	N12	—	AN3-3/ AN3-1N	G	12-bit A/D converter 3 analog 3 input (in single input mode) 12-bit A/D converter 3 analog 1 (–) side input (in differential input mode)
			PE3		General-purpose I/O port
76	L12	—	AN4-0/ AN4-0P	G	12-bit A/D converter 4 analog 0 input (in single input mode) 12-bit A/D converter 4 analog 0 (+) side input (in differential input mode)
			PE4		General-purpose I/O port
77	M11	—	AN4-1/ AN4-0N	G	12-bit A/D converter 4 analog 1 input (in single input mode) 12-bit A/D converter 4 analog 0 (–) side input (in differential input mode)
			PE5		General-purpose I/O port

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MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
78	K12	—	AN4-2/ AN4-1P	G	12-bit A/D converter 4 analog 2 input (in single input mode) 12-bit A/D converter 4 analog 1 (+) side input (in differential input mode)
			PE6		General-purpose I/O port
79	K13	—	AN4-3/ AN4-1N	G	12-bit A/D converter 4 analog 3 input (in single input mode) 12-bit A/D converter 4 analog 1 (-) side input (in differential input mode)
			PE7		General-purpose I/O port
—	—	11	CLK- POUT	D	Clock monitor output
			PF0		General-purpose I/O port
—	—	—	PF1	D	General-purpose I/O port
—	—	—	PF2	D	General-purpose I/O port
—	—	—	PF3	D	General-purpose I/O port
—	—	—	PF4	D	General-purpose I/O port
—	—	—	PF5	D	General-purpose I/O port
—	—	—	PF6	D	General-purpose I/O port
—	—	—	PF7	D	General-purpose I/O port
97	F11	77	SCK0 (SCL0)	D	Clock I/O of multi-function serial interface 0 (used in I ² C mode, SCL0)
			PG0		General-purpose I/O port
98	F10	78	SIN0	D	Data input of multi-function serial interface 0 (not used in I ² C mode)
			PG1		General-purpose I/O port
99	E13	79	SOT0 (SDA0)	D	Data output of multi-function serial interface 0 (used in I ² C mode, SDA0)
			PG2		General-purpose I/O port
100	E12	80	SCK1 (SCL1)	D	Clock I/O of multi-function serial interface 1 (used in I ² C mode, SCL1)
			PG3		General-purpose I/O port
101	E11	81	SIN1	D	Data input of multi-function serial interface 1 (not used in I ² C mode)
			PG4		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
102	E10	82	SOT1 (SDA1)	D	Data output of multi-function serial interface 1 (used in I ² C mode, SDA1)
			PG5		General-purpose I/O port
103	D13	83	SCK2 (SCL2)	D	Clock I/O of multi-function serial interface 2 (used in I ² C mode, SCL2)
			PH0		General-purpose I/O port
104	D12	84	SIN2	D	Data input of multi-function serial interface 2 (not used in I ² C mode)
			PH1		General-purpose I/O port
105	D11	85	SOT2 (SDA2)	D	Data output of multi-function serial interface 2 (used in I ² C mode, SDA2)
			PH2		General-purpose I/O port
106	C13	—	SCK3 (SCL3)	D	Clock I/O of multi-function serial interface 3 (used in I ² C mode, SCL3)
			PH3		General-purpose I/O port
107	B13	—	SIN3	D	Data input of multi-function serial interface 3 (not used in I ² C mode)
			PH4		General-purpose I/O port
108	A13	—	SOT3 (SDA3)	D	Data output of multi-function serial interface 3 (used in I ² C mode, SDA3)
			PH5		General-purpose I/O port
10	E2	86	TIN0	D	Base timer 0 input
			PJ0		General-purpose I/O port
11	E1	87	TOUT0	D	Base timer 0 output
			PJ1		General-purpose I/O port
12	D4	88	TIN1	D	Base timer 1 input
			PJ2		General-purpose I/O port
13	E3	89	TOUT1	D	Base timer 1 output
			PJ3		General-purpose I/O port
14	F2	90	TIN2	D	Base timer 2 input
			PJ4		General-purpose I/O port
15	F1	91	TOUT2	D	Base timer 2 output
			PJ5		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
16	E4	92	TIN3	D	Base timer 3 input
			PJ6		General-purpose I/O port
17	F3	93	TOUT3	D	Base timer 3 output
			PJ7		General-purpose I/O port
31	K1	—	AIN0	D	8/16-bit up count input pin for up/down counter 0
			PL0		General-purpose I/O port
32	K2	—	BIN0	D	8/16-bit down count input pin for up/down counter 0
			PL1		General-purpose I/O port
33	K3	—	ZIN0	D	8/16-bit reset input pin for up/down counter 0
			PL2		General-purpose I/O port
61	L8	7	PPG0	D	Output of PPG timer 0
			PM0		General-purpose I/O port
62	K8	8	PPG1	D	Output of PPG timer 1
			PM1		General-purpose I/O port
63	N9	9	PPG2	D	Output of PPG timer 2
			PM2		General-purpose I/O port
64	M9	10	PPG3	D	Output of PPG timer 3
			PM3		General-purpose I/O port
46	M5	12	IC0	D	Trigger input of input capture 0
			PP0		General-purpose I/O port
47	N5	13	IC1	D	Trigger input of input capture 1
			PP1		General-purpose I/O port
48	K4	14	IC2	D	Trigger input of input capture 2
			PP2		General-purpose I/O port
49	L5	15	IC3	D	Trigger input of input capture 3
			PP3		General-purpose I/O port
56	M7	16	CKI0	D	External clock input pin of free-run timer ch.0 to ch.2
			PP4		General-purpose I/O port
57	L7	17	DTTI0	D	Input signal controlling wave form generator outputs RTO0 to RTO5 of multi-function timer 0
			PP5		General-purpose I/O port

(Continued)

MB91470/480 Series

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
38	M2	20	RTO0	J	Wave form generator output of multi-function timer 0
			PQ0		General-purpose I/O port
39	N3	21	RTO1	J	Wave form generator output of multi-function timer 0
			PQ1		General-purpose I/O port
40	M3	22	RTO2	J	Wave form generator output of multi-function timer 0
			PQ2		General-purpose I/O port
41	L2	23	RTO3	J	Wave form generator output of multi-function timer 0
			PQ3		General-purpose I/O port
42	M4	24	RTO4	J	Wave form generator output of multi-function timer 0
			PQ4		General-purpose I/O port
43	N4	25	RTO5	J	Wave form generator output of multi-function timer 0
			PQ5		General-purpose I/O port
—	—	36	IC4	D	Trigger input of input capture 4
			PR0		General-purpose I/O port
—	—	37	IC5	D	Trigger input of input capture 5
			PR1		General-purpose I/O port
—	—	38	IC6	D	Trigger input of input capture 6
			PR2		General-purpose I/O port
—	—	39	IC7	D	Trigger input of input capture 7
			PR3		General-purpose I/O port
—	—	40	CKI1	D	External clock input pin of free-run timer ch.3 to ch.5
			PR4		General-purpose I/O port
—	—	41	DTTI1	D	Input signal controlling wave form generator outputs RTO6 to RTO11 of multi-function timer 1
			PR5		General-purpose I/O port
—	—	26	RTO6	J	Wave form generator output of multi-function timer 1
			PS0		General-purpose I/O port
—	—	27	RTO7	J	Wave form generator output of multi-function timer 1
			PS1		General-purpose I/O port
—	—	28	RTO8	J	Wave form generator output of multi-function timer 1
			PS2		General-purpose I/O port

(Continued)

MB91470/480 Series

(Continued)

Pin no.			Pin name	I/O circuit type*4	Function
MB91470 series		MB91480 series			
LQFP-144*1	PFBGA-144*2	LQFP-100*3			
—	—	29	RTO9	J	Wave form generator output of multi-function timer 1
			PS3		General-purpose I/O port
—	—	30	RTO10	J	Wave form generator output of multi-function timer 1
			PS4		General-purpose I/O port
—	—	31	RTO11	J	Wave form generator output of multi-function timer 1
			PS5		General-purpose I/O port

*1 : FPT-144P-M12

*2 : BGA-144P-M06

*3 : FPT-100P-M20

*4 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

MB91470/480 Series

Power supply pins and GND pins

Pin number			Pin name	Function
MB91470 series		MB91480 series		
LQFP-144*1	PFBGA-144*2	LQFP-100*3		
1 18 35 37 44 60 81 126	B1 F4 M1 N2 L3 M8 K11 D8	— 1 19 32 33 51 76 —	VCC	Power supply pins Connect all pins to the same potential.
19 36 45 55 59 80 125 144	A1 G1 N1 L4 N7 N8 L11 C8	— 18 34 47 50 75 100 —	VSS	GND pins Connect all pins to the same potential.
58	K7	35	C	Capacitor coupling pin for internal regulator
94	G10	62	AVCC10	Analog power supply pin for 8/10-bit A/D converter 0/1/2
96	F12	64	AVSS10	Analog GND pin for 8/10-bit A/D converter
74	M12	—	AVCC12	Analog power supply pin for 12-bit A/D converter 3/4
72	N13	—	AVSS12	Analog GND pin for 12-bit A/D converter 3/4
—	—	—	AVRH0	Analog reference power supply pin for 8/10-bit A/D converter 0
—	—	—	AVRH1	Analog reference power supply pin for 8/10-bit A/D converter 1
95	F13	63	AVRH2	Analog reference power supply pin for 8/10-bit A/D converter 2
73	M13	—	AVRH3	Analog reference power supply pin for 12-bit A/D converter 3
75	L13	—	AVRH4	Analog reference power supply pin for 12-bit A/D converter 4

*1 : FPT-144P-M12

*2 : BGA-144P-M06

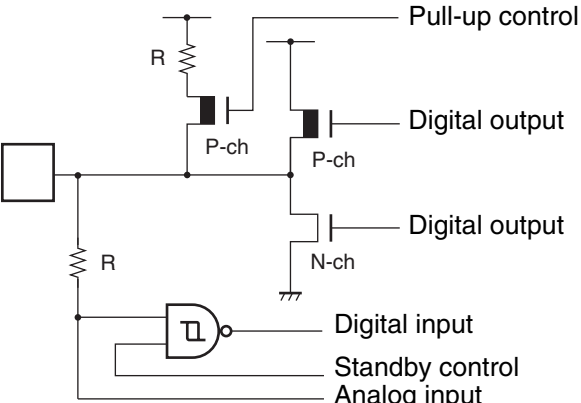
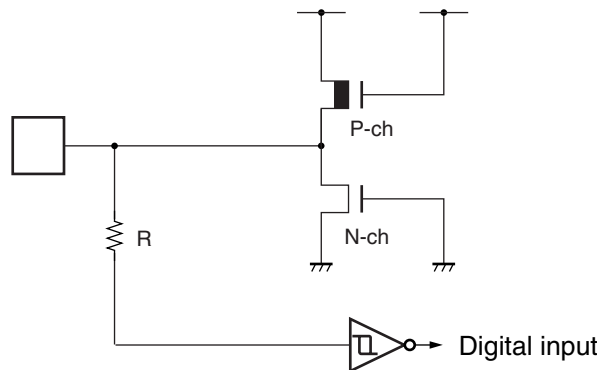
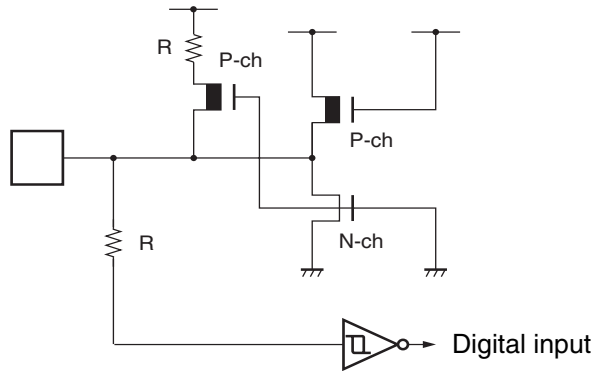
*3 : FPT-100P-M20

MB91470/480 Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	Standby control	Oscillation feedback resistance for high speed (main clock oscillation) approx. 1 MΩ
C	Pull-up control P-ch Digital output P-ch Digital output N-ch Standby control Digital input	• CMOS level output • CMOS level input • With standby control • With pull-up control
D	Pull-up control P-ch Digital output P-ch Digital output N-ch Standby control Digital input	• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control

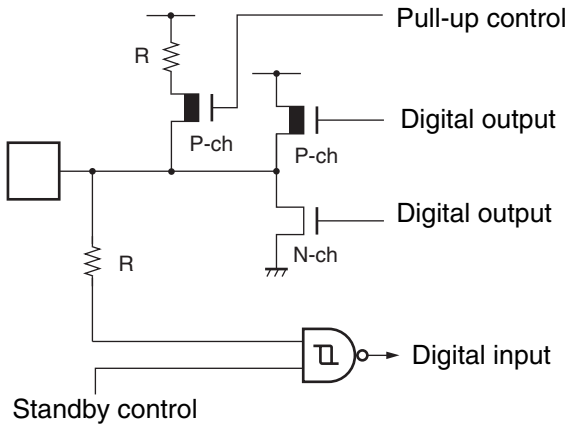
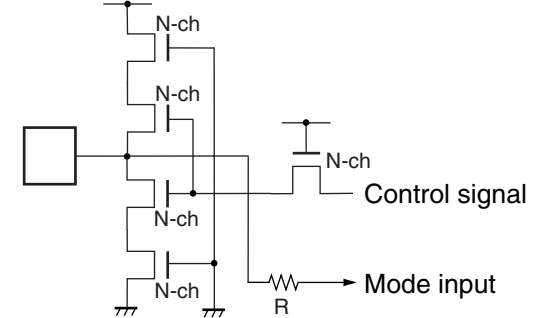
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Type	Circuit	Remarks
G		• Analog/CMOS level hysteresis I/O pin • CMOS level output • CMOS level hysteresis input (with standby control) • Analog input (Operates as an analog input when the corresponding AICR register bit is "1".) • With pull-up control
H		• CMOS level hysteresis input • Without standby control
I		• CMOS level hysteresis input • Without standby control • With pull-up resistance

(Continued)

MB91470/480 Series

(Continued)

Type	Circuit	Remarks
J		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control
K		Flash memory product only • CMOS level input • High voltage control for testing Flash memory

■ HANDLING DEVICES

- Preventing latch-up

Latch-up phenomenon may occur with CMOS IC, when a voltage higher than V_{CC} or lower than V_{SS} is applied to either the input or output terminals, or when a voltage is applied between V_{CC} pin and V_{SS} pin that exceeds the rated voltage. When latch-up occurs, a significant power-supply current surge results, which may damage some elements due to the excess heat, so great care must be taken to ensure that the maximum rating is never exceeded during use.

- Treatment of unused input pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- Power pins

In products with multiple V_{CC} and V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to the same potential power supply and a ground line externally to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance. It is also advisable to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} near this device.

- Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout. Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- About mode pins (MD0 to MD2)

These pins should be connected directly to V_{CC} pin or V_{SS} pin.

Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and power supply or GND pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Operation at start-up

Be sure to execute setting initialized reset (INIT) with INITX pin immediately after start-up.

Immediately after that, also, hold the "L"-level input to the INITX pin for the stabilization wait time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit and the stabilization wait time for the regulator (For INIT via the INITX pin, the oscillation stabilization wait time setting is initialized to the minimum value).

MB91470/480 Series

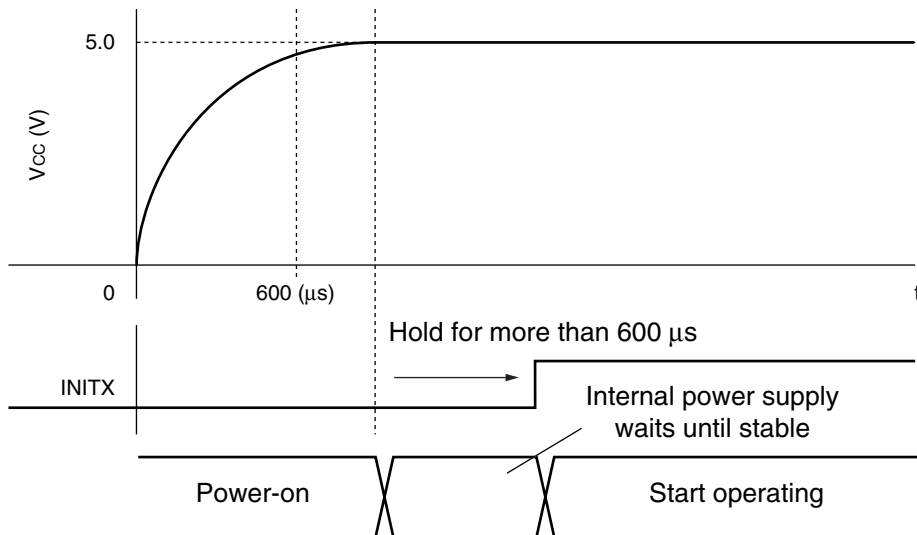
- Notes upon power-on sequence

It requires more than 600 μs (between 0.0 V to 5.0 V) to rise voltage upon power on in order to prevent the device malfunction caused by the overshooting in the built-in voltage step-down circuit.

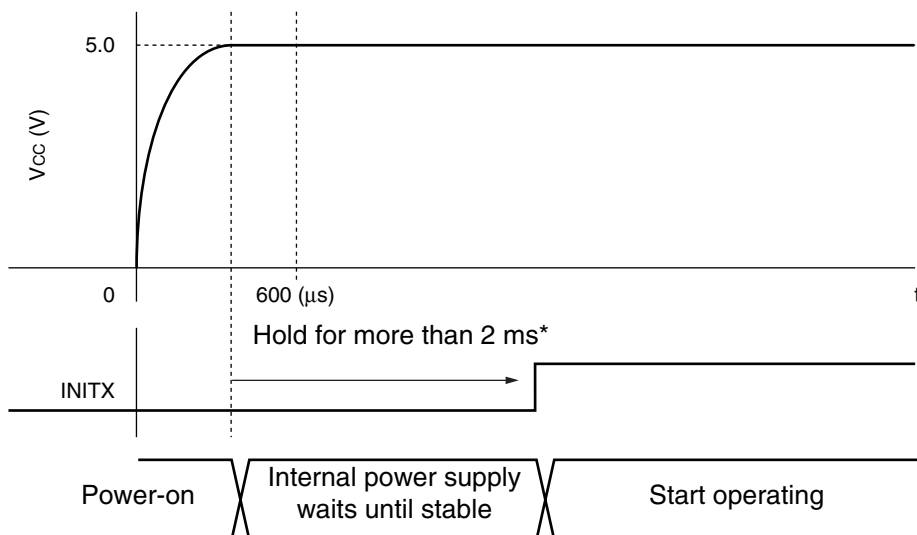
After the supply voltage is stable (voltage is risen) , it takes 600 μs until internal supply is stable. Hold the input to the INITX pin during that period.

If it takes less than 600 μs (between 0.0 V to 5.0 V) for power up, it requires 2 ms* until internal supply is stable after voltage supply is stable (voltage is risen) . Hold the input to the INITX pin during that period.

CASE : voltage rising time is more than 600 μs (0.0 V to 5.0 V)



CASE : voltage rising time is less than 600 μs (0.0 V to 5.0 V)



* : In case of which it takes less than 600 μs (between 0.0 V to 5.0 V) to rise voltage, the time to make internal power supply stable is proportional to the capacitance value of the bypass capacitor for the pin C. It takes 2 ms if the pin C = 4.7 μF ; 4 ms if the pin C = 9.4 μF .

- Order of power turning ON/OFF

Use the following procedure for turning the power on or off. If not using the A/D converter, connect $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$. Turn on the power supply in the sequence $V_{CC} \rightarrow AV_{CC} \rightarrow AVR_{H}$, and turn off the power in the reverse sequence.

- Source oscillation input when turning on the power

When turning the power on, maintain the clock input until the device is released from the oscillation stabilization wait state.

- Cautions for operation during PLL clock mode

Even if the oscillator comes off or the clock input stops with the PLL clock selected for MB91470/480 series, MB91470/480 series may continue to operate at the free-run frequency of the PLL's internal self-oscillating oscillator circuit.

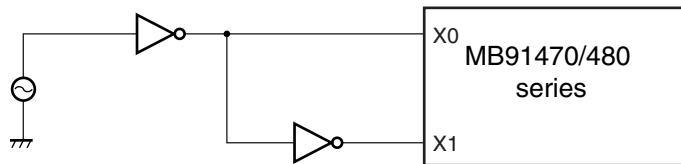
Performance of this operation, however, cannot be guaranteed.

- Using an external clock

When using an external clock, you must always input clock signals with opposite phase from X0 pin to X1 pin simultaneously. However, as the X1 pin halts with an output at the "H" level during stop mode, insert a resistor of approximately 1 k Ω externally to prevent a conflict between the two outputs if using stop mode (oscillation stop mode).

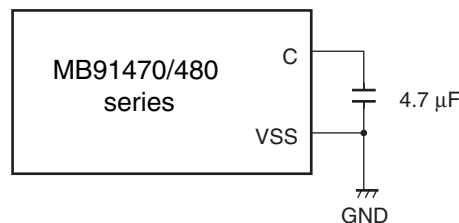
The figure below shows an example of how to use an external clock.

- Example of Using an External Clock



- C pin

As MB91470/480 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 μ F to the C pin for use by the regulator.



- Software reset on the synchronous mode

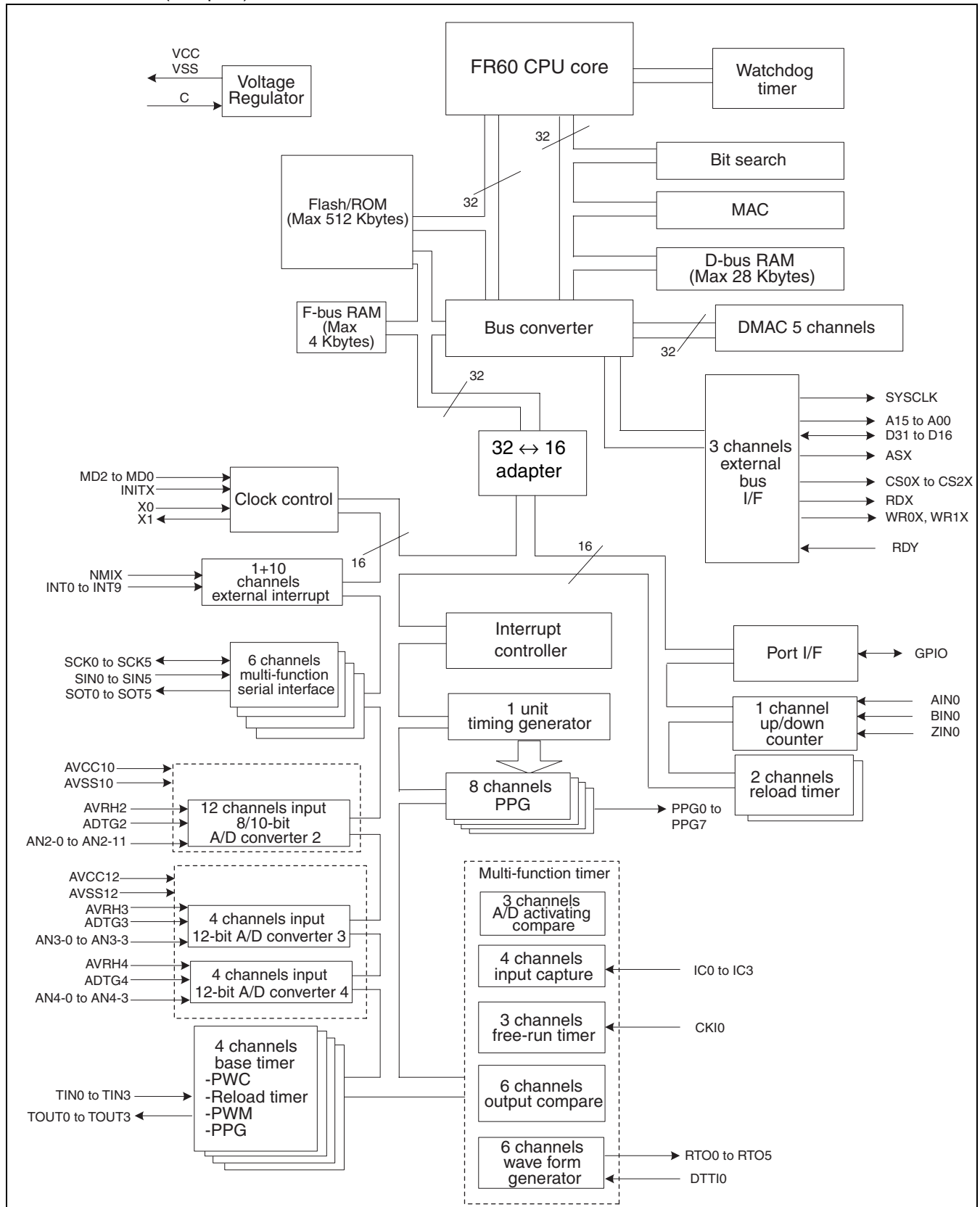
Be sure to meet the following two conditions before setting 0 to the SRST bit of STCR (standby control register) when the software reset is used on the synchronous mode.

- Set the interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0).
- Not used NMI

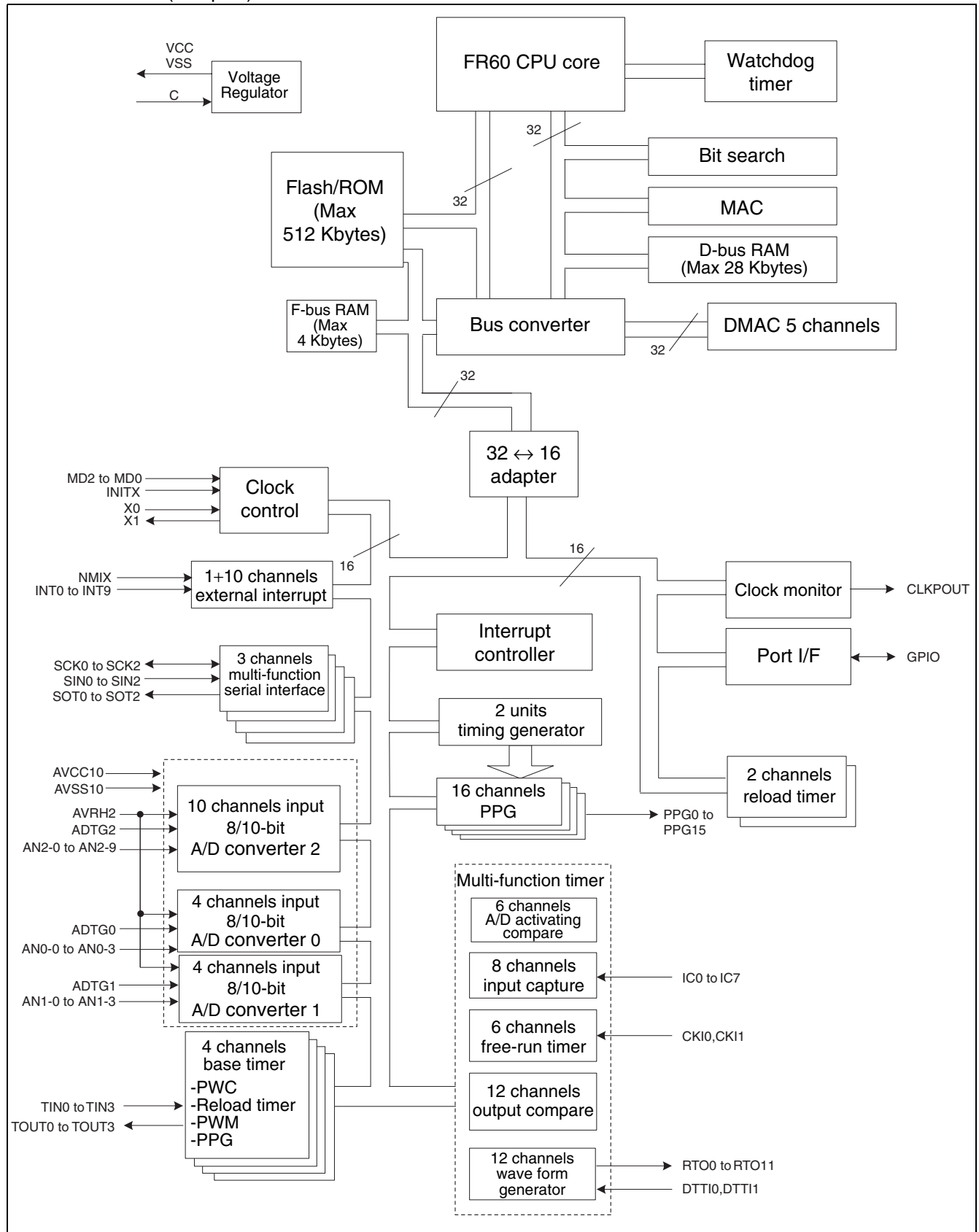
MB91470/480 Series

■ BLOCK DIAGRAM

•MB91470 series (144 pins)



• MB91480 series (100 pins)



MB91470/480 Series

■ MEMORY SPACE

1. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly by the instruction. The size of directly addressable areas depends on the length of the data being accessed as shown below.

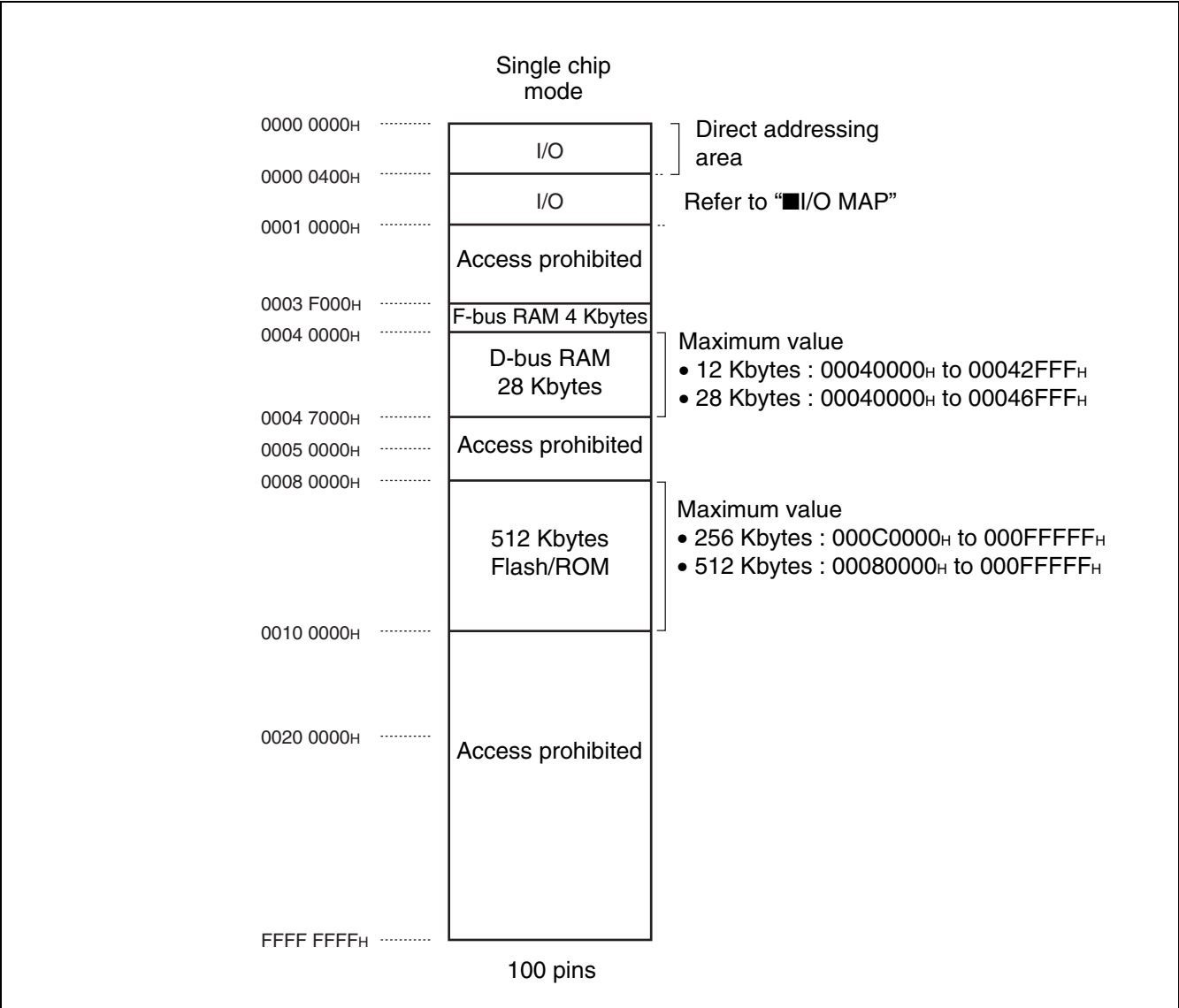
- byte data access : 000_H to 0FF_H
- half word data access : 000_H to 1FF_H
- word data access : 000_H to 3FF_H

2. Memory Map

• MB91470 series

	Single chip mode	Internal ROM external bus mode	External ROM external bus mode	
0000 0000 _H	I/O	I/O	I/O	Direct addressing area Refer to “■ I/O MAP”
0000 0400 _H	I/O	I/O	I/O	
0001 0000 _H	Access prohibited	Access prohibited	Access prohibited	
0003 F000 _H	F-bus RAM 4 Kbytes	F-bus RAM 4 Kbytes	F-bus RAM 4 Kbytes	Maximum value • 12 Kbytes : 00040000 _H to 00042FFF _H • 20 Kbytes : 00040000 _H to 00044FFF _H • 28 Kbytes : 00040000 _H to 00046FFF _H
0004 0000 _H	D-bus RAM 28 Kbytes	D-bus RAM 28 Kbytes	D-bus RAM 28 Kbytes	
0004 7000 _H	Access prohibited	Access prohibited	Access prohibited	
0005 0000 _H	512 Kbytes Flash/ROM	512 Kbytes Flash/ROM	External area	Maximum value • 256 Kbytes : 000C0000 _H to 000FFFFF _H • 384 Kbytes : 000A0000 _H to 000FFFFF _H • 512 Kbytes : 00080000 _H to 000FFFFF _H
0008 0000 _H				
0010 0000 _H				
0020 0000 _H	Access prohibited	External area	External area	
FFFF FFFF _H				
	144 pins	144 pins	144 pins	

•MB9480 series



MB91470/480 Series

■ MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and mode data to set the operation mode.

1. Mode Pins

The MD2 to MD0 pins specify how the mode vector fetch and reset vector fetch is performed. Settings other than those shown in the following table are prohibited.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	The bus width is set by mode register.

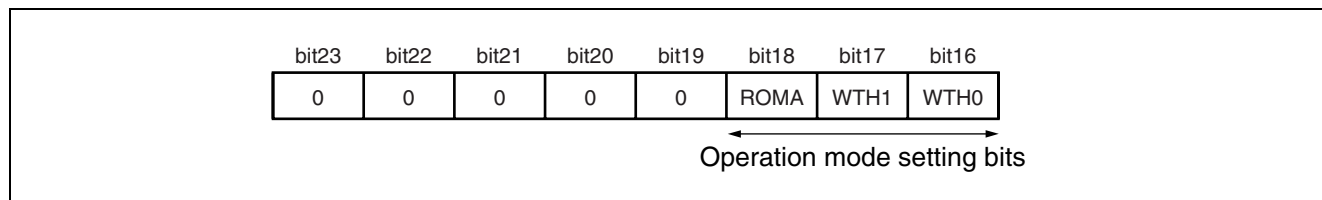
2. Mode data

The data that is written to the internal mode register (MODR) by the mode vector fetch is called mode data.

After the mode register is set, the device runs in the operating mode specified by this register.

The mode data is set by all of the reset sources. User programs cannot set the mode register.

<Details of mode data description>



[bit 23 to bit 19] Reserved bits

Be sure to set these bits to "00000_B".

Operation is not guaranteed if these bits are set to a value other than "00000_B".

[bit 18] ROMA (Internal Flash/ROM enable bit)

This bit configures whether the internal Flash/ROM area (8 0000_H to F FFFF_H) is enabled.

ROMA	Function	Remarks
0	External ROM mode	Internal Flash/ROM area (8 0000 _H to F FFFF _H) is used as an external area.
1	Internal ROM mode	Internal Flash/ROM area (8 0000 _H to F FFFF _H) is enabled.

[bit 17, bit 16] WTH1, WTH0 (Bus width specification bit)

These bits configure the bus width in external bus mode.

In external bus mode, this value is set to the DBW1 and DBW0 bits of AWR0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	—	(Setting prohibited)
1	1	Single chip mode	Single chip mode

3. Note

The mode data set in the mode vector must be stored as byte data at 0x000FFFF8_H. The data should be located in the highest byte from bit 31 to bit 24 because the FR family uses big endian byte ordering.

		bit 31	24 23	16 15	8 7	0
Incorrect	0x000FFFF8 _H	XXXXXXXX	XXXXXXXX	XXXXXXXX	Mode data	
Correct	0x000FFFF8 _H	Mode data	XXXXXXXX	XXXXXXXX	XXXXXXXX	
	0x000FFFFC _H	Reset vector				

MB91470/480 Series

■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port data register

Read/write attribute, Access unit
(B : byte, H : half word, W : word)

Initial value of register after reset

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 1...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Note : Initial values of register bits are represented as follows :

“ 1 ” : Initial Value “ 1 ”

“ 0 ” : Initial Value “ 0 ”

“ X ” : Initial Value “ undefined ”

“ - ” : No physical register at this location

Access to addresses where the data access properties have not been documented is prohibited.

MB91470/480 Series

Address	Register				Block
	+0	+1	+2	+3	
000000 _H	PDR0 [R/W] B, H, W XXXXXXXX	PDR1 [R/W] B, H, W XXXXXXXX	PDR2 [R/W] B, H, W XXXXXXXX	PDR3 [R/W] B, H, W XXXXXXXX	Port data register
000004 _H	PDR5 [R/W] B, H, W -XXXXXXXX	PDR6 [R/W] B, H, W -----XX	PDR8 [R/W] B, H, W XXXXXXXX	PDR9 [R/W] B, H, W XXXXXXXX	
000008 _H	PDRA [R/W] B, H, W ---XXXXX	PDRB [R/W] B, H, W XXXXXXXX	PDRC [R/W] B, H, W XXXXXXXX	PDRD [R/W] B, H, W ----XXXX	
00000C _H	PDRE [R/W] B, H, W XXXXXXXX	PDRF [R/W] B, H, W XXXXXXXX	PDRG [R/W] B, H, W --XXXXXX	PDRH [R/W] B, H, W --XXXXXX	
000010 _H	PDRJ [R/W] B, H, W XXXXXXXX	—	PDRL [R/W] B, H, W ----XXX	PDRM [R/W] B, H, W ----XXXX	
000014 _H	PDRP [R/W] B, H, W --XXXXXX	PDRQ [R/W] B, H, W --XXXXXX	PDRR [R/W] B, H, W --XXXXXX	PDRS [R/W] B, H, W --XXXXXX	
000018 _H to 00003C _H	—				(Reserved)
000040 _H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to INT7)
000044 _H	DICR [R/W] B, H, W -----0	HRCL [R/W, R] B, H, W 0--11111	—		Delay interrupt/ hold request
000048 _H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004C _H	—		TMCSR0 [R/W, R] B, H, W ----00-- ---00000		
000050 _H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054 _H	—		TMCSR1 [R/W, R] B, H, W ----00-- ---00000		
000058 _H to 00005C _H	—				(Reserved)

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000060 _H	SSR0 [R/W, R] B, H, W 00000011	ESCR0 [R/W]/ IBSR0 [R/W, R] B, H, W 00000000	SCR0 [R/W] / IBCR0 [R/W, R] B, H, W 00000000	SMR0 [R/W] B, H, W 000-0000	Multi- function serial interface 0
000064 _H	BGR01[R/W] B, H, W 00000000	BGR00 [R/W] B, H, W 00000000	RDR0 [R]/ TDR0 [W] H, W -----0 00000000		
000068 _H	—		ISMK0 [R/W] B, H, W 01111111	ISBA0 [R/W] B, H, W 00000000	
00006C _H	FBYTE02 [R/W] B, H, W 00000000	FBYTE01 [R/W] B, H, W 00000000	FCR01 [R/W] B, H, W ---00100	FCR00 [R/W, R] B, H, W -0000000	
000070 _H	SSR1 [R/W, R] B, H, W 00000011	ESCR1 [R/W]/ IBSR1 [R/W, R] B, H, W 00000000	SCR1 [R/W] / IBCR1 [R/W, R] B, H, W 00000000	SMR1 [R/W] B, H, W 000-0000	Multi- function serial interface 1
000074 _H	BGR11 [R/W] B, H, W 00000000	BGR10 [R/W] B, H, W 00000000	RDR1 [R]/ TDR1 [W] H, W -----0 00000000		
000078 _H	—		ISMK1 [R/W] B, H, W 01111111	ISBA1 [R/W] B, H, W 00000000	
00007C _H	FBYTE21 [R/W] B, H, W 00000000	FBYTE11 [R/W] B, H, W 00000000	FCR11 [R/W] B, H, W ---00100	FCR10 [R/W, R] B, H, W -0000000	
000080 _H	SSR2 [R/W, R] B, H, W 00000011	ESCR2 [R/W]/ IBSR2 [R/W, R] B, H, W 00000000	SCR2 [R/W] / IBCR2 [R/W, R] B, H, W 00000000	SMR2 [R/W] B, H, W 000-0000	Multi- function serial interface 2
000084 _H	BGR21 [R/W] B, H, W 00000000	BGR20 [R/W] B, H, W 00000000	RDR2 [R]/ TDR2 [W] H, W -----0 00000000		
000088 _H	—		ISMK2 [R/W] B, H, W 01111111	ISBA2 [R/W] B, H, W 00000000	
00008C _H	FBYTE22 [R/W] B, H, W 00000000	FBYTE21 [R/W] B, H, W 00000000	FCR21 [R/W] B, H, W ---00100	FCR20 [R/W, R] B, H, W -0000000	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000090 _H	SSR3 [R/W, R] B, H, W 00000011	ESCR3 [R/W]/ IBSR3 [R/W, R] B, H, W 00000000	SCR3 [R/W] / IBCR3 [R/W, R] B, H, W 00000000	SMR3 [R/W] B, H, W 000-0000	Multi- function serial interface 3
000094 _H	BGR31 [R/W] B, H, W 00000000	BGR30 [R/W] B, H, W 00000000	RDR3 [R]/ TDR3 [W] H, W -----0 00000000		
000098 _H	—		ISMK3 [R/W] B, H, W 01111111	ISBA3 [R/W] B, H, W 00000000	
00009C _H	FBYTE32 [R/W] B, H, W 00000000	FBYTE31 [R/W] B, H, W 00000000	FCR31 [R/W] B, H, W ---00100	FCR30 [R/W, R] B, H, W -0000000	
0000A0 _H	OCCPBH0, OCCPBL0 [W]/ OCCPH0, OCCPL0 [R] H, W 00000000 00000000		OCCPBH1, OCCPBL1 [W]/ OCCPH1, OCCPL1 [R] H, W 00000000 00000000		OCU0
0000A4 _H	OCCPBH2, OCCPBL2 [W]/ OCCPH2, OCCPL2 [R] H, W 00000000 00000000		OCCPBH3, OCCPBL3 [W]/ OCCPH3, OCCPL3 [R] H, W 00000000 00000000		
0000A8 _H	OCCPBH4, OCCPBL4 [W]/ OCCPH4, OCCPL4 [R] H, W 00000000 00000000		OCCPBH5, OCCPBL5 [W]/ OCCPH5, OCCPL5 [R] H, W 00000000 00000000		
0000AC _H	OCSH1 [R/W] B, H, W -110--00	OCSL0 [R/W] B, H, W 00001100	OCSH3 [R/W] B, H, W -110--00	OCSL2 [R/W] B, H, W 00001100	
0000B0 _H	OCSH5 [R/W] B, H, W -110--00	OCSL4 [R/W] B, H, W 00001100	OCMOD0 [R/W] B, H, W --000000	—	
0000B4 _H	CPCLRBH0, CPCLRBL0 [W]/ CPCLRHO, CPCLRL0 [R] H, W 11111111 11111111		TCDTH0, TCDTL0 [R/W] H, W 00000000 00000000		Free-run timer 0
0000B8 _H	TCCSH0 [R/W] B, H, W 00000000	TCCSL0 [R/W] B, H, W 01000000	TCCSM0 [R/W] B, H, W ----0000	ADTRGC0 [R/W] B, H, W -000-000	
0000BC _H	CPCLRBH1, CPCLRBL1 [W] / CPCLRHO, CPCLRL1 [R] H, W 11111111 11111111		TCDTH1, TCDTL1 [R/W] H, W 00000000 00000000		Free-run timer 1
0000C0 _H	TCCSH1 [R/W] B, H, W 00000000	TCCSL1 [R/W] B, H, W 01000000	TCCSM1 [R/W] B, H, W ----0000	ADTRGC1 [R/W] B, H, W -000-000	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
0000C4 _H	CPCLRBH2, CPCLRBL2 [W] / CPCLRH2, CPCLRL2 [R] H, W 11111111 11111111		TCDTH2, TCDTL2 [R/W] H, W 00000000 00000000		Free-run timer 2
0000C8 _H	TCCSH2 [R/W] B, H, W 00000000	TCCSL2 [R/W] B, H, W 01000000	TCCSM2 [R/W] B, H, W ----0000	ADTRGC2 [R/W] B, H, W -000-000	
0000CC _H	—	FRS2 [R/W] B, H, W -000-000	FRS1 [R/W] B, H, W -000-000	FRS0 [R/W] B, H, W -000-000	Free-run timer selector 0
0000D0 _H	—		FRS4 [R/W] B, H, W -000-000	FRS3 [R/W] B, H, W -000-000	
0000D4 _H	IPCPH0, IPCPL0 [R] H, W XXXXXXXXXX XXXXXXXXX		IPCPH1, IPCPL1 [R] H, W XXXXXXXXXX XXXXXXXXX		ICU0
0000D8 _H	IPCPH2, IPCPL2 [R] H, W XXXXXXXXXX XXXXXXXXX		IPCPH3, IPCPL3 [R] H, W XXXXXXXXXX XXXXXXXXX		
0000DC _H	PICSH01 [W, R] B, H, W 00000000	PICSL01 [R/W] B, H, W 00000000	ICSH23 [R] B, H, W -----00	ICSL23[R/W] B, H, W 00000000	
0000E0 _H	TMRRH0, TMRRL0 [R/W] H, W XXXXXXXXXX XXXXXXXXX		TMRRH1, TMRRL1 [R/W] H, W XXXXXXXXXX XXXXXXXXX		Wave form generator 0
0000E4 _H	TMRRH2, TMRRL2 [R/W] H, W XXXXXXXXXX XXXXXXXXX		—		
0000E8 _H	DTCR0 [R/W] B, H, W 00000000	DTCR1 [R/W] B, H, W 00000000	DTCR2 [R/W] B, H, W 00000000	—	
0000EC _H	—	SIGCR10 [R/W] B, H, W 00000000	—	SIGCR20 [R/W] B, H, W 000000-1	
0000F0 _H	ADCOMP0 [W]/ ADCOMPB0 [R] H, W 00000000 00000000		ADCOMP0 [W]/ ADCOMPDB0 [R] H, W 00000000 00000000		A/D activating compare 0
0000F4 _H	ADCOMP1 [W]/ ADCOMPB1 [R] H, W 00000000 00000000		ADCOMP1 [W]/ ADCOMPDB1 [R] H, W 00000000 00000000		
0000F8 _H	ADCOMP2 [W]/ ADCOMPB2 [R] H, W 00000000 00000000		ADCOMP2 [W]/ ADCOMPDB2 [R] H, W 00000000 00000000		
0000FC _H	—	ADTGBUF0 [R/W] B, H, W -000-111	ADTGSEL0 [R/W] B, H, W --000000	ADTGCE0 [R/W] B, H, W --000000	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000100 _H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	PPG
000104 _H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	
000108 _H	PPGC0 [R/W] B, H, W 00000000	PPGC1 [R/W] B, H, W 00000000	PPGC2 [R/W] B, H, W 00000000	PPGC3 [R/W] B, H, W 00000000	
00010C _H	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	
000110 _H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
000114 _H	PPGC4 [R/W] B, H, W 00000000	PPGC5 [R/W] B, H, W 00000000	PPGC6 [R/W] B, H, W 00000000	PPGC7 [R/W] B, H, W 00000000	
000118 _H	PRLH8 [R/W] B, H, W XXXXXXXX	PRLL8 [R/W] B, H, W XXXXXXXX	PRLH9 [R/W] B, H, W XXXXXXXX	PRLL9 [R/W] B, H, W XXXXXXXX	
00011C _H	PRLH10 [R/W] B, H, W XXXXXXXX	PRLL10 [R/W] B, H, W XXXXXXXX	PRLH11 [R/W] B, H, W XXXXXXXX	PRLL11 [R/W] B, H, W XXXXXXXX	
000120 _H	PPGC8 [R/W] B, H, W 00000000	PPGC9 [R/W] B, H, W 00000000	PPGC10 [R/W] B, H, W 00000000	PPGC11 [R/W] B, H, W 00000000	
000124 _H	PRLH12 [R/W] B, H, W XXXXXXXX	PRLL12 [R/W] B, H, W XXXXXXXX	PRLH13 [R/W] B, H, W XXXXXXXX	PRLL13 [R/W] B, H, W XXXXXXXX	
000128 _H	PRLH14 [R/W] B, H, W XXXXXXXX	PRLL14 [R/W] B, H, W XXXXXXXX	PRLH15 [R/W] B, H, W XXXXXXXX	PRLL15 [R/W] B, H, W XXXXXXXX	
00012C _H	PPGC12 [R/W] B, H, W 00000000	PPGC13 [R/W] B, H, W 00000000	PPGC14 [R/W] B, H, W 00000000	PPGC15 [R/W] B, H, W 00000000	
000130 _H	TRG [R/W] B, H 00000000 00000000		—	GATEC0 [R/W] B --00--00	
000134 _H	REVC [R/W] B, H 00000000 00000000		—	GATEC4 [R/W] B -----00	
000138 _H	—			GATEC8 [R/W] B --00--00	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
00013C _H	—			GATEC12 [R/W] B -----00	PPG
000140 _H	—				(Reserved)
000144 _H	TTCR0 [R/W, W, R] B, H, W 11110000	—			Timing generator 0
000148 _H	COMP0 [R/W] B, H, W 00000000	COMP2 [R/W] B, H, W 00000000	COMP4 [R/W] B, H, W 00000000	COMP6 [R/W] B, H, W 00000000	
00014C _H	TTCR1 [R/W, W, R] B, H, W 11110000	—			Timing generator 1
000150 _H	COMP1 [R/W] B, H, W 00000000	COMP3 [R/W] B, H, W 00000000	COMP5 [R/W] B, H, W 00000000	COMP7 [R/W] B, H, W 00000000	
000154 _H	EIRR1 [R/W] B, H, W 00000000	ENIR1 [R/W] B, H, W 00000000	ELVR1 [R/W] B, H, W 00000000 00000000		External interrupt (INT8 to INT15)
000158 _H	—				(Reserved)
00015C _H	—			CMCLKR [R/W] B ----0000	Clock monitor
000160 _H	BT0TMR [R] B, H, W 00000000 00000000		BT0TMCR [R/W] B, H, W -0000000 00000000		Base timer 0
000164 _H	—	BT0STC [R/W] B 00000000	—		
000168 _H	BT0PCSR/BT0PRL [R/W] H, W XXXXXXXXXX XXXXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H, W XXXXXXXXXX XXXXXXXXXX		
00016C _H	—				(Reserved)
000170 _H	AICR2 [R/W] B, H, W ----1111 11111111		—		8/10-bit A/D converter 2 (12 channels)
000174 _H	ADCS2 [R/W, W] B, H, W 0000000-	—	ADCH2 [R/W] B, H, W 00000000	ADMD2 [R/W] B, H, W 00001111	
000178 _H	ADCD002 [R] B, H, W 10----XX XXXXXXXXXX		ADCD012 [R] B, H, W 10----XX XXXXXXXXXX		
00017C _H	ADCD022 [R] B, H, W 10----XX XXXXXXXXXX		ADCD032 [R] B, H, W 10----XX XXXXXXXXXX		

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000180 _H	ADCD042 [R] B, H, W 10----XX XXXXXXXX		ADCD052 [R] B, H, W 10----XX XXXXXXXX		8/10-bit A/D converter 2 (12 channels)
000184 _H	ADCD062 [R] B, H, W 10----XX XXXXXXXX		ADCD072 [R] B, H, W 10----XX XXXXXXXX		
000188 _H	ADCD082 [R] B, H, W 10----XX XXXXXXXX		ADCD092 [R] B, H, W 10----XX XXXXXXXX		
00018C _H	ADCD102 [R] B, H, W 10----XX XXXXXXXX		ADCD112 [R] B, H, W 10----XX XXXXXXXX		
000190 _H to 00019C _H	—				(Reserved)
0001A0 _H	OCCPBH6, OCCPBL6 [W]/ OCCPH6, OCCPL6 [R] H, W 00000000 00000000		OCCPBH7, OCCPBL7 [W]/ OCCPH7, OCCPL7 [R] H, W 00000000 00000000		OCU1
0001A4 _H	OCCPBH8, OCCPBL8 [W]/ OCCPH8, OCCPL8 [R] H, W 00000000 00000000		OCCPBH9, OCCPBL9 [W]/ OCCPH9, OCCPL9 [R] H, W 00000000 00000000		
0001A8 _H	OCCPBH10, OCCPBL10 [W]/ OCCPH10, OCCPL10 [R] H, W 00000000 00000000		OCCPBH11, OCCPBL11 [W]/ OCCPH11, OCCPL11 [R] H, W 00000000 00000000		
0001AC _H	OCSH7 [R/W] B, H, W -110--00	OCSL6 [R/W] B, H, W 00001100	OCSH9 [R/W] B, H, W -110--00	OCSL8 [R/W] B, H, W 00001100	
0001B0 _H	OCSH11 [R/W] B, H, W -110--00	OCSL10 [R/W] B, H, W 00001100	OCMOD1 [R/W] B, H, W --000000	—	
0001B4 _H	CPCLRBH3, CPCLRBL3 [W]/ CPCLRHH3, CPCLRL3 [R] H, W 11111111 11111111		TCDTH3, TCDTL3 [R/W] H, W 00000000 00000000		Free-run timer 3
0001B8 _H	TCCSH3 [R/W] B, H, W 00000000	TCCSL3 [R/W] B, H, W 01000000	TCCSM3 [R/W] B, H, W ----0000	ADTRGC3 [R/W] B, H, W -000-000	
0001BC _H	CPCLRBH4, CPCLRBL4 [W] / CPCLRHH4, CPCLRL4 [R] H, W 11111111 11111111		TCDTH4, TCDTL4 [R/W] H, W 00000000 00000000		Free-run timer 4
0001C0 _H	TCCSH4 [R/W] B, H, W 00000000	TCCSL4 [R/W] B, H, W 01000000	TCCSM4 [R/W] B, H, W ----0000	ADTRGC4 [R/W] B, H, W -000-000	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
0001C4 _H	CPCLRBH5, CPCLRBL5 [W] / CPCLRH5, CPCLRL 5 [R] H, W 11111111 11111111		TCDTH5, TCDTL5 [R/W] H, W 00000000 00000000		Free-run timer 5
0001C8 _H	TCCSH5 [R/W] B, H, W 00000000	TCCSL5 [R/W] B, H, W 01000000	TCCSM5 [R/W] B, H, W ----0000	ADTRGC5 [R/W] B, H, W -000-000	
0001CC _H	—	FRS7 [R/W] B, H, W -011-011	FRS6 [R/W] B, H, W -011-011	FRS5 [R/W] B, H, W -011-011	Free-run timer selector 1
0001D0 _H	—		FRS9 [R/W] B, H, W -011-011	FRS8 [R/W] B, H, W -011-011	
0001D4 _H	IPCPH4, IPCPL4 [R] H, W XXXXXXXX XXXXXXXX		IPCPH5, IPCPL5 [R] H, W XXXXXXXX XXXXXXXX		ICU1
0001D8 _H	IPCPH6, IPCPL6 [R] H, W XXXXXXXX XXXXXXXX		IPCPH7, IPCPL7 [R] H, W XXXXXXXX XXXXXXXX		
0001DC _H	PICSH45 [W, R] B, H, W 00000000	PICSL45 [R/W] B, H, W 00000000	ICSH67 [R] B, H, W -----00	ICSL67 [R/W] B, H, W 00000000	
0001E0 _H	TMRRH3, TMRRL3 [R/W] H, W XXXXXXXX XXXXXXXX		TMRRH4, TMRRL4 [R/W] H, W XXXXXXXX XXXXXXXX		Wave form generator 1
0001E4 _H	TMRRH5, TMRRL5 [R/W] H, W XXXXXXXX XXXXXXXX		—		
0001E8 _H	DTCR3 [R/W] B, H, W 00000000	DTCR4 [R/W] B, H, W 00000000	DTCR5 [R/W] B, H, W 00000000	—	
0001EC _H	—	SIGCR11 [R/W] B, H, W 00000000	—	SIGCR21 [R/W] B, H, W 000000-1	
0001F0 _H	ADCOMP3 [W]/ ADCOMPB3 [R] H, W 00000000 00000000		ADCOMP3 [W]/ ADCOMPDB3 [R] H, W 00000000 00000000		A/D activating compare 1
0001F4 _H	ADCOMP4 [W]/ ADCOMPB4 [R] H, W 00000000 00000000		ADCOMP4 [W]/ ADCOMPDB4 [R] H, W 00000000 00000000		
0001F8 _H	ADCOMP5 [W]/ ADCOMPB5 [R] H, W 00000000 00000000		ADCOMP5 [W]/ ADCOMPDB5 [R] H, W 00000000 00000000		
0001FC _H	—	ADTGBUF1 [R/W] B, H, W -000-111	ADTGSEL1 [R/W] B, H, W --000000	ADTGCE1[R/W] B, H, W --000000	

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Address	Register				Block
	+0	+1	+2	+3	
000200 _H	DMACA0 [R/W] B, H, W ^{*1} 00000000 ----XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] B, H, W ^{*1} 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 _H	DMACA2 [R/W] B, H, W ^{*1} 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] B, H, W ^{*1} 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] B, H, W ^{*1} 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 _H to 00023C _H	—				(Reserved)
000240 _H	DMACR [R/W] B, H, W 0--00000 -----				DMAC
000244 _H to 00039C _H	—				(Reserved)
0003A0 _H	DSP-PC [R/W] B, H, W 000000-0	DSP-CSR [R/W, R, W] B, H, W 00000000	—		MAC
0003A4 _H	DSP-LY [R/W], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003A8 _H	DSP-OT0 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003AC _H	DSP-OT1 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003B0 _H	DSP-OT2 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003B4 _H	DSP-OT3 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
0003B8 _H	DSP-OT4 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				MAC
0003BC _H	DSP-OT5 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003C0 _H	DSP-OT6 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003C4 _H	DSP-OT7 [R], W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003C8 _H	DSP-AC0 [R], W ----- 00000000				
0003CC _H	DSP-AC1 [R], W 00000000 00000000 00000000 00000000				
0003D0 _H	DSP-AC2 [R], W 00000000 00000000 00000000 00000000				
0003D4 _H to 0003EC _H	—				(Reserved)
0003F0 _H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4 _H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H	DDR0 [R/W] B, H, W 00000000	DDR1 [R/W] B, H, W 00000000	DDR2 [R/W] B, H, W 00000000	DDR3 [R/W] B, H, W 00000000	Port direction register
000404 _H	DDR5 [R/W] B, H, W -0000000	DDR6 [R/W] B, H, W -----00	DDR8 [R/W] B, H, W 00000000	DDR9 [R/W] B, H, W 00000000	
000408 _H	DDRA [R/W] B, H, W ---00000	DDRB [R/W] B, H, W 00000000	DDRC [R/W] B, H, W 00000000	DDRD [R/W] B, H, W ---0000	
00040C _H	DDRE [R/W] B, H, W 00000000	DDRF [R/W] B, H, W 00000000	DDRG [R/W] B, H, W --000000	DDRH [R/W] B, H, W --000000	
000410 _H	DDRJ [R/W] B, H, W 00000000	—	DDRJ [R/W] B, H, W -----000	DDRM [R/W] B, H, W ---0000	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000414 _H	DDRP [R/W] B, H, W --000000	DDRQ [R/W] B, H, W --000000	DDRR [R/W] B, H, W --000000	DDRS [R/W] B, H, W --000000	Port direction register
000418 _H , 00041C _H	—				(Reserved)
000420 _H	PFR0 [R/W] B, H, W 11111111	PFR1 [R/W] B, H, W 11111111	PFR2 [R/W] B, H, W 11111111	PFR3 [R/W] B, H, W 11111111	Port function register
000424 _H	PFR5 [R/W] B, H, W -1111111	PFR6 [R/W] B, H, W -----11	PFR8 [R/W] B, H, W 0000----	PFR9 [R/W] B, H, W 00000000	
000428 _H	—		PFRC [R/W] B, H, W --0-00-0	—	
00042C _H	—	PFRF [R/W] B, H, W -----0	PFRG [R/W] B, H, W --0-00-0	PFRH [R/W] B, H, W --0-00-0	
000430 _H	PFRJ [R/W] B, H, W 0-0-0-0-	—		PFRM [R/W] B, H, W ----0000	
000434 _H	—	PFRQ [R/W] B, H, W --000000	—	PFRS [R/W] B, H, W --000000	
000438 _H , 00043C _H	—				(Reserved)
000440 _H	ICR00 [R/W, R] B, H, W ---11111	ICR01 [R/W, R] B, H, W ---11111	ICR02 [R/W, R] B, H, W ---11111	ICR03 [R/W, R] B, H, W ---11111	Interrupt controller
000444 _H	ICR04 [R/W, R] B, H, W ---11111	ICR05 [R/W, R] B, H, W ---11111	ICR06 [R/W, R] B, H, W ---11111	ICR07 [R/W, R] B, H, W ---11111	
000448 _H	ICR08 [R/W, R] B, H, W ---11111	ICR09 [R/W, R] B, H, W ---11111	ICR10 [R/W, R] B, H, W ---11111	ICR11 [R/W, R] B, H, W ---11111	
00044C _H	ICR12 [R/W, R] B, H, W ---11111	ICR13 [R/W, R] B, H, W ---11111	ICR14 [R/W, R] B, H, W ---11111	ICR15 [R/W, R] B, H, W ---11111	
000450 _H	ICR16 [R/W, R] B, H, W ---11111	ICR17 [R/W, R] B, H, W ---11111	ICR18 [R/W, R] B, H, W ---11111	ICR19 [R/W, R] B, H, W ---11111	
000454 _H	ICR20 [R/W, R] B, H, W ---11111	ICR21 [R/W, R] B, H, W ---11111	ICR22 [R/W, R] B, H, W ---11111	ICR23 [R/W, R] B, H, W ---11111	

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000458 _H	ICR24 [R/W, R] B, H, W ---11111	ICR25 [R/W, R] B, H, W ---11111	ICR26 [R/W, R] B, H, W ---11111	ICR27 [R/W, R] B, H, W ---11111	Interrupt controller
00045C _H	ICR28 [R/W, R] B, H, W ---11111	ICR29 [R/W, R] B, H, W ---11111	ICR30 [R/W, R] B, H, W ---11111	ICR31 [R/W, R] B, H, W ---11111	
000460 _H	ICR32 [R/W, R] B, H, W ---11111	ICR33 [R/W, R] B, H, W ---11111	ICR34 [R/W, R] B, H, W ---11111	ICR35 [R/W, R] B, H, W ---11111	
000464 _H	ICR36 [R/W, R] B, H, W ---11111	ICR37 [R/W, R] B, H, W ---11111	ICR38 [R/W, R] B, H, W ---11111	ICR39 [R/W, R] B, H, W ---11111	
000468 _H	ICR40 [R/W, R] B, H, W ---11111	ICR41 [R/W, R] B, H, W ---11111	ICR42 [R/W, R] B, H, W ---11111	ICR43 [R/W, R] B, H, W ---11111	
00046C _H	ICR44 [R/W, R] B, H, W ---11111	ICR45 [R/W, R] B, H, W ---11111	ICR46 [R/W, R] B, H, W ---11111	ICR47 [R/W, R] B, H, W ---11111	
000470 _H to 00047C _H	—				(Reserved)
000480 _H	RSRR [R/W] B, H, W 1-0-0-00	STCR [R/W] B, H, W 001100-1	TBCR [R/W] B, H, W 00XXX-00	CTBR [W] B, H, W XXXXXXXXX	Clock control block
000484 _H	CLKR [R/W] B, H, W -000-000	—	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488 _H to 0004FC _H	—				(Reserved)
000500 _H	—	AICR0 [R/W] B, H, W ----1111	—		8/10-bit A/D converter 0 (4 channels)
000504 _H	ADCS0 [R/W, W] B, H, W 0000000-	—	ADCH0 [R/W] B, H, W --00--00	ADMD0 [R/W] B, H, W 00001111	
000508 _H	ADCD000 [R] B, H, W 10----XX XXXXXXXX		ADCD010 [R] B, H, W 10----XX XXXXXXXX		
00050C _H	ADCD020 [R] B, H, W 10----XX XXXXXXXX		ADCD030 [R] B, H, W 10----XX XXXXXXXX		

(Continued)

MB91470/480 Series

Address	Register				Block
	+0	+1	+2	+3	
000510 _H	—	AICR1 [R/W] B, H, W ----1111	—		8/10-bit A/D converter 1 (4 channels)
000514 _H	ADCS1 [R/W, W] B, H, W 0000000-	—	ADCH1 [R/W] B, H, W --00--00	ADMD1 [R/W] B, H, W 00001111	
000518 _H	ADCD001 [R] B, H, W 10----XX XXXXXXXX		ADCD011 [R] B, H, W 10----XX XXXXXXXX		
00051C _H	ADCD021 [R] B, H, W 10----XX XXXXXXXX		ADCD031 [R] B, H, W 10----XX XXXXXXXX		
000520 _H	—	AICR3 [R/W] B, H, W ----1111	—		12-bit A/D converter 3 (4 channels)
000524 _H	ADCS3 [R/W, W] B, H, W 0000000-	—	ADCH3 [R/W] B, H, W --00--00	ADMD3 [R/W] B, H, W 00001111	
000528 _H	ADCD003 [R] B, H, W 10--XXXX XXXXXXXX		ADCD013 [R] B, H, W 10--XXXX XXXXXXXX		
00052C _H	ADCD023 [R] B, H, W 10--XXXX XXXXXXXX		ADCD033 [R] B, H, W 10--XXXX XXXXXXXX		
000530 _H	—	AICR4 [R/W] B, H, W ----1111	—		12-bit A/D converter 4 (4 channels)
000534 _H	ADCS4 [R/W, W] B, H, W 0000000-	—	ADCH4 [R/W] B, H, W --00--00	ADMD4 [R/W] B, H, W 00001111	
000538 _H	ADCD004 [R] B, H, W 10--XXXX XXXXXXXX		ADCD014 [R] B, H, W 10--XXXX XXXXXXXX		
00053C _H	ADCD024 [R] B, H, W 10--XXXX XXXXXXXX		ADCD034 [R] B, H, W 10--XXXX XXXXXXXX		
000540 _H	RCR10 [W] B, H, W XXXXXXXX	RCR00 [W] B, H, W XXXXXXXX	UDCR10 [R] B, H, W 00000000	UDCR00 [R] B, H, W 00000000	Up/down counter 0
000544 _H	CCR10 [R/W] B, H, W 00000000	CCRL0 [R/W, R] B, H, W -0001000	—	CSR0 [R/W, R] B, H, W 00000000	
000548 _H to 00055C _H	—				(Reserved)

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
000560 _H	SSR4 [R/W, R] B, H, W 00000011	ESCR4 [R/W]/ IBSR4 [R/W, R] B, H, W 00000000	SCR4 [R/W] / IBCR4 [R/W, R] B, H, W 00000000	SMR4 [R/W] B, H, W 000-0000	Multi- function serial interface 4
000564 _H	BGR41 [R/W] B, H, W 00000000	BGR40 [R/W] B, H, W 00000000	RDR4 [R]/TDR4 [W]H, W -----0 00000000		
000568 _H	—		ISMK4 [R/W] B, H, W 01111111	ISBA4 [R/W] B, H, W 00000000	
00056C _H	FBYTE42 [R/W] B, H, W 00000000	FBYTE41 [R/W] B, H, W 00000000	FCR41 [R/W] B, H, W ---00100	FCR40 [R/W, R] B, H, W -0000000	
000570 _H	SSR5 [R/W, R] B, H, W 00000011	ESCR5 [R/W]/ IBSR5 [R/W, R] B, H, W 00000000	SCR5 [R/W] / IBCR5 [R/W, R] B, H, W 00000000	SMR5 [R/W] B, H, W 000-0000	Multi- function serial interface 5
000574 _H	BGR51 [R/W] B, H, W 00000000	BGR50 [R/W] B, H, W 00000000	RDR5 [R]/TDR5 [W]H, W -----0 00000000		
000578 _H	—		ISMK5 [R/W] B, H, W 01111111	ISBA5 [R/W] B, H, W 00000000	
00057C _H	FBYTE52 [R/W] B, H, W 00000000	FBYTE51 [R/W] B, H, W 00000000	FCR51 [R/W] B, H, W ---00100	FCR50 [R/W, R] B, H, W -0000000	
000580 _H	BT1TMR [R] B, H, W 00000000 00000000		BT1TMCR [R/W] B, H, W -0000000 00000000		Base timer 1
000584 _H	—	BT1STC [R/W] B 00000000	—		
000588 _H	BT1PCSR/BT1PRL [R/W] H, W XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
00058C _H	—				(Reserved)
000590 _H	BT2TMR [R] B, H, W 00000000 00000000		BT2TMCR [R/W] B, H, W -0000000 00000000		Base timer 2
000594 _H	—	BT2STC [R/W] B 00000000	—		
000598 _H	BT2PCSR/BT2PRL [R/W] H, W XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
00059C _H	—				(Reserved)

(Continued)

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Address	Register				Block
	+0	+1	+2	+3	
0005A0 _H	BT3TMR [R] B, H, W 00000000 00000000		BT3TMCR [R/W] B, H, W -00000000 00000000		Base timer 3
0005A4 _H	—	BT3STC [R/W] B 00000000	—		
0005A8 _H	BT3PCSR/BT3PRLL [R/W] H, W XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
0005AC _H	—				(Reserved)
0005B0 _H to 0005FC _H	—				(Reserved)
000600 _H	PCR0 [R/W] B, H, W 00000000	PCR1 [R/W] B, H, W 00000000	PCR2 [R/W] B, H, W 00000000	PCR3 [R/W] B, H, W 00000000	Pull-up resistor control register
000604 _H	PCR5 [R/W] B, H, W -0000000	PCR6 [R/W] B, H, W -----00	PCR8 [R/W] B, H, W 00000000	PCR9 [R/W] B, H, W 00000000	
000608 _H	PCRA [R/W] B, H, W ---00000	PCRB [R/W] B, H, W 00000000	PCRC [R/W] B, H, W 00000000	PCRD [R/W] B, H, W ---0000	
00060C _H	PCRE [R/W] B, H, W 00000000	PCRF [R/W] B, H, W 00000000	PCRG [R/W] B, H, W --000000	PCRH [R/W] B, H, W --000000	
000610 _H	PCRJ [R/W] B, H, W 00000000	—	PCRL [R/W] B, H, W ----000	PCRM [R/W] B, H, W ---0000	
000614 _H	PCRP [R/W] B, H, W --000000	PCRQ [R/W] B, H, W --000000	PCRR [R/W] B, H, W --000000	PCRS [R/W] B, H, W --000000	
000618 _H to 00063C _H	—				(Reserved)
000640 _H	ASR0 [R/W] H, W 00000000 00000000 *2		ACR0 [R/W] H, W 1111XX-- --000000 *2		External bus interface
000644 _H	ASR1 [R/W] H, W XXXXXXXX XXXXXXXX *2		ACR1 [R/W] H, W XXXXXX-- --XXXXXX *2		
000648 _H	ASR2 [R/W] H, W XXXXXXXX XXXXXXXX *2		ACR2 [R/W] H, W XXXXXX-- --XXXXXX *2		
00064C _H	—				

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Address	Register				Block
	+0	+1	+2	+3	
000650 _H to 00065C _H	—				External bus interface
000660 _H	AWR0 [R/W] H, W 0111---- 1111-111 *2		AWR1 [R/W] H, W XXXX---- XXXX-XXX *2		
000664 _H	AWR2 [R/W] H, W XXXX---- XXXX-XXX *2		—		
000668 _H to 00067C _H	—				
000680 _H	CSER [R/W] B, H -----001	—			
000684 _H to 0007F8 _H	—				(Reserved)
0007FC _H	—	MODR [W] XXXXXXXX	—		Mode register
000800 _H to 000FFC _H	—				(Reserved)
001000 _H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 _H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 _H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C _H	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 _H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 _H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 _H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
00101C _H	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001020 _H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 _H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 _H to 006FFC _H	—				(Reserved)
007000 _H	FLCR [R/W, R] B ----X-0-	—			Flash memory
007004 _H	FLWC [R/W] B ----011	—			
007008 _H to 007010 _H	—				
007014 _H to 00701C _H	—				(Reserved)
007020 _H	WREN [R/W] H 00000000 00000000		—		Wild register control block
007024 _H to 00702C _H	—				
007030 _H	WA00 [R/W] W ----- ----XXXX XXXXXXXX XXXXXXX--				
007034 _H	WD00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007038 _H	WA01 [R/W] W ----- ----XXXX XXXXXXXX XXXXXXX--				
00703C _H	WD01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007040 _H	WA02 [R/W] W ----- ----XXXX XXXXXXXX XXXXXXX--				
007044 _H	WD02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007048 _H	WA03 [R/W] W ----- ----XXXX XXXXXXXX XXXXXXX--				
00704C _H	WD03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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MB91470/480 Series

Address	Register				Block
	+0	+1	+2	+3	
007050 _H	WA04 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
007054 _H	WD04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007058 _H	WA05 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00705C _H	WD05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007060 _H	WA06 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007064 _H	WD06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007068 _H	WA07 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00706C _H	WD07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007070 _H	WA08 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007074 _H	WD08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007078 _H	WA09 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00707C _H	WD09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007080 _H	WA10 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007084 _H	WD10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007088 _H	WA11 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00708C _H	WD11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007090 _H	WA12 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
007094 _H	WD12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007098 _H	WA13 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
00709C _H	WD13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+0	+1	+2	+3	
0070A0 _H	WA14 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
0070A4 _H	WD14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070A8 _H	WA15 [R/W] W ----- ----XXXX XXXXXXXX XXXXXX--				
0070AC _H	WD15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070B0 _H to 00BFFC _H	—				(Reserved)
00C000 _H to 00C0FC _H	X-RAM (coefficient RAM) [R/W] 64 × 32-bit				MAC
00C100 _H to 00C1FC _H	Y-RAM (variable RAM) [R/W] 64 × 32-bit				
00C200 _H to 00C3FC _H	I-RAM (instruction RAM) [R/W] 128 × 32-bit				
00C400 _H to 00FFFC _H	—				(Reserved)
010000 _H to 0FFFFC _H	—				(Reserved)

*1 : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed as bytes.

*2 : Register whose initial value depends on the reset level. The initial values shown are for INITX = “L”.

Notes : • Data is undefined in reserved or (—) area.

- Do not execute read modify write (RMW) instruction on registers having a write-only bit.
- The initial values are varied depending on the product series. Please refer to the hardware manual of MB91470/480 for more details.

MB91470/480 Series

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC _H	000FFFFC _H
Mode vector	1	01	—	3F8 _H	000FFFF8 _H
System reserved	2	02	—	3F4 _H	000FFFF4 _H
System reserved	3	03	—	3F0 _H	000FFFF0 _H
System reserved	4	04	—	3EC _H	000FFFE _C
System reserved	5	05	—	3E8 _H	000FFFE8 _H
System reserved	6	06	—	3E4 _H	000FFFE4 _H
Coprocessor absent trap	7	07	—	3E0 _H	000FFFE0 _H
Coprocessor error trap	8	08	—	3DC _H	000FFFD _C
INTE instruction	9	09	—	3D8 _H	000FFFD8 _H
System reserved	10	0A	—	3D4 _H	000FFFD4 _H
System reserved	11	0B	—	3D0 _H	000FFFD0 _H
Step trace trap	12	0C	—	3CC _H	000FFFCC _H
NMI request (tool)	13	0D	—	3C8 _H	000FFFC8 _H
Undefined instruction exception	14	0E	—	3C4 _H	000FFFC4 _H
NMI request	15	0F	—	3C0 _H	000FFFC0 _H
External interrupt 0	16	10	ICR00	3BC _H	000FFFB _C
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H
External interrupt 4	20	14	ICR04	3AC _H	000FFFA _C
External interrupt 5	21	15	ICR05	3A8 _H	000FFFA8 _H
External interrupt 6	22	16	ICR06	3A4 _H	000FFFA4 _H
External interrupt 7	23	17	ICR07	3A0 _H	000FFFA0 _H
Reload timer 0	24	18	ICR08	39C _H	000FFF9 _C
Reload timer 1	25	19	ICR09	398 _H	000FFF98 _H
Base timer 0 (source 0/source 1)	26	1A	ICR10	394 _H	000FFF94 _H
Multi-function serial interface 0 (UART transmission completed/reception completed/I ² C status)	27	1B	ICR11	390 _H	000FFF90 _H
Multi-function serial interface 1 (UART transmission completed/reception completed/I ² C status)	28	1C	ICR12	38C _H	000FFF8 _C
Base timer 1 (source 0/source 1)	29	1D	ICR13	388 _H	000FFF88 _H

(Continued)

MB91470/480 Series

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Base timer 2/3 (source 0/source 1) Up/down counter 0	30	1E	ICR14	384 _H	000FFF84 _H
DTTI0/DTTI1	31	1F	ICR15	380 _H	000FFF80 _H
DMAC0 (end/error)	32	20	ICR16	37C _H	000FFF7C _H
DMAC1 (end/error)	33	21	ICR17	378 _H	000FFF78 _H
DMAC2/3/4 (end/error)	34	22	ICR18	374 _H	000FFF74 _H
Multi-function serial interface 2 (UART transmission completed/reception completed/I ² C status)	35	23	ICR19	370 _H	000FFF70 _H
Multi-function serial interface 3 (UART transmission completed/reception completed/I ² C status)	36	24	ICR20	36C _H	000FFF6C _H
Multi-function serial interface 4 (UART transmission completed/reception completed/I ² C status)	37	25	ICR21	368 _H	000FFF68 _H
Multi-function serial interface 5 (UART transmission completed/reception completed/I ² C status)	38	26	ICR22	364 _H	000FFF64 _H
MAC	39	27	ICR23	360 _H	000FFF60 _H
PPG0/PPG1	40	28	ICR24	35C _H	000FFF5C _H
PPG2/PPG3/PPG8/PPG9	41	29	ICR25	358 _H	000FFF58 _H
PPG4/PPG5/PPG10/PPG11	42	2A	ICR26	354 _H	000FFF54 _H
PPG6/PPG7/PPG12/PPG13/PPG14/PPG15	43	2B	ICR27	350 _H	000FFF50 _H
Wave form generator 0/3 (underflow)	44	2C	ICR28	34C _H	000FFF4C _H
Wave form generator 1/4 (underflow)	45	2D	ICR29	348 _H	000FFF48 _H
Wave form generator 2/5 (underflow)	46	2E	ICR30	344 _H	000FFF44 _H
Timebase timer overflow	47	2F	ICR31	340 _H	000FFF40 _H
External interrupt 8/9/10/11/12/13/14/15	48	30	ICR32	33C _H	000FFF3C _H
Free-run timer 0/3 (compare clear)	49	31	ICR33	338 _H	000FFF38 _H
Free-run timer 0/3 (zero detection)	50	32	ICR34	334 _H	000FFF34 _H
Free-run timer 1/4 (compare clear)	51	33	ICR35	330 _H	000FFF30 _H
Free-run timer 1/4 (zero detection)	52	34	ICR36	32C _H	000FFF2C _H
Free-run timer 2/5 (compare clear)	53	35	ICR37	328 _H	000FFF28 _H
Free-run timer 2/5 (zero detection)	54	36	ICR38	324 _H	000FFF24 _H
8/10-bit A/D converter 2	55	37	ICR39	320 _H	000FFF20 _H
8/10-bit A/D converter 0/ 12-bit A/D converter 3	56	38	ICR40	31C _H	000FFF1C _H

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(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
8/10-bit A/D converter 1/ 12-bit A/D converter 4	57	39	ICR41	318 _H	000FFF18 _H
ICU0/ICU1/ICU4/ICU5 (capture)	58	3A	ICR42	314 _H	000FFF14 _H
ICU2/ICU3/ICU6/ICU7 (capture)	59	3B	ICR43	310 _H	000FFF10 _H
OCU0/OCU1/OCU6/OCU7 (match)	60	3C	ICR44	30C _H	000FFF0C _H
OCU2/OCU3/OCU8/OCU9 (match)	61	3D	ICR45	308 _H	000FFF08 _H
OCU4/OCU5/OCU10/OCU11 (match)	62	3E	ICR46	304 _H	000FFF04 _H
Interrupt delay source bit	63	3F	ICR47	300 _H	000FFF00 _H
System reserved (Used by REALOS)	64	40	—	2FC _H	000FFEFC _H
System reserved (Used by REALOS)	65	41	—	2F8 _H	000FFEFC _H
System reserved	66	42	—	2F4 _H	000FFEFC _H
System reserved	67	43	—	2F0 _H	000FFEFC _H
System reserved	68	44	—	2EC _H	000FFEEC _H
System reserved	69	45	—	2E8 _H	000FFEE8 _H
System reserved	70	46	—	2E4 _H	000FFEE4 _H
System reserved	71	47	—	2E0 _H	000FFEE0 _H
System reserved	72	48	—	2DC _H	000FFEDC _H
System reserved	73	49	—	2D8 _H	000FFED8 _H
System reserved	74	4A	—	2D4 _H	000FFED4 _H
System reserved	75	4B	—	2D0 _H	000FFED0 _H
System reserved	76	4C	—	2CC _H	000FFEC _H
System reserved	77	4D	—	2C8 _H	000FFEC8 _H
System reserved	78	4E	—	2C4 _H	000FFEC4 _H
System reserved	79	4F	—	2C0 _H	000FFEC0 _H
Used by INT instruction	80 to 255	50 to FF	—	2BC _H to 000 _H	000FFEB _H to 000FFC0 _H

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
Means that the input function can be used.
- Input disabled
Indicates that the input function cannot be used.
- Input fixed to "0"
A state of a pin, in which "0" is transmitted to internal circuitry, with the external input shut off by the input gate adjacent to the pin.
- Output Hi-Z
Means to place a pin in a high impedance state by disabling the pin driving transistor from driving.
- Preserving the previous state
Means to output the state existing immediately prior to entering this mode.
That is, to output according to an internal resource with an output when it is operating or to preserve an output when the output is provided, for example, as a port.
- Input enabled when external interrupt function selected and enabled
Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

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• List of pin status

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1	INITX = "H"*2		HIZ = 0	HIZ = 1
P00 to P07	D16 to D23	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
P10 to P17	D24 to D31					
P20 to P27	A00 to A07					
P30 to P37	A08 to A15					
P50 to P52	CS0X to CS2X					
P53	ASX					
P54	RDX					
P55, P56	WR0X, WR1X					
P60	SYSCLK					
P61	RDY					
NMIX	NMIX	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
P80 to P83	INT0 to INT3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Input enabled	Input enabled	Input enabled when interrupt function selected and enabled
P84	INT4/PPG4					
P85	INT5/PPG5					
P86	INT6/PPG6					
P87	INT7/PPG7					
P90	INT8/PPG8					
P91	INT9/PPG9					
P92	INT10/PPG10					
P93	INT11/PPG11					
P94	INT12/PPG12					
P95	INT13/PPG13					
P96	INT14/PPG14					
P97	INT15/PPG15					
PA0 to PA4	ADTG0 to ADTG4	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PB0 to PB3	AN0-0 to AN0-3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input "0" fixed	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PB4 to PB7	AN1-0 to AN1-3					
PC0	AN2-0/SCK4					
PC1	AN2-1/SIN4					
PC2	AN2-2/SOT4					
PC3	AN2-3/SCK5					
PC4	AN2-4/SIN5					
PC5	AN2-5/SOT5					
PC6, PC7	AN2-6, AN2-7					

(Continued)

(Continued)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1	INITX = "H"*2		HIZ = 0	HIZ = 1
PD0 to PD3	AN2-8 to AN2-11	Output Hi-Z/ Input disabled	Output Hi-Z/ Input "0" fixed	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PE0 to PE3	AN3-0 to AN3-3					
PE4 to PE7	AN4-0 to AN4-3					
PF0	CLKPOUT	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PF1 to PF6	GPIO					
PG0, PG3	SCK0, SCK1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PG1, PG4	SIN0, SIN1					
PG2, PG5	SOT0, SOT1					
PH0, PH3	SCK2, SCK3					
PH1, PH4	SIN2, SIN3					
PH2, PH5	SOT2, SOT3					
PJ0, PJ2, PJ4, PJ6	TIN0 to TIN3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PJ1, PJ3, PJ5, PJ7	TOUT0 to TOUT3					
PL0	AIN0	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PL1	BIN0					
PL2	ZIN0					
PM0 to PM3	PPG0 to PPG3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PP0 to PP3	IC0 to IC3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PP4	CKI0					
PP5	DTTI0					
PQ0 to PQ5	RTO0 to RTO5	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PR0 to PR3	IC4 to IC7					
PR4	CKI1					
PR5	DTTI1					
PS0 to PS5	RTO6 to RTO11					

*1 : INITX = "L" : Indicates the pin status with INITX remaining at the "L" level.

*2 : INITX = "H" : Indicates the pin status existing immediately after INITX transition from "L" to "H" level.

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- List of pin status (external bus mode)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1	INITX = "H"*2		HIZ = 0	HIZ = 1
P00 to P07	D16 to D23	Output Hi-Z	Output Hi-Z	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z
P10 to P17	D24 to D31					
P20 to P27	A00 to A07					
P30 to P37	A08 to A15					
P50 to P52	CS0X to CS2X					
P53	ASX					
P54	RDX					
P55, P56	WR0X, WR1X					
P60	SYSCLK	Input disabled	Input disabled			Input "0" fixed
P61	RDY					

*1 : INITX = "L" : Indicates the pin status with INITX remaining at the "L" level.

*2 : INITX = "H" : Indicates the pin status existing immediately after INITX transition from "L" to "H" level.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	
Analog power supply voltage*1,*2,*6	AVCC10 AVCC12	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	
Analog reference voltage*7	AVRHn	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Analog pin input voltage*1	V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
“L” level maximum output current*3	I_{OL}	—	10	mA	
“L” level average output current*4	I_{OLAV}	—	4	mA	Except port Q0 to Q5 and S0 to S5
			12	mA	Port Q0 to Q5 and S0 to S5
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*5	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*3	I_{OH}	—	-10	mA	
“H” level average output current *4	I_{OHAV}	—	-4	mA	Except port Q0 to Q5 and S0 to S5
			-12	mA	Port Q0 to Q5 and S0 to S5
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current*5	ΣI_{OHAV}	—	-50	mA	
Power consumption	P_D	—	800	mW	
Storage temperature	T_{STG}	-55	+125	°C	

*1 : The parameter is based on $V_{SS} = AVSS10 = AVSS12 = 0$ V.

*2 : Be careful not to exceed $V_{CC} + 0.3$ V, for example, when the power is turned on.
Be careful to set AVCC10, AVCC12 equal V_{CC} , for example, when the power is turned on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

*6 : AVCC10 is the analog supply voltage for the 8/10-bit A/D converter, and AVCC12 is the analog supply voltage for the 12-bit A/D converter.

*7 : AVRHn=AVRH0/AVRH1/AVRH2 are the analog reference voltage for the 8/10-bit A/D converter, and AVRH3/AVRH4 are the analog reference voltage for the 12-bit A/D converter.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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2. Recommended Operating Conditions

($V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.0	5.5	V	
Analog power supply voltage	AVCC10	$V_{SS} + 4.0$	$V_{SS} + 5.5$	V	For all 8/10-bit A/D converter (common use)
	AVCC12	$V_{SS} + 4.0$	$V_{SS} + 5.5$	V	For all 12-bit A/D converter (common use)
Analog reference voltage	AVRH0	AVSS10	AVCC10	V	For 8/10-bit A/D converter 0
	AVRH1	AVSS10	AVCC10	V	For 8/10-bit A/D converter 1
	AVRH2	AVSS10	AVCC10	V	For 8/10-bit A/D converter 2
	AVRH3	AVSS12	AVCC12	V	For 12-bit A/D converter 3
	AVRH4	AVSS12	AVCC12	V	For 12-bit A/D converter 4
(-) Analog input signal voltage range	ANINN	AVSS12	AVCC12/2	V	For all 12-bit A/D converters (common use) (under differential mode)
(+) Analog input signal voltage range	ANINP	AVSS12	AVCC12	V	
ANINN-ANINP voltage difference	ANINN-ANINP	—	AVCC12/4	V	
Operating temperature	T_A	- 40	+ 70	°C	When mounted on single-layer PCB*
			+ 85		When mounted on four-layer PCB*

* : The remaining rating values assume four-layer PCB.

Note : During power-on, it takes approximately 600 μs for the internal power supply to stabilize after the V_{CC} power supply has stabilized. Continue to assert the INITX pin during this period.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH}	CMOS input pin	—	$V_{CC} \times 0.7$	—	V_{CC}	V	
	V_{IHS}	CMOS hysteresis input pin	—	$V_{CC} \times 0.8$	—	V_{CC}	V	
“L” level input voltage	V_{IL}	CMOS input pin	—	V_{SS}	—	$V_{CC} \times 0.3$	V	
	V_{ILS}	CMOS hysteresis input pin	—	V_{SS}	—	$V_{CC} \times 0.2$	V	
“H” level output voltage	V_{OH1}	Except port Q0 to Q5 and port S0 to S5	$V_{CC} = 5.0\text{ V}$, $I_{OH} = 4\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OH2}	Port Q0 to Q5 and port S0 to S5	$V_{CC} = 5.0\text{ V}$, $I_{OH} = 12\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL1}	Except port Q0 to Q5 and port S0 to S5	$V_{CC} = 5.0\text{ V}$, $I_{OL} = 4\text{ mA}$	—	—	$V_{SS} + 0.4$	V	
	V_{OL2}	Port Q0 to Q5 and port S0 to S5	$V_{CC} = 5.0\text{ V}$, $I_{OL} = 12\text{ mA}$	—	—	$V_{SS} + 0.4$	V	
Input leak current	I_{LI}	—	$V_{CC} = 5.0\text{ V}$, $V_{SS} < V_I < V_{CC}$	- 5	—	—	μA	
Pull-up resistance	R_{PULL}	INITX, pull-up pin	—	—	50	—	$\text{k}\Omega$	
Power supply current	I_{CC}	VCC	Flash memory $V_{CC} = 5.0\text{ V}$, $f_C = 20\text{ MHz}$, $PLL \times 4$, $CLKB = 80\text{ MHz}$ $CLKP = 40\text{ MHz}$ $CLKT = 40\text{ MHz}$	—	—	100	mA	When the multiply and accumulate unit is not used.
				—	—	140	mA	When the multiply and accumulate unit is used.

(Continued)

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($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	VCC	MASK ROM $V_{CC} = 5.0\text{ V}$, $f_c = 20\text{ MHz}$, PLL $\times 4$, CLKB = 80 MHz CLKP = 40 MHz CLKT = 40 MHz	—	—	65	mA	When the multiply and accumulate unit is not used.
				—	—	105	mA	When the multiply and accumulate unit is used.
	I_{CCS}	VCC	$V_{CC} = 5.0\text{ V}$, $f_c = 20\text{ MHz}$, PLL $\times 4$, CLKB = 80 MHz CLKP = 40 MHz CLKT = 40 MHz	—	—	50	mA	In sleep mode (When multiplication and addition calculator circuit is not used.)
				—	—	80	mA	In sleep mode (When multiplication and addition calculator circuit is used.)
	I_{CCH}	VCC	$V_{CC} = 5.0\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$	—	—	350	μA	In stop mode
			$V_{CC} = 5.0\text{ V}$, $T_A = +85\text{ }^\circ\text{C}$	—	—	1500	μA	In stop mode
Input capacitance	C_{IN}	Other than VCC, VSS, AVSS12, AVSS10, AVCC12, AVCC10, AVRH0, AVRH1, AVRH2, AVRH3, AVRH4	—	—	5	15	pF	

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (8 Kbytes sectors)	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	0.5	2.0	s	Not including time for internal writing before deletion.
Word write time	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	6	100	μs	Not including system-level overhead time.
Chip write time	$V_{CC} = 5.0 \text{ V}$, $T_A = +25 \text{ }^{\circ}\text{C}$	—	1.8	29.5	s	Not including system-level overhead time.
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data hold time	—	10	—	—	year	

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5. AC Characteristics

(1) Clock Timing

($V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$)

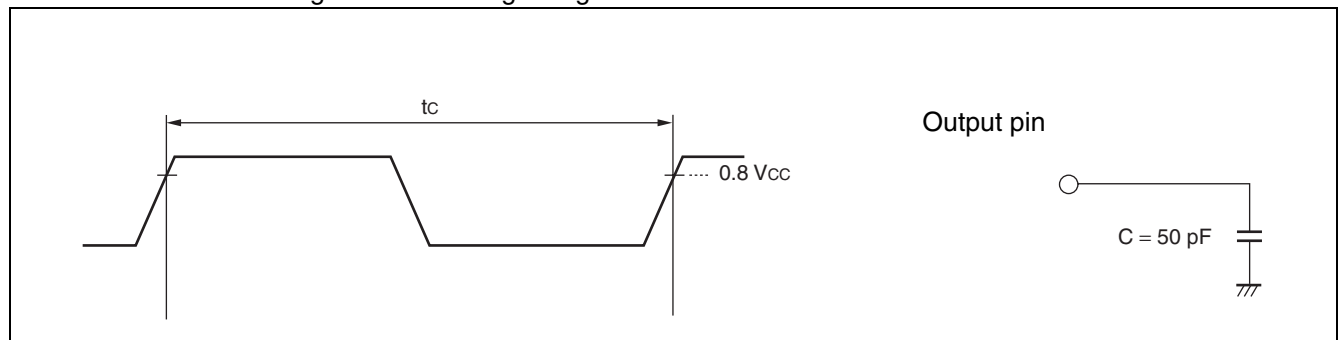
Parameter	Sym- bol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f _c	X0 X1	—	10*2	—	20	MHz	When using the PLL within the self-oscillating range, set the multiplier so that the internal clock does not exceed the internal operating clock frequency.
Clock cycle time	t _c	X0 X1		100	—	50*2	ns	
Internal operating clock frequency	f _{CPB}	—	When 20 MHz is input as the X0 clock frequency and the oscillator circuit PLL system is set to × 4 multiplication	5*1	—	80	MHz	CPU
	f _{CPP}			5*1	—	40	MHz	Peripheral
	f _{CPT}			5*1	—	40	MHz	External bus
Internal operating clock cycle time	t _{CPB}	—		12.5	—	200	ns	CPU
	t _{CPP}			25	—	200	ns	Peripheral
	t _{CPT}			25	—	200	ns	External bus

*1 : The values assume a gear cycle of 1/16.

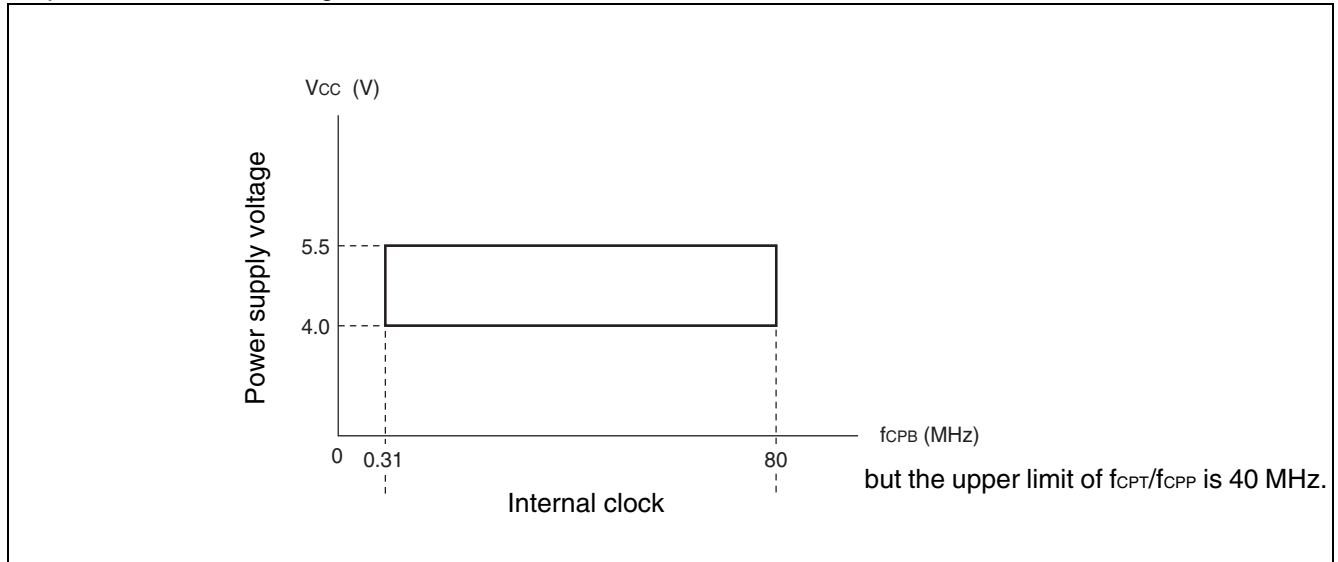
*2 : When the PLL is used, the PLL multiplication rate varies depending on the frequency of the clock input to the X0 and X1 pins. Set the PLL multiplication rate so that the PLL output clock frequency is in the range between 40 MHz and 80 MHz.

PLL Multiplication Rate	1	2	3	4	5	6	7	8
PLL output clock frequency when X0 = 10 MHz	(Setting not allowed)			40 MHz	50 MHz	60 MHz	70 MHz	80 MHz
PLL output clock frequency when X0 = 20 MHz	(Setting not allowed)	40 MHz	60 MHz	80 MHz	(Setting not allowed)			

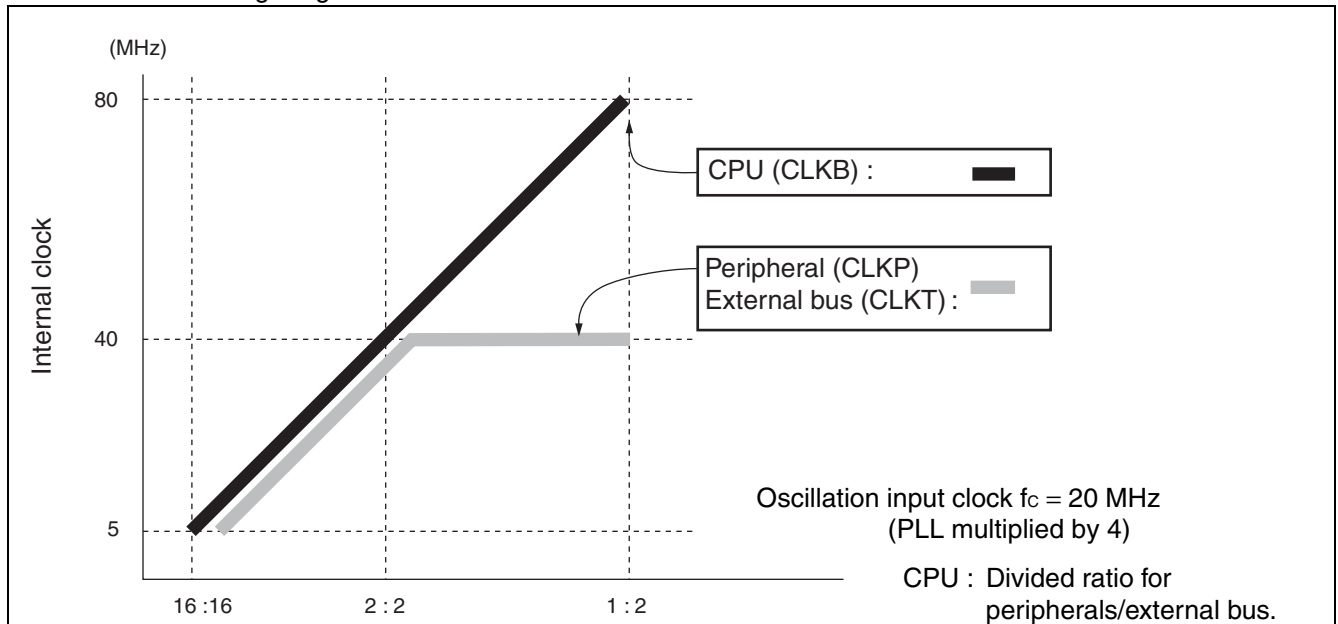
• Conditions for measuring the clock timing ratings



- Operation assurance range



- Internal clock setting range



- Notes :
- When the PLL is used, the external clock input should be in the range of 10 MHz to 20 MHz.
 - Treat the PLL oscillation stabilization time as $> 600 \mu s$
 - Set the internal clock gear setting to within the values shown in the “(1) Clock Timing” ratings table.

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(2) Clock Output Timing

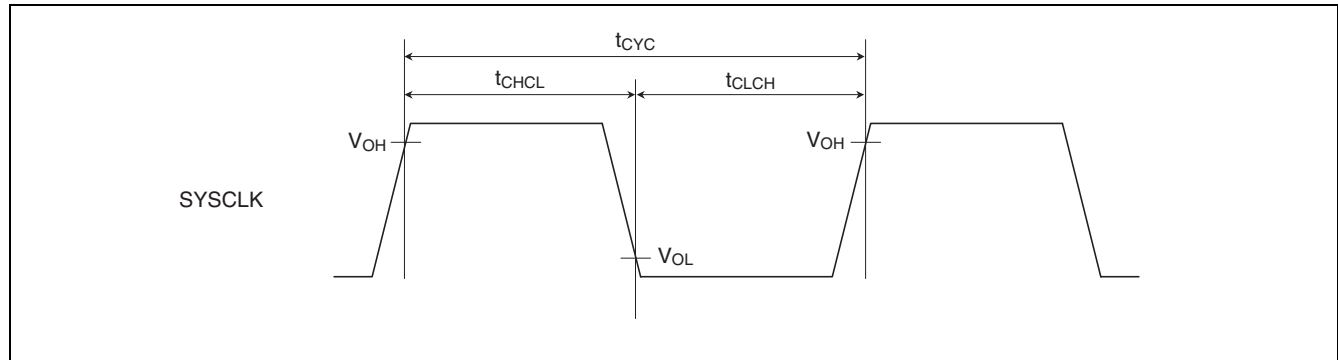
($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	*1
SYSCLK $\uparrow \rightarrow$ SYCSCLK $\downarrow$	t_{CHCL}			$t_{CYC}/2 - 5$	$t_{CYC}/2 + 5$	ns	*2
SYSCLK $\downarrow \rightarrow$ SYCSCLK $\uparrow$	t_{CLCH}			$t_{CYC}/2 - 5$	$t_{CYC}/2 + 5$	ns	

*1 : t_{CYC} is the frequency of one clock cycle including the gear cycle.

*2 : The following ratings are for the gear ratio set to $\times 2$. For the ratings when the gear ratio is set to $1/4$ and $1/8$, can be calculated by substituting $1/4$ or $1/8$ for n respectively in the following equation.
 $(1/2 \times 1/n) \times t_{CYC} - 5$

Note : For t_{CPT} (internal clock cycle time) , refer to “(1) Clock Timing”.



(3) PLL Oscillation stabilization time (LOCK UP TIME)

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
PLL Oscillation stabilization wait time (LOCK UP TIME)	t_{LOCK}^*	—	—	600	—	μs

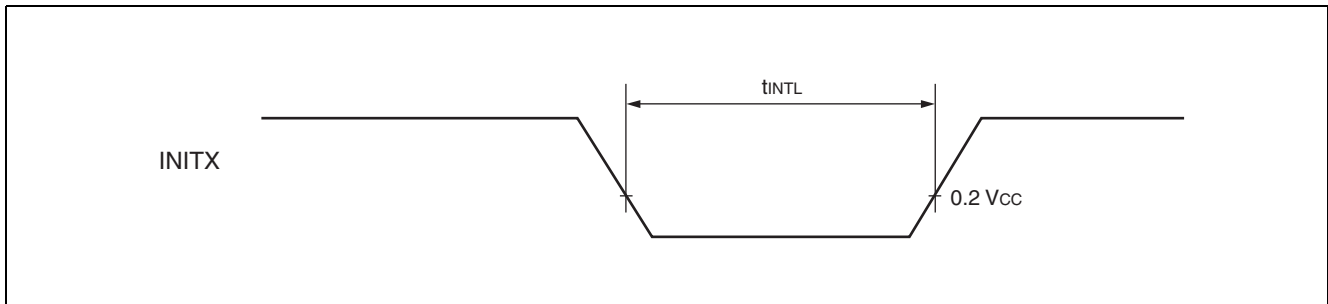
* : The length of time to wait for the PLL oscillations to stabilize.

(4) Reset Input Ratings

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on and stop mode)	t_{INTL}	INITX	—	Oscillation time of oscillator + $t_c \times 10$	—	ns
INITX input time (other than the above)				$t_c \times 10$	—	ns

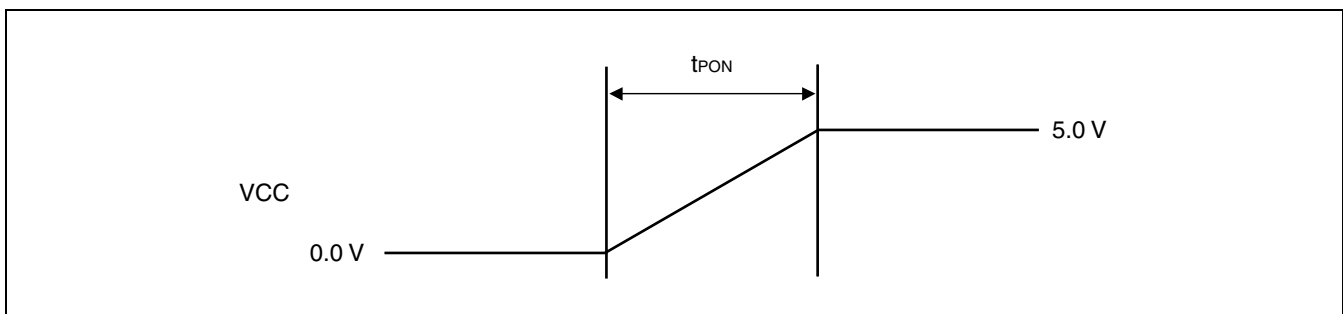
- Notes :
- It takes approximately $600\text{ }\mu\text{s}$ for the internal power to stabilize after the power supply has stabilized. Continue to input “L” level to the INITX pin during this period.
 - For t_{CPT} (internal clock cycle time) , refer to “(1) Clock Timing”.



(5) Power on Rise Time Ratings

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Power on rise time	t_{PON}	VCC	—	600	—	μs



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(6) Normal Bus Access Read/Write Operation

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
ASX setup	t_{ASLCH}	SYSCLK ASX	—	3	—	ns	
ASX hold	t_{CHASH}			3	$1/2 \times t_{CYC} + 10$	ns	
CS0X to CS2X setup	t_{CSLCH}	SYSCLK CS0X to CS2X	—	3	—	ns	
CS0X to CS2X hold	t_{CHCSH}			3	$1/2 \times t_{CYC} + 10$	ns	
Address setup	t_{ASCH}	SYSCLK A15 to A00	—	3	—	ns	
	t_{ASRL}	RDX A15 to A00		3	—	ns	
	t_{ASWL}	WR0X, WR1X A15 to A00		3	—	ns	
Address hold	t_{CHAX}	SYSCLK A15 to A00	—	3	$1/2 \times t_{CYC} + 10$	ns	
	t_{RHAX}	RDX A15 to A00		3	—	ns	
	t_{WHAX}	WR0X, WR1X A15 to A00		3	—	ns	
Valid address → Valid data input time	t_{AVDV}	A15 to A00 D31 to D16	—	—	$3/2 \times t_{CYC} - 7$	ns	*1 *2
RDX delay time	t_{CHRL}	SYSCLK RDX	—	—	10	ns	
	t_{CHRH}		—	—	10	ns	
RDX ↓ → Valid data input time	t_{RLDV}	RDX D31 to D16	—	—	$t_{CYC} - 5$	ns	*1
Data setup → RDX ↑ time	t_{DSRH}			18	—	ns	
RDX ↑ → Data hold time	t_{RHDX}			0	—	ns	
RDX minimum pulse width	t_{RLRH}	RDX	—	$t_{CYC} - 5$	—	ns	
WR0X, WR1X delay time	t_{CHWL}	SYSCLK RDX	—	—	10	ns	
	t_{CHWH}			—	10	ns	
Data setup → WR0X, WR1X ↑ time	t_{DSWH}	WR0X, WR1X D31 to D16	—	t_{CYC}	—	ns	
WR0X, WR1X ↑ → Data hold time	t_{WHDX}			3	—	ns	
WR0X, WR1X minimum pulse width	t_{WLWH}	WR0X, WR1X	—	$t_{CYC} - 5$	—	ns	

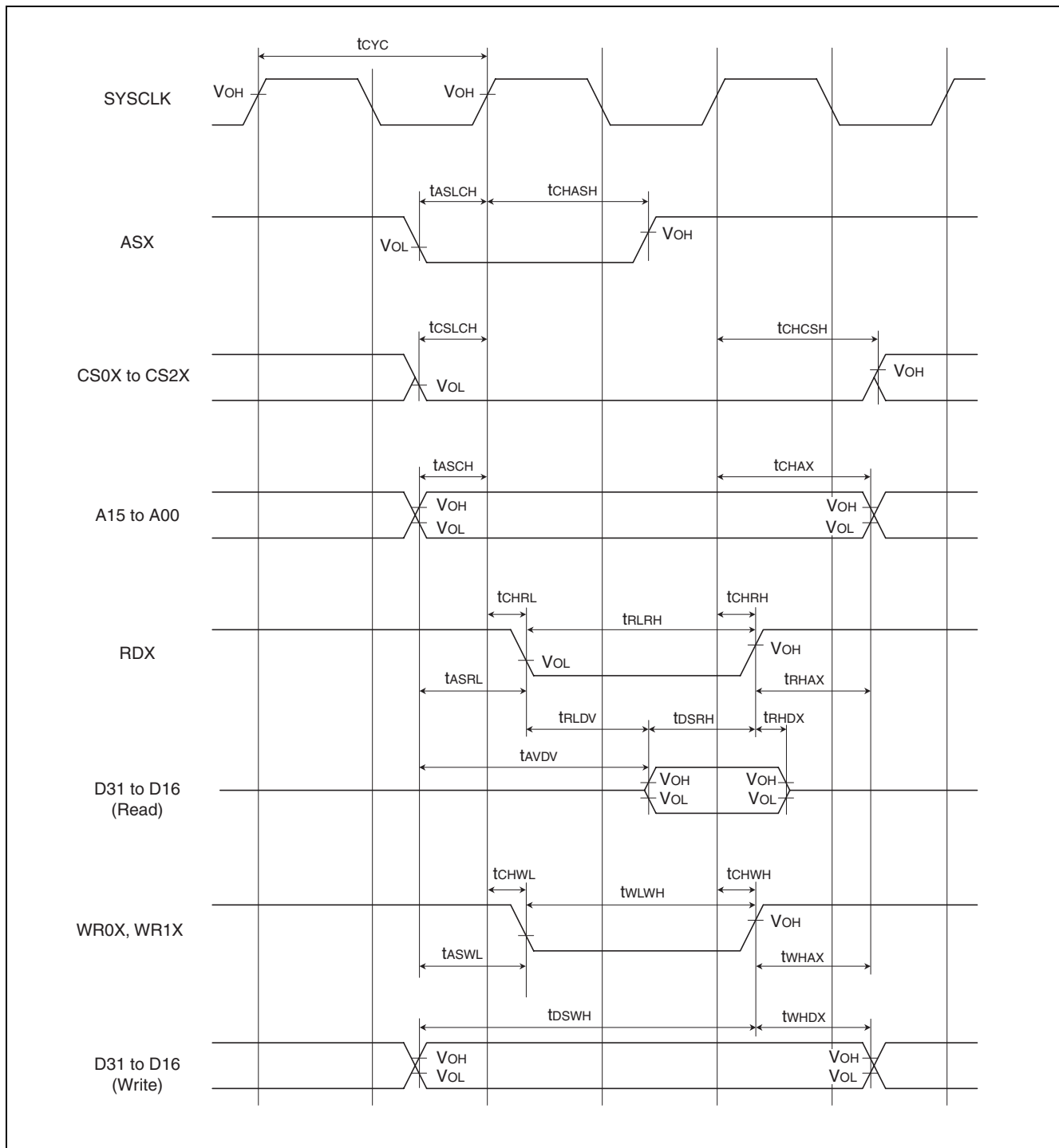
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MB91470/480 Series

(Continued)

- *1 : When the bus timing is delayed by an automatic wait instruction or RDY input, add the time ($t_{CYC} \times$ the number of delay cycles added) to this rating.

Note : Load capacitance $C = 50 \text{ pF}$



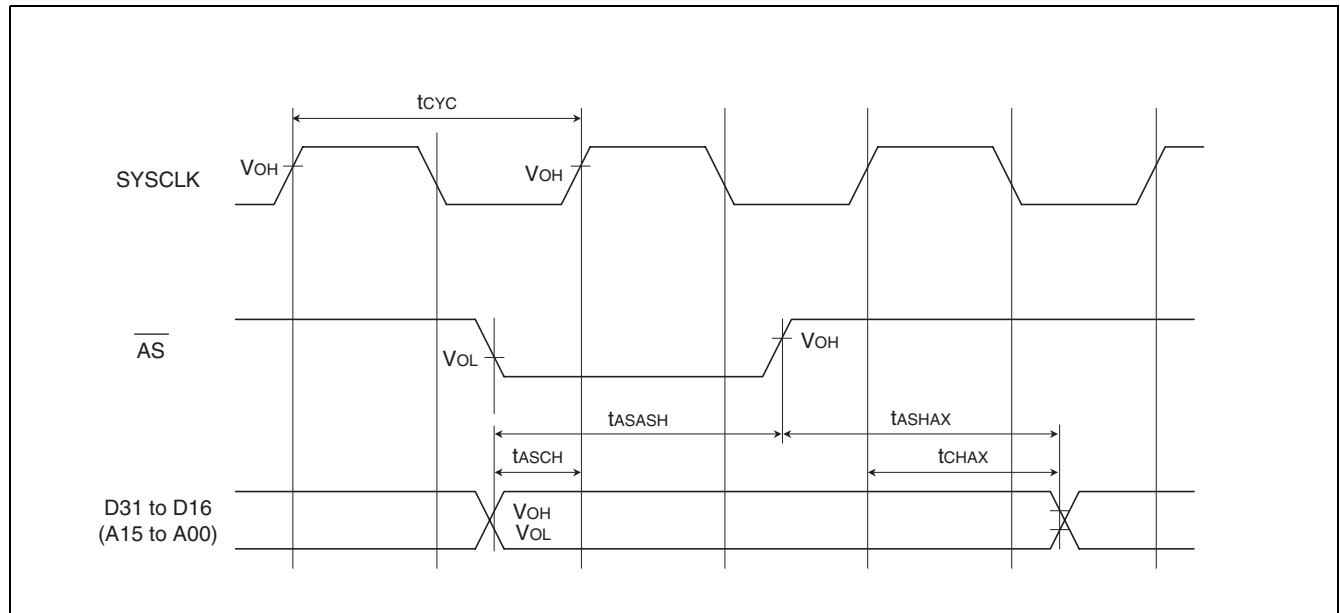
MB91470/480 Series

(7) Multiplex Bus Access Read/Write Operation

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
A15 to A00 address setup time $\rightarrow$ SYSCLK $\uparrow$	t_{ASCH}	SYSCLK, D31 to D16	—	3	—	ns
SYSCLK $\uparrow \rightarrow$ A15 to A00 address hold Time	t_{CHAX}			3	$1/2 \times t_{CYC} + 10$	ns
A15 to A00 address setup time $\rightarrow$ ASX $\uparrow$	t_{ASASH}	ASX, D31 to D16		12	—	ns
ASX $\uparrow \rightarrow$ A15 to A00 address hold time	t_{ASHAX}			$t_{CYC} - 5$	$t_{CYC} + 5$	ns

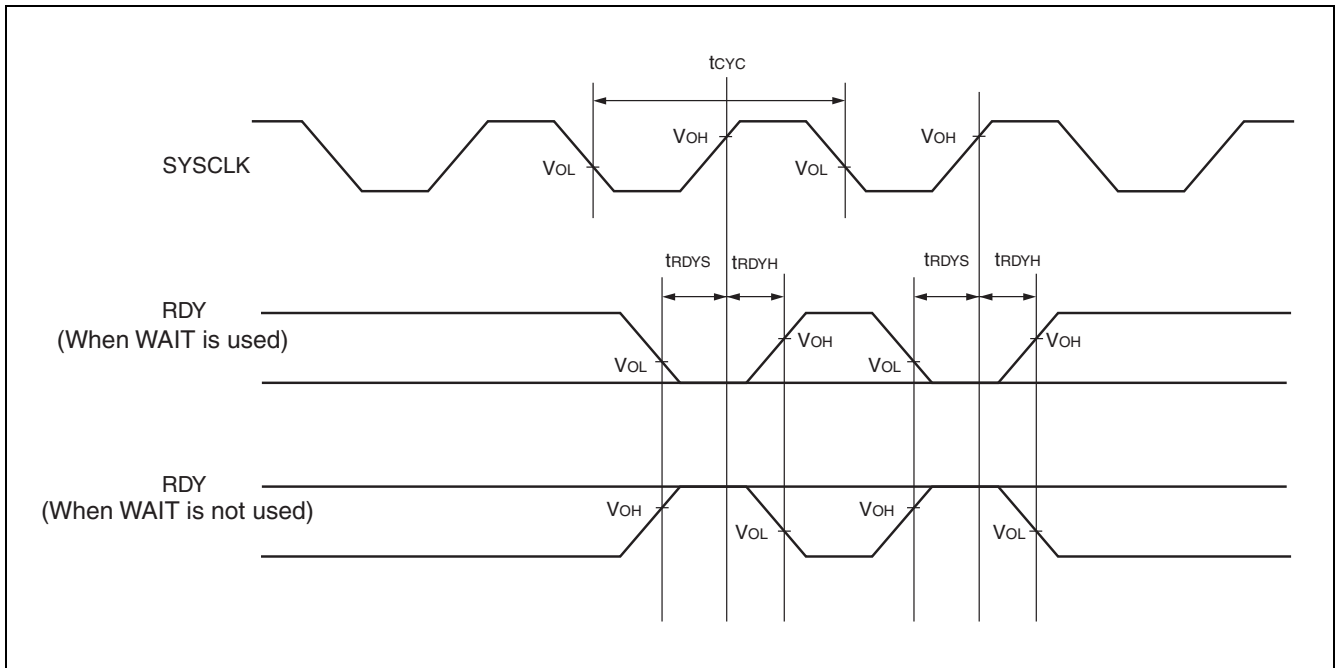
- Notes :
- This rating is not guaranteed when the CSX $\rightarrow$ RDX/WRX Setup Delay setting by AWR : bit1 is "0".
 - Normal bus interface ratings are applicable except this rating.
 - For t_{CYC} (cycle time), refer to "(2) Clock Output Timing".



(8) Ready Input Timing

($V_{CC} = 4.0 \text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
RDY setup time → SYSCLK ↑	t_{RDYS}	SYSCLK, RDY	—	18	—	ns
SYSCLK ↑ → RDY hold time	t_{RDYH}			0	—	ns



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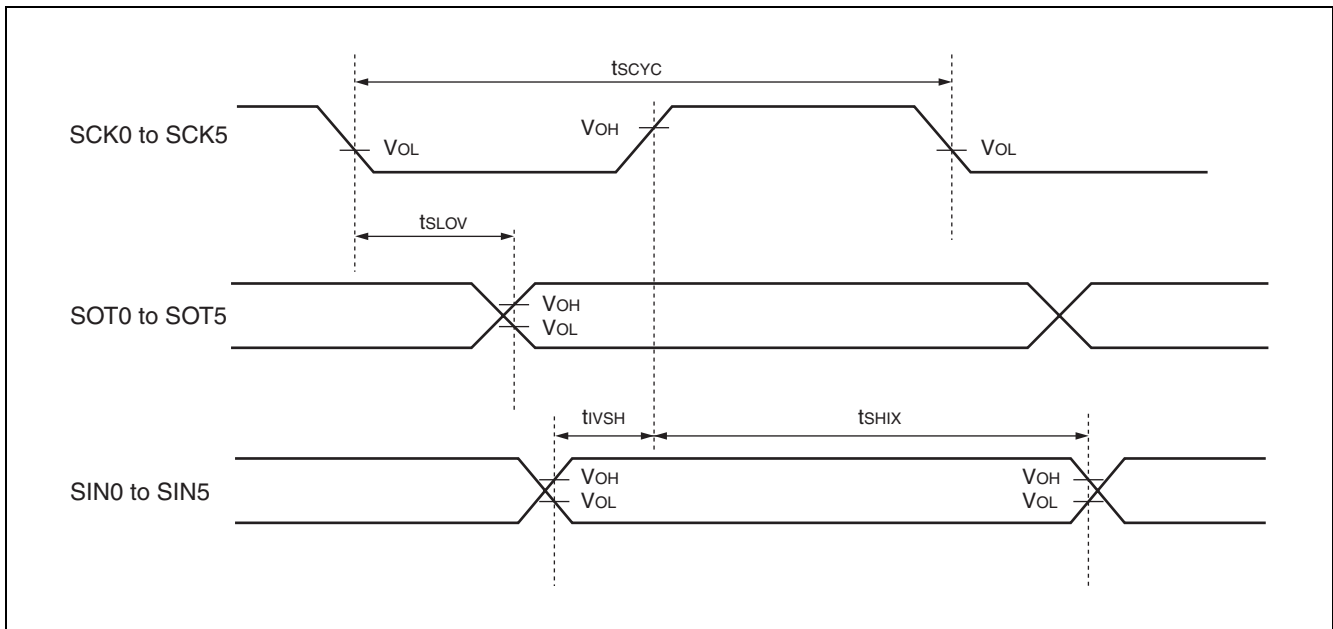
(9) UART Timing

($V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

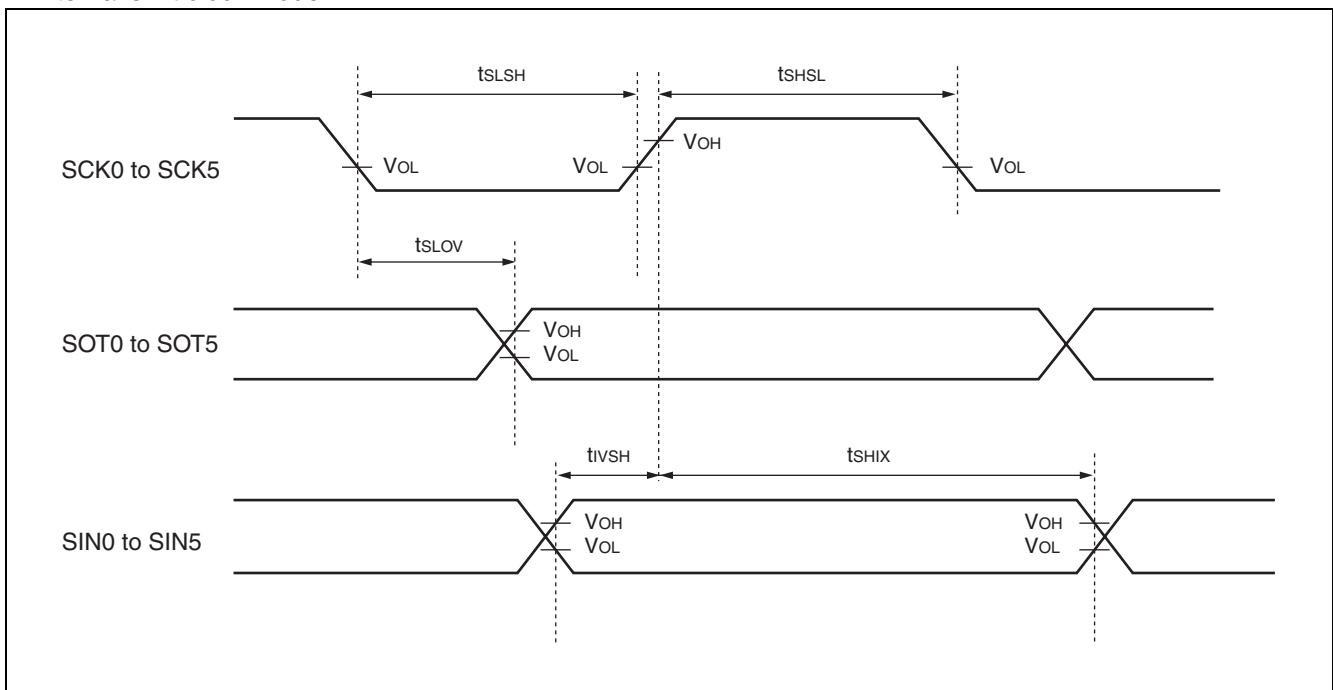
Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK5	Internal shift clock mode	$4t_{CYCP}$	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCK0 to SCK5 SOT0 to SOT5		- 20	+ 20	ns
Valid SIN→SCK↑	t_{IVSH}	SCK0 to SCK5 SIN0 to SIN5		30	—	ns
SCK↑→ Valid SIN hold time	t_{SHIX}	SCK0 to SCK5 SIN0 to SIN5		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK5	External shift clock mode	$2 \times t_{CYCP} - 10$	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK5		$t_{CYCP} + 10$	—	ns
SCK↓→SOT delay time	t_{SLOV}	SCK0 to SCK5 SOT0 to SOT5		—	25	ns
Valid SIN→SCK↑	t_{IVSH}	SCK0 to SCK5 SIN0 to SIN5		10	—	ns
SCK↑→ Valid SIN hold time	t_{SHIX}	SCK0 to SCK5 SIN0 to SIN5		20	—	ns

Notes : • The above ratings are the AC characteristics for CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

- Internal shift clock mode



- External shift clock mode



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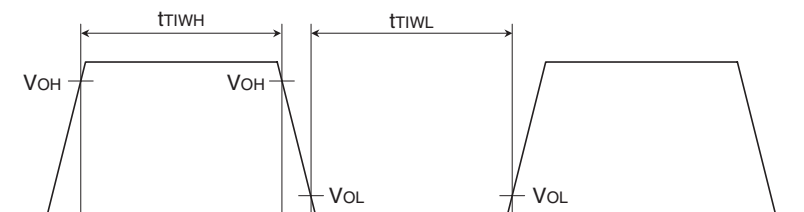
(10) Free-run Timer Clock, Up/Down Counter, Base Timer, and External Interrupt Input Timing

($V_{CC} = 4.0\text{ V}$ to 5.5 V , $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Free-run timer input clock pulse width	t_{TIWH} t_{TIWL}	CKI0, CKI1	—	$4 \times t_{CYCP}$	—	ns
Up-down counter input pulse width		AIN0 BIN0 ZIN0		$4 \times t_{CYCP}$	—	ns
Base timer input pulse width		TIN0 to TIN3		$4 \times t_{CYCP}$	—	ns
External interrupt input pulse width		INT0 to INT15		$4 \times t_{CYCP}$	—	ns
				1.0	—	μs

Note : t_{CYCP} indicates the peripheral clock cycle time.

CKI0, CKI1
AIN0, BIN0, ZIN0
TIN0 to TIN3
INT0 to INT15

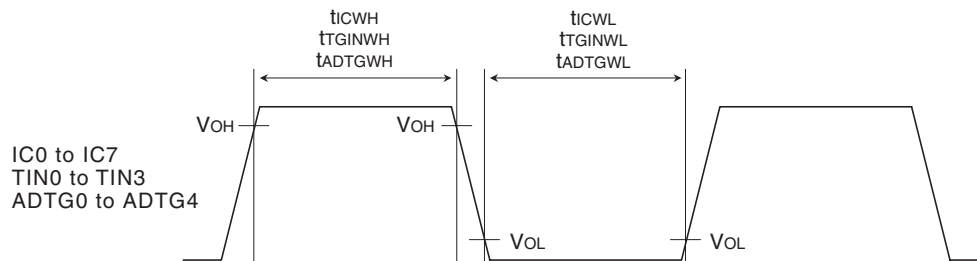


(11) Trigger Input Timing

($V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = AVSS12 = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Input Capture trigger input	t_{ICWH} t_{ICWL}	IC0 to IC7	—	$5 \times t_{CYCP}$	—	ns
Base timer trigger input	t_{TGINWH} t_{TGINWL}	TIN0 to TIN3		$4 \times t_{CYCP}$	—	ns
A/D activation trigger input	t_{ADTGWH} t_{ADTGWL}	ADTG0 to ADTG4		$5 \times t_{CYCP}$	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.



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(12) I²C Timing

a. Master Mode

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = AVSS10 = AVSS12 = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Sym- bol	Pin name	Condition	Standard Mode		Fast Mode* ³		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SDAn, SCLn	R=1 kΩ, C=50 pF* ⁴	0	100	0	400	kHz	
"L" width of the SCL clock	t _{LOW}			4.7	—	1.3	—	μs	
"H" width of the SCL clock	t _{HIGH}			4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t _{BUS}			4.7	—	1.3	—	μs	
SCL↓→ SDA output delay time	t _{DL DAT}			—	5 × t _{CYCP} * ¹	—	5 × t _{CYCP} * ¹	ns	
Setup time for a repeated START condition SCL↑→SDA↓	t _{SUSTA}			4.7	—	0.6	—	μs	
Hold time for a repeated START condition SDA↓→SCL↓	t _{HDSTA}			4.0	—	0.6	—	μs	The first clock pulse is generated after this.
Setup time for STOP condition SCL↑→SDA↑	t _{SUSTO}			4.0	—	0.6	—	μs	
SDA Data input hold time (vs. SCL↓)	t _{HDDAT}			2 × t _{CYCP} * ¹	—	2 × t _{CYCP} * ¹	—	μs	
SDA Data input setup time (vs. SCL↑)	t _{SUDAT}			250	—	100 * ²	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement

t_{SUDAT} ≥ 250 ns must then be met.

If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are the pull-up resistance and load capacitance of the SCL and SDA lines.

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b. Slave Mode

($V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AVSS10 = AVSS12 = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDAn, SCLn	$R=1\text{ k}\Omega$, $C=50\text{ pF}^{*4}$	0	100	0	400	kHz	
"L" width of the SCL clock	t_{LOW}			4.7	—	1.3	—	μs	
"H" width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	μs	
SCL $\downarrow \rightarrow$ SDA output delay time	t_{DLDAT}			—	$5 \times t_{CYCP}^{*1}$	—	$5 \times t_{CYCP}^{*1}$	ns	
Setup time for a repeated START condition SCL $\uparrow \rightarrow$ SDA $\downarrow$	t_{SUSTA}			4.7	—	0.6	—	μs	
Hold time for a repeated START condition SDA $\downarrow \rightarrow$ SCL $\downarrow$	t_{HDSTA}			4.0	—	0.6	—	μs	The first clock pulse is generated after this.
Setup time for STOP condition SCL $\uparrow \rightarrow$ SDA $\uparrow$	t_{SUSTO}			4.0	—	0.6	—	μs	
SDA Data input hold time (vs. SCL $\downarrow$)	t_{HDDAT}			$2 \times t_{CYCP}^{*1}$	—	$2 \times t_{CYCP}^{*1}$	—	μs	
SDA Data input setup time (vs. SCL $\uparrow$)	t_{SUDAT}			250	—	100 ^{*2}	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250\text{ ns}$ must then be met.

If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are pull-up resistance and load capacitance of the SCL and SDA lines.

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6. Electrical Characteristics for the A/D Converter

(1) 8/10-bit A/D Converter

($V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$, $AVRHn = 4.0 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AVSS10 = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 4	—	+ 4	LSB	When $AVRHn = 5.0 \text{ V}$
Linearity error	—	—	− 3.5	—	+ 3.5	LSB	
Differential linearity error	—	—	− 3	—	+ 3	LSB	
Zero transition voltage	V_{OT}	AN0-0 to AN0-3 AN1-0 to AN1-3 AN2-0 to AN2-11	$AVSS10-3.5$	$AVSS10+0.5$	$AVSS10+4.5$	LSB	
Full-scale transition voltage	V_{FST}	AN0-0 to AN0-3 AN1-0 to AN1-3 AN2-0 to AN2-11	$AVRHn-5.5$	$AVRHn-1.5$	$AVRHn+2.5$	LSB	
Conversion time*1	—	—	1.2	—	—	μs	
Analog port input current	I_{AIN}	AN0-0 to AN0-3 AN1-0 to AN1-3 AN2-0 to AN2-11	—	—	10	μA	
Analog input voltage	V_{AIN}	AN0-0 to AN0-3 AN1-0 to AN1-3 AN2-0 to AN2-11	$AVSS10$	—	$AVRHn$	V	
Reference voltage	—	$AVRHn$	$AVSS10$	—	$AVCC10$	V	
Power supply current (Analog + digital)	I_A	$AVCC10$	—	2	—	mA	For each 1 unit
	I_{AH}^{*2}	$AVCC10$	—	—	5	μA	
Reference voltage supply current (between $AVRH$ and $AVSS$)	I_R	$AVRHn$	—	1	—	mA	For each 1 unit, at $AVRHn = 5.0 \text{ V}$ $AVSS10 = 0 \text{ V}$
	I_{RH}^{*2}	$AVRHn$	—	—	5	μA	For each 1 unit, at stop mode
Analog input capacitance	—	—	—	—	12.5	pF	
Interchannel disparity	—	AN0-0 to AN0-3 AN1-0 to AN1-3 AN2-0 to AN2-11	—	—	4	LSB	

*1 : When $V_{CC} = AVCC10 = 5.0 \text{ V}$ and peripheral clock = 33 MHz

*2 : The current when the CPU is in stop mode and the A/D converter is not operating (at $V_{CC} = AVCC10 = AVRHn = 5.0 \text{ V}$).

Notes : • The above figures do not guarantee the accuracy between each unit.

• Output impedance of the external circuit $\leq 2 \text{ k}\Omega$.

• $AVRHn = AVRH0, AVRH1, \text{ and } AVRH2$

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(2) 12-bit A/D Converter

($V_{CC} = 4.0 \text{ V}$ to 5.5 V , $AVRHn = 4.0 \text{ V}$ to 5.5 V , $V_{SS} = AVSS12 = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	12	bit	
Linearity error	—	—	-3.6	—	+3.6	LSB	When $AVRHn = 5.0 \text{ V}$
Differential linearity error	—	—	-3	—	+3	LSB	
Zero transition voltage	V_{OT}	AN3-0 to AN3-3 AN4-0 to AN4-3	Typ - 20 mV	$AVSS12 + 0.5 \text{ LSB}$	Typ + 20 mV	—	
Full-scale transition voltage	V_{FST}	AN3-0 to AN3-3 AN4-0 to AN4-3	Typ - 20 mV	$AVRHn - 1.5 \text{ LSB}$	Typ + 20 mV	—	
Conversion time	—	—	2.0	—	—	μs	When peripheral clock = 33 MHz
			2.2	—	—	μs	When peripheral clock = 40 MHz
Analog port input current	I_{AIN}	AN3-0 to AN3-3 AN4-0 to AN4-3	—	—	10	μA	
Analog input voltage	V_{AIN}	AN3-0 to AN3-3 AN4-0 to AN4-3	$AVSS12$	—	$AVRHn$	V	
Reference voltage	—	$AVRHn$	$AVSS12$	—	$AVCC12$	V	
Analog supply current (analog + digital)	I_A	$AVCC12$	—	2	—	mA	For each unit
	I_{AH}^*	$AVCC12$	—	—	5	μA	
Reference voltage supply current (between $AVRH$ and $AVSS$)	I_R	$AVRHn$	—	1	—	mA	For each unit, at $AVRHn = 5.0 \text{ V}$, $AVSS12 = 0 \text{ V}$
	I_{RH}^*	$AVRHn$	—	—	5	μA	For each unit, at stop mode
Analog input capacitance	—	—	—	—	18	pF	
Interchannel disparity	—	AN3-0 to AN3-3 AN4-0 to AN4-3	—	—	4	LSB	

* : The current when the CPU is in stop mode and the A/D converter is not operating (at $V_{CC} = AVCC10 = AVRHn = 5.0 \text{ V}$).

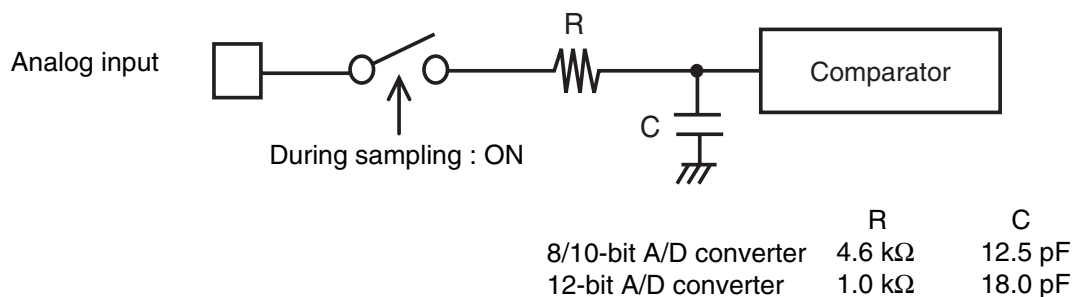
- Notes :
- The above figures do not guarantee the accuracy between each unit.
 - Output impedance of the external circuit $\leq 2 \text{ k}\Omega$
 - $AVRHn = AVRH3, AVRH4$

MB91470/480 Series

• External impedance and sampling time of analog inputs

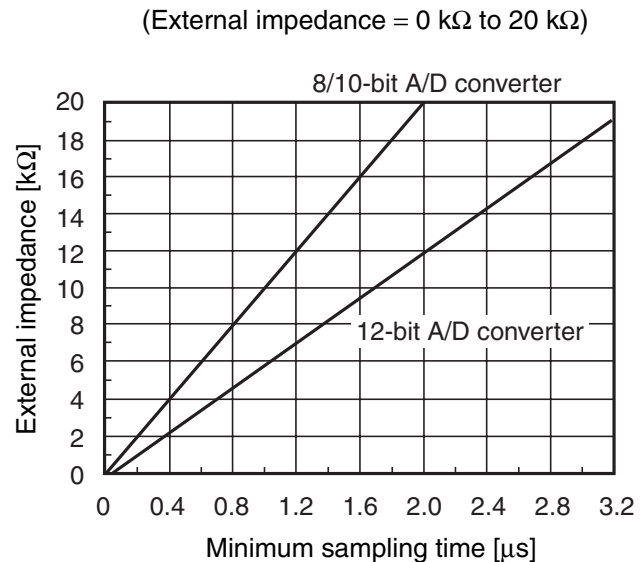
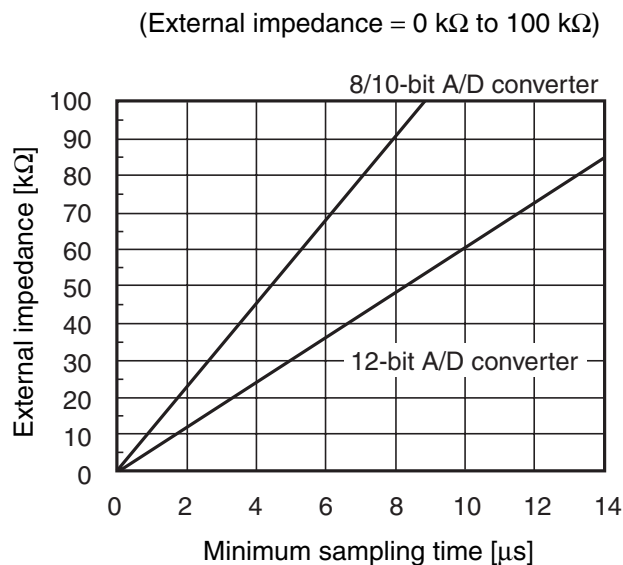
- The A/D converter is fitted with a sample and hold circuit. If the external impedance is so high that there is not sufficient time for sampling, the internal sample and hold capacitor will not fully charge to the analog voltage, and the precision of the A/D conversion will be adversely affected. Therefore, in order to satisfy the A/D conversion precision specifications, either adjust the register values and operating frequency or reduce the external impedance so that the sampling time is greater than the minimum value as given by the relationship between external impedance and minimum sampling time. If you are still unable to hold enough sampling time, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input circuit schematic



Note : The values are reference values.

• The relationship between the external impedance and minimum sampling time

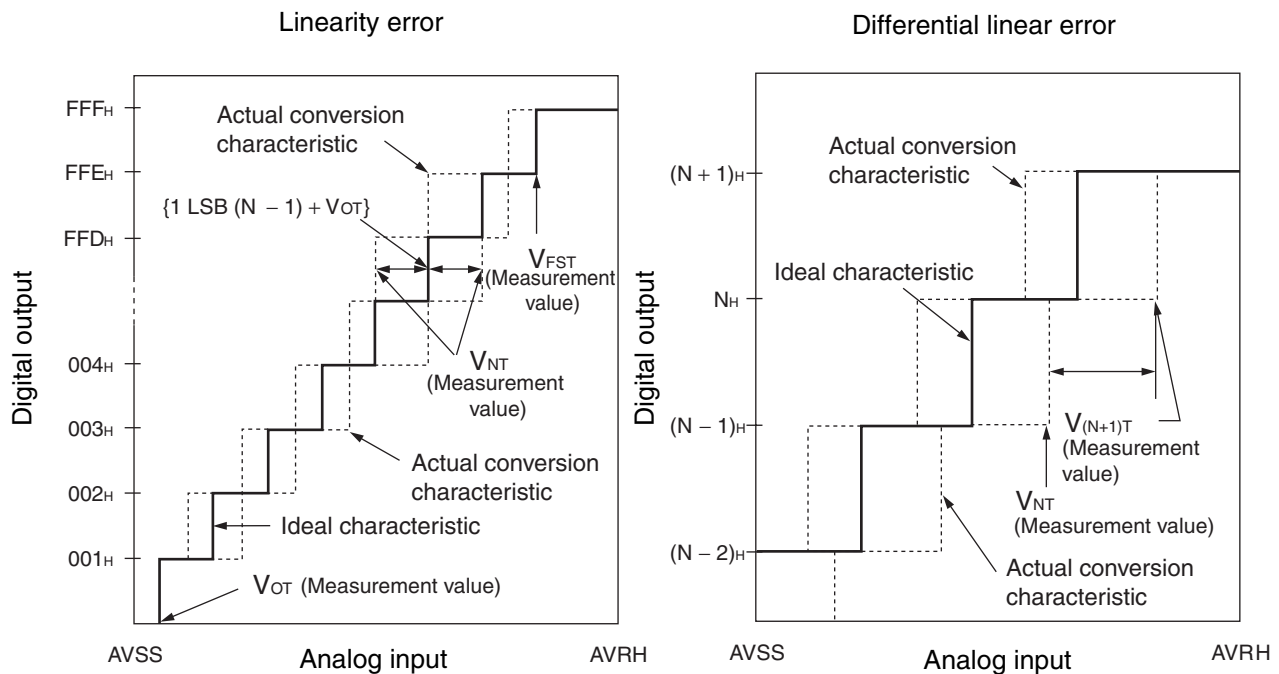


• About errors

- The relative error increases as the value of $|AVRH - AVSSI|$ decreases.

• Definition of 8/10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Linearity error : Deviation between the line connecting zero transition point (0000000000←→0000000001) and full-scale transition point (1111111110←→1111111111) and actual conversion characteristics.
- Differential linear error : Deviation from the ideal value of input voltage necessary to change the output code by 1LSB.
- Total Error : This error is the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error.



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} [\text{LSB}]$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output changes from 000_H to 001_H.

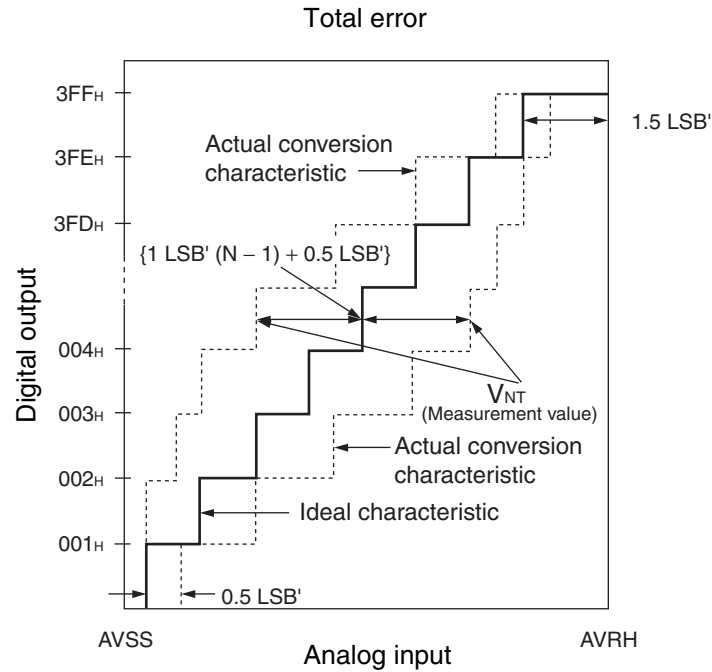
V_{FST} : Voltage at which digital output changes from 3FE_H to 3FF_H.

V_{NT} : Voltage at which digital output changes from (N - 1)_H to N_H.

(Continued)

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(Continued)



$$1 \text{ LSB}' (\text{ideal value}) = \frac{\text{AVRH} - \text{AVSS}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value

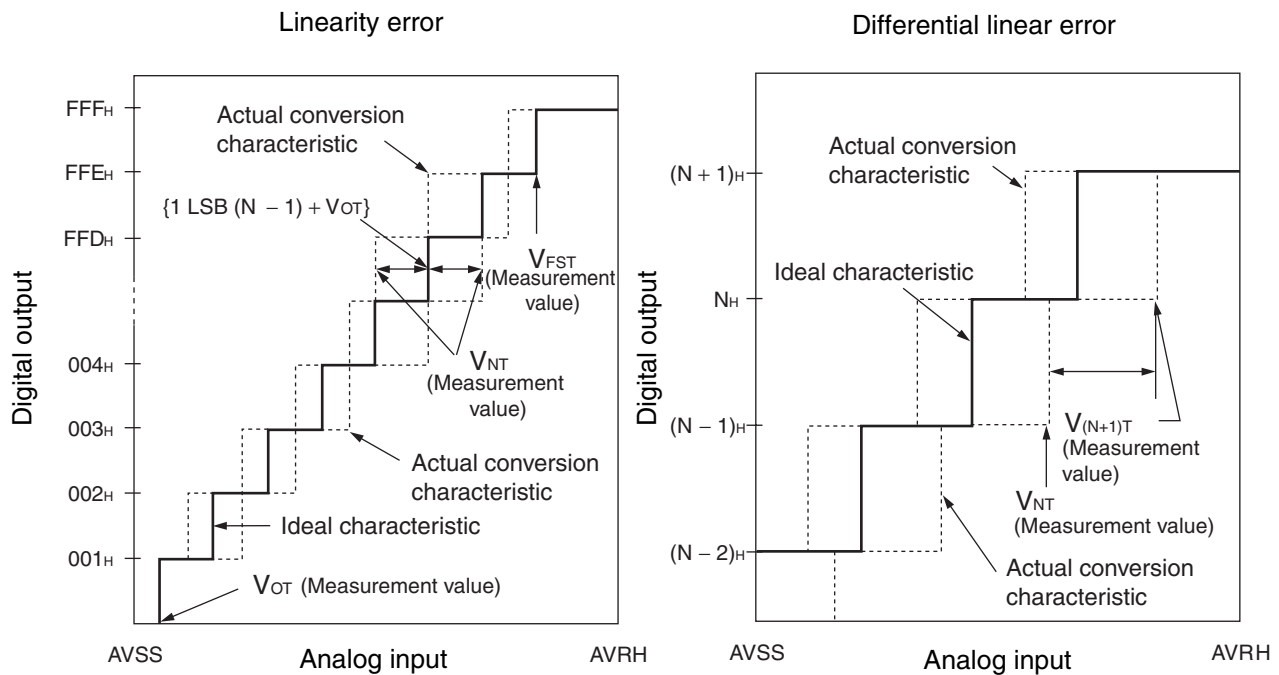
V_{NT} : Voltage at which digital output changes from $(N + 1)_H$ to N_H .

V_{OT}' (ideal value) = $\text{AVSS} + 0.5 \text{ LSB}'$ [V]

V_{FST}' (ideal value) = $\text{AVRH} - 1.5 \text{ LSB}'$ [V]

• Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Linearity error : Deviation between the line connecting zero transition point (000000000000 $\longleftrightarrow$ 000000000001) and full-scale transition point (111111111110 $\longleftrightarrow$ 111111111111) and actual conversion characteristics.
- Differential linear error : Deviation from the ideal value of input voltage necessary to the output code by 1LSB.



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + V_{OT}\}}{1 \text{ LSB}'} \text{ [LSB]}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}'} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{4094}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output changes from 000_H to 001_H.

V_{FST} : Voltage at which digital output changes from FFE_H to FFF_H.

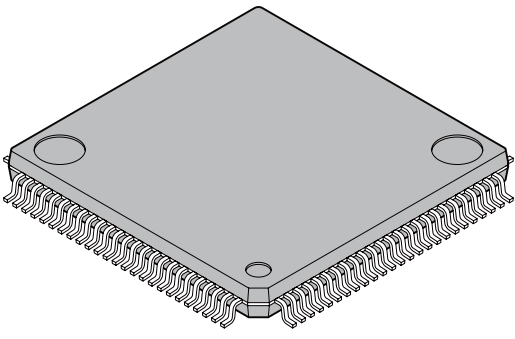
V_{NT} : Voltage at which digital output changes from (N - 1)_H to N_H.

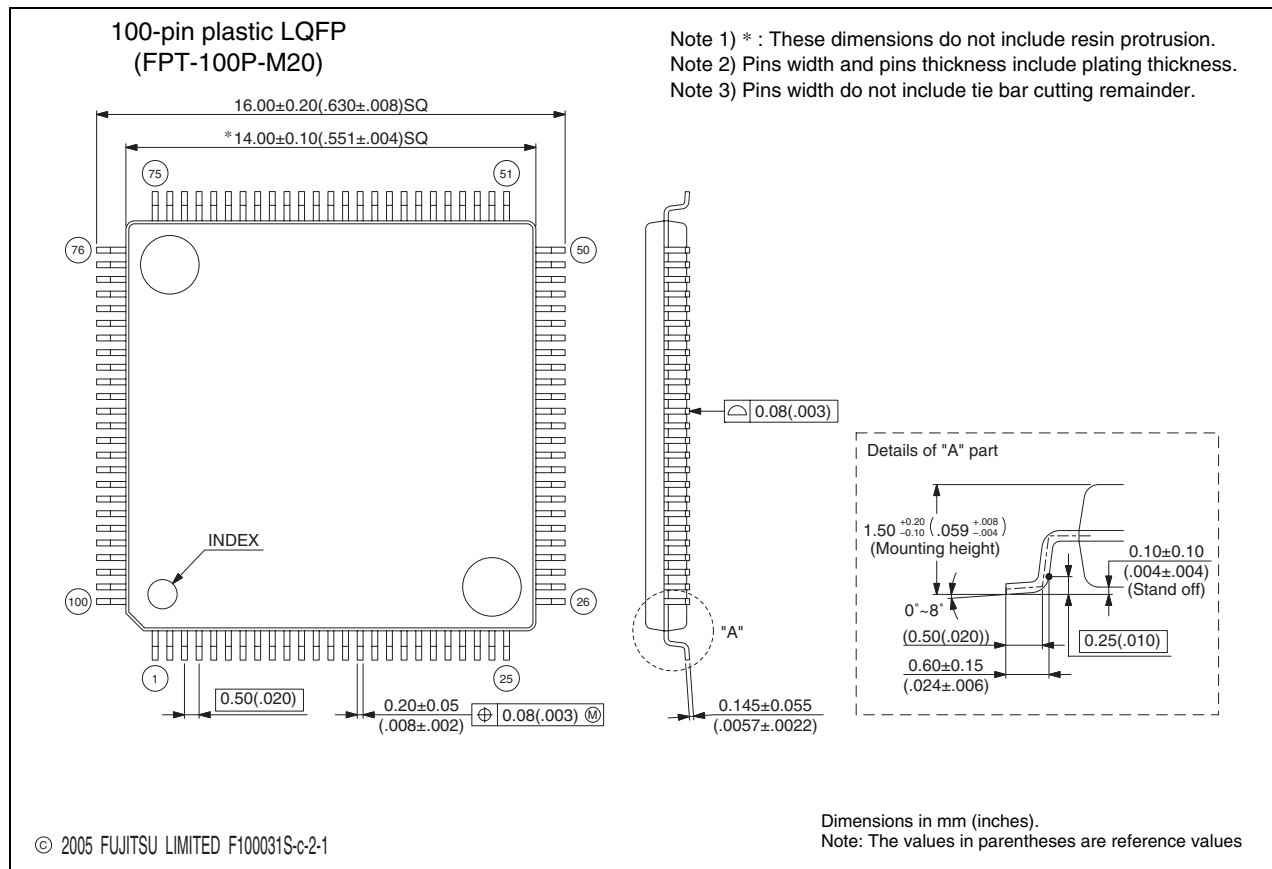
MB91470/480 Series

■ ORDERING INFORMATION

Part No.	Package
MB91F475PMC1-GE1	FPT-144P-M12
MB91F475BGL-GE1	BGA-144P-M06
MB91F478PMC1-GE1	FPT-144P-M12
MB91F478BGL-GE1	BGA-144P-M06
MB91F479PMC1-GE1	FPT-144P-M12
MB91F479BGL-GE1	BGA-144P-M06
MB91F487PMC-GE1	FPT-100P-M20
MB91F482PMC-GE1	
MB91482PMC-GE1	

■ PACKAGE DIMENSIONS

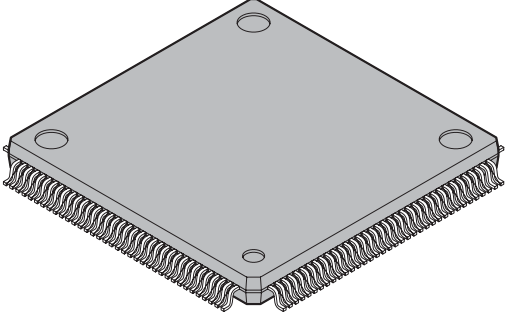
 100-pin plastic LQFP (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

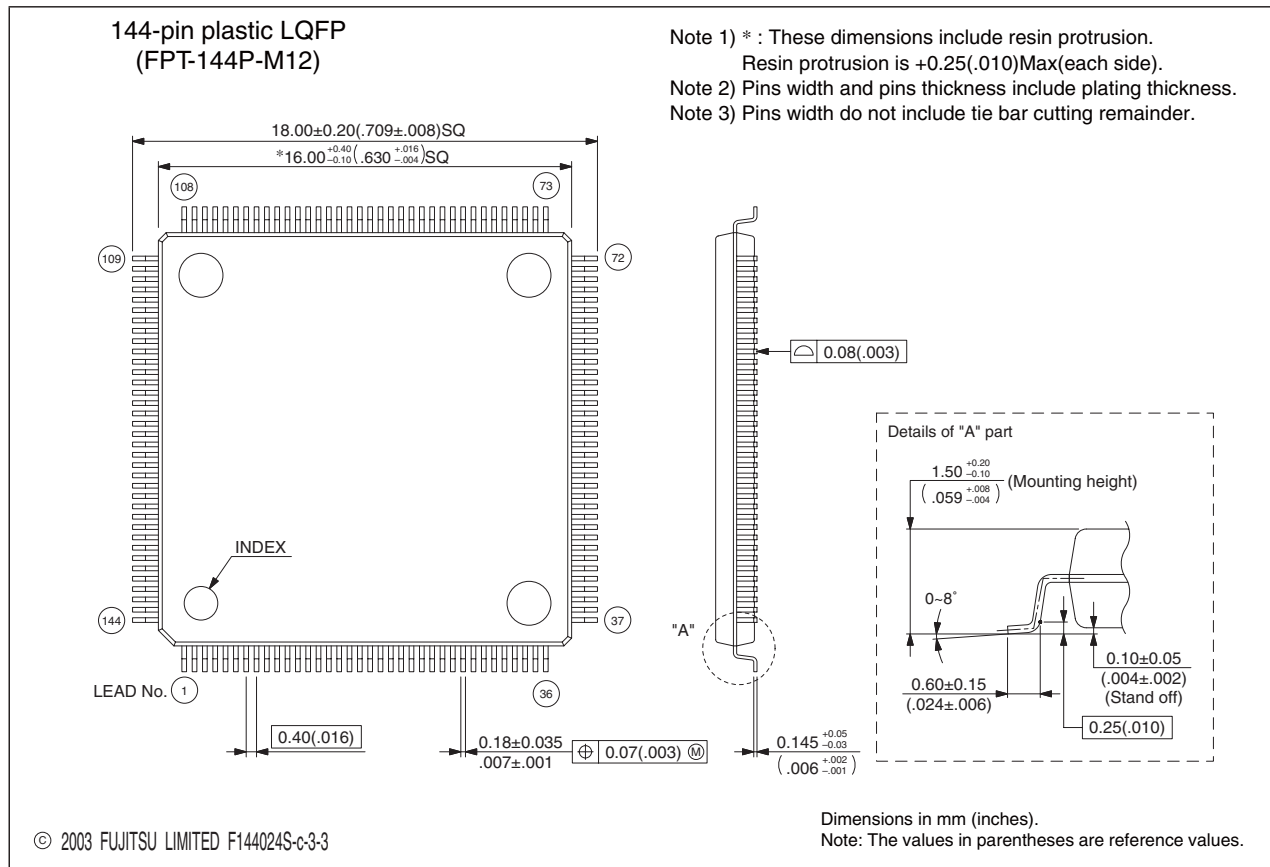


Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

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MB91470/480 Series

144-pin plastic LQFP  (FPT-144P-M12)	Lead pitch	0.40 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP144-16×16-0.40

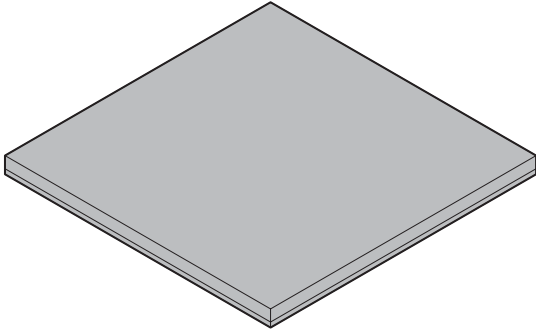


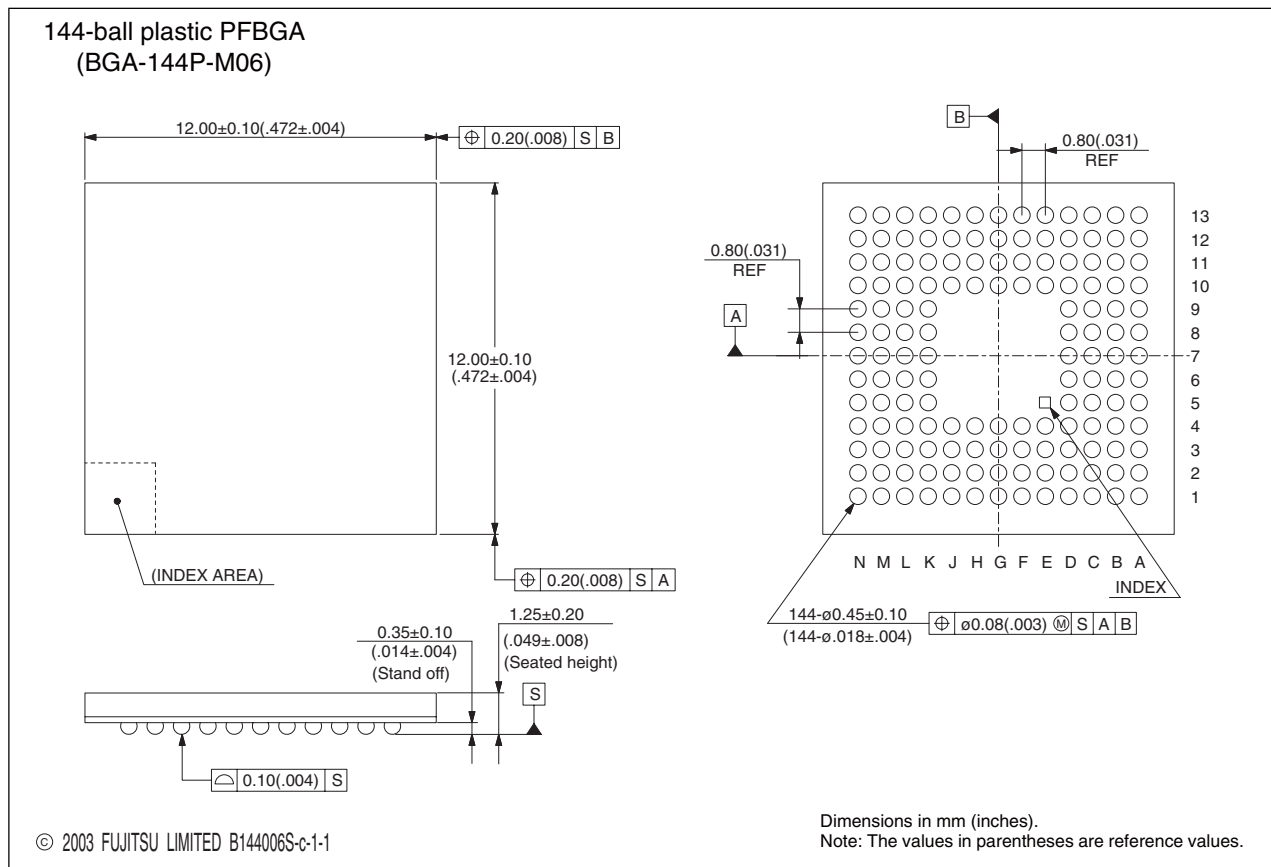
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

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MB91470/480 Series

(Continued)

144-ball plastic PFBGA  (BGA-144P-M06)	Ball pitch	0.80 mm
	Package width × package length	12.00 × 12.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Ø0.45 mm
	Mounting height	1.45 mm Max.
	Weight	0.32 g



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MB91470/480 Series

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the part number; MB91F482.
2	■ FEATURES	Changed for the 8/10-bit A/D Converter (Successive comparison type); minimum conversion time for 33 MHz system clock minimum conversion time for 40 MHz system clock → minimum conversion time for 33 MHz peripheral clock minimum conversion time for 40 MHz peripheral clock
3		Changed for the 12-bit A/D Converter (successive approximation type); minimum conversion time for 33 MHz system clock minimum conversion time for 40 MHz system clock → minimum conversion time for 33 MHz peripheral clock minimum conversion time for 40 MHz peripheral clock
12, 14	■ PIN DESCRIPTIONS	Deleted the“(MB91480 series only)”
14		Changed the pin names and added the conditions in the function; PC0/AN2-0/SCK4→PC0/AN2-0/SCK4 (SCL4), (used in I ² C mode, SCL4) PC2/AN2-2/SOT4→PC2/AN2-2/SOT4 (SDA4), (used in I ² C mode, SDA4) PC3/AN2-3/SCK5→PC3/AN2-3/SCK5 (SCL5), (used in I ² C mode, SCL5) PC5/AN2-5/SOT5→PC5/AN2-5/SOT5 (SDA5), (used in I ² C mode, SDA5)
16		Changed the pin names and added the conditions in the function; PG0/SCK0→PG0/SCK0 (SCL0), (used in I ² C mode, SCL0) PG2/SOT0→PG2/SOT0 (SDA0), (used in I ² C mode, SDA0) PG3/SCK1→PG3/SCK1 (SCL1), (used in I ² C mode, SCL1)
17		Changed the pin names and added the conditions in the function; PG5/SOT1→PG5/SOT1 (SDA1), (used in I ² C mode, SDA1) PH0/SCK2→PH0/SCK2 (SCL2), (used in I ² C mode, SCL2) PH2/SOT2→PH2/SOT2 (SDA2), (used in I ² C mode, SDA2) PH3/SCK3→PH3/SCK3 (SCL3), (used in I ² C mode, SCL3) PH5/SOT3→PH5/SOT3 (SDA3), (used in I ² C mode, SDA3)
21		Added the *1,*2 and *3 in the “power supply pins and GND pins”.
22		Changed the figure of the circuit type of “C” and “D”.
23	■ I/O CIRCUIT TYPE	Changed the figure of the circuit type of “G” and “I”.
24		Changed the figure of the circuit type of “J”.
25	■ HANDLING DEVICES	Changed the description of • About mode pins (MD0 to MD2).
28	■ BLOCK DIAGRAM	Changed in the figure :• MB91470 series (144 pins) Downconversion circuit → Voltage Regulator
29		Changed in the figure :• MB91480 series (100 pins) Downconversion circuit → Voltage Regulator

(Continued)

Page	Section	Change Results
35	■ I/O MAP	Changed as follows the register of address 000044 _H . HCRL→HRCL
37		Changed the register's initial values after the reset of address 0000AC _H . OCSH1“-1100000”→ OCSH1“-110--00”, OCSH3“-1100000”→ OCSH3“-110--00”
40		Changed the register's initial values after the reset of address 0000B0 _H . OCSH5“-1100000”→ OCSH5“-110--00”
41		Changed the register's initial values after the reset of address 000160 _H . BT0TMCR“00000000 00000000”→BT0TMCR“-0000000 00000000”
41		Changed the register's initial values after the reset of address 0001AC _H . OCSH7“-1100000”→ OCSH7“-110--00”, OCSH9“-1100000”→ OCSH9“-110--00”
41		Changed the register's initial values after the reset of address 0001B0 _H . OCSH11“-1100000”→ OCSH11“-110--00”
48		Changed the register's initial values after the reset of address 000580 _H . BT1TMCR“00000000 00000000”→ BT1TMCR“-0000000 00000000”
48		Changed the register's initial values after the reset of address 000590 _H . BT2TMCR “00000000 00000000”→ BT2TMCR “-0000000 00000000”
49		Changed the register's initial values after the reset of address 0005A0 _H . BT3TMCR “00000000 00000000”→ BT3TMCR “-0000000 00000000”
51		Changed the register's initial values after the reset of address 007004 _H . FLWC “--11-011”→ FLWC “----011”
58, 59	■ PIN STATUS IN EACH CPU STATE	• Changed the pin status; Input disabled → Input enabled for the pins P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P56, P60, P61, P80 to P87, P90 to P97, PA0 to PA4, PB0 to PB7, PC0 to PC7, PD0 to PD3, PE0 to PE7, for the INITX = "H" during initialization.
58, 59		• Changed the pin status as follows for the pins P80 to P87, P90 to P97; Input enabled for HIZ = 1 in stop mode (when external interrupt is enabled only) → Output Hi-Z/Input “0” fixed Input enabled when interrupt function selected and enabled.
58, 59		• Changed for INITX="H" during initialization; Input disabled → Input enabled
63, 64	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Changed the power supply current; Typ value → Max value

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(Continued)

Page	Section	Change Results
69	■ ELECTRICAL CHARACTERISTICS 5. AC Characteristics	Changed the ratings of the (4) Reset Input Ratings. Oscillation time of oscillator $t_c \times 10 \rightarrow$ Oscillation time of oscillator $+ t_c \times 10$
74		Added the (5) Power on Rise Time Ratings
78		Changed the ratings of the (9) UART Timing.
79		Changed the standard, fast mode and unit for the master mode in the (12) I ² C Timing.
82		Changed the standard and fast mode for the slave mode in the (12) I ² C Timing.
82	6. Electrical Characteristics for the A/D Converter (2) 12-bit A/D Converter	Changed the “• External impedance and sampling time of analog inputs” Deleted the follows: • To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.
86	■ ORDERING INFORMATION	Changed the “ ■ ORDERING INFORMATION ”.

The vertical lines marked in the left side of the page show the changes.

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