PRELIMINARY
CONFIDENTIAL

CYWB0224ABS, CYWB0224ABM
CYWB0226ABS, CYWB0226ABM

West Bridge™: Astoria™ USB and Mass Storage Peripheral Controller

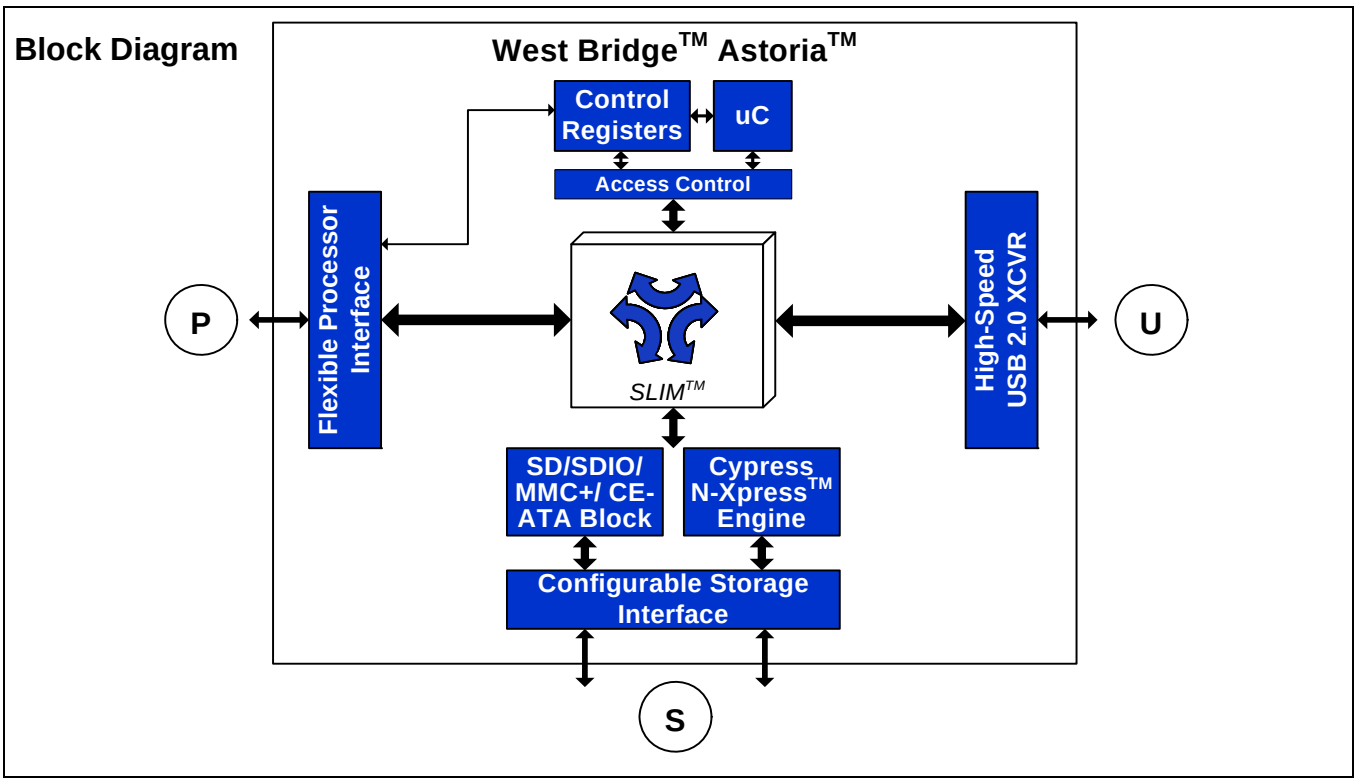
Features

- N-Xpress™ NAND controller technology
  - Interleave up to 16 NANDs with 8 chip enables (CE#) for x8 or x16 SLC (CYWB0224ABS) or MLC (CYWB0224ABM) NAND Flash devices
  - 4-bit error correction coding
  - Bad block management
  - Static wear leveling
- Multimedia device support
  - Up to 2 SD, SDIO, MMC, MMC+, and CE-ATA devices
- *SLIM*™ architecture, allowing simultaneous and independent data paths between the processor and USB, and between the USB and mass storage
- High speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB switch
  - Integrated USB 2.0 transceiver, smart serial interface engine
  - 16 programmable endpoints
- Flexible processor interface, which supports:
  - Multiplexing and nonmultiplexing address and data interface
  - SRAM interface
  - Pseudo CRAM interface (Antioch interface)
  - Pseudo NAND Flash interface
  - SPI (slave mode) interface
  - DMA slave support
- Ultra low power, 1.8V core operation
- Low power modes
- Small footprint, 6x6mm VFBGA
- Supports I2C boot and processor boot
- Selectable clock input frequencies
  - 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Portable Navigation Devices
- Digital Cameras
- POS Terminals
- Portable Video Recorders
- Data Cards and Wireless Dongles

Block Diagram



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Functional Overview

The *SLIM*™ Architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three different interfaces (P-port, S-port and U-port) to connect to one another independently.

With this architecture, connecting a device using Astoria to a PC through USB does not disturb any of the functions of the device. The device can still access mass storage at the same time the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models in which a PC can access a mass storage device independent of the main processor, or enumerate access to both the mass storage and the main processor at the same time.

In a handset, this typically enables using the phone as a thumb drive, downloading media files to the phone while still having full functionality available on the phone, or using the same phone as a modem to connect the PC to the web.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all the transactions between P-Port, S-Port, and U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports NAND, SD, SDIO, MMC+, and CE-ATA devices at the S-Port. For the NAND device, the 8051 firmware follows the smart media algorithm to support:

- Physical to logical management
- Four random bits ECC detection and correction support
- Wear leveling
- NAND Flash bad blocks handling

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory mapped registers through the processor interface. The configuration registers allow the system to specify certain behavior of Astoria. For example, it is able to mask certain status registers from raising an interrupt. The status registers convey various status, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface also can be configured to a pseudo NAND interface to support the processor's NAND interface. In addition, this interface can be configured to support SPI slave. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses can be performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers via the memory interface.

Access to these buffers is controlled by either using a DMA protocol or using an interrupt to the main processor. These two modes are configurable by the external processor.

As a DMA slave, Astoria generates a DMA request signal to signify to the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the Interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write, and it performs the appropriate read or write operations through the processor interface.

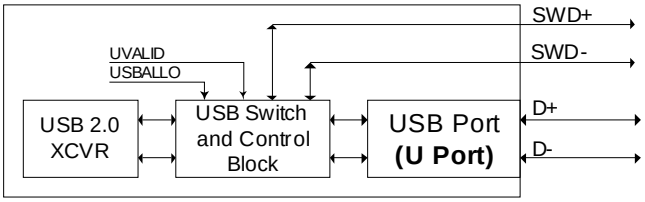
USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in Full Speed USB mode in addition to High Speed USB. The USB interface consists of the USB transceiver. The USB interface is accessible by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Astoria also has an integrated USB switch shown in Figure 1 that allows interfacing to an external Full Speed USB PHY.

Figure 1. U-Port With Switch and Control Block



Mass Storage Support (S-Port)

The S-Port is configurable in six different interface modes, either simultaneously supporting an SD/SDIO/MMC+/CE-ATA port and a 8-bit SLC or MLC NAND Flash ports, supporting two SD/SDIO/MMC+/CE-ATA ports, supporting up to eight Chip Enable (CE#) for 8-bit or 16-bit SLC or MLC NAND Flash port, supporting SD/SDIO/MMC+/CE-ATA port and GPIO, supporting NAND Flash port and GPIO, and GPIO. These configurations are controlled by the 8051 firmware. The 16-bit NAND Flash interface can only be used when there is no other mass storage device connected to the S-Port.

N-Xpress™ NAND Controller (S-Port)

Astoria, as part of its mass storage management functions, fully manages the SLC and MLC NAND Flash devices. The embedded 8051 manages the actual reading and writing of the NAND along with its required protocols. It performs standard NAND management functions such as ECC and wear leveling. The Astoria supports single bit ECC for the SLC and 4-bit ECC for MLC NAND Flash. SLC NAND Flash devices are supported by CYWB0244ABS. CYWB0244ABM supports both SLC and MLC NAND Flash devices.

S-Port Configuration Modes

The S Port is configurable in six different interface modes.

- NAND Flash and SD/SDIO/MMC/CE-ATA interface mode
- NAND Flash interface mode
- Dual SD/SDIO/MMC/CE-ATA interface mode
- SD/SDIO/MMC/CE-ATA and GPIO interface mode
- NAND Flash and GPIO interface mode
- GPIO interface mode

NAND Flash Interface Mode

The NAND Flash interface mode configures the S-Port to interface with NAND Flash devices only. In this interface mode, the S-Port is configured to interface up to sixteen 8-bit SLC or MLC NAND Flash

NAND Port (S-Port)

Astoria, as part of its mass storage management functions, fully manages the SLC and MLC NAND Flash devices. The embedded 8051 sets up reading and writing transaction of the NAND along with its required protocols. It performs standard NAND management functions such as ECC and wear leveling. The Astoria supports single bit ECC for the SLC and four bytes random ECC detection and correction for MLC NAND Flash.

SLC NAND Flash devices are supported by CYWB0244ABS. CYWB0244ABM supports both SLC and MLC NAND Flash devices.

SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured with firmware to support SD, SDIO, MMC+, and CE-ATA, this interface supports:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006.
- SD Specifications - Part E1 SDIO Specification, Version 1.10, August 18, 2004.
- CE-ATA Specification - CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005.

West Bridge Astoria provides support for 1-bit and 4-bit SD and SDIO cards, 1-bit, 4-bit and 8-bit MMC, MMC+ cards, and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command that are handled by the API.

Pin Assignments

Table 1. Astoria Pin Assignments

	Pin Name										Pin Description	Power Domain
	PCRAM Non Multiplexing	IO	PCRAM Multiplexing (ADM)	IO	SRAM	IO	PNAND	IO	SPI	IO		
P-Port	CLK (pull low in Asyn mode)	I	CLK (pull-low in Async mode)	I	Ext pull low	I	Ext pull low	I	SCK	I	Clock	PVDDQ VGND
	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	Chip Enable/PNAND Chip Select/SPI Slave Select	
	A0	I	Ext pull-up	I	A0	I	CLE	I	Ext pull-up	I	Addr. Bus 0/PNAND Command Latch	
	A1	I	Ext pull-up	I	A1	I	RB#	O	Ext pull-up	I	Addr. Bus 1/PNAND Ready_Buy	
	A[3:2]	I	A[2] = 1 A[3] = don't care	I	A[3:2]	I	A[3:2] = 00	I	A[3:2] = 10	I	Addr. Bus [3:2]	
	A4	I	Ext pull-up	I	A4	I	WP#	I	Ext pull-up	I	Addr. Bus 4/PNAND Write Protect	
	A5	I	SCL	IO	A5	I	SCL	IO	SCL	IO	Addr. Bus 5/I2C clock	
	A6	I	SDA	IO	A6	I	SDA	IO	SDA	IO	Addr. Bus 6/I2C data	
	A7	I	Ext pull-up	I	A7	I	A7 => 1:SBD A7 => 0: LBD	I	Ext pull-up	I	Addr. Bus 7	
	DQ[0]	IO	AD[0]	IO	DQ[0]	IO	IO[0]	IO	SDI	I	SPI Input/Data Bus 0	
	DQ[1]	IO	AD[1]	IO	DQ[1]	IO	IO[1]	IO	SDO	O	SPI Output/Data Bus 1	
	DQ[15:2]	IO	AD[15:2]	IO	DQ[15:2]	IO	IO[15:2]	IO	Ext pull-up	I	Data Bus	
	ADV#	I	ADV#	I		I	ALE	I	Ext pull-up	I	Address Valid	
	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull-up	I	Output Enable	
	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull-up	I	Write Enable	
DRQ & Int	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	Interrupt Request	GVDDQ VGND
	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull-up	I	DMA Acknowl-edgement	
U-Port	D+									IO/Z	USB D+	UVDDQ UVSSQ
	D-									IO/Z	USB D-	
	SWD+									IO/Z	USB Switch DP	
	SWD-									IO/Z	USB Switch DM	

Table 1. Astoria Pin Assignments (continued)

	SDIO & NAND Configuration	IO	NAND only Configuration	IO	Double SDIO Configuration	IO	NAND & GPIO Configuration	IO	SDIO & GPIO Configuration	IO	GPIO only Configuration	IO		
S-Port	SD_D[7:0]	IO	NAND_IO[15:8] or PD[7:0] (GPIO)	IO	SD_D[7:0]	IO	NAND_IO[15:8] or PD[7:0] (GPIO)	IO	SD_D[7:0]	IO	PD[7:0] (GPIO)	IO	SD Data bus/NAND Upper IO bus	SSVD-DQ VGND
	SD_CLK	O	NAND_CE8# or NAND_R/B4#	O I	SD_CLK	O	PC-7 (GPIO) or NAND_CE8# or NAND_R/B4#	IO O I	SD_CLK		PC-7 (GPIO)	IO	SD Clock, NAND CE8# or NAND R/B4#	
	SD_CMD	IO	NAND_CE7# or NAND_R/B3#	O I	SD_CMD	IO	PC-3 (GPIO) or NAND_CE7# or NAND_R/B3#	IO O I	SD_CMD	IO	PC-3 (GPIO)	IO	SD Command, NAND CE7# or NAND R/B4#	
	SD_POW	O	NAND_CE6#	O	SD_POW		PC-6 (GPIO) or NAND_CE6#	IO O	SD_POW		PC-6 (GPIO)	IO	SD Power Control/NAND CE6#	
	SD_WP	I	NAND_CE5#	O	SD_WP	I	PC-5 (GPIO) or NAND_CE5#	IO	SD_WP	I	N/C	I	GPIO (SD Write Protection Microswitch) or NAND CE5#	
	NAND_IO[7:0]	IO	NAND_IO[7:0]	IO	SD2_D[7:0]	IO	NAND_IO[7:0]	O	PB[7:0] (GPIO)	IO	PB[7:0] (GPIO)	IO	NAND Lower IO bus	SNVD-DQ VGND
	NAND_CLE	O	NAND_CLE	O	SD2_CLK	O	NAND_CLE	O	PA-6 (GPIO)	IO	PA-6 (GPIO)	IO	CMD Latch Enable	
	NAND_ALE	O	NAND_ALE	O	SD2_CMD	IO	NAND_ALE	O	PA-7 (GPIO)	IO	PA-7 (GPIO)	IO	Address Latch Enable	
	NAND_CE#	O	NAND_CE#	O	SD2_POW	O	NAND_CE#	O	PC-0 (GPIO)	IO	PC-0 (GPIO)	IO	Chip Enable	
	NAND_RE#	O	NAND_RE#	O	N/C	O	NAND_RE#	O	N/C	O	N/C	O	Read Enable	
	NAND_WE#	O	NAND_WE#	O	N/C	O	NAND_WE#	O	N/C	O	N/C	O	Write Enable	
	NAND_WP#	O	NAND_WP#	O	PA-5 (GPIO)	IO	NAND_WP#	I	PA-5 (GPIO)	IO	PA-5 (GPIO)	IO	Write Protect	
	NAND_R/B#	I	NAND_R/B#	I	N/C	I	NAND_R/B#	I	N/C	I	N/C	I	Ready/Busy	
	NAND_CE2#	O	NAND_CE2#	O	SD2_WP	O	NAND_CE2#	O	PC-2 (GPIO)	IO	PC-2 (GPIO)	IO	Chip Enable 2	
Other	RESETOUT / NAND_R/B2#	O I	NAND_R/B2#	I	RESETOUT	O	RESETOUT or NAND_R/B2#	0 I	RESETOUT	O	RESETOUT	O	RESET OUT or NAND Busy/Ready	GVDDQ VGND
	PC-4 (GPIO[0]) / SD_CD / NAND_CE4#	IO I O	NAND_CE4#	O	PC-4 (GPIO[0]) / SD_CD	IO I	PC-4 (GPIO[0]) or NAND_CE4#	IO O	PC-4 (GPIO[0]) or SD_CD	IO I	PC-4 (GPIO[0])	IO	General Input/Output 0 or SD/MMC Card Detection or NAND CE4#	
	PC-5 (GPIO[1]) / NAND_CE3#	IO O	NAND_CE3#	O	PC-5 (GPIO[1]) / SD2_CD	IO I	PC-5 (GPIO[1]) or NAND_CE3#	IO O	PC-5 (GPIO[1])	IO	PC-5 (GPIO[1])	IO	General Input/Output 1, NAND CE3#, or SD2_CD	
	RESET#											I	RESET	
	WAKEUP											I	Wake Up Signal	
Conf	XTALSLC[1:0]											I	Clock Select 0 and 1	GVDDQ VGND
	TEST[2:0]											I	Test Configuration	
Clock	XTALIN											I	Crystal/Clock IN	XVDDQ VGND
	XTALOUT											O	Crystal Out	

Table 1. Astoria Pin Assignments (continued)

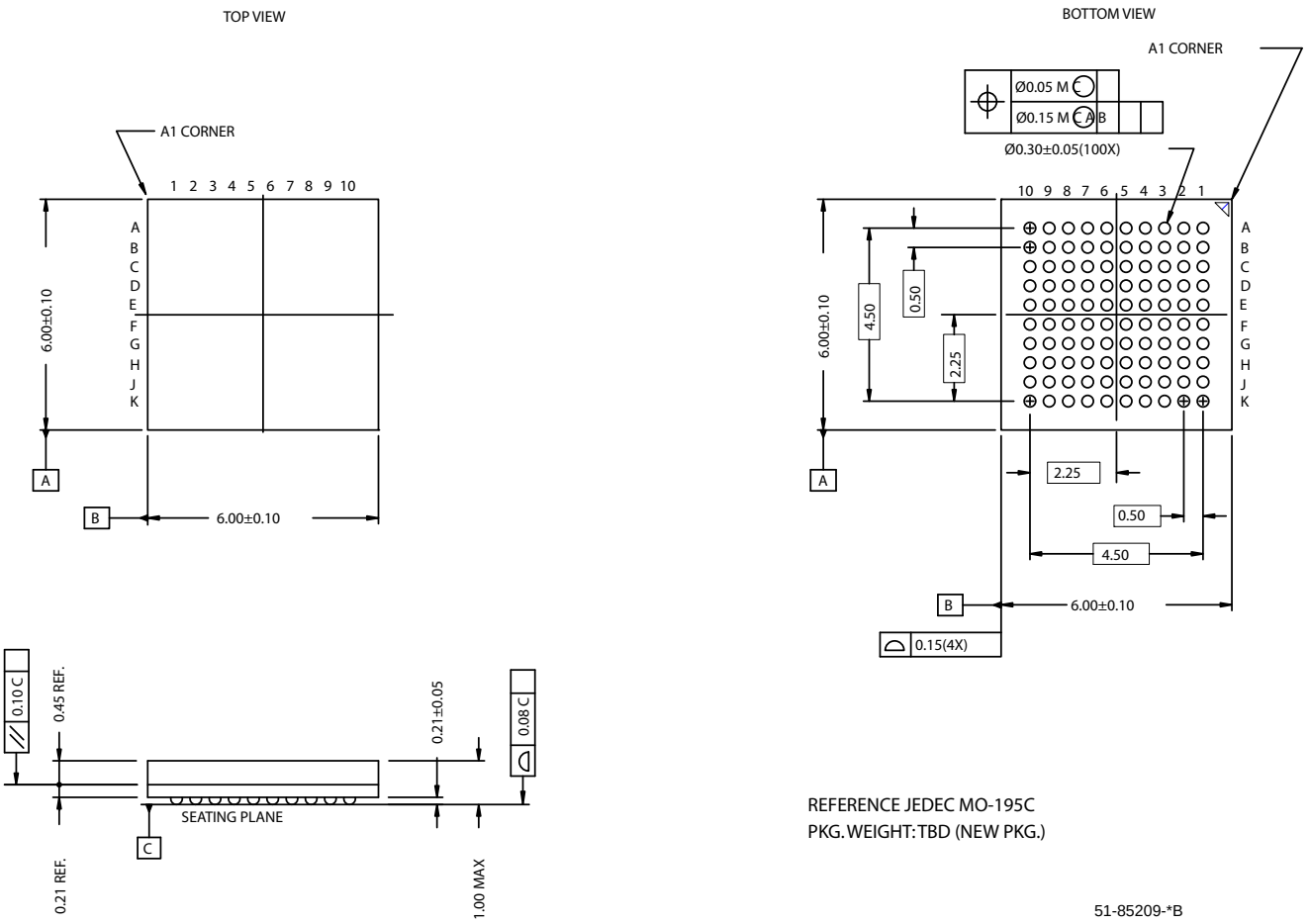
Power	PVDDQ	Power	Processor I/F VDD	
	SNVDDQ	Power	NAND VDD	
	UVDDQ	Power	USB VDD	
	SSVDDQ	Power	SDIO VDD	
	GVDDQ	Power	Misc IO VDD	
	AVDDQ	Power	Analog VDD	
	XVDDQ	Power	Crystal VDD	
	VDD	Power	Core VDD	
	VDD33	Power	Independent 3.3V	
	UVSSQ	Power	USB GND	
	AVSSQ	Power	Analog GND	
	VGND	Power	Core GND	

Ordering Information

Ordering Code	Package Type	NAND Flash Support	Available Clock Input Frequencies (MHz)
CYWB0224ABS-BVXI	100 VFBGA – Pb-Free	Support SLC NAND Flash only	19.2, 24, 26, 48
CYWB0224ABM-BVXI	100 VFBGA – Pb-Free	Support SLC and MLC NAND Flash	19.2, 24, 26, 48
CYWB0226ABS-BVXI	100 VFBGA – Pb-Free	Support SLC NAND Flash and USB switch	19.2, 24, 26, 48
CYWB0226ABM-BVXI	100 VFBGA – Pb-Free	Support SLC and MLC NAND Flash and USB switch	19.2, 24, 26, 48

Package Diagram

Figure 2. 100 VFBGA (6 x 6 x 1.0 MM) BZ100A



REFERENCE JEDEC MO-195C
PKG. WEIGHT: TBD (NEW PKG.)

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