



CYW4354

Single-Chip 5G Wi-Fi IEEE 802.11ac 2x2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and FM Receiver

The Cypress CYW4354 is a complete dual-band (2.4 GHz and 5 GHz) 5G Wi-Fi 2 x 2 MIMO[®] MAC/PHY/Radio System-on-a-Chip. This Wi-Fi single-chip device provides a high level of integration with dual-stream IEEE 802.11ac MAC/baseband/radio, Bluetooth 4.1, and FM radio receiver. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the rates specified in IEEE 802.11a/b/g/n are supported. Included on-chip are 2.4 GHz and 5 GHz transmit power amplifiers and receive low noise amplifiers.

For the WLAN section, several alternative host interface options are included: an SDIO v3.0 interface that can operate in 4b or 1b modes, a high-speed inter-chip (HSIC) interface, and a PCIe v3.0 compliant interface running at Gen1 speeds. For the Bluetooth section, host interface options of a high-speed 4-wire UART and USB 2.0 full-speed (12 Mbps) are provided.

The CYW4354 uses advanced design techniques and process technology to reduce active and idle power, and includes an embedded power management unit that simplifies the system power topology.

In addition, the CYW4354 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

| Broadcom Part Number | Cypress Part Number |
|----------------------|---------------------|
| BCM4354 | CYW4354 |
| BCM4354XKUBG | CYW4354XKUBG |
| BCM4354XKWBG | CYW4354XKWBG |
| BCM4354ZKUBG | CYW4354ZKUBG |

Features

IEEE 802.11X Key Features

- IEEE 802.11ac Draft compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Supports IEEE 802.11ac/n beamforming.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Supports various RF front-end architectures including:
 - Two antennas with one each dedicated to Bluetooth and WLAN.
 - Two antennas with WLAN diversity and a shared Bluetooth antenna.
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE or GPS.
- Supports standard SDIO v3.0 (up to SDR104 mode at 208 MHz, 4-bit and 1-bit) host interfaces.
- Backward compatible with SDIO v2.0 host interfaces.
- Alternative host interface supports HSIC v1.0
- PCIe mode complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen1 speeds.
- Integrated ARMCR4™ processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 768 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

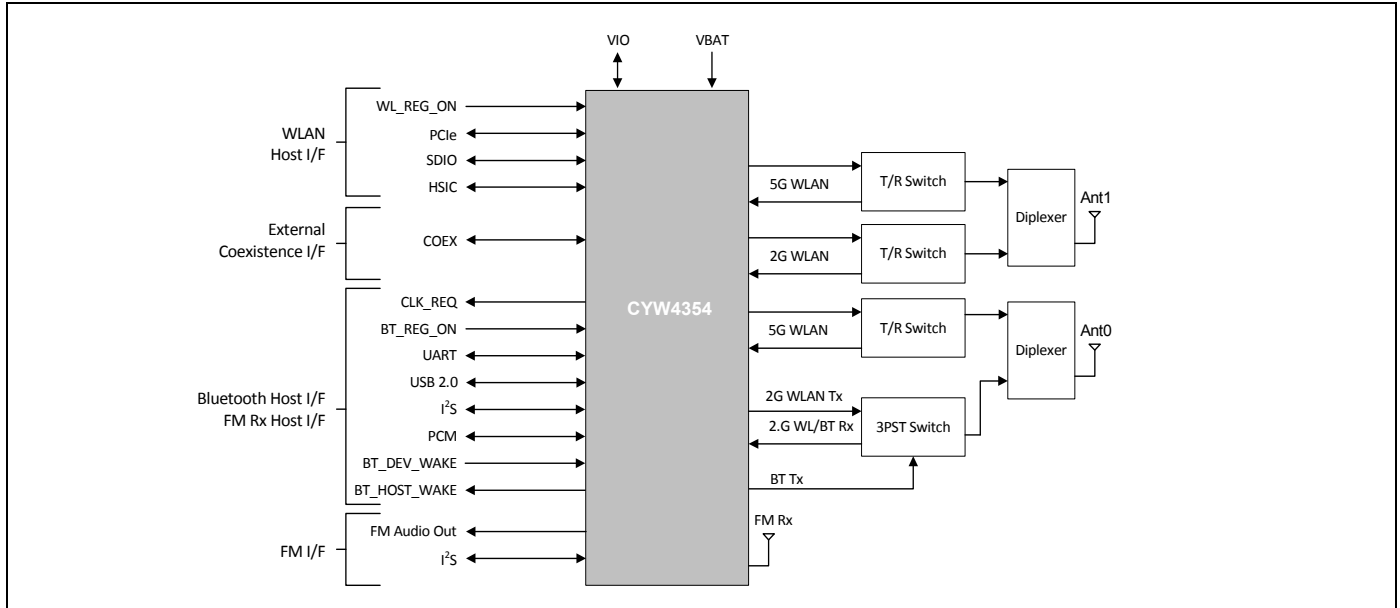
Bluetooth and FM Key Features

- Complies with Bluetooth Core Specification Version 4.1 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a USB or high-speed UART interface and PCM for audio data.
- USB 2.0 full-speed (12 Mbps) supported for Bluetooth.
- The FM unit supports HCI for communication.
- Low power consumption improves battery life of handheld devices.
- FM receiver: 65 MHz to 108 MHz FM bands; supports the European radio data systems (RDS) and the North American radio broadcast data system (RBDS) standards.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.
- Supports serial flash interfaces.

General Features

- Supports battery range from 3.0V to 5.25V supplies with internal switching regulator.
- Programmable dynamic power management
- 484 bytes of user-accessible OTP for storing board parameters
- GPIOs: 11 in WLBGA, 16 in WLCSP
- Package options:
 - 192-ball WLBGA (4.87 mm × 7.67 mm, 0.4 mm pitch)
 - 395-bump WLCSP (4.87 mm × 7.67 mm, 0.2 mm pitch)
- Security:
 - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
 - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
 - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
 - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Figure 1. Functional Block Diagram



IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<http://community.cypress.com/>)

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1. Overview

1.1 Overview

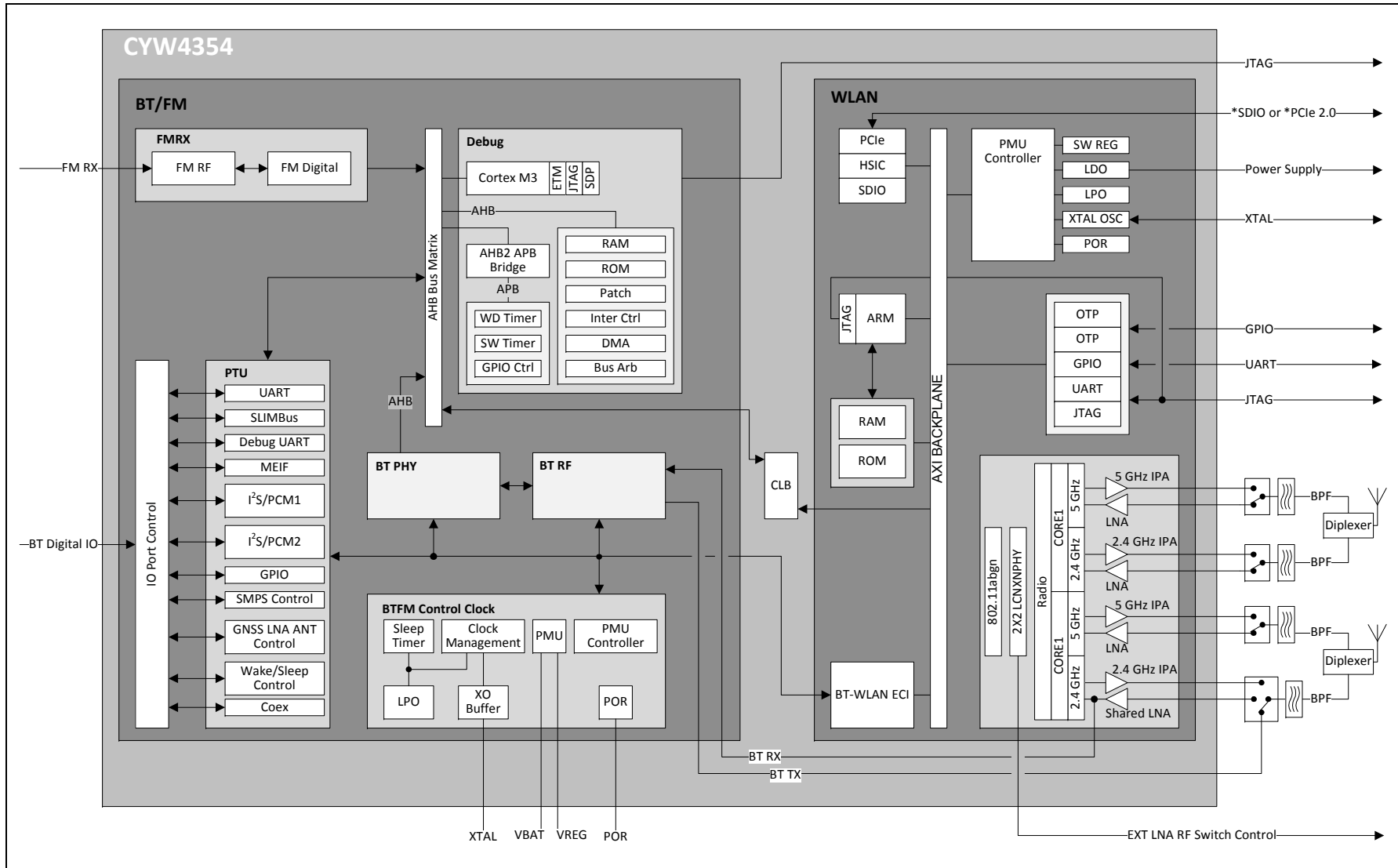
The Cypress CYW4354 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 a/b/g/n/ac MAC/baseband/radio, Bluetooth 4.1 + EDR (enhanced data rate), and FM receiver. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

[Figure 2 on page 7](#) shows the interconnect of all the major physical blocks in the CYW4354 and their associated external interfaces, which are described in greater detail in the following sections.

Table 2. Device Options and Features

| Feature | WLBGA | WLCSP |
|--------------------|--|-----------|
| Package ball count | 192 pins | 395 bumps |
| PCIe | Yes | Yes |
| USB2.0 (Bluetooth) | Yes | Yes |
| HSIC | Yes | Yes |
| I ² S | Multiplexed onto six parallel flash pins | No |
| GPIO | 11 | 16 |
| SDIO 3.0 | Yes | Yes |

Figure 2. CYW4354 Block Diagram



1.2 Features

The CYW4354 supports the following features:

- IEEE 802.11a/b/g/n/ac dual-band 2x2 MIMO radio with virtual-simultaneous dual-band operation
- Bluetooth v4.1 + EDR with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support
 - Single antenna with shared LNA
 - Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
 - SDIO v3.0 (1-bit/4-bit)—up to 208 MHz clock rate in SDR104 mode
 - HSIC (USB device interface for short distance on-board applications)
 - PCIe 2.0
- BT host digital interface (can be used concurrently with above interfaces):
 - UART (up to 4 Mbps)
- BT supports full-speed USB 2.0-compliant interface
- ECI—enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I²S/PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4, H4+, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I²S and PCM interface)
- Bluetooth SmartAudio[®] technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wide Band Speech (WBS)
- FM advanced internal antenna support
- FM auto search/tuning functions
- FM multiple audio routing options: I²S, PCM, eSCO, and A2DP
- FM mono-stereo blend and switch, and soft mute support
- FM audio pause detect support
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio stream
- FM over Bluetooth operation and on-chip stereo headset emulation (SBC)

1.3 Standards Compliance

The CYW4354 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0 + HS
- Bluetooth 4.1 (Bluetooth Low Energy)
- 65 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
 - WEP
 - WPA™ Personal
 - WPA2™ Personal
 - WMM
 - WMM-PS (U-APSD)
 - WMM-SA
 - AES (Hardware Accelerator)
 - TKIP (HW Accelerator)
 - CKIP (SW Support)
- Proprietary Protocols:
 - CCXv2
 - CCXv3
 - CCXv4
 - CCXv5
- IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

The CYW4354 will support the following future drafts/standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
 - IEEE 802.11e QoS Enhancements (In accordance with the WMM® specification, QoS is already supported.)
 - IEEE 802.11h 5 GHz Extensions
 - IEEE 802.11i MAC Enhancements
 - IEEE 802.11k Radio Resource Measurement

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4354. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, and FM functions in embedded designs.

A single VBAT (3.0V to 5.25V DC max.) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4354.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

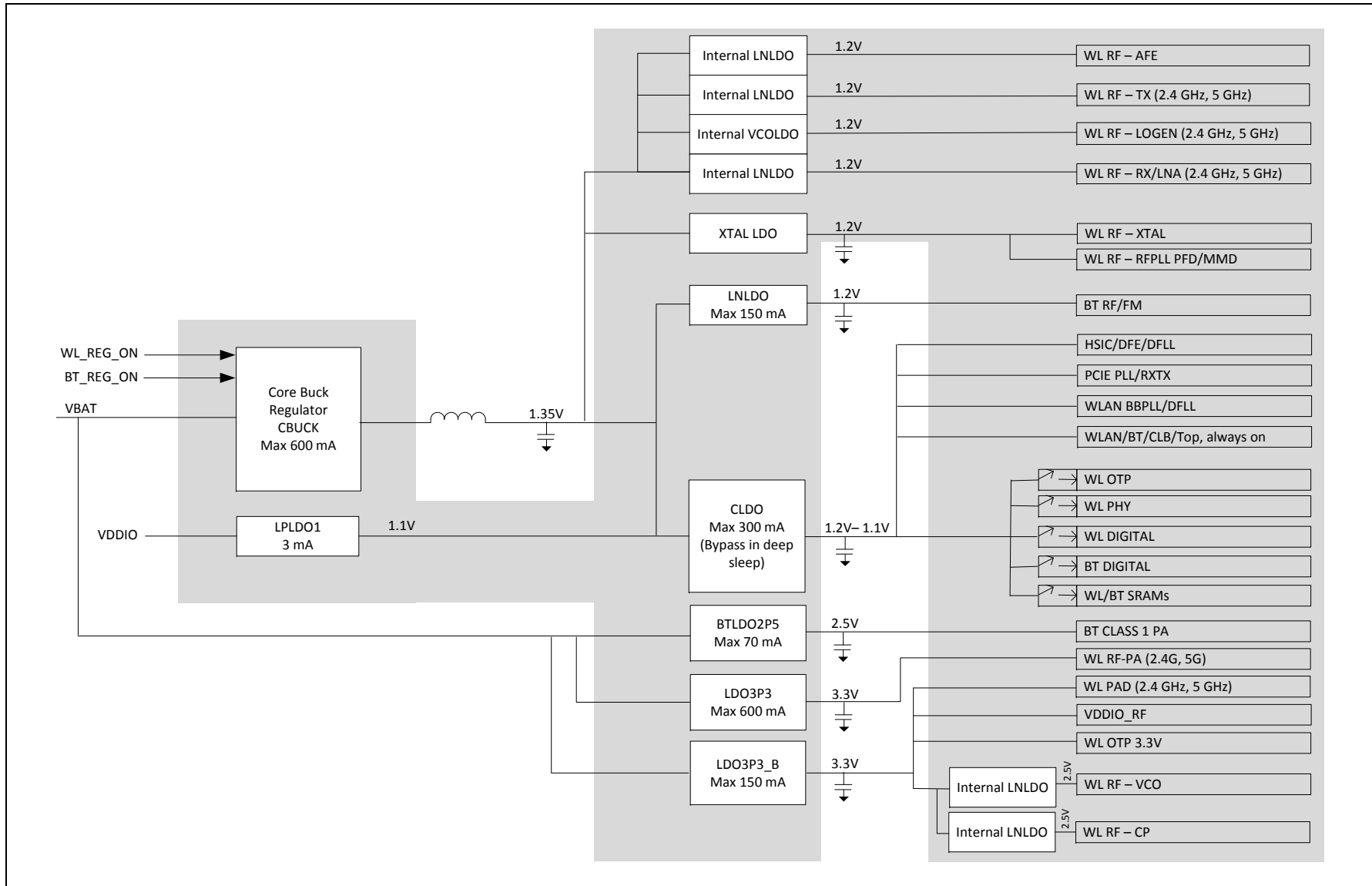
The CYW4354 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 (which is a low-power linear regulator supplied by the system VIO supply) provides the CYW4354 with all the voltages it requires, further reducing leakage currents.

2.2 CYW4354 PMU Features

- VBAT to 1.35Vout (600 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (600 mA maximum) LDO3P3
- VBAT to 3.3Vout (150 mA maximum) LDO3P3_B
- VBAT to 2.5V out (70 mA maximum) BTLDO2P5
- 1.35V to 1.2Vout (150 mA maximum) LNLDO
- 1.35V to 1.2Vout (300 mA maximum) CLDO with bypass mode for deep-sleep
- Additional internal LDOs (not externally accessible)

Figure 3 on page 11 illustrates the typical power topology for the CYW4354. The shaded areas are internal to the CYW4354.

Figure 3. Typical Power Topology for the CYW4354



2.3 WLAN Power Management

The CYW4354 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4354 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW4354 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4354 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4354 WLAN power states are described as follows:

- **Active mode**—All WLAN blocks in the CYW4354 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Deep-sleep mode**—Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the HSIC or SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization. In Deep-sleep mode, the primary source of power consumption is leakage current.
- **Power-down mode**—The CYW4354 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW4354 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW4354 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4354 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the CYW4354, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW4354 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW4354 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW4354 has two signals (see [Table 3](#)) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see [Power-Up Sequence and Timing on page 153](#).

Table 3. Power-Up/Power-Down/Reset Control Signals

| Signal | Description |
|-----------|---|
| WL_REG_ON | This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4354 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| BT_REG_ON | This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4354 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |

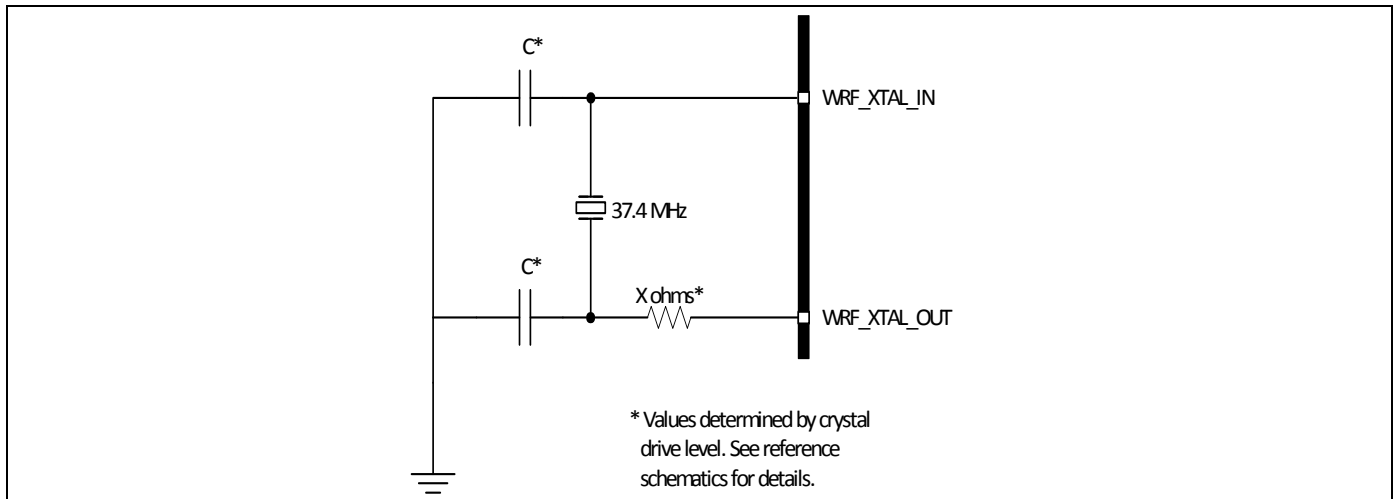
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW4354 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW4354 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

For SDIO, HSIC, and PCIe WLAN host applications, the recommended default frequency reference is a 37.4 MHz crystal. For PCIe applications, see Table 4 on page 15 for details on alternatives for the external frequency reference. The signal characteristics for the crystal oscillator interface are also listed in Table 4.

For SDIO WLAN host applications, the recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are also listed in Table 4.

Note:

Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

3.2 External Frequency Reference

For operation in SDIO and HSIC modes only, an alternative to a crystal (an external precision frequency reference) can be used. The recommended default frequency is 52 MHz \pm 10 ppm, and it must meet the phase noise requirements listed in [Table 4](#).

If used, the external clock should be connected to the WRF_XTAL_IN pin through an external 1000 pF coupling capacitor, as shown in [Figure 5](#). The internal clock buffer connected to this pin will be turned OFF when the CYW4354 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P5 pin.

Figure 5. Recommended Circuit to Use with an External Reference Clock

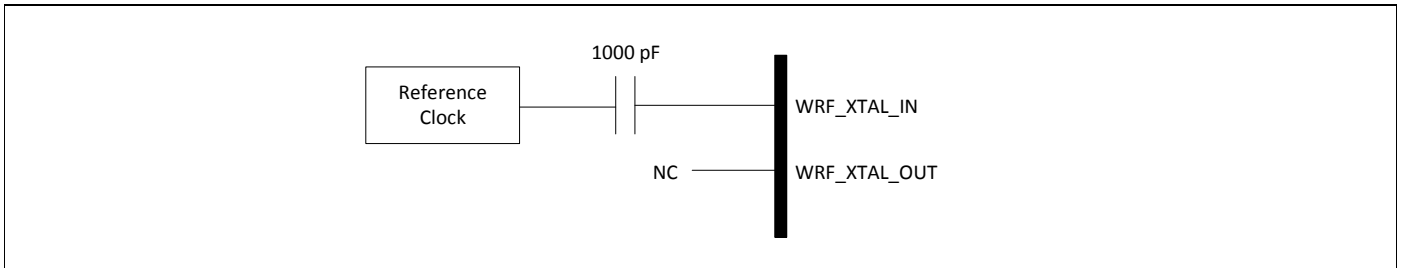


Table 4. Crystal Oscillator and External Clock—Requirements and Performance

| Parameter | Conditions/Notes | Crystal ^a | | | External Frequency Reference ^{b,c} | | | Units |
|--|---|---|------|------|---|------|------|-------------------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Frequency | 2.4G and 5G bands: IEEE 802.11ac operation, SDIO3.0, HSIC and PCIe WLAN interfaces | 35 | 37.4 | – | – | 52 | – | MHz |
| | 2.4G and 5G bands, IEEE 802.11ac operation, PCIe interface alternative frequency | – | 40 | – | – | – | – | MHz |
| | 5G band: IEEE 802.11n operation only | 19 | – | 52 | 35 | – | 52 | MHz |
| | 2.4G band: IEEE 802.11n operation, and both bands legacy 802.11a/b/g operation only | Ranges between 19 MHz and 52 MHz ^{d,e} | | | | | | |
| Frequency tolerance over the lifetime of the equipment, including temperature ^f | Without trimming | –20 | – | 20 | –20 | – | 20 | ppm |
| Crystal load capacitance | – | – | 12 | – | – | – | – | pF |
| ESR | – | – | – | 60 | – | – | – | Ω |
| Drive level | External crystal must be able to tolerate this drive level. | 200 | – | – | – | – | – | μ W |
| Input impedance (WRF_XTAL_IN) | Resistive | – | – | – | 30 | 100 | – | k Ω |
| | Capacitive | – | – | 7.5 | – | – | 7.5 | pF |
| WRF_XTAL_IN Input low level | DC-coupled digital signal | – | – | – | 0 | – | 0.2 | V |
| WRF_XTAL_IN Input high level | DC-coupled digital signal | – | – | – | 1.0 | – | 1.26 | V |
| WRF_XTAL_IN input voltage (see Figure 5) | AC-coupled analog signal | – | – | – | 400 | – | 1200 | mV _{p-p} |
| Duty cycle | 37.4 MHz clock | – | – | – | 40 | 50 | 60 | % |

Table 4. Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

| Parameter | Conditions/Notes | Crystal ^a | | | External Frequency Reference ^{b,c} | | | Units |
|---|----------------------------------|----------------------|------|------|---|------|------|--------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Phase Noise ^g (IEEE 802.11b/g) | 37.4 MHz clock at 10 kHz offset | – | – | – | – | – | –129 | dBc/Hz |
| | 37.4 MHz clock at 100 kHz offset | – | – | – | – | – | –136 | dBc/Hz |
| Phase Noise ^g (IEEE 802.11a) | 37.4 MHz clock at 10 kHz offset | – | – | – | – | – | –137 | dBc/Hz |
| | 37.4 MHz clock at 100 kHz offset | – | – | – | – | – | –144 | dBc/Hz |
| Phase Noise ^g (IEEE 802.11n, 2.4 GHz) | 37.4 MHz clock at 10 kHz offset | – | – | – | – | – | –134 | dBc/Hz |
| | 37.4 MHz clock at 100 kHz offset | – | – | – | – | – | –141 | dBc/Hz |
| Phase Noise ^{g,h} (IEEE 802.11n, 5 GHz) | 37.4 MHz clock at 10 kHz offset | – | – | – | – | – | –142 | dBc/Hz |
| | 37.4 MHz clock at 100 kHz offset | – | – | – | – | – | –149 | dBc/Hz |
| Phase Noise ^g (IEEE 802.11ac, 5 GHz) | 37.4 MHz clock at 10 kHz offset | – | – | – | – | – | –150 | dBc/Hz |
| | 37.4 MHz clock at 100 kHz offset | – | – | – | – | – | –157 | dBc/Hz |

- a. (Crystal) Use WRF_XTAL_IN and WRF_XTAL_OUT.
- b. See “External Frequency Reference” on page 15 for alternate connection methods.
- c. For a clock reference other than 37.4 MHz, $20 \times \log_{10}(f/37.4)$ dB should be added to the limits, where f = the reference clock frequency in MHz.
- d. BT_TM6 should be tied low for a 52 MHz clock reference. For other frequencies, BT_TM6 should be tied high. Note that 52 MHz is not an auto-detected frequency using the LPO clock.
- e. The frequency step size is approximately 80 Hz resolution.
- f. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
- g. Assumes that external clock has a flat phase noise response above 100 kHz.
- h. If the reference clock frequency is <35 MHz the phase noise requirements must be tightened by an additional 2 dB.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW4354 uses a secondary low-frequency clock for Low-Power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ($\pm 30\%$) over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock which meets the requirements listed in [Table 5](#).

Table 5. External 32.768 kHz Sleep Clock Specifications

| Parameter | LPO Clock | Unit |
|--|--------------------------|----------|
| Nominal input frequency | 32.768 | kHz |
| Frequency accuracy | ± 200 | ppm |
| Duty cycle | 30–70 | % |
| Input signal amplitude | 200–3300 | mV, p-p |
| Signal type | Square-wave or sine-wave | – |
| Input impedance ^a | > 100k | Ω |
| | < 5 | pF |
| Clock jitter (during initial start-up) | < 10,000 | ppm |

a. When power is applied or switched off.

4. Bluetooth + FM Subsystem Overview

The Cypress CYW4354 is a Bluetooth 4.1 + EDR-compliant, baseband processor/2.4 GHz transceiver with an integrated FM/RDS/RBDS receiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus FM radio solution.

The CYW4354 is the optimal solution for any Bluetooth voice and/or data application that also requires an FM radio receiver. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and PCM for audio. The FM subsystem supports the HCI control interface, analog output, as well as I²S and PCM interfaces. The CYW4354 incorporates all Bluetooth 4.1 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The CYW4354 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Features

Major Bluetooth features of the CYW4354 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.1 + (Enhanced Data Rate) EDR features:
 - Adaptive Frequency Hopping (AFH)
 - Quality of Service (QoS)
 - Extended Synchronous Connections (eSCO)—Voice Connections
 - Fast Connect (interlaced page and inquiry scans)
 - Secure Simple Pairing (SSP)
 - Sniff Subrating (SSR)
 - Encryption Pause Resume (EPR)
 - Extended Inquiry Response (EIR)
 - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.1 packet types
- Supports maximum Bluetooth data rates over HCI UART
- BT supports full-speed USB 2.0-compliant interface
- Multipoint operation with up to seven active slaves
 - Maximum of seven simultaneous active ACL links
 - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Broadcom fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see [“Host Controller Power Management”](#) on page 23)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
 - Bluetooth clock request
 - Bluetooth standard sniff
 - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

Major FM Radio features include:

- 65 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- FM subsystem control using the Bluetooth HCI interface
- FM subsystem operates from reference clock inputs.
- Improved audio interface capabilities with full-featured bidirectional PCM and I²S
- I²S can be master or slave.

FM Receiver-Specific Features Include:

- Excellent FM radio performance with 1 μ V sensitivity for 26 dB (S+N)/N
- Signal-dependent stereo/mono blending
- Signal dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RSSI, IF frequency, status indicators
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump

4.2 Bluetooth Radio

The CYW4354 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit

The CYW4354 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates $\pi/4$ -DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$ -DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW4354 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW4354 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW4354 uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW4354 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewatering in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

- Dual-mode bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Bluetooth Low Energy

The CYW4354 supports the Bluetooth Low Energy operating mode.

5.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
 - Standby
 - Connection
- Substates:
 - Page
 - Page Scan
 - Inquiry
 - Inquiry Scan
 - Sniff

5.4 Test Mode Support

The CYW4354 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW4354 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
 - Simplifies some type-approval measurements (Japan)
 - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
 - Receiver output directed to I/O pin
 - Allows for direct BER measurements using standard RF test equipment
 - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
 - Eight-bit fixed pattern or PRBS-9
 - Enables modulated signal measurements with standard RF test equipment

5.5 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW4354 are:

- [RF Power Management](#)
- [Host Controller Power Management](#)
- [BBC Power Management](#)
- [FM Power Management](#)

5.5.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.5.2 Host Controller Power Management

When running in UART mode, the CYW4354 may be configured so that dedicated signals are used for power management hand-shaking between the CYW4354 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. [Table 6](#) describes the power-control hand-shake signals used with the UART interface.

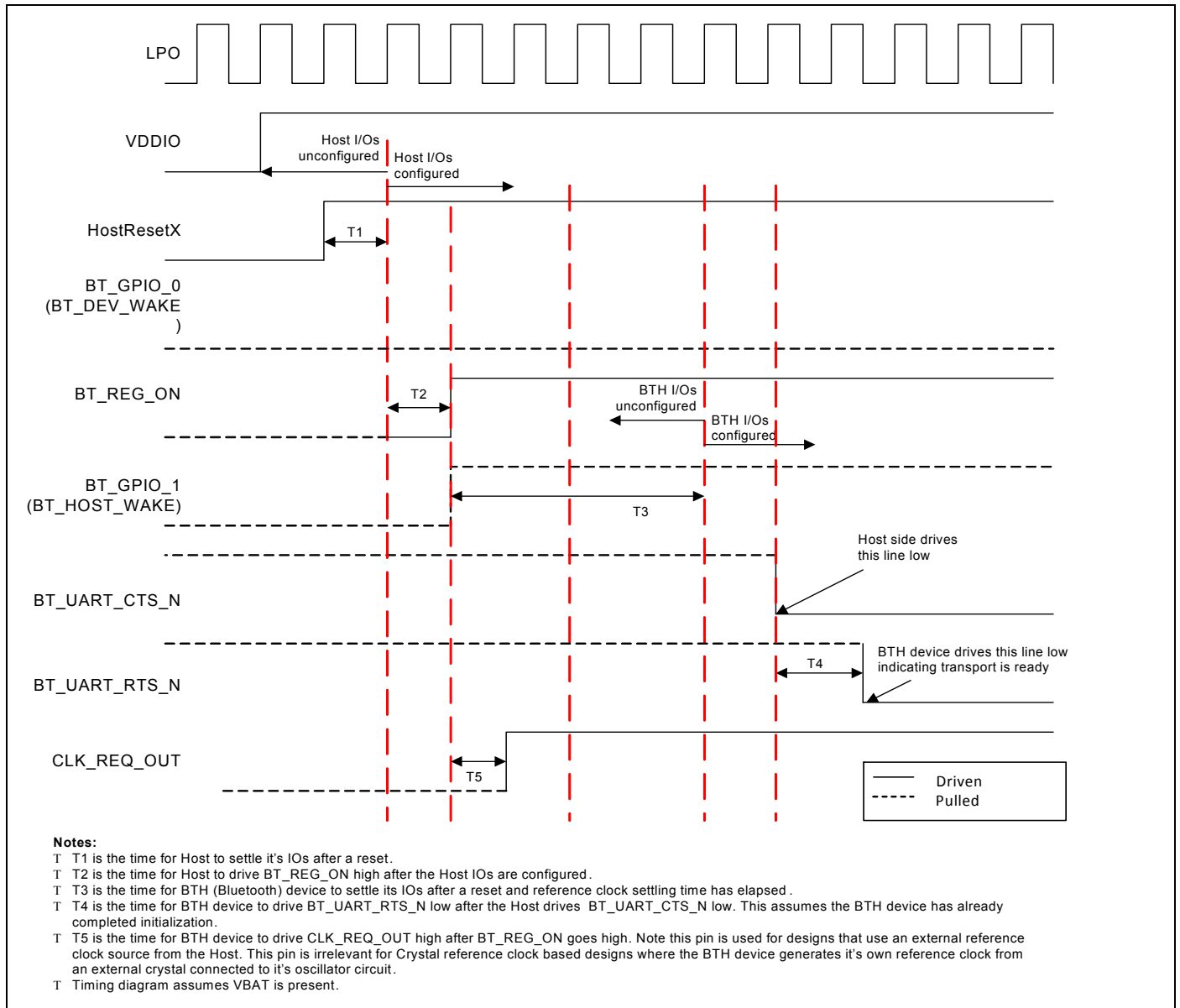
Table 6. Power Control Pin Description

| Signal | Mapped to Pin | Type | Description |
|--------------|----------------------------------|------|--|
| BT_DEV_WAKE | BT_GPIO_0 | I | Bluetooth device wake-up: Signal from the host to the CYW4354 indicating that the host requires attention. <ul style="list-style-type: none"> ■ Asserted: The Bluetooth device must wake-up or remain awake. ■ Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |
| BT_HOST_WAKE | BT_GPIO_1 | O | Host wake up. Signal from the CYW4354 to the host indicating that the CYW4354 requires attention. <ul style="list-style-type: none"> ■ Asserted: host device must wake-up or remain awake. ■ Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |
| CLK_REQ | BT_CLK_REQ_OUT WL_CLK_REQ_OUT | O | The CYW4354 asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW4354 powers up or resets when VDDIO is present. |

Note: Pad function Control Register is set to 0 for these pins. See “[DC Characteristics](#)” on page 128 for more details

The timing for the startup sequence is defined in Figure 6.

Figure 6. Startup Signaling Sequence



5.5.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW4354 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW4354 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW4354 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shut-down state, provided VDDIO remains applied to the CYW4354, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW4354 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW4354 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW4354 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.5.4 FM Power Management

The CYW4354 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems. The FM block does not have a low power state, it is either on or off.

5.5.5 Wideband Speech

The CYW4354 provides support for wideband speech (WBS) using on-chip SmartAudio technology. The CYW4354 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.5.6 Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW4354 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. [Figure 7](#) and [Figure 8](#) show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wide band speech.

Figure 7. CVSD Decoder Output Waveform Without PLC

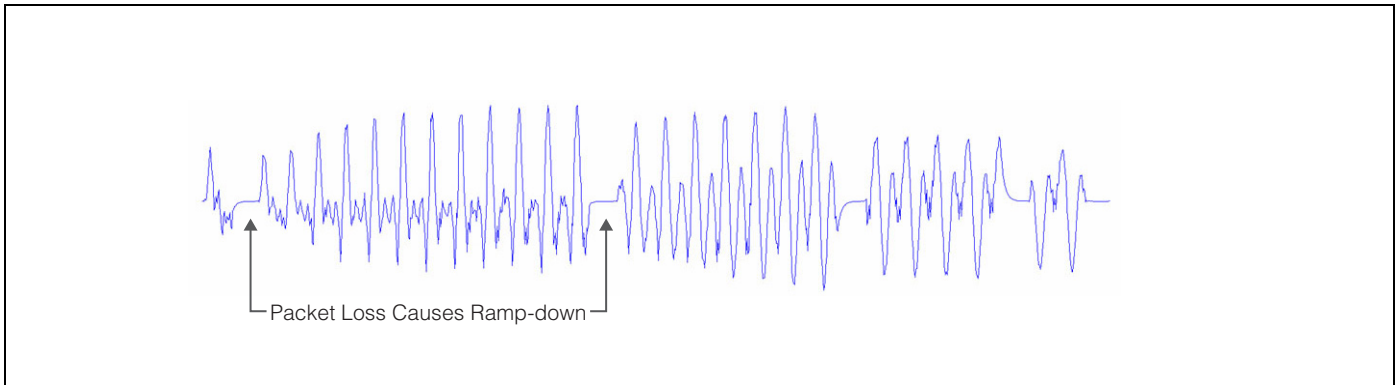
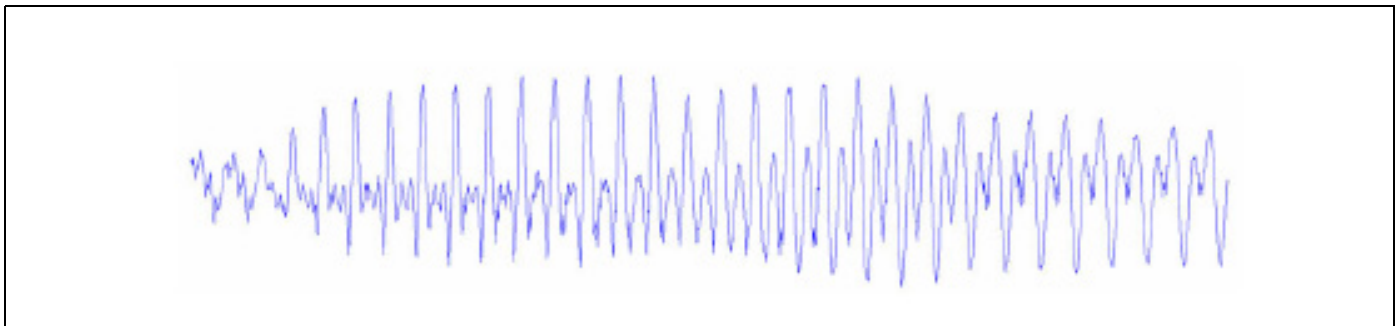


Figure 8. CVSD Decoder Output Waveform After Applying PLC



5.5.7 Audio Rate-Matching Algorithms

The CYW4354 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth or FM audio data rates.

5.5.8 Codec Encoding

The CYW4354 can support SBC and mSBC encoding and decoding for wideband speech.

5.5.9 Multiple Simultaneous A2DP Audio Stream

The CYW4354 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.5.10 FM Over Bluetooth

FM Over Bluetooth enables the CYW4354 to stream data from FM over Bluetooth without requiring the host to be awake. This can significantly extend battery life for usage cases where someone is listening to FM radio on a Bluetooth headset.

5.5.11 Burst Buffer Operation

The CYW4354 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.6 Adaptive Frequency Hopping

The CYW4354 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.7 Advanced Bluetooth/WLAN Coexistence

The CYW4354 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW4354 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW4354 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW4354 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

5.8 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW4354 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 668 KB of ROM memory for program storage and boot ROM, 200 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the CYW4354 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the CYW4330 device.

6.1 RAM, ROM, and Patch Memory

The CYW4354 Bluetooth core has 200 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 668 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

The CYW4354 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Unit

7.1 SPI Interface

The CYW4354 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates can be possible. The physical interface between the SPI master and the CYW4354 consists of the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The SPI signals are muxed onto the UART signals, see Table 7. The CYW4354 can be configured to accept active-low or active-high polarity on the SPI_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal. Bit ordering on the SPI_SI and SPI_SO data lines can be configured as either little-endian or big-endian. Additionally, proprietary sleep mode and half-duplex handshaking is implemented between the SPI master and the CYW4354. The SPI_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI_CSB and SPI_CLK. Flow control should be implemented in the higher layer protocols.

Table 7. SPI to UART Signal Mapping

| SPI Signals | UART Signals |
|-------------|--------------|
| SPI_CLK | UART_CTS_N |
| SPI_CSB | UART_RTS_N |
| SPI_MISO | UART_TXD |
| SPI_MOSI | UART_RXD |
| SPI_INT | BT_DEV_WAKE |

7.2 SPI/UART Transport Detection

The BT_HOST_WAKE (BT_GPIO1) pin is also used for BT transport detection. The transport detection occurs during the power-up sequence. It selects either UART or SPI transport operation based on the following pin state:

- If the BT_HOST_WAKE (BT_GPIO1) pin is pulled low by an external pull-down during power-up, it selects the SPI transport interface.
- If the BT_HOST_WAKE (BT_GPIO1) pin is not pulled low externally during power-up, then the default internal pull-up is detected as a high and it selects the UART transport interface.

7.3 PCM Interface

The CYW4354 supports two independent PCM interfaces that share the pins with the I²S interfaces. The PCM Interface on the CYW4354 can connect to linear PCM Codec devices in master or slave mode. In master mode, the CYW4354 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW4354.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.3.1 Slot Mapping

The CYW4354 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.3.2 Frame Synchronization

The CYW4354 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.3.3 Data Formatting

The CYW4354 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW4354 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

7.3.4 Wideband Speech Support

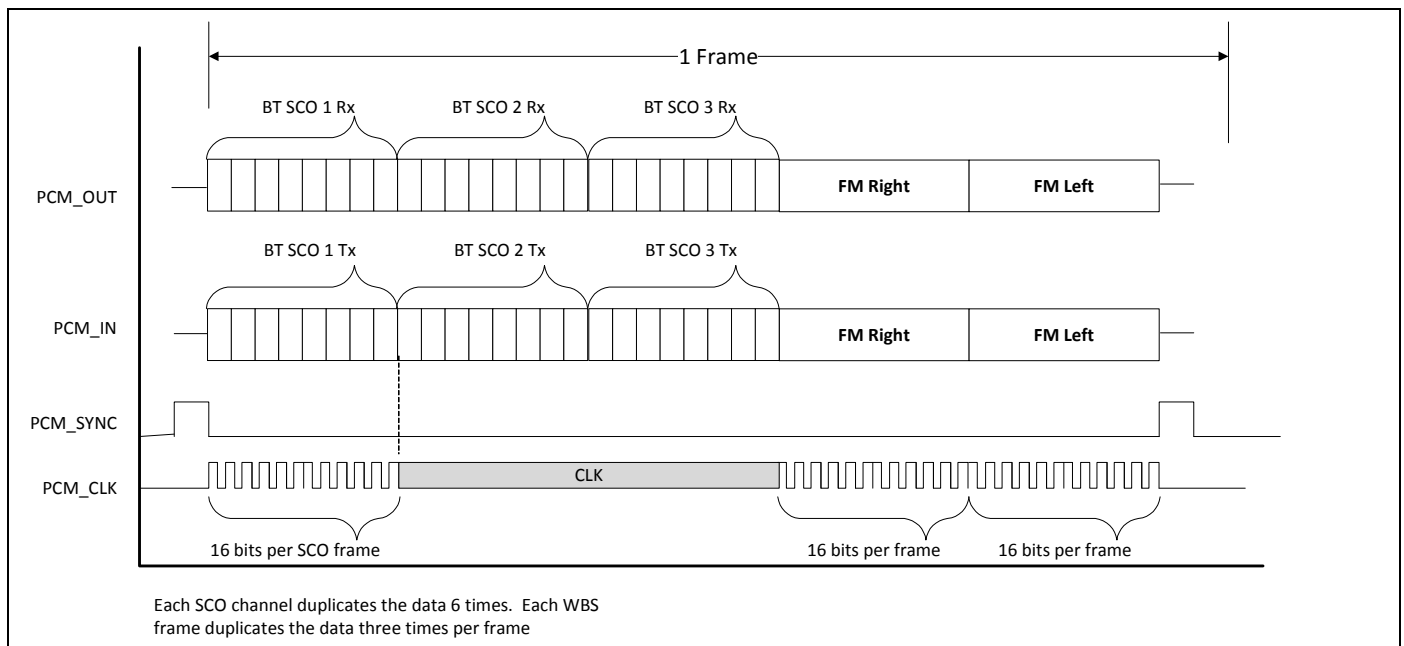
When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The CYW4354 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.3.5 Multiplexed Bluetooth and FM Over PCM

In this mode of operation, the CYW4354 multiplexes both FM and Bluetooth audio PCM channels over the same interface, reducing the number of required I/Os. This mode of operation is initiated through an HCI command from the host. The format of the data stream consists of three channels: a Bluetooth channel followed by two FM channels (audio left and right). In this mode of operation, the bus data rate only supports 48 kHz operation per channel with 16 bits sent for each channel. This is done to allow the low data rate Bluetooth data to coexist in the same interface as the higher speed I²S data. To accomplish this, the Bluetooth data is repeated six times for 8 kHz data and three times for 16 kHz data. An initial sync pulse on the PCM_SYNC line is used to indicate the beginning of the frame.

To support multiple Bluetooth audio streams within the Bluetooth channel, both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure 9 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

Figure 9. Functional Multiplex Data Diagram



7.3.6 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

7.3.7 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 10. PCM Timing Diagram (Short Frame Sync, Master Mode)

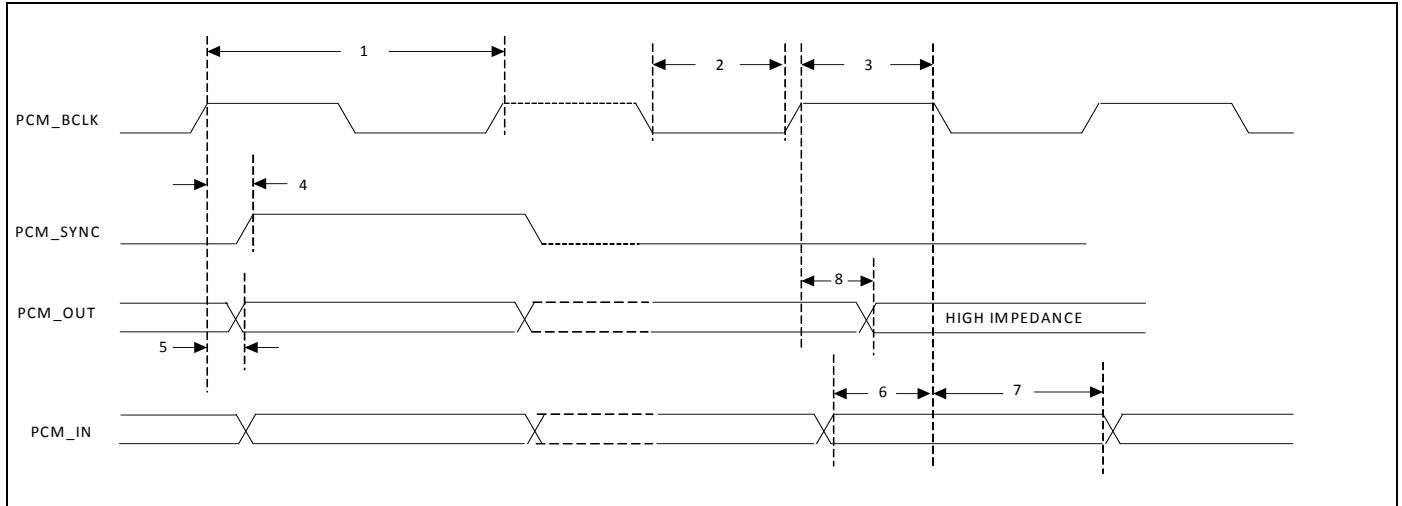


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|--|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC delay | 0 | – | 25 | ns |
| 5 | PCM_OUT delay | 0 | – | 25 | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |

Short Frame Sync, Slave Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Slave Mode)

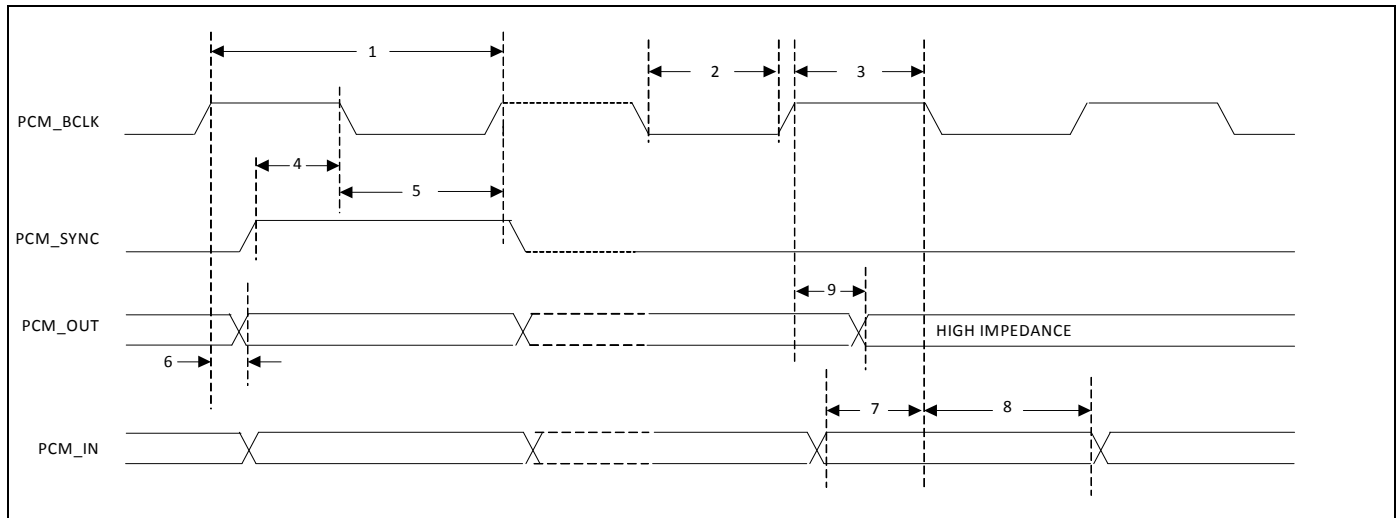


Table 9. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|--|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_OUT delay | 0 | – | 25 | ns |
| 7 | PCM_IN setup | 8 | – | – | ns |
| 8 | PCM_IN hold | 8 | – | – | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |

Long Frame Sync, Master Mode

Figure 12. PCM Timing Diagram (Long Frame Sync, Master Mode)

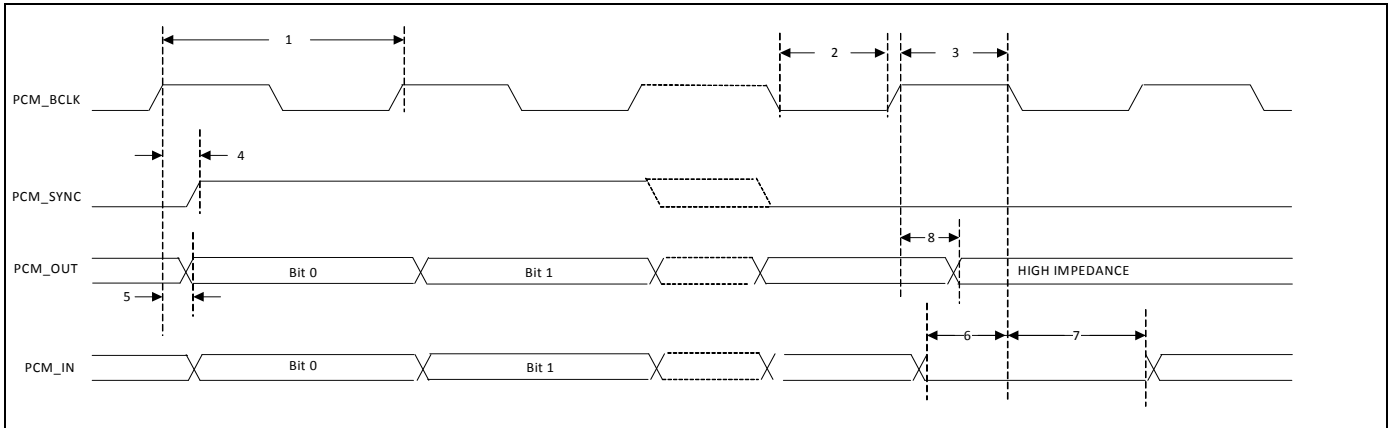


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|--|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC delay | 0 | – | 25 | ns |
| 5 | PCM_OUT delay | 0 | – | 25 | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |

Long Frame Sync, Slave Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Slave Mode)

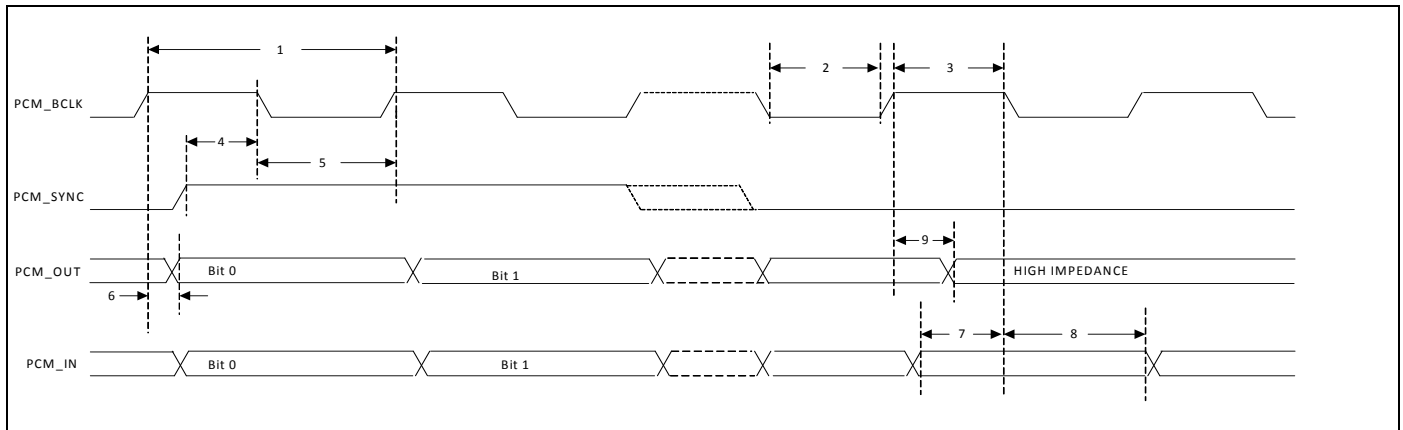


Table 11. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|--|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | – | – | ns |
| 3 | PCM bit clock HIGH | 41 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_OUT delay | 0 | – | 25 | ns |
| 7 | PCM_IN setup | 8 | – | – | ns |
| 8 | PCM_IN hold | 8 | – | – | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | – | 25 | ns |

Short Frame Sync, Burst Mode

Figure 14. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

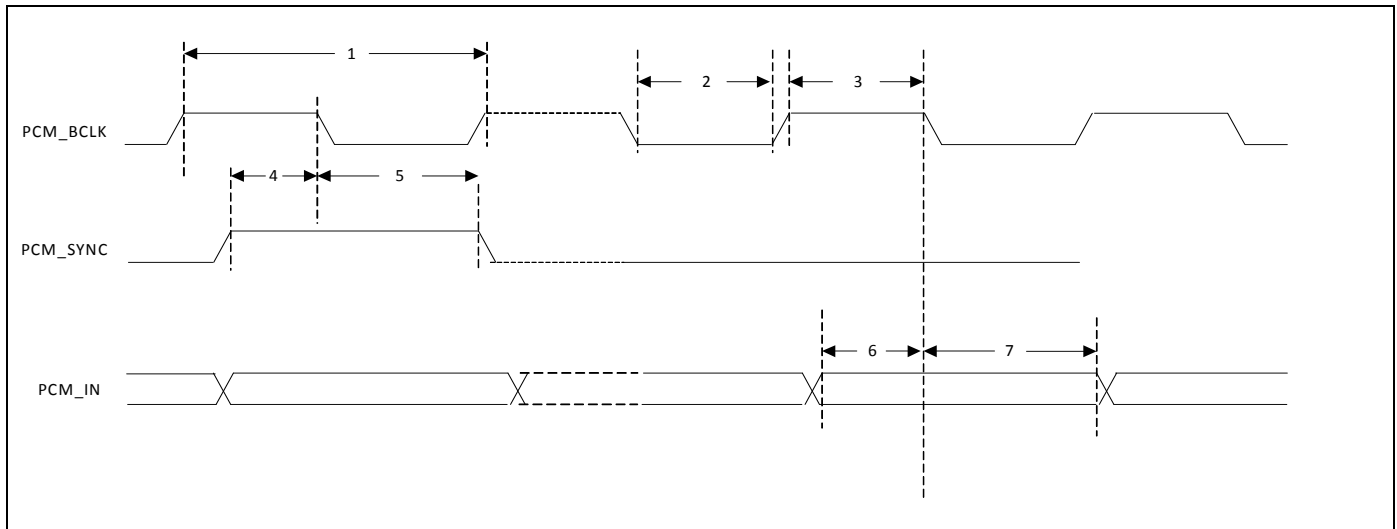


Table 12. PCM Burst Mode (Receive Only, Short Frame Sync)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|-------------------------|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | – | – | ns |
| 3 | PCM bit clock HIGH | 20.8 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |

Long Frame Sync, Burst Mode

Figure 15. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

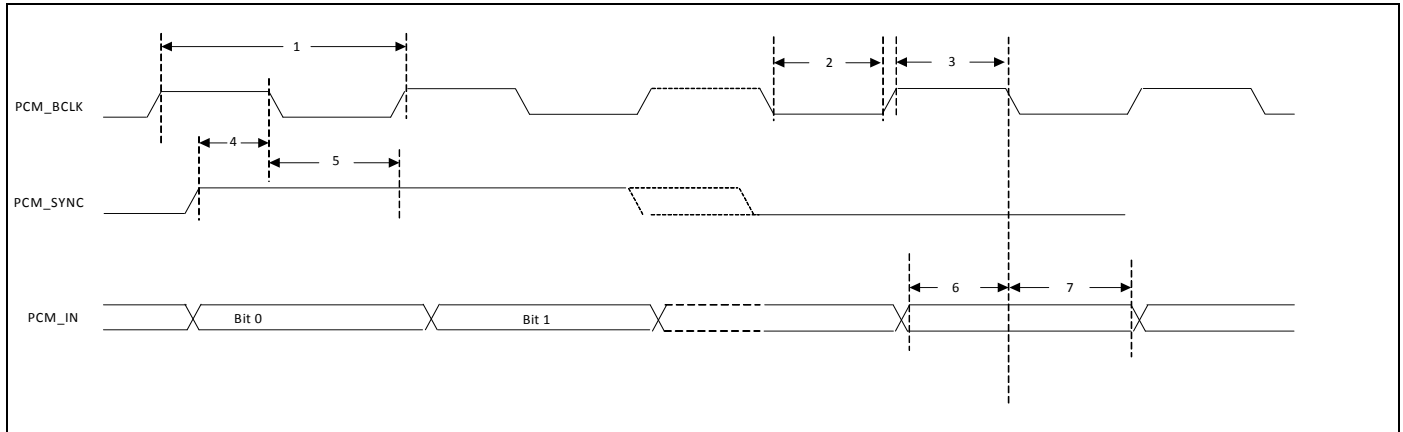


Table 13. PCM Burst Mode (Receive Only, Long Frame Sync)

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|-------------------------|---------|---------|---------|------|
| 1 | PCM bit clock frequency | – | – | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | – | – | ns |
| 3 | PCM bit clock HIGH | 20.8 | – | – | ns |
| 4 | PCM_SYNC setup | 8 | – | – | ns |
| 5 | PCM_SYNC hold | 8 | – | – | ns |
| 6 | PCM_IN setup | 8 | – | – | ns |
| 7 | PCM_IN hold | 8 | – | – | ns |

7.4 USB Interface

7.4.1 Features

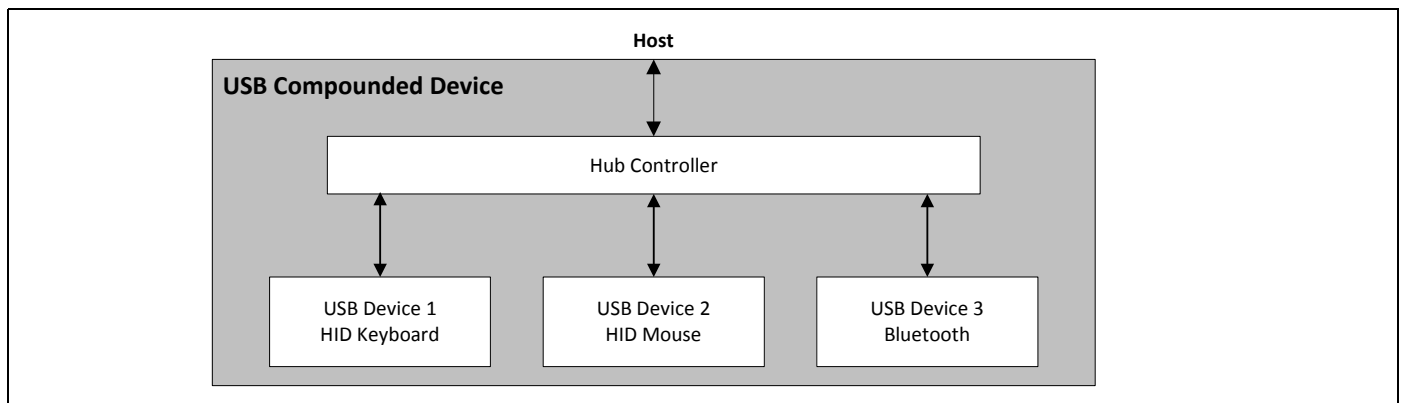
The following USB interface features are supported:

- USB Protocol, Revision 2.0, full-speed (12 Mbps) compliant including the hub
- Optional hub compound device with up to three device cores internal to device
- Bus or self-power, dynamic configuration for the hub
- Global and selective suspend and resume with remote wake-up
- Bluetooth HCI
- HID, DFU, UHE (proprietary method to emulate an HID device at system bootup)
- Integrated detach resistor

7.4.2 Operation

The CYW4354 can be configured to boot up as either a single USB peripheral or a USB hub with several USB peripherals attached. As a single peripheral, the host detects a single USB Bluetooth device. In hub mode, the host detects a hub with one to three of the ports already connected to USB devices (see [Figure 16](#)).

Figure 16. USB Compounded Device Configuration



Depending on the desired hub mode configuration, the CYW4354 can boot up showing the three ports connected to logical USB devices internal to the CYW4354: a generic Bluetooth device, a mouse, and a keyboard. In this mode, the mouse and keyboard are emulated devices, since they connect to real HID devices via a Bluetooth link. The Bluetooth link to these HID devices is hidden from the USB host. To the host, the mouse and/or keyboard appear to be directly connected to the USB port. This Broadcom proprietary architecture is called USB HID Emulation (UHE).

The USB device, configuration, and string descriptors are fully programmable, allowing manufacturers to customize the descriptors, including vendor and product IDs, the CYW4354 uses to identify itself on the USB port. To make custom USB descriptor information available at boot time, stored it in external NVRAM.

Despite the mode of operation (single peripheral or hub), the Bluetooth device is configured to include the following interfaces:

| | |
|-------------|---|
| Interface 0 | Contains a Control endpoint (Endpoint 0x00) for HCI commands, a Bulk In Endpoint (Endpoint 0x82) for receiving ACL data, a Bulk Out Endpoint (Endpoint 0x02) for transmitting ACL data, and an Interrupt Endpoint (Endpoint 0x81) for HCI events. |
| Interface 1 | Contains Isochronous In and Out endpoints (Endpoints 0x83 and 0x03) for SCO traffic. Several alternate Interface 1 settings are available for reserving the proper bandwidth of isochronous data (depending on the application). |
| Interface 2 | Contains Bulk In and Bulk Out endpoints (Endpoints 0x84 and 0x04) used for proprietary testing and debugging purposes. These endpoints can be ignored during normal operation. |

7.4.3 USB Hub and UHE Support

The CYW4354 supports the USB hub and device model (USB, Revision 2.0, full-speed compliant). Optional mouse and keyboard devices utilize Broadcom’s proprietary USB HID Emulation (UHE) architecture, which allows these devices appear as standalone HID devices even though connected through a Bluetooth link.

The presence of UHE devices requires the hub to be enabled. The CYW4354 cannot appear as a single keyboard or a single mouse device without the hub. Once either mouse or keyboard UHE device is enabled, the hub must also be enabled.

When the hub is enabled, the CYW4354 handles all standard USB functions for the following devices:

- HID keyboard
- HID mouse
- Bluetooth

All hub and device descriptors are firmware-programmable. This USB compound device configuration (see [Figure 16 on page 37](#)) supports up to three downstream ports. This configuration can also be programmed to a single USB device core. The device automatically detects activity on the USB interface when connected. Therefore, no special configuration is needed to select HCI as the transport.

The hub’s downstream port definition is as follows:

- Port 1 USB lite device core (for HID applications)
- Port 2 USB lite device core (for HID applications)
- Port 3 USB full device core (for Bluetooth applications)

When operating in hub mode, all three internal devices do not have to be enabled. Each internal USB device can be optionally enabled. The configuration record in NVRAM determines which devices are present.

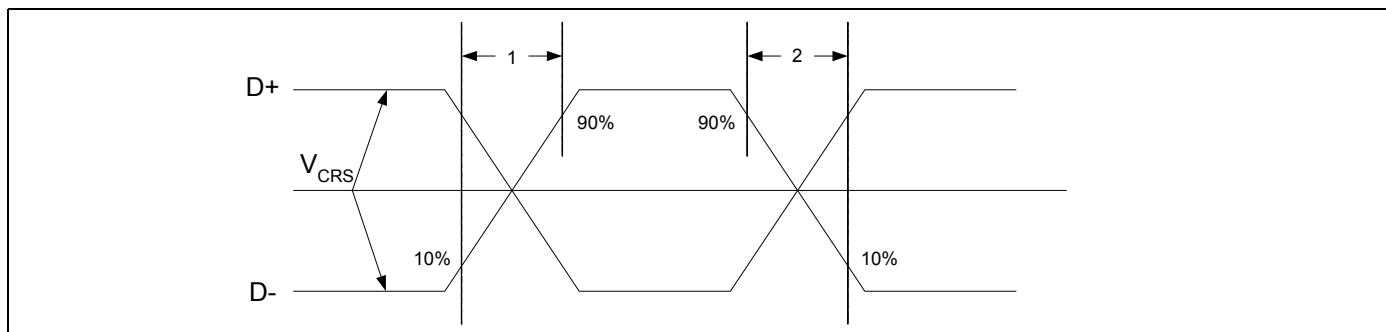
7.4.4 USB Full-Speed Timing

[Table 14](#) shows timing specifications for the $V_{DD_USB} = 3.3V$, $V_{SS} = 0V$, and $T_A = 0^{\circ}C$ to $85^{\circ}C$ operating temperature range.

Table 14. USB Full-Speed Timing Specifications

| Reference | Characteristics | Minimum | Maximum | Unit |
|-----------|---------------------------|------------|------------|------|
| 1 | Transition rise time | 4 | 20 | ns |
| 2 | Transition fall time | 4 | 20 | ns |
| 3 | Rise/fall timing matching | 90 | 111 | % |
| 4 | Full-speed data rate | 12 – 0.25% | 12 + 0.25% | Mb/s |

Figure 17. USB Full-Speed Timing



7.5 UART Interface

The CYW4354 shares a single UART for Bluetooth and FM. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.1 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW4354 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW4354 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Table 15. Example of Common Baud Rates

| Desired Rate | Actual Rate | Error (%) |
|--------------|-------------|-----------|
| 4000000 | 4000000 | 0.00 |
| 3692000 | 3692308 | 0.01 |
| 3000000 | 3000000 | 0.00 |
| 2000000 | 2000000 | 0.00 |
| 1500000 | 1500000 | 0.00 |
| 1444444 | 1454544 | 0.70 |
| 921600 | 923077 | 0.16 |
| 460800 | 461538 | 0.16 |
| 230400 | 230796 | 0.17 |
| 115200 | 115385 | 0.16 |
| 57600 | 57692 | 0.16 |
| 38400 | 38400 | 0.00 |
| 28800 | 28846 | 0.16 |
| 19200 | 19200 | 0.00 |
| 14400 | 14423 | 0.16 |
| 9600 | 9600 | 0.00 |

Figure 18. UART Timing

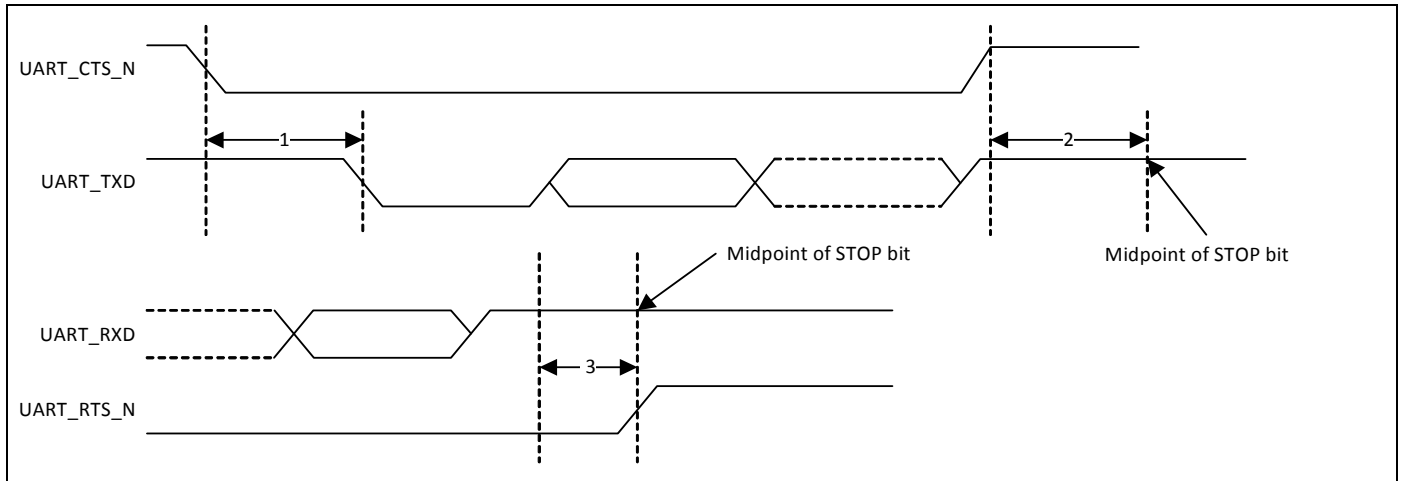


Table 16. UART Timing Specifications

| Ref No. | Characteristics | Minimum | Typical | Maximum | Unit |
|---------|---|---------|---------|---------|-------------|
| 1 | Delay time, UART_CTS_N low to UART_TXD valid | – | – | 1.5 | Bit periods |
| 2 | Setup time, UART_CTS_N high before midpoint of stop bit | – | – | 0.5 | Bit periods |
| 3 | Delay time, midpoint of stop bit to UART_RTS_N high | – | – | 0.5 | Bit periods |

7.6 I²S Interface

The CYW4354 supports two independent I²S digital audio ports: one for Bluetooth audio, and one for high-fidelity FM audio. The I²S interface for FM audio supports both master and slave modes. The I²S signals are:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in master mode and inputs in slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, in accord with the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is low, and right-channel data is transmitted when BT_I2S_WS is high. Data bits sent by the CYW4354 are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

The clock rate in master mode is either of the following:

$$48 \text{ kHz} \times 32 \text{ bits per frame} = 1.536 \text{ MHz}$$

$$48 \text{ kHz} \times 50 \text{ bits per frame} = 2.400 \text{ MHz}$$

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

7.6.1 I²S Timing

Note: Timing values specified in Table 16 are relative to high and low threshold levels

Table 17. Timing for I²S Transmitters and Receivers

| | Transmitter | | | | Receiver | | | | Notes |
|--|---------------------|---------------------|---------------------|------|---------------------|---------------------|-------------|------|-------|
| | Lower Limit | | Upper Limit | | Lower Limit | | Upper Limit | | |
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Period T | T _{tr} | – | – | – | T _r | – | – | – | a |
| Master Mode: Clock generated by transmitter or receiver | | | | | | | | | |
| HIGH t _{HC} | 0.35T _{tr} | – | – | – | 0.35T _{tr} | – | – | – | b |
| LOW t _{LC} | 0.35T _{tr} | – | – | – | 0.35T _{tr} | – | – | – | b |
| Slave Mode: Clock accepted by transmitter or receiver | | | | | | | | | |
| HIGH t _{HC} | – | 0.35T _{tr} | – | – | – | 0.35T _{tr} | – | – | c |
| LOW t _{LC} | – | 0.35T _{tr} | – | – | – | 0.35T _{tr} | – | – | c |
| Rise time t _{RC} | – | – | 0.15T _{tr} | – | – | – | – | – | d |
| Transmitter | | | | | | | | | |
| Delay t _{dtr} | – | – | – | 0.8T | – | – | – | – | e |
| Hold time t _{htr} | 0 | – | – | – | – | – | – | – | d |
| Receiver | | | | | | | | | |
| Setup time t _{sr} | – | – | – | – | – | 0.2T _r | – | – | f |
| Hold time t _{hr} | – | – | – | – | – | 0 | – | – | f |

- a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35T_r, any clock that meets the requirements can be used.
- d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than 0.15T_{tr}.
- e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- f. The data setup and hold time must not be less than the specified receiver setup and hold time.

Note: The time periods specified in Figure 19 and Figure 20 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 19. I²S Transmitter Timing

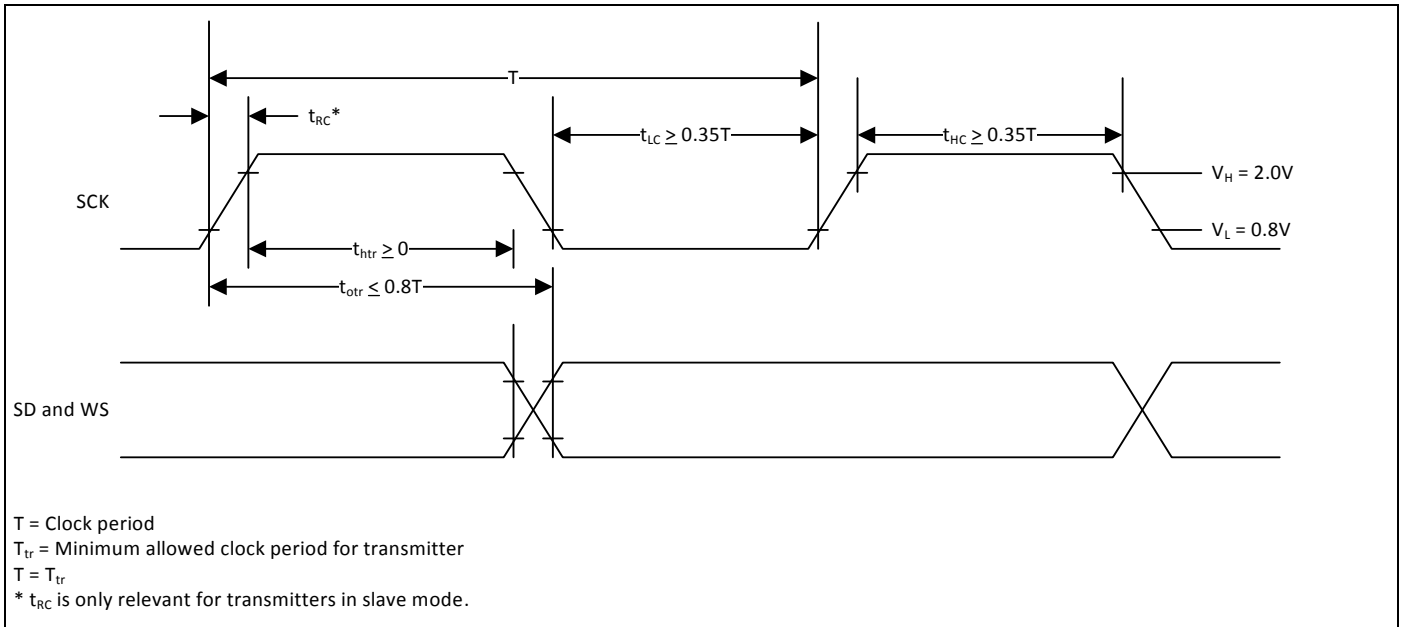
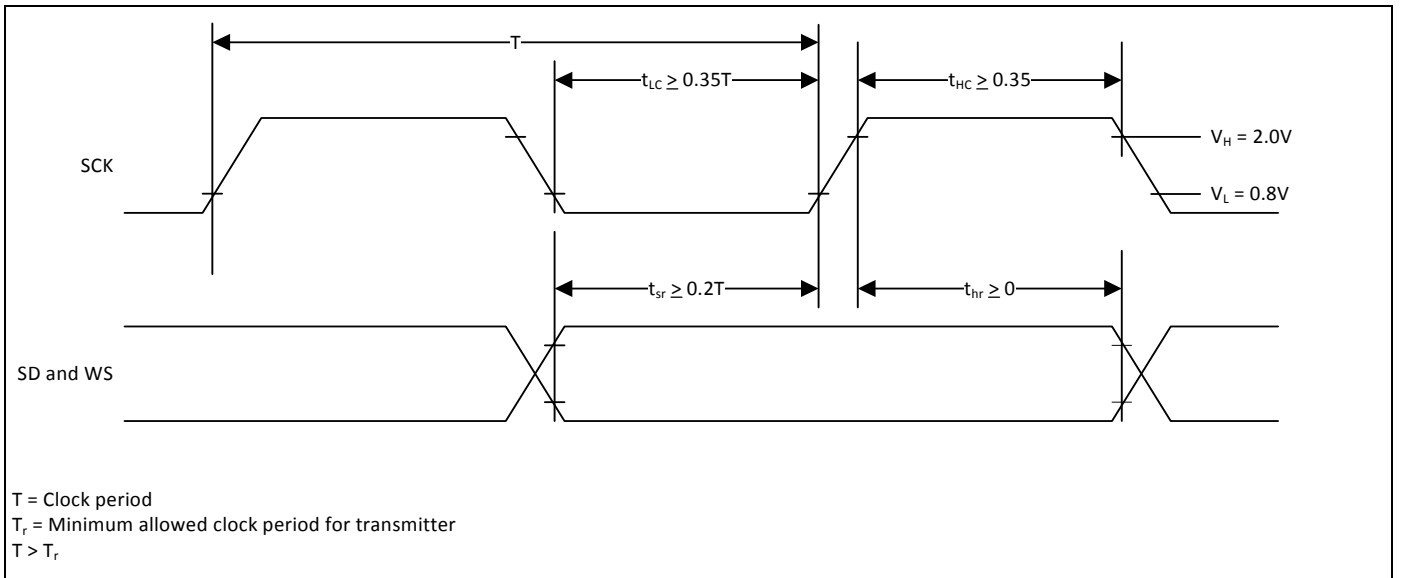


Figure 20. I²S Receiver Timing



8. FM Receiver Subsystem

8.1 FM Radio

The CYW4354 includes a completely integrated FM radio receiver with RDS/RBDS covering all FM bands from 65 MHz to 108 MHz. The receiver is controlled through commands on the HCI. FM received audio is available as stereo or in digital form through I²S or PCM. The FM radio operates from the external clock reference.

8.2 Digital FM Audio Interfaces

The FM audio can be transmitted via the shared PCM and I²S pins, and the sampling rate is programmable. The CYW4354 supports a three-wire PCM or I²S audio interface in either master or slave configuration. The master or slave configuration is selected using vendor specific commands over the HCI interface. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks. In master mode, the clock rate is either of the following:

- 48 kHz × 32 bits per frame = 1.536 MHz
- 48 kHz × 50 bits per frame = 2.400 MHz

In slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

8.3 FM Over Bluetooth

The CYW4354 can output received FM audio onto Bluetooth using one of following three links: eSCO, WBS, and A2DP. In all of the above modes, once the link has been set up, the host processor can enter sleep mode while the CYW4354 continues to stream FM audio to the remote Bluetooth device, allowing the system current consumption to be minimized.

8.4 eSCO

In this use case, the stereo FM audio is downsampled to 8 kHz and a mono or stereo stream is then sent through the Bluetooth eSCO link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

8.5 Wide Band Speech Link

In this case, the stereo FM audio is downsampled to 16 kHz and a mono or stereo stream is then sent through the Bluetooth wideband speech link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

8.6 A2DP

In this case, the stereo FM audio is encoded by the on-chip SBC encoder and transported as an A2DP link to a remote Bluetooth device. Sampling rates of 48 kHz, 44.1 kHz, and 32 kHz joint stereo are supported. An A2DP “lite” stack is implemented in the CYW4354 to support this use case, which eliminates the need to route the SBC-encoded audio back to the host to create the A2DP packets.

8.7 Autotune and Search Algorithms

The CYW4354 supports a number of FM search and tune functions that allows the host to implement many convenient user functions, which are accessed through the Broadcom FM stack.

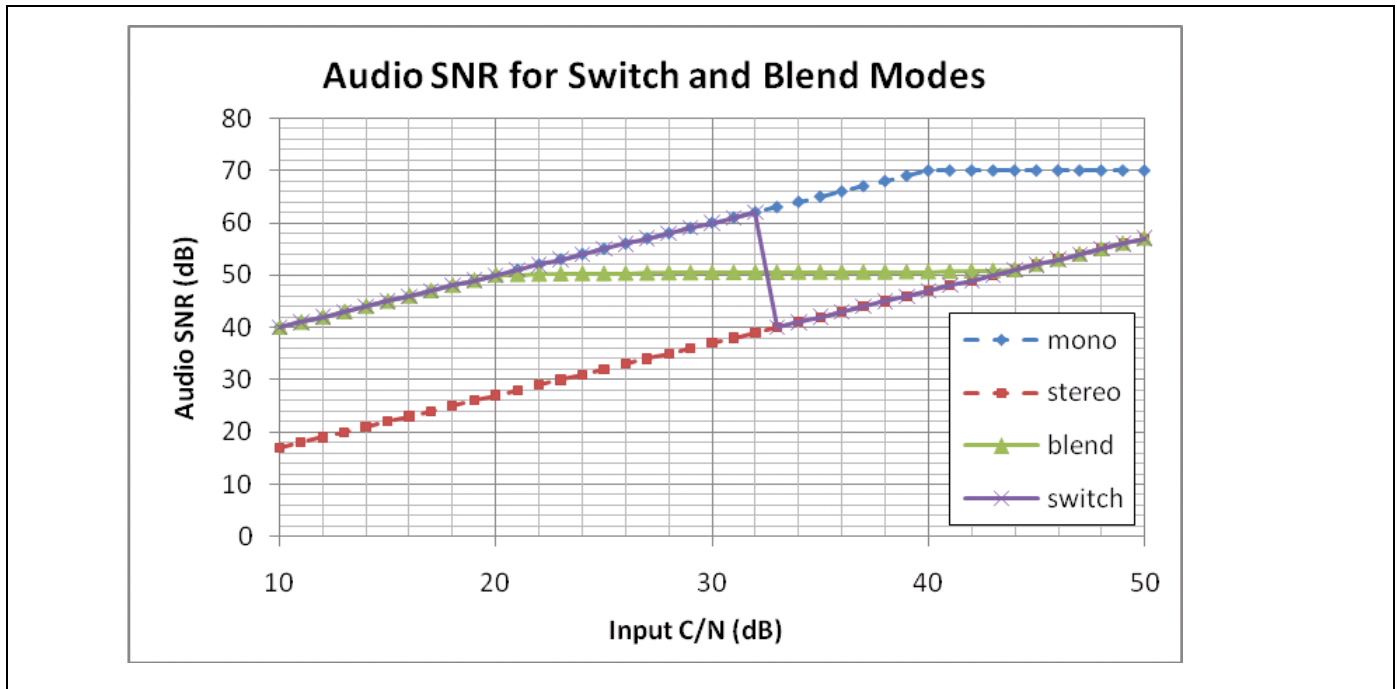
- Tune to Play: Allows the FM receiver to be programmed to a specific frequency.
- Search for SNR > Threshold: Checks the power level of the available channel and the estimated SNR of the channel to help achieve precise control of the expected sound quality for the selected FM channel. Specifically, the host can adjust its SNR requirements to retrieve a signal with a specific sound quality, or adjust this to return the weakest channels.
- Alternate Frequency Jump: Allows the FM receiver to automatically jump to an alternate FM channel that carries the same information, but has a better SNR. For example, when traveling, a user may pass through a region where a number of channels carry the same station. When the user passes from one area to the next, the FM receiver can automatically switch to another channel with a stronger signal to spare the user from having to manually change the channel to continue listening to the same station.

8.8 Audio Features

A number of features are implemented in the CYW4354 to provide the best possible audio experience for the user.

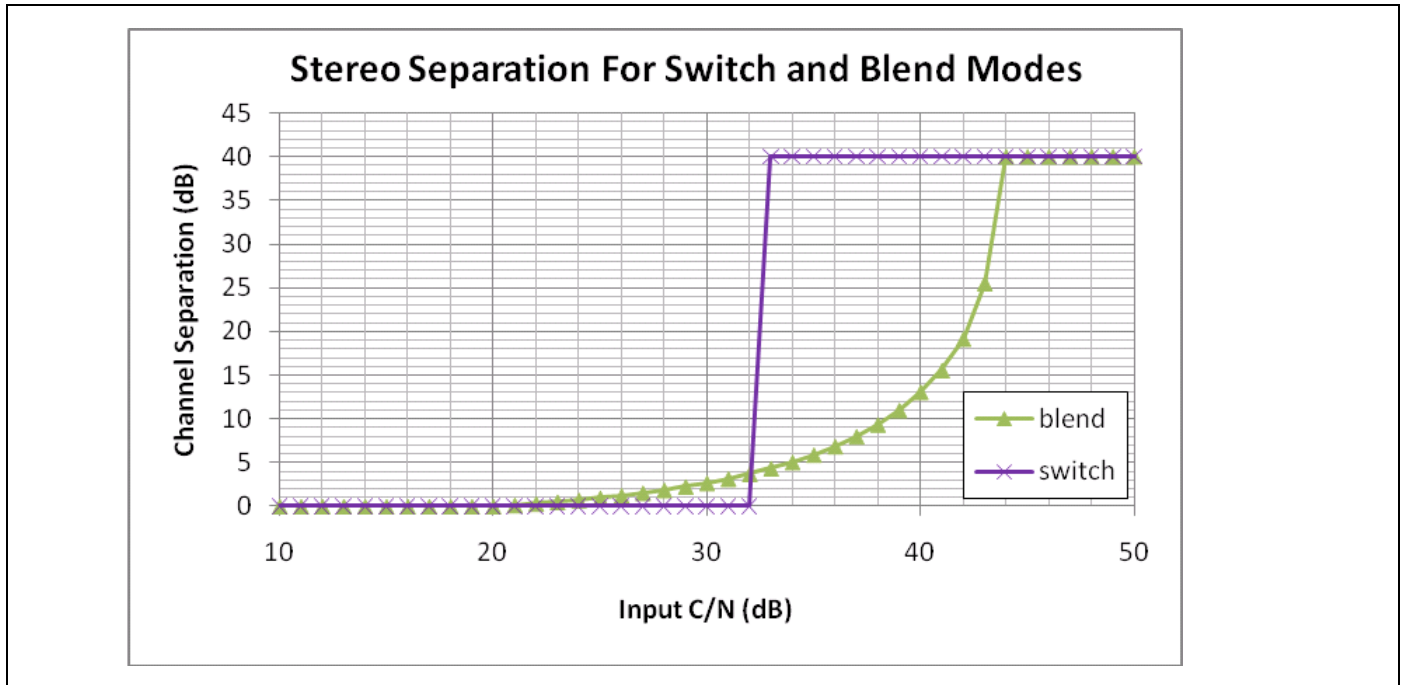
- Mono/Stereo Blend or Switch: The CYW4354 provides automatic control of the stereo or mono settings based on the FM signal carrier-to-noise ratio (C/N). This feature is used to maintain the best possible audio SNR based on the FM channel condition. Two modes of operation are supported:
 - Blend: In this mode, fine control of stereo separation is used to achieve optimal audio quality over a wide range of input C/N. The amount of separation is fully programmable. In [Figure 21](#), the separation is programmed to maintain a minimum 50 dB SNR across the blend range.
 - Extended blend: In this mode, stereo separation is maximized across a wide range of input CNR. Broadcom static suppression typically gives a static-free user experience to within 3 dB of ultimate sensitivity.

Figure 21. Example Blend/Switch Usage



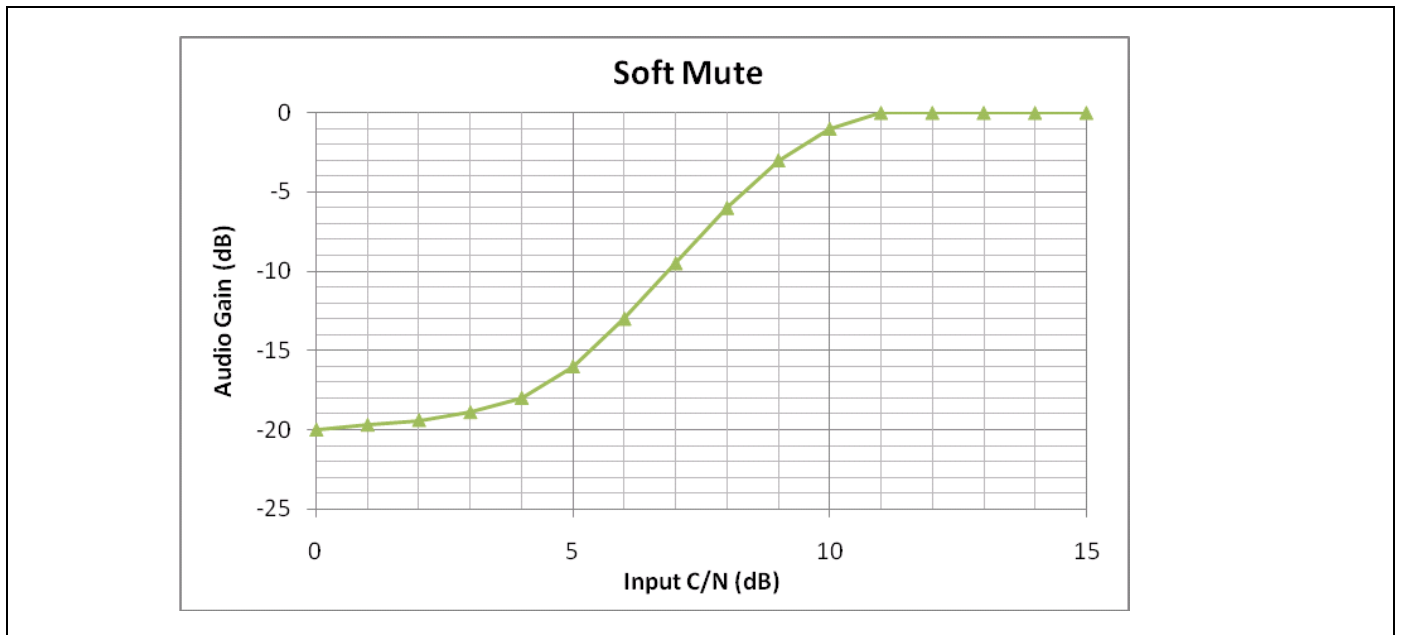
- Switch: In this mode, the audio switches from full stereo to full mono at a predetermined level to maintain optimal audio quality. The stereo-to-mono switch point and the mono-to-stereo switch points are fully programmable to provide the desired amount of audio SNR. In [Figure 22](#), the switch point is programmed to switch to mono to maintain a 40 dB SNR.

Figure 22. Example Blend/Switch Separation



- Soft Mute: Improves the user experience by dynamically muting the output audio proportionate to the FM signal C/N. This prevents the user from being assaulted with a blast of static. The mute characteristic is fully programmable to accommodate fine tuning of the output signal level. An example mute characteristic is shown in [Figure 23](#).

Figure 23. Example Soft Mute Characteristic



- **High Cut:** A programmable high-cut filter is provided to reduce the amount of high-frequency noise caused by static in the output audio signal. Like the soft mute circuit, it is fully programmable to allow for any amount of high cut based on the FM signal C/N.
- **Audio Pause Detect:** The FM receiver monitors the magnitude of the audio signal and notifies the host through an interrupt when the magnitude of the signal has fallen below the threshold set for a programmable period. This feature can be used to provide alternate frequency jumps during periods of silence to minimize disturbances to the listener. Filtering techniques are used within the audio pause detection block to provide more robust presence-to-silence detection and silence-to-presence detection.
- **Automatic Antenna Tuning:** The CYW4354 has an on-chip automatic antenna tuning network. When used with a single off-chip inductor, the on-chip circuitry automatically chooses an optimal on-chip matching component to obtain the highest signal strength for the desired frequency. The high-Q nature of this matching network simultaneously provides out-of-band blocking protection as well as a reduction of radiated spurious emissions from the FM antenna. It is designed to accommodate a wide range of external wire antennas.

8.9 RDS/RBDS

The CYW4354 integrates a RDS/RBDS modem and codec, the decoder includes programmable filtering and buffering functions, and the encoder includes the option to encode messages to PS or RT frame format with programmable scrolling in PS mode. The RDS/RBDS data can be read out in receive mode or delivered in transmit mode through either the HCI interface.

In addition, the RDS/RBDS functionality supports the following:

Receive

- Block decoding, error correction and synchronization
- Flywheel synchronization feature, allowing the host to set parameters for acquisition, maintenance, and loss of sync. (It is possible to set up the CYW4354 such that synch is achieved when a minimum of two good blocks (error free) are decoded in sequence. The number of good blocks required for sync is programmable.)
- Storage capability up to 126 blocks of RDS data
- Full or partial block B match detect and interrupt to host
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection and interrupt to host
- Automatic frequency jump
- Block E filtering
- Soft mute
- Signal dependent mono/stereo blend
- Programmable pre-emphasis

9. WLAN Global Functions

9.1 WLAN CPU and Memory Subsystem

The CYW4354 WLAN section includes an integrated ARM Cortex-R4™ 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering a performance gain of more than 30% over the ARM7TDMI® processor, the ARM Cortex-R4 processor implements the ARM v7-R architecture with support for the Thumb®-2 instruction set.

At 0.19 $\mu\text{W}/\text{MHz}$, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/ μW .

Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), integrated sleep modes, and extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 768 KB SRAM and 640 KB ROM.

9.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 484 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

9.3 GPIO Interface

The CYW4354 has 11 general-purpose I/O (GPIO) pins in the WLAN section that can be used to connect to various external devices.

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see [Table 27 on page 97](#).

9.4 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as GPS, or LTE, to manage wireless medium sharing for optimal performance.

Figure 24 and Figure 25 on page 49 show the LTE coexistence interface (including UART) for each CYW4354 package type. See Table 27 on page 97 for further details on multiplexed signals, such as the GPIO pins.

See Table 16 on page 40 for the UART baud rate.

Figure 24. Cypress GCI Mode LTE Coexistence Interface

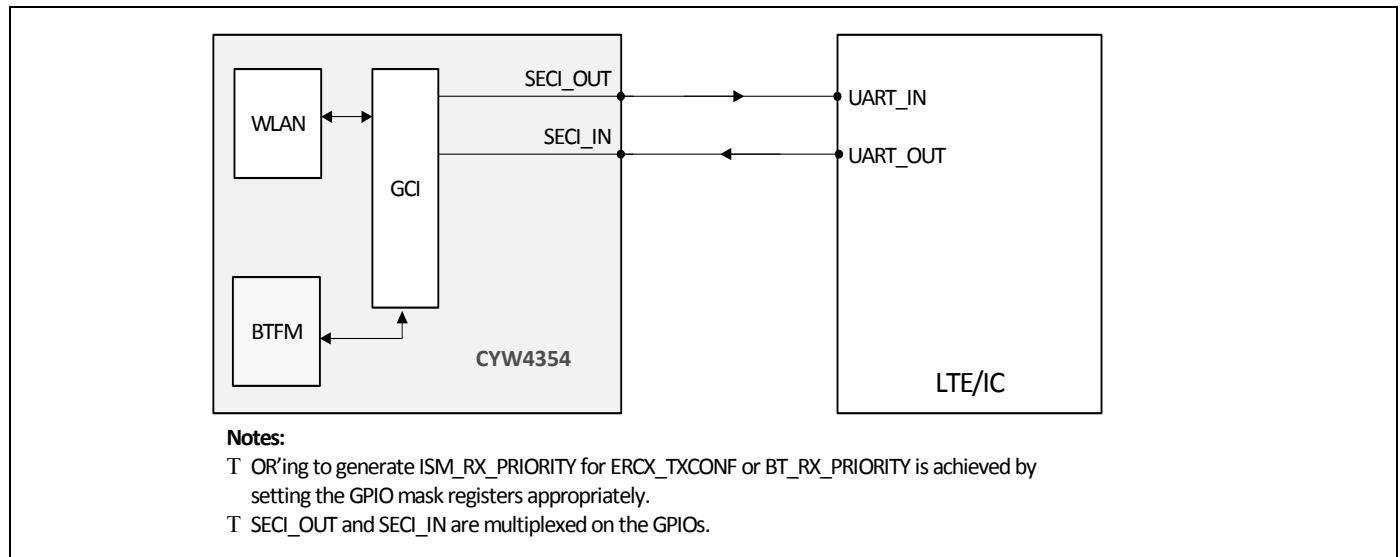
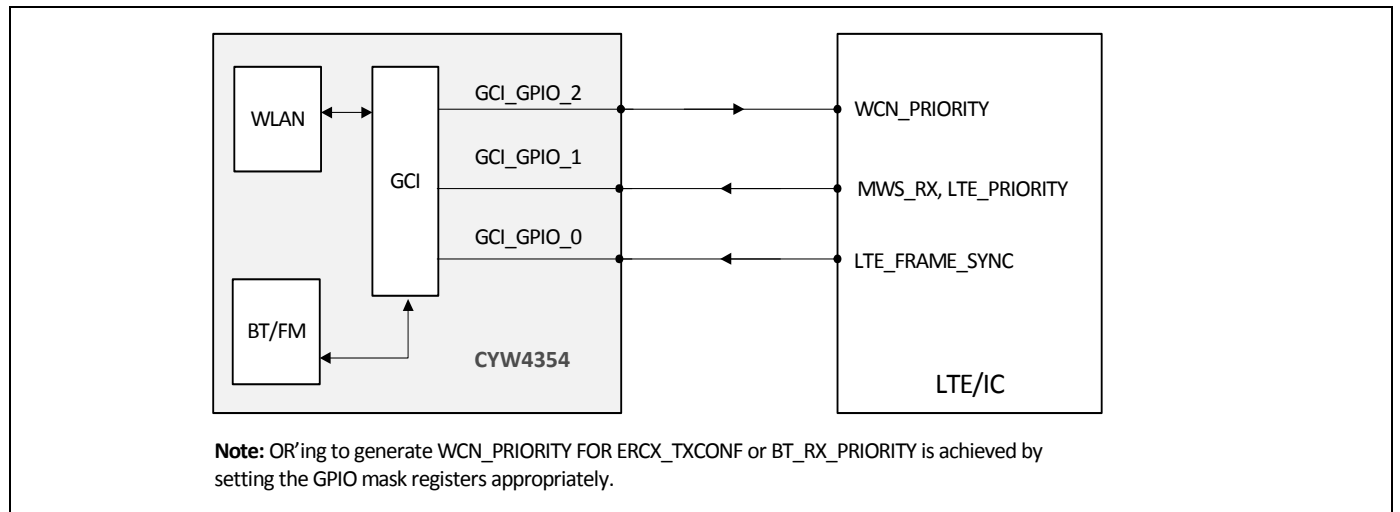


Figure 25. Legacy 3-Wire LTE Coexistence Interface



9.5 UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Refer to [Table 27 on page 97](#). Provided primarily for debugging during development, this UART enables the CYW4354 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

9.6 JTAG Interface

The CYW4354 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

Refer to [Table 27 on page 97](#) for JTAG pin assignments.

9.7 SPROM Interface

Various hardware configuration parameters may be stored in an external SPROM instead of the OTP. The SPROM is read by system software after device reset. In addition, depending on the board design, customer-specific parameters may be stored in SPROM.

The four SPROM control signals —SPROM_CS, SPROM_CLK, SPROM_MI, and SPROM_MO are multiplexed on the SDIO interface (see [Table 27 on page 97](#) for additional details). By default, the SPROM interface supports 2 kbit serial SPROMs, and it can also support 4 kbit and 16 kbit serial SPROMs by using the appropriate strapping option.

9.8 SFLASH Interface

For use only when the HSIC interface mode is selected, an interface to external SFLASH is available.

The four SFLASH control signals —SFLASH_CS#, SFLASH_CLK, SFLASH_MI, and SFLASH_MO are multiplexed on the SDIO interface (see [Table 27 on page 97](#) for additional details).

10. WLAN Host Interfaces

10.1 SDIO v3.0

All three package options of the CYW4354 WLAN section provide support for SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
- HS: High-speed up to 50 MHz (3.3V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 100 MHz (1.8V signaling).
- SDR104: SDR up to 208 MHz (1.8V signaling)
- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The CYW4354 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. Refer to [Table 24 on page 96](#) WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (max. BlockSize/ByteCount = 512B)

10.1.1 SDIO Pins

Table 18. SDIO Pin Descriptions

| SD 4-Bit Mode | | SD 1-Bit Mode | |
|---------------|--------------------------|---------------|--------------|
| DATA0 | Data line 0 | DATA | Data line |
| DATA1 | Data line 1 or Interrupt | IRQ | Interrupt |
| DATA2 | Data line 2 or Read Wait | RW | Read Wait |
| DATA3 | Data line 3 | N/C | Not used |
| CLK | Clock | CLK | Clock |
| CMD | Command line | CMD | Command line |

Figure 26. Signal Connections to SDIO Host (SD 4-Bit Mode)

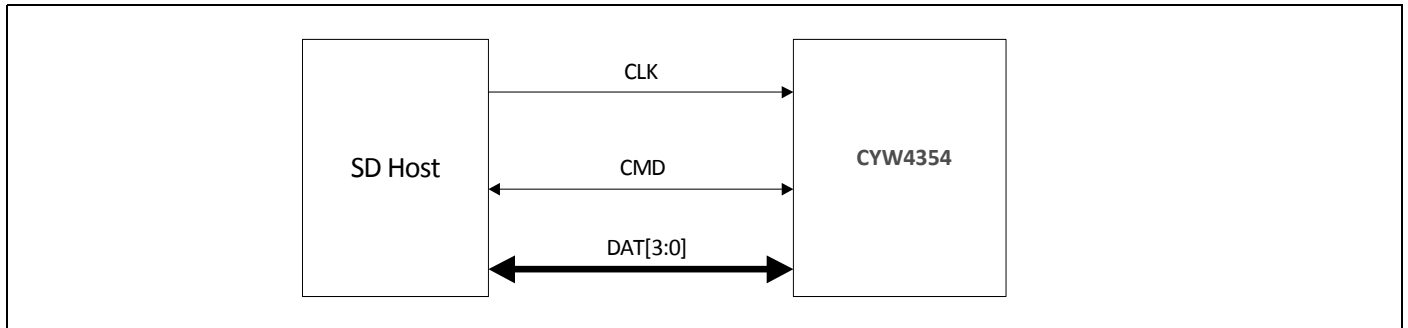
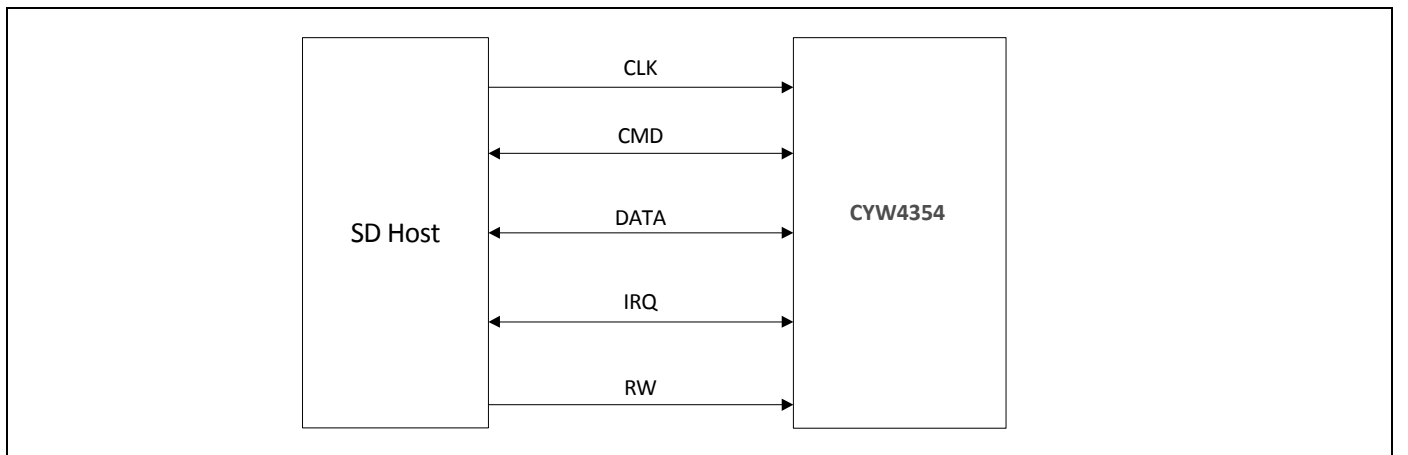


Figure 27. Signal Connections to SDIO Host (SD 1-Bit Mode)



Note:

Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

10.2 HSIC Interface

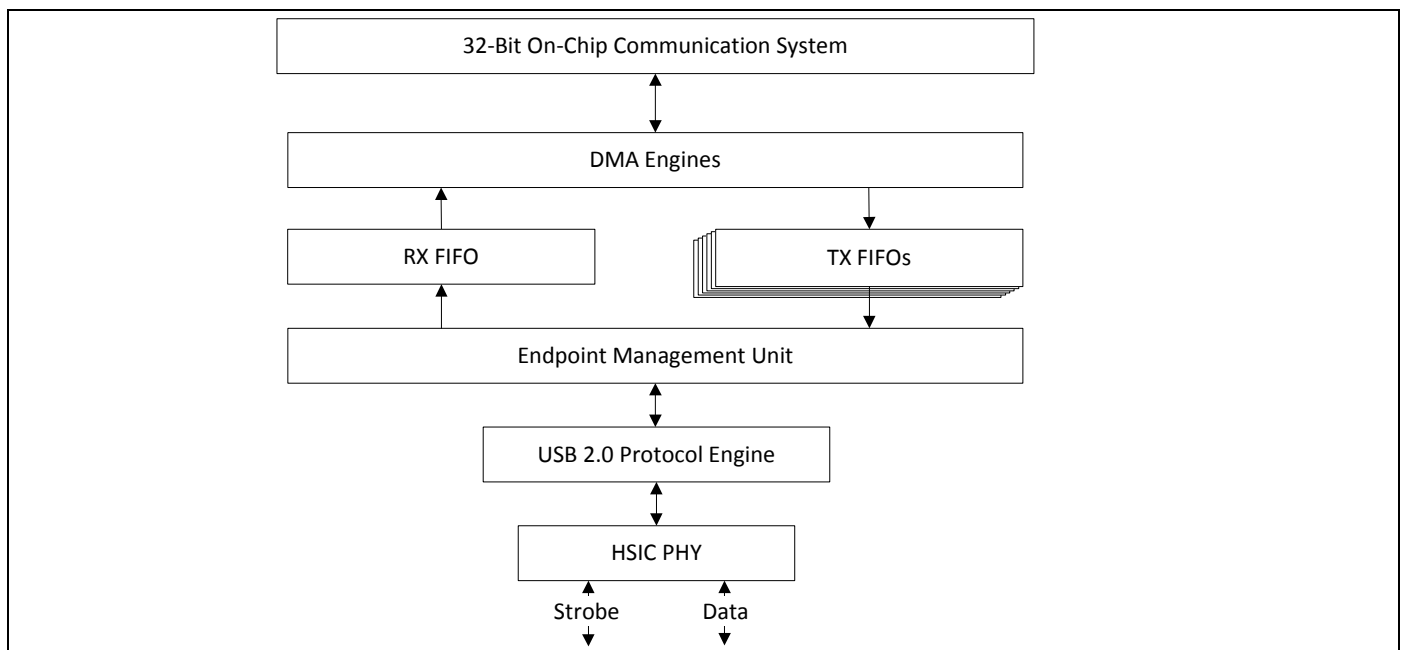
As an alternative to SDIO, an HSIC host interface can be enabled using the strapping option pins `strap_host_ifc_[3:1]`. HSIC is a simplified derivative of the USB2.0 interface designed to replace a standard USB PHY and cable for short distances (up to 10 cm) on board point-to-point connections. Using two signals, a bidirectional data strobe (STROBE) and a bidirectional DDR data signal (DATA), it provides high-speed serial 480 Mbps data transfers that are 100% host driver compatible with traditional USB 2.0 cable-connected topologies.

Figure 28 shows the blocks in the HSIC device core.

Key features of HSIC include:

- High-speed 480 Mbps data rate
- Source-synchronous serial interface using 1.2V LVCMOS signal levels
- No power consumed except when a data transfer is in progress
- Maximum trace length of 10 cm.
- No Plug-n-Play support, no hot attach/removal

Figure 28. HSIC Device Block Diagram



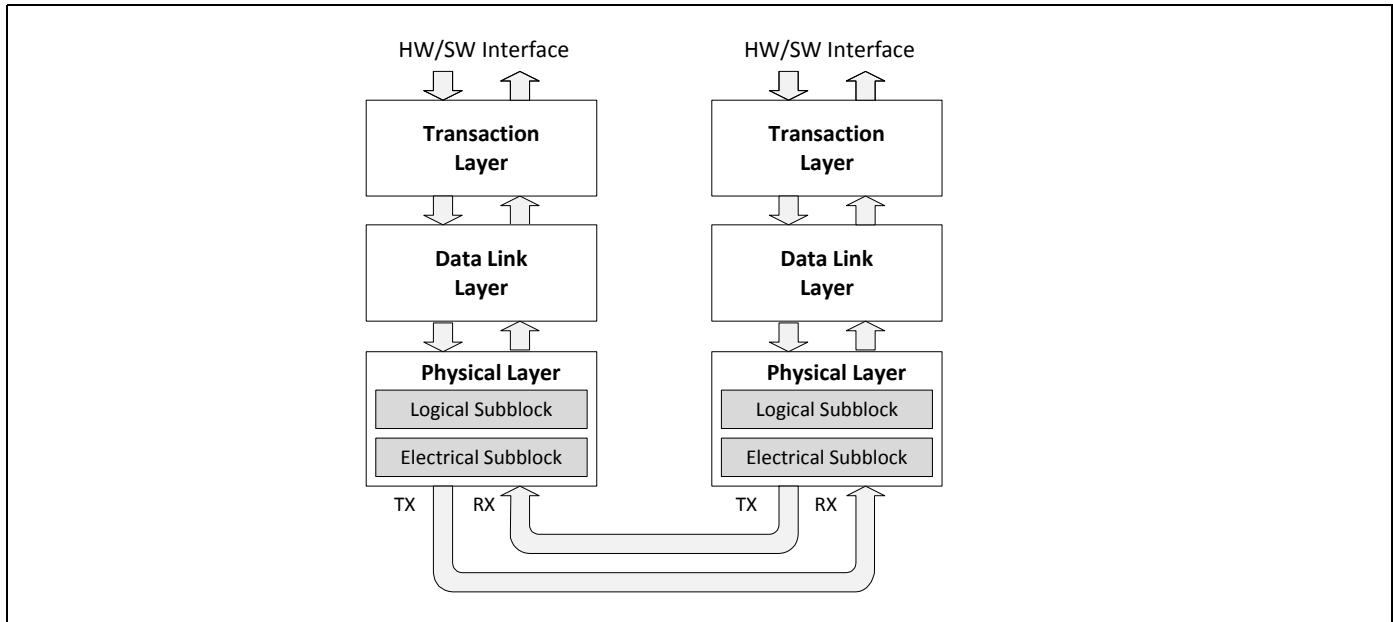
10.3 PCI Express Interface

The PCI Express (PCIe™) core on the CYW4354 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v3.0* running at Gen1 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 29. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW4354 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 29. PCI Express Layer Model



10.3.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW4354 device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and End-to-End CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

10.3.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

10.3.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW4354 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

10.3.4 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

10.3.5 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

10.3.6 8B/10B Encoder/Decoder

The PCIe core on the CYW4354 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

10.3.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

10.3.8 Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of Intersymbol Interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable Bit-Error Rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

10.3.9 Configuration Space

The PCIe function in the CYW4354 implements the configuration space as defined in the *PCI Express Base Specification v3.0*.

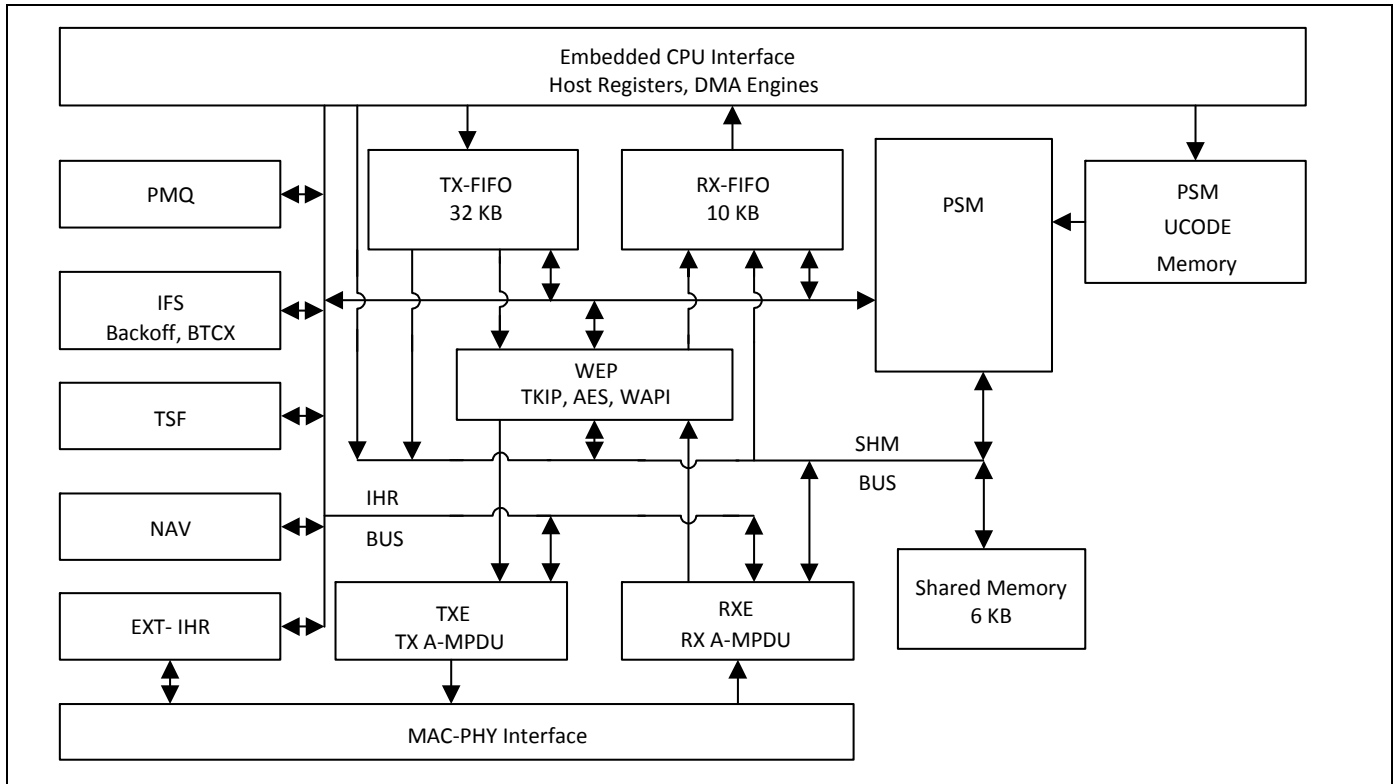
11. Wireless LAN MAC and PHY

11.1 IEEE 802.11ac Draft MAC

The CYW4354 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 30.

The following sections provide an overview of the important modules in the MAC.

Figure 30. WLAN MAC Architecture



The CYW4354 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac Draft features
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

11.1.1 PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

11.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

11.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

11.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

11.1.5 IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

11.1.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

11.1.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

11.1.8 MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

11.2 IEEE 802.11ac Draft PHY

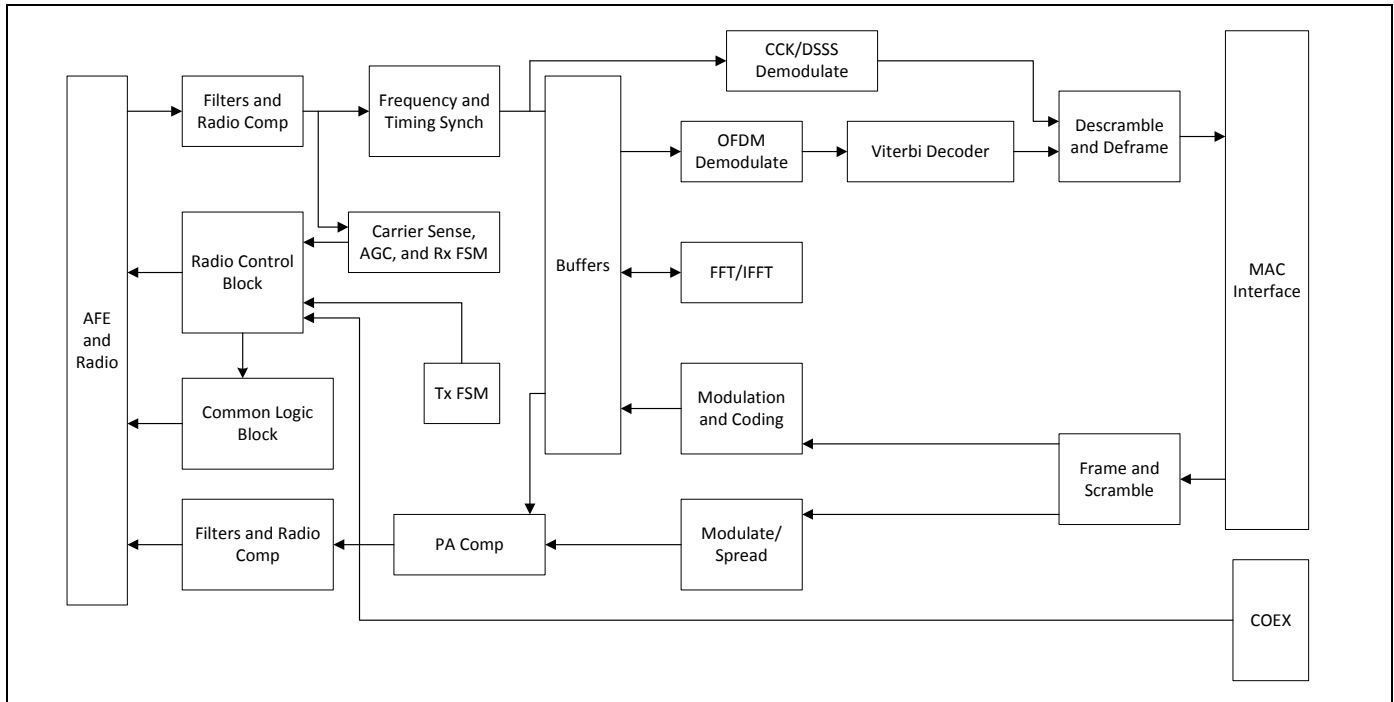
The CYW4354 WLAN Digital PHY (see [Figure 31 on page 60](#)) is designed to comply with IEEE 802.11ac Draft and IEEE 802.11a/b/g/n dual-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 866.7 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for sharing an antenna between WL and BT to support simultaneous RX-RX.

The key PHY features include:

- Programmable data rates from MCS0–15 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac Draft
- Supports Optional Short GI and Green Field modes in TX and RX
- TX and RX LDPC for improved range and power efficiency
- Beamforming support
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet RX antenna diversity
- Available per-packet channel quality and signal strength measurements
- Designed to meet FCC and other worldwide regulatory requirements

Figure 31. WLAN PHY Block Diagram



12. WLAN Radio Subsystem

The CYW4354 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Sixteen RF control signals are available (eight per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

A block diagram of the radio subsystem (core 0) is shown in [Figure 32 on page 62](#). Core 1, is identical to Core 0 without the Bluetooth blocks. The integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

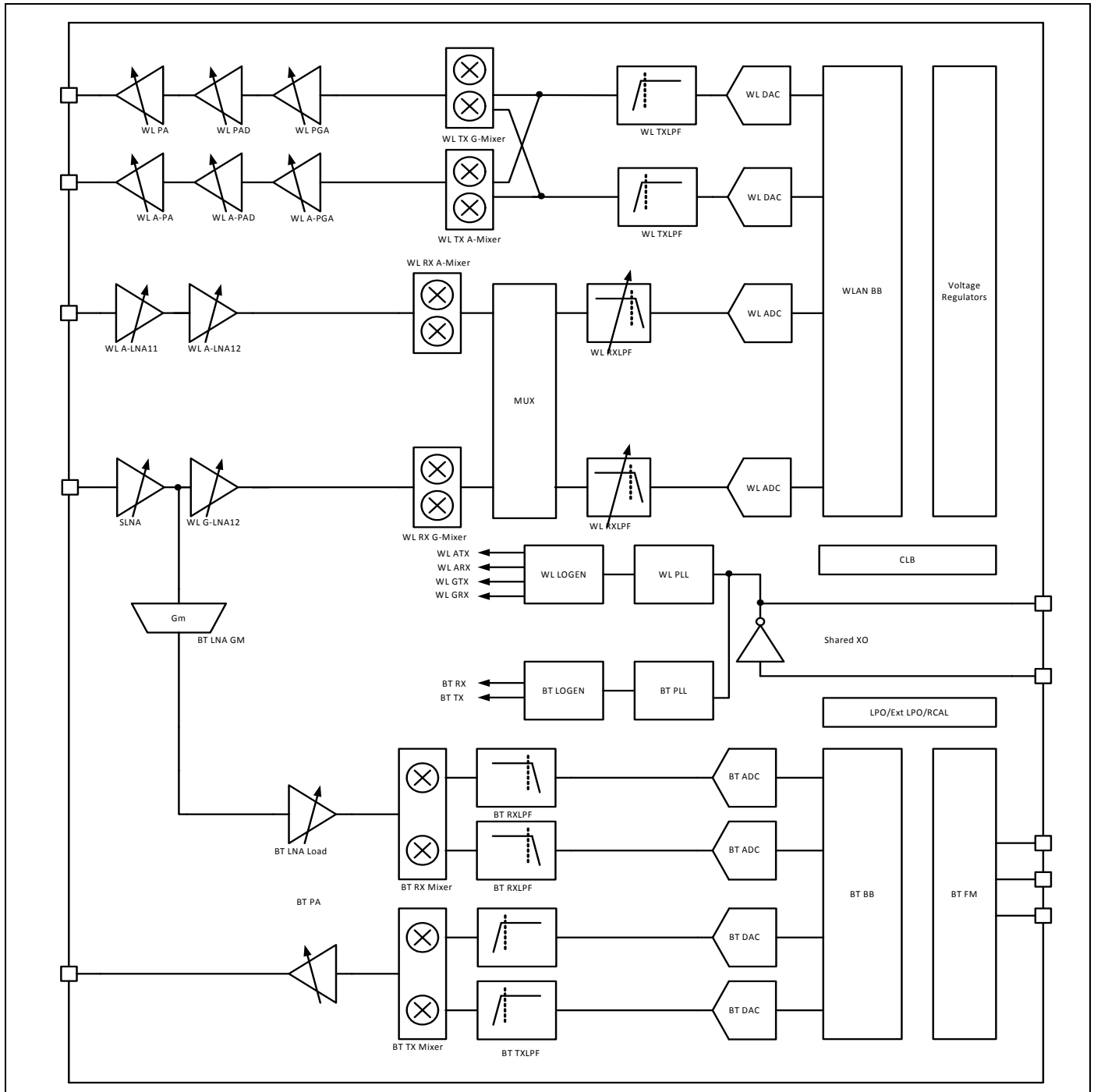
12.1 Receiver Path

The CYW4354 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low noise amplifier (LNA) in the 2.4 GHz path in core 0 is shared between the Bluetooth and WLAN receivers, whereas the 5 GHz receive path and the core 1 2.4 GHz receive path have dedicated on-chip LNAs. Control signals are available that can support the use of external LNAs for each band, which can increase the receive sensitivity by several dB.

12.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output power while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications, and without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated.

Figure 32. Radio Functional Block Diagram (core 0)



12.3 Calibration

The CYW4354 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

13. Pinout and Signal Descriptions

13.1 Ball Maps

Figure 33 and Figure 34 on page 64 show the WLBGA ball map.

Figure 33. WLBGA Ball Map, 4.87 mm × 7.67 mm Array, 192-Ball, A1–V6 (Bottom View—Balls Facing Up)

| 6 | 5 | 4 | 3 | 2 | 1 | |
|-----------------------|-------------------|-----------------------|-----------------------------|----------------------------|----------------------------|---|
| HSIC_DATA | PCIE_REFCLKN | PCIE_REFCLKP | PCIE_TDN | PCIE_TDP | | A |
| HSIC_AGND12PLL | PCIE_PLL_AVSS | PCIE_RXTX_AVSS | PCIE_PLL_AVDD1P2 | PCIE_RXTX_AVDD1P2 | PCIE_RDN | B |
| HSIC_DVDD12 | PCIE_PME_L | PCIE_PERST_L | PCIE_TESTP | PCIE_TESTN | PCIE_RDP | C |
| VSSC | PCIE_CLKREQ_L | VDDC | VSSC | | | D |
| GPIO_9 | BT_USB_DN | BT_VDDC | | FM_AUDIOVDD1P2 | FM_AOUT1 | E |
| LPO_IN | BT_USB_DP | CLK_REQ | FM_PLLVDD1P2 | FM_AUDIOVSS | FM_AOUT2 | F |
| BT_I2S_DO | BT_I2S_DI | VSSC | FM_PLLVSS | FM_VCOVSS | FM_LNAVCOVDD1P2 | G |
| | BT_UART_RXD | BT_PCM_OUT | BT_VDDC | FM_LNAVSS | FM_RFIN | H |
| BT_I2S_CLK | BT_UART_TXD | BT_PCM_IN | BT_HOST_WAKE | BT_VCOVSS | BT_VCOVDD1P2 | J |
| BT_PCM_SYNC | BT_UART_RTS_L | BT_GPIO_4 | BT_IFVDD1P2 | BT_PLLVDD1P2 | BT_LNAVDD1P2 | K |
| BT_I2S_WS | BT_UART_CTS_L | BT_DEV_WAKE | BT_PLLVSS | BT_PAVSS | BT_RF | L |
| BT_PCM_CLK | BT_VDDC | VSSC | BT_IFVSS | | BT_PAVDD2P5 | M |
| | RF_SW_CTRL_4 | | WRF_RX2G_GND1P2_CORE0 | WRF_LNA_2G_GND1P2_CORE0 | WRF_RFIN_2G_CORE0 | N |
| | RF_SW_CTRL_6 | WRF_AFE_GND1P2_CORE0 | WRF_TX_GND1P2_CORE0 | WRF_PA2G_VBAT_GND3P3_CORE0 | WRF_RFOUT_2G_CORE0 | P |
| WRF_LOGEN_GND1P2 | WRF_LOGENG_GND1P2 | WRF_GPIO_OUT_CORE0 | WRF_PADRV_VBAT_VDD3P3_CORE0 | WRF_PA2G_VBAT_GND3P3_CORE0 | WRF_PA2G_VBAT_VDD3P3_CORE0 | R |
| WRF_MMID_GND1P2 | WRF_MMID_VDD1P2 | WRF_PFD_VDD1P2 | WRF_PADRV_VBAT_GND3P3_CORE0 | WRF_PA5G_VBAT_GND3P3_CORE0 | WRF_PA5G_VBAT_VDD3P3_CORE0 | T |
| WRF_VCO_GND1P2 | WRF_PFD_GND1P2 | WRF_BUCK_VDD1P5_CORE0 | WRF_TSSI_A_CORE0 | WRF_PA5G_VBAT_GND3P3_CORE0 | WRF_RFOUT_5G_CORE0 | U |
| WRF_SYNTH_VBAT_VDD3P3 | WRF_CP_GND1P2 | WRF_BUCK_GND1P5_CORE0 | WRF_RX5G_GND1P2_CORE0 | WRF_LNA_5G_GND1P2_CORE0 | WRF_RFIN_5G_CORE0 | V |
| 6 | 5 | 4 | 3 | 2 | 1 | |

Figure 34. WLBGA Ball Map, 4.87 × 7.67 Array, 192-Ball, A7 – V12 (Bottom View—Balls Facing Up)

| | 12 | 11 | 10 | 9 | 8 | 7 |
|---|-------------------------|----------------------------|-----------------------------|-----------------------------|----------------------------|-------------------------|
| A | SR_PVSS | SR_VLX | WL_REG_ON | SDIO_CMD | SDIO_CLK | HSIC_STROBE |
| B | SR_VDDBATP5V | SR_VDDBATA5V | PMU_AVSS | SDIO_DATA_0 | SDIO_DATA_2 | VDDC |
| C | LDO_VDD1P5 | VOUT_CLDO | VSSC | SDIO_DATA_1 | SDIO_DATA_3 | HSIC_AVDD12PLL |
| D | VOUT_BTLD02P5 | VOUT_LNLDO | BT_REG_ON | JTAG_SEL | | RREFHSIC |
| E | LDO_VDDBAT5V | VOUT_LDO3P3_B | VDDIO | VDDC | VDDIO_SD | GPIO_7 |
| F | VOUT_3P3 | GPIO_2 | GPIO_1 | GPIO_5 | GPIO_6 | GPIO_8 |
| G | VSSC | GPIO_0 | VDDC | GPIO_3 | VSSC | AVSS_BBPLL |
| H | GPIO_10 | VDDIO_RF | | GPIO_4 | | AVDD_BBPLL |
| J | VDDC | RF_SW_CTRL_9 | | RF_SW_CTRL_12 | VDDC | |
| K | RF_SW_CTRL_8 | | RF_SW_CTRL_13 | | | BT_VDDIO |
| L | | VSSC | VDDC | RF_SW_CTRL_11 | RF_SW_CTRL_15 | VSSC |
| M | RF_SW_CTRL_10 | | RF_SW_CTRL_14 | | RF_SW_CTRL_7 | VDDC |
| N | WRF_XTAL_OUT | WRF_XTAL_GND1P2 | WRF_XTAL_VDD1P2 | | RF_SW_CTRL_1 | RF_SW_CTRL_3 |
| P | WRF_XTAL_IN | WRF_XTAL_VDD1P5 | | RF_SW_CTRL_2 | | RF_SW_CTRL_5 |
| R | WRF_BUCK_GND1P5_CORE1 | WRF_BUCK_VDD1P5_CORE1 | | WRF_GPIO_OUT_CORE1 | WRF_AFE_GND1P2_CORE1 | RF_SW_CTRL_0 |
| T | WRF_RX5G_GND1P2_CORE1 | WRF_TSSI_A_CORE1 | WRF_PADRV_VBAT_GND3P3_CORE1 | WRF_PADRV_VBAT_VDD3P3_CORE1 | WRF_TX_GND1P2_CORE1 | WRF_RX2G_GND1P2_CORE1 |
| U | WRF_LNA_5G_GND1P2_CORE1 | WRF_PA5G_VBAT_GND3P3_CORE1 | WRF_PA5G_VBAT_GND3P3_CORE1 | WRF_PA2G_VBAT_GND3P3_CORE1 | WRF_PA2G_VBAT_GND3P3_CORE1 | WRF_LNA_2G_GND1P2_CORE1 |
| V | WRF_RFIN_5G_CORE1 | WRF_RFOUT_5G_CORE1 | WRF_PA5G_VBAT_VDD3P3_CORE1 | WRF_PA2G_VBAT_VDD3P3_CORE1 | WRF_RFOUT_2G_CORE1 | WRF_RFIN_2G_CORE1 |
| | 12 | 11 | 10 | 9 | 8 | 7 |

13.2 Pin Lists
Table 19. Pin List by Pin Number (192-Pin WLBGA Package)

| WLBGA Ball# | Pin Name |
|-------------|-------------------|
| A10 | WL_REG_ON |
| A11 | SR_VLX |
| A12 | SR_PVSS |
| A2 | PCIE_TDP0 |
| A3 | PCIE_TDNO |
| A4 | PCIE_REFCLKP |
| A5 | PCIE_REFCLKN |
| A6 | HSIC_DATA |
| A7 | HSIC_STROBE |
| A8 | SDIO_CLK |
| A9 | SDIO_CMD |
| B1 | PCIE_RDN0 |
| B10 | PMU_AVSS |
| B11 | SR_VDDBATA5V |
| B12 | SR_VDDBATP5V |
| B2 | PCIE_RXTX_AVDD1P2 |
| B3 | PCIE_PLL_AVDD1P2 |
| B4 | PCIE_RXTX_AVSS |
| B5 | PCIE_PLL_AVSS |
| B6 | HSIC_AGND12PLL |
| B7 | VDD/VDDC |
| B8 | SDIO_DATA_2 |
| B9 | SDIO_DATA_0 |
| C1 | PCIE_RDP0 |
| C10 | VSSC/VSS |
| C11 | VOUT_CLDO |
| C12 | LDO_VDD1P5 |
| C2 | PCIE_TESTN |
| C3 | PCIE_TESTP |
| C4 | PCIE_PERST_L |
| C5 | PCIE_PME_L |
| C6 | HSIC_DVDD12 |
| C7 | HSIC_AVDD12PLL |
| C8 | SDIO_DATA_3 |
| C9 | SDIO_DATA_1 |
| D10 | BT_REG_ON |
| D11 | VOUT_LNLDO |
| D12 | VOUT_BTLDO2P5 |
| D3 | VSSC/VSS |
| D4 | VDD/VDDC |
| D5 | PCIE_CLKREQ_L |

| WLBGA Ball# | Pin Name |
|-------------|-----------------|
| D6 | VSSC/VSS |
| D7 | RREFHSIC |
| D9 | JTAG_SEL |
| E1 | FM_AOUT1 |
| E10 | VDDIO |
| E11 | VOUT_LDO3P3_B |
| E12 | LDO_VDDBAT5V |
| E2 | FM_AUDIOVDD1P2 |
| E4 | BT_VDD/VDDC |
| E5 | BT_USB_DN |
| E6 | GPIO_9 |
| E7 | GPIO_7 |
| E8 | VDDIO_SD |
| E9 | VDD/VDDC |
| F1 | FM_AOUT2 |
| F10 | GPIO_1 |
| F11 | GPIO_2 |
| F12 | VOUT_3P3 |
| F2 | FM_AUDIOVSS |
| F3 | FM_PLLVDD1P2 |
| F4 | CLK_REQ |
| F5 | BT_USB_DP |
| F6 | LPO_IN |
| F7 | GPIO_8 |
| F8 | GPIO_6 |
| F9 | GPIO_5 |
| G1 | FM_LNAVCOVDD1P2 |
| G10 | VDD/VDDC |
| G11 | GPIO_0 |
| G12 | VSSC/VSS |
| G2 | FM_VCOVSS |
| G3 | FM_PLLVSS |
| G4 | VSSC/VSS |
| G5 | BT_I2S_DI |
| G6 | BT_I2S_DO |
| G7 | AVSS_BBPLL |
| G8 | VSSC/VSS |
| G9 | GPIO_3 |
| H1 | FM_RFIN |
| H11 | VDDIO_RF |
| H12 | GPIO_10 |

| WLBGA Ball# | Pin Name |
|-------------|---------------|
| H2 | FM_LNAVSS |
| H3 | BT_VDD/VDDC |
| H4 | BT_PCM_OUT |
| H5 | BT_UART_RXD |
| H7 | AVDD_BBPLL |
| H9 | GPIO_4 |
| J1 | BT_VCOVDD1P2 |
| J11 | RF_SW_CTRL_9 |
| J12 | VDD/VDDC |
| J2 | BT_VCOVSS |
| J3 | BT_HOST_WAKE |
| J4 | BT_PCM_IN |
| J5 | BT_UART_TXD |
| J6 | BT_I2S_CLK |
| J8 | VDD/VDDC |
| J9 | RF_SW_CTRL_12 |
| K1 | BT_LNAVDD1P2 |
| K10 | RF_SW_CTRL_13 |
| K12 | RF_SW_CTRL_8 |
| K2 | BT_PLLVDD1P2 |
| K3 | BT_IFVDD1P2 |
| K4 | BT_GPIO_4 |
| K5 | BT_UART_RTS_L |
| K6 | BT_PCM_SYNC |
| K7 | BT_VDDIO |
| L1 | BT_RF |
| L10 | VDD/VDDC |
| L11 | VSSC/VSS |
| L2 | BT_PAVSS |
| L3 | BT_PLLVSS |
| L4 | BT_DEV_WAKE |
| L5 | BT_UART_CTS_L |
| L6 | BT_I2S_WS |
| L7 | VSSC/VSS |
| L8 | RF_SW_CTRL_15 |
| L9 | RF_SW_CTRL_11 |
| M1 | BT_PAVDD2P5 |
| M10 | RF_SW_CTRL_14 |
| M12 | RF_SW_CTRL_10 |
| M3 | BT_IFVSS |
| M4 | VSSC/VSS |
| M5 | BT_VDD/VDDC |
| M6 | BT_PCM_CLK |

| WLBGA Ball# | Pin Name |
|-------------|-----------------------------|
| M7 | VDD/VDDC |
| M8 | RF_SW_CTRL_7 |
| N1 | WRF_RFIN_2G_CORE0 |
| N10 | WRF_XTAL_VDD1P2 |
| N11 | WRF_XTAL_GND1P2 |
| N12 | WRF_XTAL_OUT |
| N2 | WRF_LNA_2G_GND1P2_CORE0 |
| N3 | WRF_RX2G_GND1P2_CORE0 |
| N5 | RF_SW_CTRL_4 |
| N7 | RF_SW_CTRL_3 |
| N8 | RF_SW_CTRL_1 |
| P1 | WRF_RFOUT_2G_CORE0 |
| P11 | WRF_XTAL_VDD1P5 |
| P12 | WRF_XTAL_IN |
| P2 | WRF_PA2G_VBAT_GND3P3_CORE0 |
| P3 | WRF_TX_GND1P2_CORE0 |
| P4 | WRF_AFE_GND1P2_CORE0 |
| P5 | RF_SW_CTRL_6 |
| P7 | RF_SW_CTRL_5 |
| P9 | RF_SW_CTRL_2 |
| R1 | WRF_PA2G_VBAT_VDD3P3_CORE0 |
| R11 | WRF_BUCK_VDD1P5_CORE1 |
| R12 | WRF_BUCK_GND1P5_CORE1 |
| R2 | WRF_PA2G_VBAT_GND3P3_CORE0 |
| R3 | WRF_PADRV_VBAT_VDD3P3_CORE0 |
| R4 | WRF_GPIO_OUT_CORE0 |
| R5 | WRF_LOGENG_GND1P2 |
| R6 | WRF_LOGEN_GND1P2 |
| R7 | RF_SW_CTRL_0 |
| R8 | WRF_AFE_GND1P2_CORE1 |
| R9 | WRF_GPIO_OUT_CORE1 |
| T1 | WRF_PA5G_VBAT_VDD3P3_CORE0 |
| T10 | WRF_PADRV_VBAT_GND3P3_CORE1 |
| T11 | WRF_TSSI_A_CORE1 |
| T12 | WRF_RX5G_GND1P2_CORE1 |
| T2 | WRF_PA5G_VBAT_GND3P3_CORE0 |
| T3 | WRF_PADRV_VBAT_GND3P3_CORE0 |
| T4 | WRF_PFD_VDD1P2 |
| T5 | WRF_MMD_VDD1P2 |
| T6 | WRF_MMD_GND1P2 |
| T7 | WRF_RX2G_GND1P2_CORE1 |
| T8 | WRF_TX_GND1P2_CORE1 |
| T9 | WRF_PADRV_VBAT_VDD3P3_CORE1 |

| WLBGA Ball# | Pin Name |
|-------------|----------------------------|
| U1 | WRF_RFOUT_5G_CORE0 |
| U10 | WRF_PA5G_VBAT_GND3P3_CORE1 |
| U11 | WRF_PA5G_VBAT_GND3P3_CORE1 |
| U12 | WRF_LNA_5G_GND1P2_CORE1 |
| U2 | WRF_PA5G_VBAT_GND3P3_CORE0 |
| U3 | WRF_TSSI_A_CORE0 |
| U4 | WRF_BUCK_VDD1P5_CORE0 |
| U5 | WRF_PFD_GND1P2 |
| U6 | WRF_VCO_GND1P2 |
| U7 | WRF_LNA_2G_GND1P2_CORE1 |
| U8 | WRF_PA2G_VBAT_GND3P3_CORE1 |
| U9 | WRF_PA2G_VBAT_GND3P3_CORE1 |
| V1 | WRF_RFIN_5G_CORE0 |
| V10 | WRF_PA5G_VBAT_VDD3P3_CORE1 |
| V11 | WRF_RFOUT_5G_CORE1 |
| V12 | WRF_RFIN_5G_CORE1 |
| V2 | WRF_LNA_5G_GND1P2_CORE0 |
| V3 | WRF_RX5G_GND1P2_CORE0 |
| V4 | WRF_BUCK_GND1P5_CORE0 |
| V5 | WRF_CP_GND1P2 |
| V6 | WRF_SYNTH_VBAT_VDD3P3 |
| V7 | WRF_RFIN_2G_CORE1 |
| V8 | WRF_RFOUT_2G_CORE1 |
| V9 | WRF_PA2G_VBAT_VDD3P3_CORE1 |

Table 20. Pin List by Pin Name (192-Pin WLBGA Package)

| Pin Name | WLBGA Ball# |
|-----------------|-------------|
| AVDD_BBPLL | H7 |
| AVSS_BBPLL | G7 |
| BT_DEV_WAKE | L4 |
| BT_GPIO_4 | K4 |
| BT_HOST_WAKE | J3 |
| BT_I2S_CLK | J6 |
| BT_I2S_DI | G5 |
| BT_I2S_DO | G6 |
| BT_I2S_WS | L6 |
| BT_IFVDD1P2 | K3 |
| BT_IFVSS | M3 |
| BT_LNAVDD1P2 | K1 |
| BT_PAVDD2P5 | M1 |
| BT_PAVSS | L2 |
| BT_PCM_CLK | M6 |
| BT_PCM_IN | J4 |
| BT_PCM_OUT | H4 |
| BT_PCM_SYNC | K6 |
| BT_PLLVDD1P2 | K2 |
| BT_PLLVSS | L3 |
| BT_REG_ON | D10 |
| BT_RF | L1 |
| BT_UART_CTS_L | L5 |
| BT_UART_RTS_L | K5 |
| BT_UART_RXD | H5 |
| BT_UART_TXD | J5 |
| BT_USB_DN | E5 |
| BT_USB_DP | F5 |
| BT_VCOVDD1P2 | J1 |
| BT_VCOVSS | J2 |
| BT_VDDIO | K7 |
| CLK_REQ | F4 |
| FM_AOUT1 | E1 |
| FM_AOUT2 | F1 |
| FM_AUDIOVDD1P2 | E2 |
| FM_AUDIOVSS | F2 |
| FM_LNAVCOVDD1P2 | G1 |
| FM_LNAVSS | H2 |
| FM_PLLVDD1P2 | F3 |
| FM_PLLVSS | G3 |
| FM_RFIN | H1 |
| FM_VCOVSS | G2 |
| GPIO_0 | G11 |

| Pin Name | WLBGA Ball# |
|-------------------|-------------|
| GPIO_1 | F10 |
| GPIO_10 | H12 |
| GPIO_2 | F11 |
| GPIO_3 | G9 |
| GPIO_4 | H9 |
| GPIO_5 | F9 |
| GPIO_6 | F8 |
| GPIO_7 | E7 |
| GPIO_8 | F7 |
| GPIO_9 | E6 |
| HSIC_AGND12PLL | B6 |
| HSIC_AVDD12PLL | C7 |
| HSIC_DATA | A6 |
| HSIC_DVDD12 | C6 |
| HSIC_STROBE | A7 |
| JTAG_SEL | D9 |
| LDO_VDD1P5 | C12 |
| LDO_VDDBAT5V | E12 |
| LPO_IN | F6 |
| PCIE_PME_L | C5 |
| PCIE_CLKREQ_L | D5 |
| PCIE_PERST_L | C4 |
| PCIE_PLL_AVDD1P2 | B3 |
| PCIE_PLL_AVSS | B5 |
| PCIE_RDN0 | B1 |
| PCIE_RDP0 | C1 |
| PCIE_REFCLKN | A5 |
| PCIE_REFCLKP | A4 |
| PCIE_RXTX_AVDD1P2 | B2 |
| PCIE_RXTX_AVSS | B4 |
| PCIE_TDN0 | A3 |
| PCIE_TDP0 | A2 |
| PCIE_TESTN | C2 |
| PCIE_TESTP | C3 |
| PMU_AVSS | B10 |
| RF_SW_CTRL_0 | R7 |
| RF_SW_CTRL_1 | N8 |
| RF_SW_CTRL_10 | M12 |
| RF_SW_CTRL_11 | L9 |
| RF_SW_CTRL_12 | J9 |
| RF_SW_CTRL_13 | K10 |
| RF_SW_CTRL_14 | M10 |
| RF_SW_CTRL_15 | L8 |

| Pin Name | WLBGA Ball# |
|---------------|-------------|
| RF_SW_CTRL_2 | P9 |
| RF_SW_CTRL_3 | N7 |
| RF_SW_CTRL_4 | N5 |
| RF_SW_CTRL_5 | P7 |
| RF_SW_CTRL_6 | P5 |
| RF_SW_CTRL_7 | M8 |
| RF_SW_CTRL_8 | K12 |
| RF_SW_CTRL_9 | J11 |
| RREFHSIC | D7 |
| SDIO_CLK | A8 |
| SDIO_CMD | A9 |
| SDIO_DATA_0 | B9 |
| SDIO_DATA_1 | C9 |
| SDIO_DATA_2 | B8 |
| SDIO_DATA_3 | C8 |
| SR_PVSS | A12 |
| SR_VDDBATA5V | B11 |
| SR_VDDBATP5V | B12 |
| SR_VLX | A11 |
| VDD/VDDC | B7 |
| VDD/VDDC | D4 |
| BT_VDD/VDDC | E4 |
| VDD/VDDC | E9 |
| VDD/VDDC | G10 |
| BT_VDD/VDDC | H3 |
| VDD/VDDC | J12 |
| VDD/VDDC | J8 |
| VDD/VDDC | L10 |
| BT_VDD/VDDC | M5 |
| VDD/VDDC | M7 |
| VDDIO | E10 |
| VDDIO_RF | H11 |
| VDDIO_SD | E8 |
| VOUT_3P3 | F12 |
| VOUT_BTLDO2P5 | D12 |
| VOUT_CLDO | C11 |
| VOUT_LDO3P3_B | E11 |
| VOUT_LNLDO | D11 |
| VSSC/VSS | C10 |
| VSSC/VSS | D3 |
| VSSC/VSS | D6 |
| VSSC/VSS | G12 |
| VSSC/VSS | G4 |
| VSSC/VSS | G8 |

| Pin Name | WLBGA Ball# |
|-----------------------------|-------------|
| VSSC/VSS | L11 |
| VSSC/VSS | L7 |
| VSSC/VSS | M4 |
| WL_REG_ON | A10 |
| WRF_AFE_GND1P2_CORE0 | P4 |
| WRF_AFE_GND1P2_CORE1 | R8 |
| WRF_BUCK_GND1P5_CORE0 | V4 |
| WRF_BUCK_GND1P5_CORE1 | R12 |
| WRF_BUCK_VDD1P5_CORE0 | U4 |
| WRF_BUCK_VDD1P5_CORE1 | R11 |
| WRF_CP_GND1P2 | V5 |
| WRF_GPIO_OUT_CORE0 | R4 |
| WRF_GPIO_OUT_CORE1 | R9 |
| WRF_LNA_2G_GND1P2_CORE0 | N2 |
| WRF_LNA_2G_GND1P2_CORE1 | U7 |
| WRF_LNA_5G_GND1P2_CORE0 | V2 |
| WRF_LNA_5G_GND1P2_CORE1 | U12 |
| WRF_LOGEN_GND1P2 | R6 |
| WRF_LOGENG_GND1P2 | R5 |
| WRF_MMD_GND1P2 | T6 |
| WRF_MMD_VDD1P2 | T5 |
| WRF_PA2G_VBAT_GND3P3_CORE0 | P2 |
| WRF_PA2G_VBAT_GND3P3_CORE0 | R2 |
| WRF_PA2G_VBAT_GND3P3_CORE1 | U8 |
| WRF_PA2G_VBAT_GND3P3_CORE1 | U9 |
| WRF_PA2G_VBAT_VDD3P3_CORE0 | R1 |
| WRF_PA2G_VBAT_VDD3P3_CORE1 | V9 |
| WRF_PA5G_VBAT_GND3P3_CORE0 | T2 |
| WRF_PA5G_VBAT_GND3P3_CORE0 | U2 |
| WRF_PA5G_VBAT_GND3P3_CORE1 | U10 |
| WRF_PA5G_VBAT_GND3P3_CORE1 | U11 |
| WRF_PA5G_VBAT_VDD3P3_CORE0 | T1 |
| WRF_PA5G_VBAT_VDD3P3_CORE1 | V10 |
| WRF_PADRV_VBAT_GND3P3_CORE0 | T3 |
| WRF_PADRV_VBAT_GND3P3_CORE1 | T10 |
| WRF_PADRV_VBAT_VDD3P3_CORE0 | R3 |
| WRF_PADRV_VBAT_VDD3P3_CORE1 | T9 |
| WRF_PFD_GND1P2 | U5 |
| WRF_PFD_VDD1P2 | T4 |
| WRF_RFIN_2G_CORE0 | N1 |
| WRF_RFIN_2G_CORE1 | V7 |
| WRF_RFIN_5G_CORE0 | V1 |
| WRF_RFIN_5G_CORE1 | V12 |
| WRF_RFOUT_2G_CORE0 | P1 |

| Pin Name | WLBGA Ball# |
|-----------------------|-------------|
| WRF_RFOUT_2G_CORE1 | V8 |
| WRF_RFOUT_5G_CORE0 | U1 |
| WRF_RFOUT_5G_CORE1 | V11 |
| WRF_RX2G_GND1P2_CORE0 | N3 |
| WRF_RX2G_GND1P2_CORE1 | T7 |
| WRF_RX5G_GND1P2_CORE0 | V3 |
| WRF_RX5G_GND1P2_CORE1 | T12 |
| WRF_SYNTH_VBAT_VDD3P3 | V6 |
| WRF_TSSI_A_CORE0 | U3 |
| WRF_TSSI_A_CORE1 | T11 |
| WRF_TX_GND1P2_CORE0 | P3 |
| WRF_TX_GND1P2_CORE1 | T8 |
| WRF_VCO_GND1P2 | U6 |
| WRF_XTAL_GND1P2 | N11 |
| WRF_XTAL_IN | P12 |
| WRF_XTAL_OUT | N12 |
| WRF_XTAL_VDD1P2 | N10 |
| WRF_XTAL_VDD1P5 | P11 |

Table 21. 395-Bump WLCSP Coordinates

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|-------------------|---------------------------------|---------|----------|---------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 1 | PCIE_RXTX_AVSS | 2300.51 | 3659.87 | -2300.51 | 3659.87 |
| 2 | PCIE_PLL_AVSS | 1966.81 | 3659.87 | -1966.81 | 3659.87 |
| 3 | PCIE_REFCLKP | 1966.81 | 3434.87 | -1966.81 | 3434.87 |
| 4 | PCIE_REFCLKN | 1800.31 | 3547.37 | -1800.31 | 3547.37 |
| 5 | PCIE_TDN0 | 2134.01 | 3547.37 | -2134.01 | 3547.37 |
| 6 | PCIE_TDP0 | 2134.01 | 3322.37 | -2134.01 | 3322.37 |
| 7 | PCIE_RXTX_AVDD1P2 | 2134.01 | 3068.53 | -2134.01 | 3068.53 |
| 8 | PCIE_RDP0 | 2300.51 | 3209.87 | -2300.51 | 3209.87 |
| 9 | PCIE_RDN0 | 2300.51 | 3434.87 | -2300.51 | 3434.87 |
| 10 | PCIE_PLL_AVSS | 1966.81 | 3209.87 | -1966.81 | 3209.87 |
| 11 | PCIE_PLL_AVDD1P2 | 1800.31 | 3322.37 | -1800.31 | 3322.37 |
| 12 | USB3_REFCLKN | 508.44 | 3481.00 | -508.44 | 3481.00 |
| 13 | USB3_PVDD1P2 | 768.62 | 3062.57 | -768.62 | 3062.57 |
| 14 | USB3_REFCLKP | 508.44 | 3281.00 | -508.44 | 3281.00 |
| 15 | USB3_RVDD1P2 | 1177.22 | 3062.57 | -1177.22 | 3062.57 |
| 16 | USB3_TVDD1P2 | 972.92 | 3062.57 | -972.92 | 3062.57 |
| 17 | USB3_PGND | 553.11 | 3681.00 | -553.11 | 3681.00 |
| 18 | USB3_PGND | 753.11 | 3681.00 | -753.11 | 3681.00 |
| 19 | USB3_PTESTP | 773.17 | 3481.00 | -773.17 | 3481.00 |
| 20 | USB3_PTESTN | 773.17 | 3281.00 | -773.17 | 3281.00 |
| 21 | USB3_TDP | 974.72 | 3481.00 | -974.72 | 3481.00 |
| 22 | USB3_TDN | 974.72 | 3281.00 | -974.72 | 3281.00 |
| 23 | USB3_TGND | 982.37 | 3681.00 | -982.37 | 3681.00 |
| 24 | USB3_RDP | 1176.88 | 3281.00 | -1176.88 | 3281.00 |
| 25 | USB3_RDN | 1176.88 | 3481.00 | -1176.88 | 3481.00 |
| 26 | USB3_RGND | 1186.67 | 3681.00 | -1186.67 | 3681.00 |
| 27 | USB3_PVDD1P2 | 526.91 | 3062.57 | -526.91 | 3062.57 |
| 28 | USB3_DVDD1P2 | 1177.22 | 2860.07 | -1177.22 | 2860.07 |
| 29 | USB3_DVDD1P2 | 768.62 | 2860.07 | -768.62 | 2860.07 |
| 30 | USB2_AVSS | 1601.79 | 3595.19 | -1601.79 | 3595.19 |
| 31 | USB2_MONCDR | 1601.79 | 2792.39 | -1601.79 | 2792.39 |
| 32 | USB2_RREF | 1401.09 | 3394.49 | -1401.09 | 3394.49 |
| 33 | USB2_DP | 1601.79 | 3394.49 | -1601.79 | 3394.49 |
| 34 | USB2_AVDD3P3 | 1601.79 | 2993.09 | -1601.79 | 2993.09 |
| 35 | USB2_DM | 1601.79 | 3193.79 | -1601.79 | 3193.79 |
| 36 | USB2_AVDD1P2 | 1401.09 | 2792.39 | -1401.09 | 2792.39 |
| 37 | USB2_AVSSBG | 1401.09 | 3595.19 | -1401.09 | 3595.19 |
| 38 | USB2_MONPLL | 1401.09 | 2993.09 | -1401.09 | 2993.09 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|----------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 39 | USB2_DVSS | 1401.09 | 3193.79 | -1401.09 | 3193.79 |
| 40 | BT_PAVSS | 2217.95 | -736.50 | -2217.95 | -736.50 |
| 41 | BT_AGPIO | 2017.95 | -1298.03 | -2017.95 | -1298.03 |
| 42 | BT_IFVDD1P2 | 1768.91 | -1298.03 | -1768.91 | -1298.03 |
| 43 | BT_IFVSS | 1568.92 | -1298.03 | -1568.92 | -1298.03 |
| 44 | BT_LNAVDD1P2 | 2228.18 | -392.72 | -2228.18 | -392.72 |
| 45 | BT_LNAVSS | 1843.60 | -524.82 | -1843.60 | -524.82 |
| 46 | BT_PAVDD2P5 | 2176.03 | -1164.53 | -2176.03 | -1164.53 |
| 47 | BT_PLLVDD1P2 | 1768.91 | -223.55 | -1768.91 | -223.55 |
| 48 | BT_PLLVSS | 1568.92 | -223.55 | -1568.92 | -223.55 |
| 49 | BT_RF | 2252.39 | -936.50 | -2252.39 | -936.50 |
| 50 | BT_VCOVDD1P2 | 2227.01 | -189.65 | -2227.01 | -189.65 |
| 51 | BT_VCOVSS | 1967.62 | -45.40 | -1967.62 | -45.40 |
| 52 | FM_AUDIOVDD1P2 | 2044.00 | 931.81 | -2044.00 | 931.81 |
| 53 | FM_AUDIOAVSS | 2044.00 | 1143.58 | -2044.00 | 1143.58 |
| 54 | FM_AOUT1 | 2244.00 | 1143.58 | -2244.00 | 1143.58 |
| 55 | FM_AOUT2 | 2244.00 | 931.81 | -2244.00 | 931.81 |
| 56 | FM_IFVDD1P2 | 1614.95 | 371.79 | -1614.95 | 371.79 |
| 57 | FM_IFVSS | 1614.95 | 171.80 | -1614.95 | 171.80 |
| 58 | FM_PLLVSS | 1793.21 | 871.61 | -1793.21 | 871.61 |
| 59 | FM_PLLVDD1P2 | 1686.40 | 695.87 | -1686.40 | 695.87 |
| 60 | FM_RFAUX | 2273.40 | 68.08 | -2273.40 | 68.08 |
| 61 | FM_RFIN | 2260.02 | 313.69 | -2260.02 | 313.69 |
| 62 | FM_LNAVDD1P2 | 2060.02 | 354.59 | -2060.02 | 354.59 |
| 63 | FM_LNAVSS | 2060.02 | 154.59 | -2060.02 | 154.59 |
| 64 | FM_VCOVDD1P2 | 2273.40 | 731.81 | -2273.40 | 731.81 |
| 65 | FM_VCOVSS | 2273.40 | 531.81 | -2273.40 | 531.81 |
| 66 | RF_SW_CTRL_0 | -2202.33 | -1494.00 | 2202.33 | -1494.00 |
| 67 | VDDC | -661.10 | -1355.99 | 661.10 | -1355.99 |
| 68 | VSSC | 740.99 | 2052.00 | -740.99 | 2052.00 |
| 69 | VSSC | -616.50 | -408.01 | 616.50 | -408.01 |
| 70 | VSSC | -459.00 | -198.00 | 459.00 | -198.00 |
| 71 | VSSC | -546.71 | -1008.00 | 546.71 | -1008.00 |
| 72 | VSSC | -546.71 | -708.00 | 546.71 | -708.00 |
| 73 | VSSC | -459.00 | 252.00 | 459.00 | 252.00 |
| 74 | VDDC | -661.10 | -21.01 | 661.10 | -21.01 |
| 75 | VSSC | 740.99 | 2352.00 | -740.99 | 2352.00 |
| 76 | VDDIO_SD | -405.00 | 2299.50 | 405.00 | 2299.50 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|--------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 77 | SDIO_DATA_1 | -337.05 | 2531.57 | 337.05 | 2531.57 |
| 78 | SDIO_CLK | -337.05 | 2731.57 | 337.05 | 2731.57 |
| 79 | SDIO_DATA_3 | -337.05 | 2931.58 | 337.05 | 2931.58 |
| 80 | SDIO_DATA_2 | -337.05 | 3131.59 | 337.05 | 3131.59 |
| 81 | SDIO_CMD | -337.05 | 3331.59 | 337.05 | 3331.59 |
| 82 | SDIO_DATA_0 | -337.05 | 3531.60 | 337.05 | 3531.60 |
| 83 | VSSC | -316.50 | -408.01 | 316.50 | -408.01 |
| 84 | VSSC | -266.51 | -1008.00 | 266.51 | -1008.00 |
| 85 | VSSC | -266.51 | -708.00 | 266.51 | -708.00 |
| 86 | RF_SW_CTRL_4 | -2072.12 | -1125.00 | 2072.12 | -1125.00 |
| 87 | VDDC | -261.11 | -21.01 | 261.11 | -21.01 |
| 88 | VSSC | -259.00 | 1651.99 | 259.00 | 1651.99 |
| 89 | VSSC | -159.00 | 252.00 | 159.00 | 252.00 |
| 90 | VSSC | -159.00 | 552.00 | 159.00 | 552.00 |
| 91 | VSSC | -159.00 | 851.99 | 159.00 | 851.99 |
| 92 | VSSC | -159.00 | 1151.99 | 159.00 | 1151.99 |
| 93 | VSSC | -159.00 | 1451.99 | 159.00 | 1451.99 |
| 94 | VSSC | -159.00 | 2052.00 | 159.00 | 2052.00 |
| 95 | VSSC | -459.00 | 552.00 | 459.00 | 552.00 |
| 96 | DGNDHSIC | -67.05 | 2286.36 | 67.05 | 2286.36 |
| 97 | AGND12PLL | -67.05 | 2486.57 | 67.05 | 2486.57 |
| 98 | AVDD12PLL | -67.05 | 2686.57 | 67.05 | 2686.57 |
| 99 | RREFHSIC | -67.05 | 2886.58 | 67.05 | 2886.58 |
| 100 | STROBE | -67.05 | 3086.59 | 67.05 | 3086.59 |
| 101 | DATA | -67.05 | 3286.59 | 67.05 | 3286.59 |
| 102 | DVDD12HSIC | -67.05 | 3486.60 | 67.05 | 3486.60 |
| 103 | VDDC | -61.11 | -1220.99 | 61.11 | -1220.99 |
| 104 | VSSC | -61.11 | -1008.00 | 61.11 | -1008.00 |
| 105 | VSSC | -61.11 | -708.00 | 61.11 | -708.00 |
| 106 | VSSC | -61.11 | -408.01 | 61.11 | -408.01 |
| 107 | VDDC | -61.11 | -21.01 | 61.11 | -21.01 |
| 108 | VDDC | -61.11 | 1843.97 | 61.11 | 1843.97 |
| 109 | VDDC | 138.89 | -1220.99 | -138.89 | -1220.99 |
| 110 | VDDC | 138.89 | -1021.00 | -138.89 | -1021.00 |
| 111 | VDDC | 138.89 | -821.00 | -138.89 | -821.00 |
| 112 | VDDC | -261.11 | -1220.99 | 261.11 | -1220.99 |
| 113 | VDDC | 138.89 | -421.00 | -138.89 | -421.00 |
| 114 | VDDC | 138.89 | -221.00 | -138.89 | -221.00 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|-----------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 115 | VDDC | 138.89 | -21.01 | -138.89 | -21.01 |
| 116 | VSSC | 140.99 | 252.00 | -140.99 | 252.00 |
| 117 | VSSC | 140.99 | 552.00 | -140.99 | 552.00 |
| 118 | VSSC | 140.99 | 851.99 | -140.99 | 851.99 |
| 119 | VSSC | 140.99 | 1151.99 | -140.99 | 1151.99 |
| 120 | VSSC | 140.99 | 1451.99 | -140.99 | 1451.99 |
| 121 | VSSC | 140.99 | 1651.99 | -140.99 | 1651.99 |
| 122 | VSSC | 140.99 | 2052.00 | -140.99 | 2052.00 |
| 123 | PACKAGEOPTION_4 | 140.99 | 2352.00 | -140.99 | 2352.00 |
| 124 | BT_VSSC | 768.37 | -1186.86 | -768.37 | -1186.86 |
| 125 | BT_VSSC | 816.40 | 21.84 | -816.40 | 21.84 |
| 126 | BT_VSSC | 599.69 | -715.49 | -599.69 | -715.49 |
| 127 | VDDC | 338.89 | 443.99 | -338.89 | 443.99 |
| 128 | VDDC | 338.89 | 643.99 | -338.89 | 643.99 |
| 129 | VDDC | 338.89 | 1843.97 | -338.89 | 1843.97 |
| 130 | VSSC | -459.00 | 851.99 | 459.00 | 851.99 |
| 131 | PACKAGEOPTION_2 | 440.99 | 2352.00 | -440.99 | 2352.00 |
| 132 | PACKAGEOPTION_3 | 440.99 | 2592.00 | -440.99 | 2592.00 |
| 133 | BT_VSSC | 468.37 | -1186.86 | -468.37 | -1186.86 |
| 134 | VDDC | 538.88 | 643.99 | -538.88 | 643.99 |
| 135 | VDDC | 538.88 | 843.98 | -538.88 | 843.98 |
| 136 | VDDC | 538.88 | 1043.98 | -538.88 | 1043.98 |
| 137 | VDDC | 538.88 | 1243.98 | -538.88 | 1243.98 |
| 138 | VDDC | 538.88 | 1443.98 | -538.88 | 1443.98 |
| 139 | VDDC | 538.88 | 1643.98 | -538.88 | 1643.98 |
| 140 | VDDC | 538.88 | 1843.97 | -538.88 | 1843.97 |
| 141 | BT_VDDC_ISO_1 | 601.19 | -970.04 | -601.19 | -970.04 |
| 142 | BT_VDDC_ISO_2 | 620.91 | -500.07 | -620.91 | -500.07 |
| 143 | AVDD_BBPLL | 655.50 | 168.14 | -655.50 | 168.14 |
| 144 | AVSS_BBPLL | 655.50 | 437.48 | -655.50 | 437.48 |
| 145 | BT_VDDC | 1480.37 | 555.67 | -1480.37 | 555.67 |
| 146 | PACKAGEOPTION_1 | 740.99 | 2592.00 | -740.99 | 2592.00 |
| 147 | BT_VDDC | 1480.37 | 780.66 | -1480.37 | 780.66 |
| 148 | BT_VDDIO | 830.29 | -445.06 | -830.29 | -445.06 |
| 149 | BT_VDDIO | 840.29 | -724.53 | -840.29 | -724.53 |
| 150 | BT_VDDIO | 865.28 | -245.06 | -865.28 | -245.06 |
| 151 | BT_VDDIO | 915.28 | -973.39 | -915.28 | -973.39 |
| 152 | PACKAGEOPTION_0 | 1040.99 | 2592.00 | -1040.99 | 2592.00 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|---------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 153 | BT_GPIO_5 | 1048.37 | 420.67 | -1048.37 | 420.67 |
| 154 | BT_GPIO_3 | 1048.37 | 620.67 | -1048.37 | 620.67 |
| 155 | BT_GPIO_2 | 1048.37 | 820.67 | -1048.37 | 820.67 |
| 156 | BT_I2S_DI | 1444.06 | 1426.01 | -1444.06 | 1426.01 |
| 157 | BT_UART_TXD | 1444.06 | 1643.00 | -1444.06 | 1643.00 |
| 158 | BT_I2S_WS | 1143.51 | 1940.00 | -1143.51 | 1940.00 |
| 159 | LPO_IN | 1143.51 | 2237.00 | -1143.51 | 2237.00 |
| 160 | OTP_VDD33 | 1348.51 | 2444.00 | -1348.51 | 2444.00 |
| 161 | BT_CLK_REQ | 1644.06 | 1426.01 | -1644.06 | 1426.01 |
| 162 | BT_UART_RXD | 1644.06 | 1643.00 | -1644.06 | 1643.00 |
| 163 | BT_PCM_SYNC | 1343.51 | 1940.00 | -1343.51 | 1940.00 |
| 164 | BT_USB_DN | 1343.51 | 2237.00 | -1343.51 | 2237.00 |
| 165 | PCIE_PME_L | 1548.50 | 2444.00 | -1548.50 | 2444.00 |
| 166 | BT_TM1 | 1844.06 | 1346.00 | -1844.06 | 1346.00 |
| 167 | BT_I2S_CLK | 1844.06 | 1643.00 | -1844.06 | 1643.00 |
| 168 | BT_GPIO_4 | 1543.51 | 1940.00 | -1543.51 | 1940.00 |
| 169 | BT_USB_DP | 1543.51 | 2237.00 | -1543.51 | 2237.00 |
| 170 | BT_HOST_WAKE | 2044.05 | 1346.00 | -2044.05 | 1346.00 |
| 171 | BT_I2S_DO | 2044.05 | 1643.00 | -2044.05 | 1643.00 |
| 172 | BT_UART_CTS_N | 1743.51 | 1940.00 | -1743.51 | 1940.00 |
| 173 | BT_PCM_IN | 1743.51 | 2237.00 | -1743.51 | 2237.00 |
| 174 | PCIE_CLKREQ_L | 1858.50 | 2534.00 | -1858.50 | 2534.00 |
| 175 | RF_SW_CTRL_1 | -2002.32 | -1494.00 | 2002.32 | -1494.00 |
| 176 | BT_DEV_WAKE | 2244.05 | 1346.00 | -2244.05 | 1346.00 |
| 177 | BT_PCM_OUT | 2244.05 | 1643.00 | -2244.05 | 1643.00 |
| 178 | BT_UART_RTS_N | 1943.51 | 1940.00 | -1943.51 | 1940.00 |
| 179 | BT_PCM_CLK | 1943.51 | 2237.00 | -1943.51 | 2237.00 |
| 180 | PERST_L | 2058.50 | 2534.00 | -2058.50 | 2534.00 |
| 181 | RF_SW_CTRL_8 | -1945.91 | -806.00 | 1945.91 | -806.00 |
| 182 | GPIO_13 | -2040.71 | 516.01 | 2040.71 | 516.01 |
| 183 | RF_SW_CTRL_5 | -1872.11 | -1125.00 | 1872.11 | -1125.00 |
| 184 | RF_SW_CTRL_12 | -1760.12 | -327.01 | 1760.12 | -327.01 |
| 185 | GPIO_10 | -1959.30 | 229.01 | 1959.30 | 229.01 |
| 186 | RF_SW_CTRL_2 | -1802.31 | -1494.00 | 1802.31 | -1494.00 |
| 187 | RF_SW_CTRL_9 | -1745.90 | -806.00 | 1745.90 | -806.00 |
| 188 | GPIO_14 | -1840.71 | 516.01 | 1840.71 | 516.01 |
| 189 | GPIO_7 | -1853.50 | -18.00 | 1853.50 | -18.00 |
| 190 | RF_SW_CTRL_6 | -1672.10 | -1125.00 | 1672.10 | -1125.00 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|---------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 191 | RF_SW_CTRL_13 | -1560.11 | -327.01 | 1560.11 | -327.01 |
| 192 | GPIO_11 | -1759.91 | 279.00 | 1759.91 | 279.00 |
| 193 | RF_SW_CTRL_3 | -1602.31 | -1494.00 | 1602.31 | -1494.00 |
| 194 | RF_SW_CTRL_10 | -1545.89 | -806.00 | 1545.89 | -806.00 |
| 195 | GPIO_15 | -1640.70 | 516.01 | 1640.70 | 516.01 |
| 196 | GPIO_8 | -1593.91 | 22.00 | 1593.91 | 22.00 |
| 197 | RF_SW_CTRL_7 | -1472.09 | -1125.00 | 1472.09 | -1125.00 |
| 198 | RF_SW_CTRL_14 | -1360.11 | -327.01 | 1360.11 | -327.01 |
| 199 | GPIO_12 | -1559.91 | 279.00 | 1559.91 | 279.00 |
| 200 | VSSC | -459.00 | 1151.99 | 459.00 | 1151.99 |
| 201 | VSSC | -459.00 | 1451.99 | 459.00 | 1451.99 |
| 202 | RF_SW_CTRL_11 | -1346.09 | -756.00 | 1346.09 | -756.00 |
| 203 | VDDC | -459.00 | 1651.99 | 459.00 | 1651.99 |
| 204 | VDDC | -1345.37 | 1017.54 | 1345.37 | 1017.54 |
| 205 | GPIO_9 | -1393.90 | 22.00 | 1393.90 | 22.00 |
| 206 | VDDIO | -1215.90 | 576.00 | 1215.90 | 576.00 |
| 207 | RF_SW_CTRL_15 | -1160.10 | -327.01 | 1160.10 | -327.01 |
| 208 | VDDC | -1261.10 | 1843.97 | 1261.10 | 1843.97 |
| 209 | VDDC | -1061.11 | -1156.00 | 1061.11 | -1156.00 |
| 210 | VDDC | -1061.11 | -776.00 | 1061.11 | -776.00 |
| 211 | VDDC | -1061.10 | -1355.99 | 1061.10 | -1355.99 |
| 212 | VDDC_ISO_PHY | -1402.10 | -1494.00 | 1402.10 | -1494.00 |
| 213 | VDDC | -1180.10 | -587.00 | 1180.10 | -587.00 |
| 214 | VDDC_ISO_PHY | -1151.11 | -956.00 | 1151.11 | -956.00 |
| 215 | VDDC_ISO_DIG | -1058.99 | 2052.00 | 1058.99 | 2052.00 |
| 216 | VDDC_ISO_DIG | -816.10 | 1843.97 | 816.10 | 1843.97 |
| 217 | VSSC | -459.00 | 2052.00 | 459.00 | 2052.00 |
| 218 | GPIO_0 | -996.05 | 2877.58 | 996.05 | 2877.58 |
| 219 | GPIO_1 | -996.05 | 3077.59 | 996.05 | 3077.59 |
| 220 | GPIO_2 | -996.05 | 3277.59 | 996.05 | 3277.59 |
| 221 | GPIO_3 | -996.05 | 3477.60 | 996.05 | 3477.60 |
| 222 | VDDIO | -990.90 | 576.00 | 990.90 | 576.00 |
| 223 | VDDIO_RF | -960.10 | -117.00 | 960.10 | -117.00 |
| 224 | VDDC | -1061.10 | 1843.97 | 1061.10 | 1843.97 |
| 225 | VDDC_ISO_PHY | -1061.10 | 843.98 | 1061.10 | 843.98 |
| 226 | VDDC_ISO_PHY | -1058.99 | 1151.99 | 1058.99 | 1151.99 |
| 227 | VDDIO_RF | -852.10 | -387.00 | 852.10 | -387.00 |
| 228 | VDDC | -461.11 | -1355.99 | 461.11 | -1355.99 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|-----------------------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 229 | GPIO_4 | -769.05 | 3196.59 | 769.05 | 3196.59 |
| 230 | VDDIO_PCIE ^a | -759.00 | 252.00 | 759.00 | 252.00 |
| 231 | VDDIO | -759.00 | 552.00 | 759.00 | 552.00 |
| 232 | VSSC | -1359.90 | 279.00 | 1359.90 | 279.00 |
| 233 | VSSC | -1319.39 | 2052.00 | 1319.39 | 2052.00 |
| 234 | VSSC | -1358.99 | 2302.00 | 1358.99 | 2302.00 |
| 235 | VSSC | -1351.11 | -956.00 | 1351.11 | -956.00 |
| 236 | GPIO_6 | -751.05 | 2996.59 | 751.05 | 2996.59 |
| 237 | GPIO_5 | -751.05 | 3396.60 | 751.05 | 3396.60 |
| 238 | VDDIO_SD | -745.50 | 2352.00 | 745.50 | 2352.00 |
| 239 | JTAG_SEL | -733.05 | 2796.58 | 733.05 | 2796.58 |
| 240 | VDDC_ISO_PHY | -729.00 | -220.50 | 729.00 | -220.50 |
| 241 | VDDC | -951.31 | -956.00 | 951.31 | -956.00 |
| 242 | VDDC | -861.10 | -1355.99 | 861.10 | -1355.99 |
| 243 | VSSC | -1440.90 | 576.00 | 1440.90 | 576.00 |
| 244 | VSSC | -1159.90 | -98.00 | 1159.90 | -98.00 |
| 245 | VSSC | -1159.90 | 279.00 | 1159.90 | 279.00 |
| 246 | VDDC | -616.10 | 1843.97 | 616.10 | 1843.97 |
| 247 | WRF_SYNTH_VBAT_VDD3P3 | 75.91 | -3598.00 | -75.91 | -3598.00 |
| 248 | WRF_XTAL_GND1P2 | -2003.12 | -1834.98 | 2003.12 | -1834.98 |
| 249 | WRF_XTAL_VDD1P5 | -2003.12 | -2065.65 | 2003.12 | -2065.65 |
| 250 | WRF_VCO_GND1P2 | 198.52 | -3109.71 | -198.52 | -3109.71 |
| 251 | WRF_XTAL_IN | -2205.82 | -2065.65 | 2205.82 | -2065.65 |
| 252 | WRF_LOGEN_GND1P2 | 126.11 | -2303.63 | -126.11 | -2303.63 |
| 253 | WRF_XTAL_OUT | -2205.82 | -1818.42 | 2205.82 | -1818.42 |
| 254 | WRF_XTAL_VDD1P2 | -1807.98 | -1960.54 | 1807.98 | -1960.54 |
| 255 | WRF_TX_GND1P2_core1 | -437.83 | -2417.93 | 437.83 | -2417.93 |
| 256 | WRF_BUCK_GND1P5_core1 | -2137.36 | -2823.85 | 2137.36 | -2823.85 |
| 257 | WRF_RX5G_GND1P2_core1 | -1968.14 | -2944.01 | 1968.14 | -2944.01 |
| 258 | WRF_GPIO_OUT_core1 | -877.08 | -2398.01 | 877.08 | -2398.01 |
| 259 | WRF_RX2G_GND1P2_core1 | -167.27 | -2716.52 | 167.27 | -2716.52 |
| 260 | WRF_RFIN_5G_core1 | -2253.44 | -3538.14 | 2253.44 | -3538.14 |
| 261 | WRF_RFIN_2G_core1 | -201.47 | -3598.00 | 201.47 | -3598.00 |
| 262 | WRF_PFD_VDD1P2 | 901.40 | -2994.96 | -901.40 | -2994.96 |
| 263 | WRF_PFD_GND1P2 | 818.12 | -3198.01 | -818.12 | -3198.01 |
| 264 | WRF_PADRV_VBAT_VDD3P3_core1 | -1090.70 | -2792.61 | 1090.70 | -2792.61 |
| 265 | WRF_PADRV_VBAT_GND3P3_core1 | -1401.46 | -2798.01 | 1401.46 | -2798.01 |
| 266 | WRF_PA5G_VBAT_VDD3P3_core1 | -1401.46 | -3679.00 | 1401.46 | -3679.00 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|-----------------------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 267 | WRF_AFE_GND1P2_core1 | -631.56 | -2293.35 | 631.56 | -2293.35 |
| 268 | WRF_PA5G_VBAT_GND3P3_core0 | 1825.51 | -2798.01 | -1825.51 | -2798.01 |
| 269 | WRF_PA5G_VBAT_VDD3P3_core0 | 2297.50 | -2998.01 | -2297.50 | -2998.01 |
| 270 | WRF_MMD_VDD1P2 | 692.41 | -2994.96 | -692.41 | -2994.96 |
| 271 | WRF_MMD_GND1P2 | 499.12 | -2798.01 | -499.12 | -2798.01 |
| 272 | WRF_PA2G_VBAT_GND3P3_core0 | 1744.51 | -1940.22 | -1744.51 | -1940.22 |
| 273 | WRF_LNA_5G_GND1P2_core0 | 1877.39 | -3673.49 | -1877.39 | -3673.49 |
| 274 | WRF_CP_GND1P2 | 539.26 | -3598.00 | -539.26 | -3598.00 |
| 275 | WRF_LNA_2G_GND1P2_core0 | 1798.51 | -1598.02 | -1798.51 | -1598.02 |
| 276 | WRF_TSSI_A_core1 | -1839.15 | -2716.77 | 1839.15 | -2716.77 |
| 277 | WRF_BUCK_VDD1P5_core0 | 1024.35 | -3433.91 | -1024.35 | -3433.91 |
| 278 | WRF_LOGENG_GND1P2 | 770.31 | -2353.01 | -770.31 | -2353.01 |
| 279 | WRF_RFOUT_2G_core1 | -601.47 | -3679.00 | 601.47 | -3679.00 |
| 280 | WRF_RFOUT_5G_core0 | 2288.50 | -3198.01 | -2288.50 | -3198.01 |
| 281 | WRF_AFE_GND1P2_core0 | 880.13 | -2028.11 | -880.13 | -2028.11 |
| 282 | WRF_LNA_2G_GND1P2_core1 | -201.47 | -3198.01 | 201.47 | -3198.01 |
| 283 | WRF_LNA_5G_GND1P2_core1 | -2276.94 | -3276.89 | 2276.94 | -3276.89 |
| 284 | WRF_PA2G_VBAT_GND3P3_core1 | -543.68 | -3144.01 | 543.68 | -3144.01 |
| 285 | WRF_PA2G_VBAT_VDD3P3_core1 | -801.47 | -3697.00 | 801.47 | -3697.00 |
| 286 | WRF_PA5G_VBAT_GND3P3_core1 | -1801.46 | -3225.01 | 1801.46 | -3225.01 |
| 287 | WRF_PA5G_VBAT_VDD3P3_core0 | 2279.50 | -2798.01 | -2279.50 | -2798.01 |
| 288 | WRF_PADRV_VBAT_GND3P3_core0 | 1398.51 | -2798.01 | -1398.51 | -2798.01 |
| 289 | WRF_PADRV_VBAT_VDD3P3_core0 | 1393.11 | -2487.25 | -1393.11 | -2487.25 |
| 290 | WRF_RFIN_2G_core0 | 2198.50 | -1598.02 | -2198.50 | -1598.02 |
| 291 | WRF_RX2G_GND1P2_core0 | 1317.02 | -1563.82 | -1317.02 | -1563.82 |
| 292 | WRF_RX5G_GND1P2_core0 | 1544.51 | -3364.69 | -1544.51 | -3364.69 |
| 293 | WRF_TX_GND1P2_core0 | 1018.43 | -1834.38 | -1018.43 | -1834.38 |
| 294 | WRF_TSSI_A_core0 | 1317.27 | -3235.69 | -1317.27 | -3235.69 |
| 295 | WRF_BUCK_GND1P5_core0 | 1424.35 | -3533.90 | -1424.35 | -3533.90 |
| 296 | WRF_BUCK_VDD1P5_core1 | -2237.36 | -2423.85 | 2237.36 | -2423.85 |
| 297 | WRF_GPIO_OUT_core0 | 998.51 | -2273.63 | -998.51 | -2273.63 |
| 298 | WRF_RFOUT_2G_core0 | 2279.50 | -1998.02 | -2279.50 | -1998.02 |
| 299 | WRF_RFOUT_5G_core1 | -1801.46 | -3688.00 | 1801.46 | -3688.00 |
| 300 | WRF_PA2G_VBAT_GND3P3_core0 | 1714.63 | -2523.25 | -1714.63 | -2523.25 |
| 301 | WRF_PA2G_VBAT_GND3P3_core1 | -1126.70 | -3114.13 | 1126.70 | -3114.13 |
| 302 | WRF_RFIN_5G_core0 | 2138.64 | -3649.99 | -2138.64 | -3649.99 |
| 303 | WRF_PA5G_VBAT_GND3P3_core0 | 1825.51 | -3198.01 | -1825.51 | -3198.01 |
| 304 | WRF_PA5G_VBAT_GND3P3_core1 | -1401.46 | -3225.01 | 1401.46 | -3225.01 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|----------------------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 305 | WRF_PA2G_VBAT_VDD3P3_core0 | 2279.50 | -2398.01 | -2279.50 | -2398.01 |
| 306 | WRF_PA2G_VBAT_VDD3P3_core0 | 2297.50 | -2198.02 | -2297.50 | -2198.02 |
| 307 | WRF_RX2G_GND1P2_core0 | 1488.79 | -1700.51 | -1488.79 | -1700.51 |
| 308 | WRF_BUCK_VDD1P5_core0 | 1024.35 | -3633.90 | -1024.35 | -3633.90 |
| 309 | WRF_BUCK_VDD1P5_core0 | 1224.35 | -3633.90 | -1224.35 | -3633.90 |
| 310 | WRF_BUCK_VDD1P5_core0 | 1224.35 | -3433.91 | -1224.35 | -3433.91 |
| 311 | WRF_BUCK_VDD1P5_core1 | -2037.36 | -2423.85 | 2037.36 | -2423.85 |
| 312 | WRF_BUCK_VDD1P5_core1 | -2037.36 | -2623.85 | 2037.36 | -2623.85 |
| 313 | WRF_BUCK_VDD1P5_core1 | -2237.36 | -2623.85 | 2237.36 | -2623.85 |
| 314 | WRF_PA5G_VBAT_VDD3P3_core1 | -1601.46 | -3697.00 | 1601.46 | -3697.00 |
| 315 | WRF_PA2G_VBAT_VDD3P3_core1 | -1001.47 | -3679.00 | 1001.47 | -3679.00 |
| 316 | WRF_LOGEN_GND1P2 | 326.11 | -2303.63 | -326.11 | -2303.63 |
| 317 | WRF_RX2G_GND1P2_core1 | -303.96 | -2888.29 | 303.96 | -2888.29 |
| 318 | WRF_CP_GND1P2 | 339.26 | -3598.00 | -339.26 | -3598.00 |
| 319 | WL_REG_ON | -1710.77 | 3277.01 | 1710.77 | 3277.01 |
| 320 | BT_REG_ON | -1569.35 | 1721.37 | 1569.35 | 1721.37 |
| 321 | LDO_VDDBAT5V | -1852.20 | 1721.37 | 1852.20 | 1721.37 |
| 322 | LDO_VDDBAT5V | -1852.20 | 1438.53 | 1852.20 | 1438.53 |
| 323 | LDO_VDDBAT5V | -1852.20 | 1155.69 | 1852.20 | 1155.69 |
| 324 | VOUT_3P3 | -1993.62 | 1297.11 | 1993.62 | 1297.11 |
| 325 | VOUT_3P3 | -2135.04 | 1155.69 | 2135.04 | 1155.69 |
| 326 | VDDIO_PMU | -1710.77 | 1297.11 | 1710.77 | 1297.11 |
| 327 | LDO_VDDBAT5V | -1852.20 | 872.84 | 1852.20 | 872.84 |
| 328 | LDO_VDDBAT5V | -2135.04 | 872.84 | 2135.04 | 872.84 |
| 329 | LDO_VDDBAT5V | -2276.46 | 1014.26 | 2276.46 | 1014.26 |
| 330 | VOUT_3P3_SENSE | -2276.46 | 1297.11 | 2276.46 | 1297.11 |
| 331 | LDO_VDDBAT5V | -1710.77 | 1862.79 | 1710.77 | 1862.79 |
| 332 | VOUT_3P3 | -1993.62 | 1579.95 | 1993.62 | 1579.95 |
| 333 | VSSC | -1569.35 | 1155.69 | 1569.35 | 1155.69 |
| 334 | VSSC | -1569.35 | 1438.53 | 1569.35 | 1438.53 |
| 335 | PMU_AVSS | -1569.35 | 2287.06 | 1569.35 | 2287.06 |
| 336 | SR_VLX | -1569.35 | 2852.74 | 1569.35 | 2852.74 |
| 337 | SR_VLX | -1569.35 | 3135.59 | 1569.35 | 3135.59 |
| 338 | SR_PVSS | -1852.20 | 3135.59 | 1852.20 | 3135.59 |
| 339 | SR_VLX | -1852.20 | 2852.74 | 1852.20 | 2852.74 |
| 340 | SR_VDDBATA5V | -1852.20 | 2569.90 | 1852.20 | 2569.90 |
| 341 | VOUT_CLDO | -1852.20 | 2287.06 | 1852.20 | 2287.06 |
| 342 | LDO_VDD1P5 | -1852.20 | 2004.21 | 1852.20 | 2004.21 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|---------------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 343 | LDO_VDDBAT5V | -1993.62 | 1014.26 | 1993.62 | 1014.26 |
| 344 | VOUT_3P3 | -2135.04 | 1438.53 | 2135.04 | 1438.53 |
| 345 | LDO_VDDBAT5V | -2135.04 | 1721.37 | 2135.04 | 1721.37 |
| 346 | VOUT_LDO3P3_B | -2135.04 | 2004.21 | 2135.04 | 2004.21 |
| 347 | LDO_VDD1P5 | -2135.04 | 2287.06 | 2135.04 | 2287.06 |
| 348 | SR_VDDBATP5V | -2135.04 | 2569.90 | 2135.04 | 2569.90 |
| 349 | SR_PVSS | -2135.04 | 3135.59 | 2135.04 | 3135.59 |
| 350 | VDDIO_PMU | -1710.77 | 1579.95 | 1710.77 | 1579.95 |
| 351 | VOUT_LNLDO | -1710.77 | 2145.64 | 1710.77 | 2145.64 |
| 352 | VOUT_CLDO | -1710.77 | 2428.48 | 1710.77 | 2428.48 |
| 353 | SR_VLX | -1710.77 | 2711.32 | 1710.77 | 2711.32 |
| 354 | SR_VLX | -1710.77 | 2994.17 | 1710.77 | 2994.17 |
| 355 | VOUT_LDO3P3_B | -1993.62 | 1862.79 | 1993.62 | 1862.79 |
| 356 | LDO_VDD1P5 | -1993.62 | 2145.64 | 1993.62 | 2145.64 |
| 357 | VOUT_CLDO | -1993.62 | 2428.48 | 1993.62 | 2428.48 |
| 358 | SR_VDDBATP5V | -1993.62 | 2711.32 | 1993.62 | 2711.32 |
| 359 | SR_VLX | -1993.62 | 2994.17 | 1993.62 | 2994.17 |
| 360 | SR_PVSS | -1993.62 | 3277.01 | 1993.62 | 3277.01 |
| 361 | VOUT_3P3 | -2276.46 | 1862.79 | 2276.46 | 1862.79 |
| 362 | VOUT_BTLD02P5 | -2276.46 | 2145.64 | 2276.46 | 2145.64 |
| 363 | LDO_VDD1P5 | -2276.46 | 2428.48 | 2276.46 | 2428.48 |
| 364 | SR_PVSS | -2276.46 | 3277.01 | 2276.46 | 3277.01 |
| 365 | VOUT_3P3 | -2276.46 | 1579.95 | 2276.46 | 1579.95 |
| 366 | SR_VDDBATP5V | -2276.46 | 2711.32 | 2276.46 | 2711.32 |
| 367 | PCIE_TESTP | 1800.31 | 3068.53 | -1800.31 | 3068.53 |
| 368 | PCIE_TESTN | 1966.81 | 2956.03 | -1966.81 | 2956.03 |
| 369 | BT_VDDC | 1480.37 | 1005.66 | -1480.37 | 1005.66 |
| 370 | BT_VDDC | 1480.37 | 1225.66 | -1480.37 | 1225.66 |
| 371 | BT_VDDC | 1408.19 | 248.05 | -1408.19 | 248.05 |
| 372 | BT_VDDC | 1322.34 | 55.02 | -1322.34 | 55.02 |
| 373 | BT_VDDC | 1060.28 | -1186.86 | -1060.28 | -1186.86 |
| 374 | BT_VDDC | 666.40 | -198.15 | -666.40 | -198.15 |
| 375 | BT_VDDC | 617.61 | -1324.61 | -617.61 | -1324.61 |
| 376 | BT_VSSC | 338.89 | -475.07 | -338.89 | -475.07 |
| 377 | BT_VSSC | 1040.28 | -724.53 | -1040.28 | -724.53 |
| 378 | BT_VSSC | 1063.38 | 1020.66 | -1063.38 | 1020.66 |
| 379 | BT_VSSC | 1063.38 | 1320.66 | -1063.38 | 1320.66 |
| 380 | BT_VSSC | 1273.37 | 505.67 | -1273.37 | 505.67 |

Table 21. 395-Bump WLCSP Coordinates (Cont.)

| No. | Net Name | Coordinates (0,0 center of die) | | | |
|-----|----------|---------------------------------|----------|----------|----------|
| | | Bump Side | | Top Side | |
| | | X | Y | X | Y |
| 381 | BT_VSSC | 1273.37 | 705.66 | -1273.37 | 705.66 |
| 382 | BT_VSSC | 1273.37 | 1005.66 | -1273.37 | 1005.66 |
| 383 | BT_VSSC | 1273.37 | 1225.66 | -1273.37 | 1225.66 |
| 384 | VSSC | 440.99 | 2052.00 | -440.99 | 2052.00 |
| 385 | VSSC | -1293.24 | -1317.60 | 1293.24 | -1317.60 |
| 386 | VSSC | -1202.10 | -1504.00 | 1202.10 | -1504.00 |
| 387 | VSSC | -1058.99 | 1451.99 | 1058.99 | 1451.99 |
| 388 | VSSC | -1058.99 | 2302.00 | 1058.99 | 2302.00 |
| 389 | VSSC | -959.90 | 279.00 | 959.90 | 279.00 |
| 390 | VSSC | -759.00 | 851.99 | 759.00 | 851.99 |
| 391 | VSSC | -759.00 | 1151.99 | 759.00 | 1151.99 |
| 392 | VSSC | -759.00 | 1451.99 | 759.00 | 1451.99 |
| 393 | VSSC | -759.00 | 2052.00 | 759.00 | 2052.00 |
| 394 | VSSC | -746.31 | -956.00 | 746.31 | -956.00 |
| 395 | VSSC | -746.31 | -756.00 | 746.31 | -756.00 |

a. This net name was changed to VDDIO_PCIE to correct an error in the pin definition of bump 230. The correction applies to WLCSP package PCIe platform only, and is inconsequential for SDIO platforms.

13.3 Signal Descriptions

The signal name, type, and description of each pin in the CYW4354 is listed in [Table 22 \(WLCSP\)](#) and [Table 23 on page 89 \(WLBGA\)](#). The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 22. WLCSP Signal Descriptions

| Bump# | Signal Name | Type | Description |
|---|--------------------|------|--|
| WLAN and Bluetooth Receive RF Signal Interface | | | |
| 290 | WRF_RFIN_2G_CORE0 | I | 2.4 GHz Bluetooth and WLAN CORE0 receiver shared input |
| 261 | WRF_RFIN_2G_CORE1 | I | 2.4 GHz Bluetooth and WLAN CORE1 receiver shared input |
| 302 | WRF_RFIN_5G_CORE0 | I | 5 GHz WLAN CORE0 receiver input |
| 260 | WRF_RFIN_5G_CORE1 | I | 5 GHz WLAN CORE1 receiver input |
| 298 | WRF_RFOUT_2G_CORE0 | O | 2.4 GHz WLAN CORE0 PA output |
| 279 | WRF_RFOUT_2G_CORE1 | O | 2.4 GHz WLAN CORE1 PA output |
| 280 | WRF_RFOUT_5G_CORE0 | O | 5 GHz WLAN CORE0 PA output |
| 299 | WRF_RFOUT_5G_CORE1 | O | 5 GHz WLAN CORE1 PA output |
| 294 | WRF_TSSI_A_CORE0 | I | 5 GHz TSSI CORE0 input from an optional external power amplifier/power detector. |
| 276 | WRF_TSSI_A_CORE1 | I | 5 GHz TSSI CORE1 input from an optional external power amplifier/power detector. |
| 297 | WRF_GPIO_OUT_CORE0 | I/O | GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector |
| 258 | WRF_GPIO_OUT_CORE1 | I/O | GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector |
| RF Switch Control Lines | | | |
| 66 | RF_SW_CTRL_0 | O | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file. |
| 175 | RF_SW_CTRL_1 | O | |
| 186 | RF_SW_CTRL_2 | O | |
| 193 | RF_SW_CTRL_3 | O | |
| 86 | RF_SW_CTRL_4 | O | |
| 183 | RF_SW_CTRL_5 | O | |
| 190 | RF_SW_CTRL_6 | O | |
| 197 | RF_SW_CTRL_7 | O | |
| 181 | RF_SW_CTRL_8 | O | |
| 187 | RF_SW_CTRL_9 | O | |
| 194 | RF_SW_CTRL_10 | O | |
| 202 | RF_SW_CTRL_11 | O | |
| 184 | RF_SW_CTRL_12 | O | |
| 191 | RF_SW_CTRL_13 | O | |
| 198 | RF_SW_CTRL_14 | O | |
| 207 | RF_SW_CTRL_15 | O | |
| WLAN PCI Express Interface | | | |
| 174 | PCIE_CLKREQ_L | OD | PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|---|--------------|--------|--|
| 180 | PCIE_PERST_L | I (PU) | PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1. |
| 9 | PCIE_RDN0 | I | Receiver differential pair (×1 lane) |
| 8 | PCIE_RDP0 | I | |
| 4 | PCIE_REFCLKN | I | PCIe Differential Clock inputs (negative and positive). 100 MHz differential. |
| 3 | PCIE_REFCLKP | I | |
| 5 | PCIE_TDN0 | O | Transmitter differential pair (×1 lane) |
| 6 | PCIE_TDP0 | O | |
| 165 | PCIE_PME_L | OD | PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3. |
| 367 | PCIE_TESTP | – | PCIe test pin |
| 368 | PCIE_TESTN | – | |
| WLAN SDIO Bus Interface | | | |
| These signals can support alternate functionality depending on package and host interface mode. See Table 27 on page 97 | | | |
| 78 | SDIO_CLK | I | SDIO clock input |
| 81 | SDIO_CMD | I/O | SDIO command line |
| 82 | SDIO_DATA_0 | I/O | SDIO data line 0 |
| 77 | SDIO_DATA_1 | I/O | SDIO data line 1 |
| 80 | SDIO_DATA_2 | I/O | SDIO data line 2 |
| 79 | SDIO_DATA_3 | I/O | SDIO data line 3 |
| WLAN HSIC Interface | | | |
| 100 | HSIC_STROBE | I/O | HSIC Strobe |
| 101 | HSIC_DATA | I/O | HSIC Data |
| 99 | RREFHSIC | I | HSIC reference resistor input. If HSIC is used, connect this pin to ground via a 51-ohm 5% resistor. On SDIO designs this pin should not be connected. |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|---|--------------|------|---|
| WLAN GPIO Interface | | | |
| The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 24 on page 96 and Table 27 on page 97 for additional details. | | | |
| 218 | GPIO_0 | I/O | Programmable GPIO pins |
| 219 | GPIO_1 | I/O | |
| 220 | GPIO_2 | I/O | |
| 221 | GPIO_3 | I/O | |
| 229 | GPIO_4 | I/O | |
| 237 | GPIO_5 | I/O | |
| 236 | GPIO_6 | I/O | |
| 189 | GPIO_7 | I/O | |
| 196 | GPIO_8 | I/O | |
| 205 | GPIO_9 | I/O | |
| 185 | GPIO_10 | I/O | |
| 192 | GPIO_11 | I/O | |
| 199 | GPIO_12 | I/O | |
| 182 | GPIO_13 | I/O | |
| 188 | GPIO_14 | I/O | |
| 195 | GPIO_15 | I/O | |
| JTAG Interface | | | |
| 239 | JTAG_SEL | I/O | JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. Note: See Table 27 on page 97 for the JTAG signal pins. |
| Clocks | | | |
| 251 | WRF_XTAL_IN | I | XTAL oscillator input |
| 253 | WRF_XTAL_OUT | O | XTAL oscillator output |
| 159 | LPO_IN | I | External sleep clock input (32.768 kHz) |
| 161 | CLK_REQ | O | Reference clock request (shared by BT and WLAN). If not used, this can be no-connect. |
| Bluetooth/FM Transceiver | | | |
| 49 | BT_RF | O | Bluetooth PA output |
| – | BT_SF_CLK | I | SFLASH_CLK |
| – | BT_SF_CS_L | I/O | SFLASH_CSN |
| – | BT_SF_MISO | I/O | SFLASH master input, slave output |
| – | BT_SF_MOSI | I/O | SFLASH master output, slave input |
| 61 | FM_RFIN | I | FM radio antenna port |
| 60 | FM_RFAUX | I | FM radio auxiliary antenna port |
| 54 | FM_AOUT1 | O | FM DAC output 1 |
| 55 | FM_AOUT2 | O | FM DAC output 2 |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|------------------------------------|---------------|------|---|
| Bluetooth PCM | | | |
| 179 | BT_PCM_CLK | I/O | PCM clock; can be master (output) or slave (input) |
| 173 | BT_PCM_IN | I | PCM data input |
| 177 | BT_PCM_OUT | O | PCM data output |
| 163 | BT_PCM_SYNC | I/O | PCM sync; can be master (output) or slave (input). |
| Bluetooth USB Interface | | | |
| 164 | BT_USB_DN | I/O | USB (Host) data negative. Negative terminal of the USB transceiver. |
| 169 | BT_USB_DP | I/O | USB (Host) data positive. Positive terminal of the USB transceiver. |
| Bluetooth UART | | | |
| 172 | BT_UART_CTS_L | I | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface. |
| 178 | BT_UART_RTS_L | O | UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin. |
| 162 | BT_UART_RXD | I | UART serial input. Serial data input for the HCI UART interface. |
| 157 | BT_UART_TXD | O | UART serial output. Serial data output for the HCI UART interface. |
| Bluetooth/FM I²S | | | |
| 167 | BT_I2S_CLK | I/O | I ² S clock, can be master (output) or slave (input). |
| 171 | BT_I2S_DO | I/O | I ² S data output |
| 156 | BT_I2S_DI | I/O | I ² S data input |
| 158 | BT_I2S_WS | I/O | I ² S WS; can be master (output) or slave (input). |
| Bluetooth GPIOs | | | |
| 155 | BT_GPIO_2 | I/O | Bluetooth general-purpose I/O |
| 154 | BT_GPIO_3 | I/O | Bluetooth general-purpose I/O |
| 168 | BT_GPIO_4 | I/O | Bluetooth general-purpose I/O |
| 153 | BT_GPIO_5 | I/O | Bluetooth general-purpose I/O |
| Miscellaneous | | | |
| 319 | WL_REG_ON | I | Used by PMU to power up or power down the internal CYW4354 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 320 | BT_REG_ON | I | Used by PMU to power up or power down the internal CYW4354 regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 176 | BT_DEV_WAKE | I/O | Bluetooth DEV_WAKE |
| 170 | BT_HOST_WAKE | I/O | Bluetooth HOST_WAKE |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|--------------------------------------|-----------------------------|------|--|
| Integrated Voltage Regulators | | | |
| 340 | SR_VDDBATA5V | I | Quiet VBAT |
| 348 | SR_VDDBATP5V | I | Power VBAT |
| 336 | SR_VLX | O | CBuck switching regulator output. Refer to Table 44 on page 132 for details of the inductor and capacitor required on this output. |
| 342 | LDO_VDD1P5 | I | LNLDO input |
| 327 | LDO_VDDBAT5V | I | LDO VBAT. |
| 249 | WRF_XTAL_VDD1P5 | I | XTAL LDO input (1.35V) |
| 254 | WRF_XTAL_VDD1P2 | O | XTAL LDO output (1.2V) |
| 351 | VOUT_LNLDO | O | Output of LNLDO |
| 341 | VOUT_CLDO | O | Output of core LDO |
| 362 | VOUT_BTLD02P5 | O | Output of BT LDO |
| 346 | VOUT_LDO3P3_B | O | Output of 3.3V LDO |
| 324 | VOUT_3P3 | O | LDO 3.3V output |
| 330 | VOUT_3P3_SENSE | O | Voltage sense pin for LDO 3.3V output |
| Bluetooth Supplies | | | |
| 46 | BT_PAVDD2P5 | PWR | Bluetooth PA power supply |
| 44 | BT_LNAVDD1P2 | PWR | Bluetooth LNA power supply |
| 42 | BT_IFVDD1P2 | PWR | Bluetooth IF block power supply |
| 47 | BT_PLLVDD1P2 | PWR | Bluetooth RF PLL power supply |
| 50 | BT_VCOVDD1P2 | PWR | Bluetooth RF power supply |
| 148, 149, 150,151 | BT_VDDIO | PWR | Core supply |
| FM Transceiver Supplies | | | |
| – | FM_LNAVCOVDD1P2 | PWR | FM LNA and VCO 1.2V power supply |
| 62 | FM_LNAVDD1P2 | PWR | FM LNA 1.2V power supply |
| 64 | FM_VCOVDD1P2 | PWR | FM VCO 1.2V power supply |
| 59 | FM_PLLVDD1P2 | PWR | FM PLL 1.2V power supply |
| 52 | FM_AUDIOVDD1P2 | PWR | FM AUDIO power supply |
| WLAN Supplies | | | |
| 277 | WRF_BUCK_VDD1P5_CORE0 | PWR | Internal capacitor-less CORE0 LDO supply |
| 296 | WRF_BUCK_VDD1P5_CORE1 | PWR | Internal capacitor-less CORE1 LDO supply |
| 262 | WRF_SYNTN_VBAT_VDD3P3 | PWR | Synth VDD 3.3V supply |
| 289 | WRF_PADRV_VBAT_VDD3P3_CORE0 | PWR | CORE0 PA Driver VBAT supply |
| 264 | WRF_PADRV_VBAT_VDD3P3_CORE1 | PWR | CORE1 PA Driver VBAT supply |
| 269 | WRF_PA5G_VBAT_VDD3P3_CORE0 | PWR | 5 GHz CORE0 PA 3.3V VBAT supply |
| 266 | WRF_PA5G_VBAT_VDD3P3_CORE1 | PWR | 5 GHz CORE1 PA 3.3V VBAT supply |
| 305 | WRF_PA2G_VBAT_VDD3P3_CORE0 | PWR | 2 GHz CORE0 PA 3.3V VBAT supply |
| 285 | WRF_PA2G_VBAT_VDD3P3_CORE1 | PWR | 2 GHz CORE1 PA 3.3V VBAT supply |
| 270 | WRF_MMD_VDD1P2 | PWR | 1.2V supply |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|---|-----------------------------|------|---|
| 262 | WRF_PFD_VDD1P2 | PWR | 1.2V supply |
| Miscellaneous Supplies | | | |
| 160 | OTP_VDD33 | PWR | OTP 3.3V supply |
| 67, 74, 87, 103, 107–115, 127–129, 134–140, 203, 204, 208–211, 213, 224, 228, 241, 242, 246 | VDDC | PWR | 1.2V core supply for WLAN |
| 206, 222, 231 | VDDIO | PWR | 1.8V–3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDIO on the PCB. |
| 145, 147, 369–375, | BT_VDDC | PWR | 1.2V core supply for BT |
| 326 | VDDIO_PMU | PWR | 1.8V–3.3V supply for PMU controls. Must be directly connected to VDDIO and BT_VDDIO on the PCB. |
| 76 | VDDIO_SD | PWR | 1.8V–3.3V supply for SDIO pads |
| 223 | VDDIO_RF | PWR | IO supply for RF switch control pads (3.3V) |
| 98 | HSIC_AVDD12PLL | PWR | 1.2V supply for HSIC PLL |
| 102 | HSIC_DVDD12 | PWR | 1.2V supply for HSIC digital |
| 143 | AVDD_BBPLL | PWR | Baseband PLL supply |
| 11 | PCIE_PLL_AVDD1P2 | PWR | 1.2V supply for PCIe PLL |
| 7 | PCIE_RXTX_AVDD1P2 | PWR | 1.2V supply for PCIe TX and RX |
| 230 | VDDIO_PCIE | PWR | Supply the same voltage to this pin as used for the PCIe out-of-band signals (that is, PCIE_PME_L). This would be 1.8V or 3.3V, and cannot be turned off. |
| Ground | | | |
| 250 | WRF_VCO_GND1P2 | GND | VCO/LOGEN ground |
| 281 | WRF_AFE_GND1P2_CORE0 | GND | CORE0 AFE ground |
| 267 | WRF_AFE_GND1P2_CORE1 | GND | CORE1 AFE ground |
| 295 | WRF_BUCK_GND1P5_CORE0 | GND | Internal capacitor-less CORE0 LDO ground |
| 256 | WRF_BUCK_GND1P5_CORE1 | GND | Internal capacitor-less CORE1 LDO ground |
| 275 | WRF_LNA_2G_GND1P2_CORE0 | GND | 2 GHz internal CORE0 LNA ground |
| 282 | WRF_LNA_2G_GND1P2_CORE1 | GND | 2 GHz internal CORE1 LNA ground |
| 273 | WRF_LNA_5G_GND1P2_CORE0 | GND | 5 GHz internal CORE0 LNA ground |
| 283 | WRF_LNA_5G_GND1P2_CORE1 | GND | 5 GHz internal CORE1 LNA ground |
| 293 | WRF_TX_GND1P2_CORE0 | GND | TX CORE0 ground |
| 255 | WRF_TX_GND1P2_CORE1 | GND | TX CORE1 ground |
| 288 | WRF_PADRV_VBAT_GND3P3_CORE0 | GND | PAD CORE0 ground |
| 265 | WRF_PADRV_VBAT_GND3P3_CORE1 | GND | PAD CORE1 ground |
| 248 | WRF_XTAL_GND1P2 | GND | XTAL ground |

Table 22. WLCSP Signal Descriptions (Cont.)

| Bump# | Signal Name | Type | Description |
|--|----------------------------|------|-----------------------------|
| 291, 307 | WRF_RX2G_GND1P2_CORE0 | GND | RX 2GHz CORE0 ground |
| 259, 317 | WRF_RX2G_GND1P2_CORE1 | GND | RX 2GHz CORE1 ground |
| 292 | WRF_RX5G_GND1P2_CORE0 | GND | RX 5GHz CORE0 ground |
| 257 | WRF_RX5G_GND1P2_CORE1 | GND | RX 5GHz CORE1 ground |
| 252, 316 | WRF_LOGEN_GND1P2 | GND | LOGEN ground |
| 278 | WRF_LOGENG_GND1P2 | GND | LOGEN ground |
| 268, 030 | WRF_PA5G_VBAT_GND3P3_CORE0 | GND | 5 GHz PA CORE0 ground |
| 286, 304 | WRF_PA5G_VBAT_GND3P3_CORE1 | GND | 5 GHz PA CORE1 ground |
| 272, 300 | WRF_PA2G_VBAT_GND3P3_CORE0 | GND | 2 GHz PA CORE0 ground |
| 284, 301 | WRF_PA2G_VBAT_GND3P3_CORE1 | GND | 2 GHz PA CORE1 ground |
| 271 | WRF_MMD_GND1P2 | GND | Ground |
| 274, 318 | WRF_CP_GND1P2 | GND | Ground |
| 263 | WRF_PFD_GND1P2 | GND | Ground |
| 68–73, 75, 83–85, 88–95, 104–106, 116–122, 130, 200, 201, 217, 232–235, 254–245, 333, 334, 384–395 | VSSC | GND | Core ground for WLAN and BT |
| 338, 349, 360, 364 | SR_PVSS | GND | Power ground |
| 335 | PMU_AVSS | GND | Quiet ground |
| 97 | HSIC_AGND12PLL | GND | HSIC PLL ground |
| 40 | BT_PAVSS | GND | Bluetooth PA ground |
| 43 | BT_IFVSS | GND | Bluetooth IF block ground |
| 48 | BT_PLLVSS | GND | Bluetooth PLL ground |
| 51 | BT_VCOVSS | GND | Bluetooth VCO ground |
| 65 | FM_VCOVSS | GND | FM VCO ground |
| 63 | FM_LNAVSS | GND | FM LNA ground |
| 58 | FM_PLLVSS | GND | FM PLL ground |
| 53 | FM_AUDIOVSS | GND | FM AUDIO ground |
| 144 | AVSS_BBPLL | GND | Baseband PLL ground |
| 10 | PCIE_AVSS | GND | PCIE ground |
| 1 | PCIE_RXTX_AVSS | GND | PCIE ground |
| 2 | PCIE_PLL_AVSS | GND | PCIE ground |
| 17, 18, 23, 26, 96 | RGND | GND | Ground |
| – | BTRGND | GND | Ground |

Table 23. WLBGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|---|--------------------|--------|--|
| WLAN and Bluetooth Receive RF Signal Interface | | | |
| N1 | WRF_RFIN_2G_CORE0 | I | 2.4 GHz Bluetooth and WLAN CORE0 receiver shared input |
| V7 | WRF_RFIN_2G_CORE1 | I | 2.4 GHz Bluetooth and WLAN CORE1 receiver shared input |
| V1 | WRF_RFIN_5G_CORE0 | I | 5 GHz WLAN CORE0 receiver input |
| V12 | WRF_RFIN_5G_CORE1 | I | 5 GHz WLAN CORE1 receiver input |
| P1 | WRF_RFOUT_2G_CORE0 | O | 2.4 GHz WLAN CORE0 PA output |
| V8 | WRF_RFOUT_2G_CORE1 | O | 2.4 GHz WLAN CORE1 PA output |
| U1 | WRF_RFOUT_5G_CORE0 | O | 5 GHz WLAN CORE0 PA output |
| V11 | WRF_RFOUT_5G_CORE1 | O | 5 GHz WLAN CORE1 PA output |
| U3 | WRF_TSSI_A_CORE0 | I | 5 GHz TSSI CORE0 input from an optional external power amplifier/power detector. |
| T11 | WRF_TSSI_A_CORE1 | I | 5 GHz TSSI CORE1 input from an optional external power amplifier/power detector. |
| R4 | WRF_GPIO_OUT_CORE0 | I/O | GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector |
| R9 | WRF_GPIO_OUT_CORE1 | I/O | GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector |
| RF Switch Control Lines | | | |
| R7 | RF_SW_CTRL_0 | O | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file. |
| N8 | RF_SW_CTRL_1 | O | |
| P9 | RF_SW_CTRL_2 | O | |
| N7 | RF_SW_CTRL_3 | O | |
| N5 | RF_SW_CTRL_4 | O | |
| P7 | RF_SW_CTRL_5 | O | |
| P5 | RF_SW_CTRL_6 | O | |
| M8 | RF_SW_CTRL_7 | O | |
| K12 | RF_SW_CTRL_8 | O | |
| J11 | RF_SW_CTRL_9 | O | |
| M12 | RF_SW_CTRL_10 | O | |
| L9 | RF_SW_CTRL_11 | O | |
| J9 | RF_SW_CTRL_12 | O | |
| K10 | RF_SW_CTRL_13 | O | |
| M10 | RF_SW_CTRL_14 | O | |
| L8 | RF_SW_CTRL_15 | O | |
| WLAN PCI Express Interface | | | |
| D5 | PCIE_CLKREQ_L | OD | PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required |
| C4 | PCIE_PERST_L | I (PU) | PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1. |

Table 23. WLPGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|--|--------------|------|--|
| B1 | PCIE_RDN0 | I | Receiver differential pair (×1 lane) |
| C1 | PCIE_RDP0 | I | |
| A5 | PCIE_REFCLKN | I | PCIE Differential Clock inputs (negative and positive). 100 MHz differential. |
| A4 | PCIE_REFCLKP | I | |
| A3 | PCIE_TDN0 | O | Transmitter differential pair (×1 lane) |
| A2 | PCIE_TDP0 | O | |
| C5 | PCIE_PME_L | OD | PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3. |
| C3 | PCIE_TESTP | – | PCIe test pin |
| C2 | PCIE_TESTN | – | |
| WLAN SDIO Bus Interface | | | |
| Note: These signals can support alternate functionality depending on package and host interface mode. See Table 27 on page 97 for additional details. | | | |
| A8 | SDIO_CLK | I | SDIO clock input |
| A9 | SDIO_CMD | I/O | SDIO command line |
| B9 | SDIO_DATA_0 | I/O | SDIO data line 0 |
| C9 | SDIO_DATA_1 | I/O | SDIO data line 1 |
| B8 | SDIO_DATA_2 | I/O | SDIO data line 2 |
| C8 | SDIO_DATA_3 | I/O | SDIO data line 3 |
| WLAN HSIC Interface | | | |
| A7 | HSIC_STROBE | I/O | HSIC Strobe |
| A6 | HSIC_DATA | I/O | HSIC Data |
| D7 | RREFHSIC | I | HSIC reference resistor input. If HSIC is used, connect this pin to ground via a 51-ohm 5% resistor. On SDIO designs this pin should not be connected. |

Table 23. WLPGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|--|--------------|------|--|
| WLAN GPIO Interface | | | |
| Note: The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 24 on page 96 and Table 27 on page 97 for additional details. | | | |
| G11 | GPIO_0 | I/O | Programmable GPIO pins |
| F10 | GPIO_1 | I/O | |
| F11 | GPIO_2 | I/O | |
| G9 | GPIO_3 | I/O | |
| H9 | GPIO_4 | I/O | |
| F9 | GPIO_5 | I/O | |
| F8 | GPIO_6 | I/O | |
| E7 | GPIO_7 | I/O | |
| F7 | GPIO_8 | I/O | |
| E6 | GPIO_9 | I/O | |
| H12 | GPIO_10 | I/O | |
| – | GPIO_11 | I/O | |
| – | GPIO_12 | I/O | |
| – | GPIO_13 | I/O | |
| – | GPIO_14 | I/O | |
| – | GPIO_15 | I/O | |
| JTAG Interface | | | |
| D9 | JTAG_SEL | I/O | JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. Note: See Table 27 on page 97 for the JTAG signal pins. |
| Clocks | | | |
| P12 | WRF_XTAL_IN | I | XTAL oscillator input |
| N12 | WRF_XTAL_OUT | O | XTAL oscillator output |
| F6 | LPO_IN | I | External sleep clock input (32.768 kHz) |
| F4 | CLK_REQ | O | Reference clock request (shared by BT and WLAN). If not used, this can be no-connect. |
| Bluetooth/FM Transceiver | | | |
| L1 | BT_RF | O | Bluetooth PA output |
| – | BT_SF_CLK | I | SFLASH_CLK |
| – | BT_SF_CS_L | I/O | SFLASH_CSN |
| – | BT_SF_MISO | I/O | SFLASH master input, slave output |
| – | BT_SF_MOSI | I/O | SFLASH master output, slave input |
| H1 | FM_RFIN | I | FM radio antenna port |
| – | FM_RFAUX | I | FM radio auxiliary antenna port |
| E1 | FM_AOUT1 | O | FM DAC output 1 |
| F1 | FM_AOUT2 | O | FM DAC output 2 |
| Bluetooth PCM | | | |

Table 23. WLBGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|------------------------------------|---------------|------|---|
| M6 | BT_PCM_CLK | I/O | PCM clock; can be master (output) or slave (input) |
| J4 | BT_PCM_IN | I | PCM data input |
| H4 | BT_PCM_OUT | O | PCM data output |
| K6 | BT_PCM_SYNC | I/O | PCM sync; can be master (output) or slave (input). |
| Bluetooth USB Interface | | | |
| E5 | BT_USB_DN | I/O | USB (Host) data negative. Negative terminal of the USB transceiver. |
| F5 | BT_USB_DP | I/O | USB (Host) data positive. Positive terminal of the USB transceiver. |
| Bluetooth UART | | | |
| L5 | BT_UART_CTS_L | I | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface. |
| K5 | BT_UART_RTS_L | O | UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin. |
| H5 | BT_UART_RXD | I | UART serial input. Serial data input for the HCI UART interface. |
| J5 | BT_UART_TXD | O | UART serial output. Serial data output for the HCI UART interface. |
| Bluetooth/FM I²S | | | |
| J6 | BT_I2S_CLK | I/O | I ² S clock, can be master (output) or slave (input). |
| G6 | BT_I2S_DO | I/O | I ² S data output |
| G5 | BT_I2S_DI | I/O | I ² S data input |
| L6 | BT_I2S_WS | I/O | I ² S WS; can be master (output) or slave (input). |
| Bluetooth GPIO | | | |
| – | BT_GPIO_2 | I/O | Bluetooth general-purpose I/O |
| – | BT_GPIO_3 | I/O | Bluetooth general-purpose I/O |
| K4 | BT_GPIO_4 | I/O | Bluetooth general-purpose I/O |
| – | BT_GPIO_5 | I/O | Bluetooth general-purpose I/O |
| Miscellaneous | | | |
| A10 | WL_REG_ON | I | Used by PMU to power up or power down the internal CYW4354 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| D10 | BT_REG_ON | I | Used by PMU to power up or power down the internal CYW4354 regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| L4 | BT_DEV_WAKE | I/O | Bluetooth DEV_WAKE |
| J3 | BT_HOST_WAKE | I/O | Bluetooth HOST_WAKE |

Table 23. WLBGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|--------------------------------------|-----------------------------|------|--|
| Integrated Voltage Regulators | | | |
| B11 | SR_VDDBATA5V | I | Quiet VBAT |
| B12 | SR_VDDBATP5V | I | Power VBAT |
| A11 | SR_VLX | O | CBuck switching regulator output. Refer to Table 44 on page 132 for details of the inductor and capacitor required on this output. |
| C12 | LDO_VDD1P5 | I | LNLDO input |
| E12 | LDO_VDDBAT5V | I | LDO VBAT. |
| P11 | WRF_XTAL_VDD1P5 | I | XTAL LDO input (1.35V) |
| N10 | WRF_XTAL_VDD1P2 | O | XTAL LDO output (1.2V) |
| D11 | VOUT_LNLDO | O | Output of LNLDO |
| C11 | VOUT_CLDO | O | Output of core LDO |
| D12 | VOUT_BTLD02P5 | O | Output of BT LDO |
| E11 | VOUT_LDO3P3_B | O | Output of 3.3V LDO |
| F12 | VOUT_3P3 | O | LDO 3.3V output |
| – | VOUT_3P3_SENSE | O | Voltage sense pin for LDO 3.3V output |
| Bluetooth Supplies | | | |
| M1 | BT_PAVDD2P5 | PWR | Bluetooth PA power supply |
| K1 | BT_LNAVDD1P2 | PWR | Bluetooth LNA power supply |
| K3 | BT_IFVDD1P2 | PWR | Bluetooth IF block power supply |
| K2 | BT_PLLVDD1P2 | PWR | Bluetooth RF PLL power supply |
| J1 | BT_VCOVDD1P2 | PWR | Bluetooth RF power supply |
| K7 | BT_VDDIO | PWR | Core supply |
| FM Transceiver Supplies | | | |
| G1 | FM_LNAVCOVDD1P2 | PWR | FM LNA and VCO 1.2V power supply |
| – | FM_LNAVDD1P2 | PWR | FM LNA 1.2V power supply |
| – | FM_VCOVDD1P2 | PWR | FM VCO 1.2V power supply |
| F3 | FM_PLLVDD1P2 | PWR | FM PLL 1.2V power supply |
| E2 | FM_AUDIOVDD1P2 | PWR | FM AUDIO power supply |
| WLAN Supplies | | | |
| U4 | WRF_BUCK_VDD1P5_CORE0 | PWR | Internal capacitor-less CORE0 LDO supply |
| R11 | WRF_BUCK_VDD1P5_CORE1 | PWR | Internal capacitor-less CORE1 LDO supply |
| V6 | WRF_SYNTH_VBAT_VDD3P3 | PWR | Synth VDD 3.3V supply |
| R3 | WRF_PADRV_VBAT_VDD3P3_CORE0 | PWR | CORE0 PA Driver VBAT supply |
| T9 | WRF_PADRV_VBAT_VDD3P3_CORE1 | PWR | CORE1 PA Driver VBAT supply |
| T1 | WRF_PA5G_VBAT_VDD3P3_CORE0 | PWR | 5 GHz CORE0 PA 3.3V VBAT supply |
| V10 | WRF_PA5G_VBAT_VDD3P3_CORE1 | PWR | 5 GHz CORE1 PA 3.3V VBAT supply |
| R1 | WRF_PA2G_VBAT_VDD3P3_CORE0 | PWR | 2 GHz CORE0 PA 3.3V VBAT supply |
| V9 | WRF_PA2G_VBAT_VDD3P3_CORE1 | PWR | 2 GHz CORE1 PA 3.3V VBAT supply |
| T5 | WRF_MMD_VDD1P2 | PWR | 1.2V supply |
| T4 | WRF_PFD_VDD1P2 | PWR | 1.2V supply |

Table 23. WLBGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|-----------------------------------|-----------------------------|------|---|
| Miscellaneous Supplies | | | |
| – | OTP_VDD33 | PWR | OTP 3.3V supply |
| B7, D4, E9, G10, J8, J12, L10, M7 | VDDC | PWR | 1.2V core supply for WLAN |
| E10 | VDDIO | PWR | 1.8V–3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDIO on the PCB. |
| E4, H3, M5 | BT_VDDC | PWR | 1.2V core supply for BT |
| – | VDDIO_PMU | PWR | 1.8V–3.3V supply for PMU controls. Must be directly connected to VDDIO and BT_VDDIO on the PCB. |
| E8 | VDDIO_SD | PWR | 1.8V–3.3V supply for SDIO pads |
| H11 | VDDIO_RF | PWR | IO supply for RF switch control pads (3.3V) |
| C7 | HSIC_AVDD12PLL | PWR | 1.2V supply for HSIC PLL |
| C6 | HSIC_DVDD12 | PWR | 1.2V supply for HSIC digital |
| H7 | AVDD_BBPLL | PWR | Baseband PLL supply |
| B3 | PCIE_PLL_AVDD1P2 | PWR | 1.2V supply for PCIe PLL |
| B2 | PCIE_RXTX_AVDD1P2 | PWR | 1.2V supply for PCIe TX and RX |
| Ground | | | |
| U6 | WRF_VCO_GND1P2 | GND | VCO/LOGEN ground |
| P4 | WRF_AFE_GND1P2_CORE0 | GND | CORE0 AFE ground |
| R8 | WRF_AFE_GND1P2_CORE1 | GND | CORE1 AFE ground |
| V4 | WRF_BUCK_GND1P5_CORE0 | GND | Internal capacitor-less CORE0 LDO ground |
| R12 | WRF_BUCK_GND1P5_CORE1 | GND | Internal capacitor-less CORE1 LDO ground |
| N2 | WRF_LNA_2G_GND1P2_CORE0 | GND | 2 GHz internal CORE0 LNA ground |
| U7 | WRF_LNA_2G_GND1P2_CORE1 | GND | 2 GHz internal CORE1 LNA ground |
| V2 | WRF_LNA_5G_GND1P2_CORE0 | GND | 5 GHz internal CORE0 LNA ground |
| U12 | WRF_LNA_5G_GND1P2_CORE1 | GND | 5 GHz internal CORE1 LNA ground |
| P3 | WRF_TX_GND1P2_CORE0 | GND | TX CORE0 ground |
| T8 | WRF_TX_GND1P2_CORE1 | GND | TX CORE1 ground |
| T3 | WRF_PADRV_VBAT_GND3P3_CORE0 | GND | PAD CORE0 ground |
| T10 | WRF_PADRV_VBAT_GND3P3_CORE1 | GND | PAD CORE1 ground |
| N11 | WRF_XTAL_GND1P2 | GND | XTAL ground |
| N3 | WRF_RX2G_GND1P2_CORE0 | GND | RX 2GHz CORE0 ground |
| T7 | WRF_RX2G_GND1P2_CORE1 | GND | RX 2GHz CORE1 ground |
| V3 | WRF_RX5G_GND1P2_CORE0 | GND | RX 5GHz CORE0 ground |
| T12 | WRF_RX5G_GND1P2_CORE1 | GND | RX 5GHz CORE1 ground |
| R6 | WRF_LOGEN_GND1P2 | GND | LOGEN ground |
| R5 | WRF_LOGENG_GND1P2 | GND | LOGEN ground |
| T2, U2 | WRF_PA5G_VBAT_GND3P3_CORE0 | GND | 5 GHz PA CORE0 ground |
| U10, U11 | WRF_PA5G_VBAT_GND3P3_CORE1 | GND | 5 GHz PA CORE1 ground |

Table 23. WLBGA Signal Descriptions

| Ball# | Signal Name | Type | Description |
|---|----------------------------|------|-----------------------------|
| P2, R2 | WRF_PA2G_VBAT_GND3P3_CORE0 | GND | 2 GHz PA CORE0 ground |
| U8, U9 | WRF_PA2G_VBAT_GND3P3_CORE1 | GND | 2 GHz PA CORE1 ground |
| T6 | WRF_MMD_GND1P2 | GND | Ground |
| V5 | WRF_CP_GND1P2 | GND | Ground |
| U5 | WRF_PFD_GND1P2 | GND | Ground |
| C10, D3, D6, G4, G8, G12, L7, L11, M4 | VSSC | GND | Core ground for WLAN and BT |
| A12 | SR_PVSS | GND | Power ground |
| B10 | PMU_AVSS | GND | Quiet ground |
| B6 | HSIC_AGND12PLL | GND | HSIC PLL ground |
| L2 | BT_PAVSS | GND | Bluetooth PA ground |
| M3 | BT_IFVSS | GND | Bluetooth IF block ground |
| L3 | BT_PLLVSS | GND | Bluetooth PLL ground |
| J2 | BT_VCOVSS | GND | Bluetooth VCO ground |
| G2 | FM_VCOVSS | GND | FM VCO ground |
| H2 | FM_LNAVSS | GND | FM LNA ground |
| G3 | FM_PLLVSS | GND | FM PLL ground |
| F2 | FM_AUDIOVSS | GND | FM AUDIO ground |
| G7 | AVSS_BBPLL | GND | Baseband PLL ground |
| – | PCIE_AVSS | GND | PCIe ground |
| B4 | PCIE_RXTX_AVSS | GND | PCIe ground |
| B5 | PCIE_PLL_AVSS | GND | PCIe ground |
| – | RGND | GND | Ground |
| – | BTRGND | GND | Ground |

13.4 WLAN/BT GPIO Signals and Strapping Options

The pins listed in [Table 24](#) and [Table 25](#) are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 24. WLAN GPIO Functions and Strapping Options

| Pin Name | Default Function | Description |
|-----------------|------------------|---|
| GPIO_4 | 0 | 1: SPROM is present 0: SPROM is absent (default). Applicable in PCIe Host mode. Note: In SDIO Host mode, sdioPadVddio is 3.3V while set to 1, and 1.8V while set to 0. |
| GPIO_5 | 0 | 0: sflash absent (default) 1: sflash present |
| GPIO_[10, 9, 8] | [0,0,0] | Host interface selection: see Table 26 . |
| GPIO_12 | 1 | 1 = HTAvailable (default) 0 = ResourceModelInit is ALPAvailable. On PCBs, use a pull-down and tie to ALP clock mode. |

Table 25. BT GPIO Functions and Strapping Options

| Pin Name | Default Function | Description |
|----------|------------------|--|
| BT_GPIO4 | 0 | 1: BT Serial Flash is present. 0: BT Serial Flash is absent (default) |

Table 26. GPIO_[10, 9, 8] Host Interface Selection

| GPIO_[10, 9, 8] Bit Setting | WLAN Host Interface Mode | Bluetooth Mode |
|-----------------------------|--------------------------|--|
| 000 | SDIO | BTUART or BTUSB; BT tPorts stand-alone. |
| 010 | HSIC_30D | BTUART or BTUSB; BT tPorts stand-alone |
| 011 | PCIE | BTUART or BTUSB; BT tPorts stand-alone |

13.5 GPIO Alternative Signal Functions

Table 27. GPIO Alternative Signal Functions

| | Test Mode | UART | SFLASH | SPROM | BSC | Miscellaneous-0 (JTAG_SEL = 1) | GCI | Miscellaneous-1 | Miscellaneous-2 | PWDOG | |
|-----------|-----------------|-------------------|-------------|-----------|----------|-----------------------------------|------------|--------------------|-----------------|--------------|---------------------------|
| Pin Names | Function Select | | | | | | | | | | Additional Functionality |
| | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
| GPIO_0 | TEST_GPIO_0 | FAST_UART_RX | UART_DBG_TX | - | BSC_CLK | - | GCI_GPIO_4 | SDIO_SEP_INT | SDIO_SEP_INT_OD | PWDOG_GPIO_0 | WL_HOST_WAKE |
| GPIO_1 | TEST_GPIO_1 | FAST_UART_TX | UART_DBG_RX | - | BSC_SDA | RF_DISABLE_L | GCI_GPIO_5 | - | - | PWDOG_GPIO_1 | WL_DEV_WAKE/HSIC_HOST_RDY |
| GPIO_2 | TEST_GPIO_2 | FAST_UART_CTS_IN | - | - | N/A | TCK | GCI_GPIO_1 | - | - | - | - |
| GPIO_3 | TEST_GPIO_3 | FAST_UART_RTS_OUT | - | - | N/A | TMS | GCI_GPIO_0 | - | - | - | - |
| GPIO_4 | TEST_GPIO_4 | UART_RX | UART_DBG_RX | - | N/A | TDI | SECI_IN | - | - | - | - |
| GPIO_5 | TEST_GPIO_5 | UART_TX | UART_DBG_TX | - | N/A | TDO | SECI_OUT | - | - | - | - |
| GPIO_6 | TEST_GPIO_6 | - | - | - | N/A | TRST_L | GCI_GPIO_2 | SECI_IN | - | - | - |
| GPIO_7 | TEST_GPIO_7 | FAST_UART_RTS_OUT | SFLASH_CS | SPROM_CS | BSC_SDA | PMU_TEST_O | GCI_GPIO_3 | USB_MDC/HSIC_MDC | - | PWDOG_GPIO_2 | WL_LED (For WLPGA) |
| GPIO_8 | TEST_GPIO_8 | FAST_UART_CTS_IN | SFLASH_CLK | SPROM_CLK | BSC_CLK | - | SECI_IN | USB_MDIO/HSIC_MDIO | - | PWDOG_GPIO_3 | - |
| GPIO_9 | TEST_GPIO_9 | FAST_UART_RX | SFLASH_MI | SPROM_MI | PALDO_PU | - | SECI_OUT | PALDO_PD | - | PWDOG_GPIO_4 | - |
| GPIO_10 | TEST_GPIO_10 | FAST_UART_TX | SFLASH_MO | SPROM_MO | - | - | GCI_GPIO_4 | - | - | PWDOG_GPIO_5 | HSIC_DEV_RDY |
| GPIO_11 | TEST_GPIO_11 | FAST_UART_RX | - | - | PALDO_PU | - | GCI_GPIO_5 | PALDO_PD | - | - | USB_VBUS_PRESENT |
| GPIO_12 | TEST_GPIO_12 | FAST_UART_TX | - | - | - | - | GCI_GPIO_1 | - | - | - | - |

Table 27. GPIO Alternative Signal Functions (Cont.)

| | Test Mode | UART | SFLASH | SPROM | BSC | Miscellaneous-0 (JTAG_SEL = 1) | GCI | Miscellaneous-1 | Miscellaneous-2 | PWDOG | |
|---|-----------------|--------------------|-------------|-------|-----|-----------------------------------|------------|-----------------|-----------------|-------|--------------------------|
| Pin Names | Function Select | | | | | | | | | | Additional Functionality |
| | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
| GPIO_13 | TEST_GPIO_13 | usbphy_scan_resetb | – | – | – | – | GCI_GPIO_0 | – | – | – | – |
| GPIO_14 | TEST_GPIO_14 | FAST_UART_RT_OUT | UART_DBG_RX | – | – | – | GCI_GPIO_2 | – | – | – | – |
| GPIO_15 | TEST_GPIO_15 | FAST_UART_CTS_IN | UART_DBG_TX | – | – | – | GCI_GPIO_3 | – | – | – | – |
| <p>Note:</p> <ol style="list-style-type: none"> GPIO_0 and WL_DEV_WAKE signals are selected by using software. USB_VBUS_PRESENT indicates that USB30D is selected. SDIO_PADVDDIO = 1 (not in straps table) is set to 3.3V by default for all packages. GPIO_7 can be used as WL_LED in WLPGA packages. USB_MDx/HSIC_MDx MDIO is the interface of USB1.0/2.0/3.0 PHY or of HSIC PHY (depending on the strap option). | | | | | | | | | | | |

Table 28 defines status for all CYW4354 GPIOs based on the tristate test mode.

Table 28. GPIO Status Vs. Test Modes

| Test Mode | Function Select | Status for All GPIOs |
|--------------|-----------------|----------------------|
| TRISTATE_IND | 12 | Input disable |
| TRISTATE_PDN | 13 | Pull down |
| TRISTATE_PUP | 14 | Pull up |
| TRISTATE | 15 | Tristate |

13.6 I/O States

The following notations are used in [Table 29 on page 99](#):

I: Input signal

O: Output signal

I/O: Input/Output signal

PU = Pulled up

PD = Pulled down

NoPull = Neither pulled up nor pulled down

Note: Where applicable, the default value is shown in bold brackets (for example, **[default value]**).

Table 29. I/O States

| Name | I/O | Keeper ^a | Active Mode | Low Power State/Sleep (All Power Present) | Power-down ^b (BT_REG_ON and WL_REG_ON Held Low) | Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High) | (WL_REG_ON High and BT_REG_ON Low) and VDDIOs Are Present | Power Rail |
|--------------|-----|---------------------|--|--|---|--|---|------------|
| WL_REG_ON | I | N | I: PD Pull-down can be disabled | I: PD Pull-down can be disabled | I: PD (of 200K) | I: PD (of 200K) | I: PD (of 200K) | – |
| BT_REG_ON | | | | | | | | |
| CLK_REQ | I/O | Y | Open drain or push-pull Programmable Active high | Open drain or push-pull Programmable Active high | High-Z, NoPull | Open drain Active high | Open drain Active high | BT_VDDIO |
| BT_HOST_WAKE | I/O | Y | I/O: PU, PD, NoPull Programmable | I/O: PU, PD, NoPull Programmable | High-Z, NoPull | I: PD | I: PD | |
| BT_DEV_WAKE | | | | | | | | |
| BT_GPIO 5 | | | | | | | | |
| BT_GPIO 4 | | | | | | | | |
| BT_GPIO 2, 3 | | | | | | | | |
| | | | | | | I: Floating, but input disabled | | |
| | | | | | | I: PU | I: PU | |
| BT_UART_CTS | I | Y | I: NoPull; PU programmable | I: NoPull | High-Z, NoPull | I: PU | I: PU | |
| BT_UART_RTS | O | | O: NoPull | O: NoPull | | | | |
| BT_UART_RXD | I | | I: PU | I: NoPull | | | | |
| BT_UART_TXD | O | | O: NoPull | O: NoPull | | | | |

Table 29. I/O States (Cont.)

| Name | I/O | Keeper ^a | Active Mode | Low Power State/Sleep (All Power Present) | Power-down ^b (BT_REG_ON and WL_REG_ON Held Low) | Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High) | (WL_REG_ON High and BT_REG_ON Low) and VDDIOs Are Present | Power Rail | |
|-------------|-----|---------------------|------------------------|---|---|--|---|------------|---------------------------------|
| SDIO Data | I/O | N | I/O: PU (SDIO Mode) | I: PU (SDIO Mode) | High-Z, NoPull | I: PU (SDIO Mode) | I: PU (SDIO Mode) | VDDIO_SD | |
| SDIO CMD | | | | | | | | | |
| SDIO_CLK | | | | | | | | | I |
| BT_PCM_CLK | I/O | Y | I: NoPull ^c | I: NoPull ^c | High-Z, NoPull | I: PD | I: PD | BT_VDDIO | |
| BT_PCM_IN | | | | | | | | | |
| BT_PCM_OUT | | | | | | | | | |
| BT_PCM_SYNC | | | | | | | | | I: Floating, but input disabled |
| BT_I2S_WS | | | | | | | | | I: NoPull ^d |
| BT_I2S_CLK | | | | | | | | | |
| BT_I2S_DI | | | | | | | | | |
| BT_I2S_DO | | | | | | | | | |

Table 29. I/O States (Cont.)

| Name | I/O | Keeper ^a | Active Mode | Low Power State/Sleep (All Power Present) | Power-down ^b (BT_REG_ON and WL_REG_ON Held Low) | Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High) | (WL_REG_ON High and BT_REG_ON Low) and VDDIOs Are Present | Power Rail |
|--------------|-----|---------------------|--|--|--|---|---|------------|
| GPIO_0 | I/O | Y | I/O: PU, PD, NoPull Programmable [NoPull] | I/O: PU, PD, NoPull Programmable [NoPull] | High-Z, NoPull | I: NoPull | I: NoPull | VDDIO |
| GPIO_1 | | Y | | | | | | |
| GPIO_2 | | Y | | | | | | |
| GPIO_3 | | Y | | | | | | |
| GPIO_4 | | Y | I/O: PU, PD, NoPull Programmable [PD] | I/O: PU, PD, NoPull Programmable [PD] | I: PD | I: PD | | |
| GPIO_5 | | Y | I/O: PU, PD, NoPull Programmable [PD] | I/O: PU, PD, NoPull Programmable [PD] | | | | |
| GPIO_6 | | Y | I/O: PU, PD, NoPull Programmable [NoPull] | I/O: PU, PD, NoPull Programmable [NoPull] | | | High-Z, NoPull | |
| GPIO_7 | | Y | I/O: PU, PD, NoPull Programmable | I/O: PU, PD, NoPull Programmable | I: PD | I ^e | I: NoPull | |
| GPIO_8 | | Y | | | | | | |
| GPIO_9 | | Y | | | | | | |
| GPIO_10 | | Y | I/O: PU, PD, NoPull Programmable [PD] | I/O: PU, PD, NoPull Programmable [PD] | High-Z, NoPull | I: PD | I: PD | |
| GPIO_11 | | Y | I/O: PU, PD, NoPull Programmable [NoPull] | I/O: PU, PD, NoPull Programmable [NoPull] | I: PD | I: NoPull | I: NoPull | |
| GPIO_12 | | Y | I/O: PU, PD, NoPull Programmable [PU] | I/O: PU, PD, NoPull Programmable [PU] | High-Z, NoPull | I: PU | I: PU | |
| GPIO_13 | | Y | I/O: PU, PD, NoPull Programmable [NoPull] | I/O: PU, PD, NoPull Programmable [NoPull] | | I: NoPull | I: NoPull | |
| GPIO_14 | | Y | | | | | | |
| GPIO_15 | Y | | | | | | | |
| RF_SW_CTRL_X | I/O | Y | O: NoPull | O: NoPull | I: PD | O: NoPull | : NoPull | VDDIO_RF |

- a. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in Power-down state. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).
- b. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.
- c. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either input or output.
- d. Depending on whether the I²S interface is enabled and the configuration of I²S is in master or slave mode, it can be either input or output.
- e. For WLPGA this GPIO has NoPull in this state. For WLCSP this GPIO has a PU in this state.

14. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization

14.1 Absolute Maximum Ratings

Caution:

The absolute maximum ratings in Table 30 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 30. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|--|-------------------------|---------------|------|
| DC supply for VBAT and PA driver supply ^a | VBAT | -0.5 to +6.0 | V |
| DC supply voltage for digital I/O | VDDIO | -0.5 to 3.9 | V |
| DC supply voltage for RF switch I/Os | VDDIO_RF | -0.5 to 3.9 | V |
| DC input supply voltage for CLDO and LNLDO | - | -0.5 to 1.575 | V |
| DC supply voltage for RF analog | VDDRF | -0.5 to 1.32 | V |
| DC supply voltage for core | VDDC | -0.5 to 1.32 | V |
| WRF_TCXO_VDD | - | -0.5 to 3.63 | V |
| Maximum undershoot voltage for I/O ^b | V _{undershoot} | -0.5 | V |
| Maximum overshoot voltage for I/O ^b | V _{overshoot} | VDDIO + 0.5 | V |
| Maximum junction temperature | T _j | 125 | °C |

a. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.

b. Duration not to exceed 25% of the duty cycle.

14.2 Environmental Ratings

The environmental ratings are shown in [Table 31](#).

Table 31. Environmental Ratings

| Characteristic | Value | Units | Conditions/Comments |
|---------------------------------------|--------------|-------|-----------------------------------|
| Ambient Temperature (T _A) | -30 to +85 | °C | Functional operation ^a |
| Storage Temperature | -40 to +125 | °C | - |
| Relative Humidity | Less than 60 | % | Storage |
| | Less than 85 | % | Operation |

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

14.3 Electrostatic Discharge Specifications

Proper use of wrist and heel grounding straps is required to discharge static electricity when handling the CYW4354.

Caution:

Electrostatic discharge (ESD) damage can occur if the CYW4354 is mishandled. Always wear an ESD-preventive wrist or heel ground strap when handling the CYW4354. As with all electrical devices of this type, take all necessary safety precautions to prevent damage to the equipment. When not being used, always store the CYW4354 in antistatic packaging.

Table 32. Electrostatic Discharge Specifications

| Pin Type | Symbol | Condition | ESD Rating | Unit |
|------------------|--------------|---|-------------------------|------|
| ESD ^a | ESD_HAND_HBM | Human body model contact discharge per JEDEC EID/JESD22-A114. | WLBGA:1.k WLCSP:1.5k | V |
| CDM | ESD_HAND_CDM | Charged device model contact JEDEC EIA/JESD22-C101. | WLBGA:300 WLCSP:500 | V |

a. Handling Reference: NQY00083, Section 3.4, Group D9, Table B.

14.4 Recommended Operating Conditions and DC Characteristics

Caution:

Functional operation is not guaranteed outside of the limits shown in [Table 33](#), and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 33. Recommended Operating Conditions and DC Characteristics

| Parameter | Symbol | Value | | | Unit |
|---|---------------------|------------------|---------|-------------------|------|
| | | Minimum | Typical | Maximum | |
| DC supply voltage for VBAT | VBAT | 3.0 ^a | – | 5.25 ^b | V |
| DC supply voltage for core | VDD | 1.14 | 1.2 | 1.26 | V |
| DC supply voltage for RF blocks in chip | VDDRF | 1.14 | 1.2 | 1.26 | V |
| DC supply voltage for TCXO input buffer | WRF_TCXO_VDD | 1.62 | 1.8 | 1.98 | V |
| DC supply voltage for digital I/O | VDDIO, VDDIO_SD | 1.62 | – | 3.63 | V |
| DC supply voltage for RF switch I/Os | VDDIO_RF | 3.13 | 3.3 | 3.46 | V |
| External TSSI input | TSSI | 0.15 | – | 0.95 | V |
| Internal POR threshold | V _{th_POR} | 0.4 | – | 0.7 | V |
| SDIO Interface I/O Pins | | | | | |
| For VDDIO_SD = 1.8V: | | | | | |
| Input high voltage | VIH | 1.27 | – | – | V |
| Input low voltage | VIL | – | – | 0.58 | V |
| Output high voltage @ 2 mA | VOH | 1.40 | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.45 | V |
| For VDDIO_SD = 3.3V: | | | | | |
| Input high voltage | VIH | 0.625 × VDDIO | – | – | V |
| Input low voltage | VIL | – | – | 0.25 × VDDIO | V |
| Output high voltage @ 2 mA | VOH | 0.75 × VDDIO | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.125 × VDDIO | V |
| Other Digital I/O Pins | | | | | |
| For VDDIO = 1.8V: | | | | | |
| Input high voltage | VIH | 0.65 × VDDIO | – | – | V |
| Input low voltage | VIL | – | – | 0.35 × VDDIO | V |
| Output high voltage @ 2 mA | VOH | VDDIO – 0.45 | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.45 | V |
| For VDDIO = 3.3V: | | | | | |
| Input high voltage | VIH | 2.00 | – | – | V |
| Input low voltage | VIL | – | – | 0.80 | V |
| Output high voltage @ 2 mA | VOH | VDDIO – 0.4 | – | – | V |
| Output low Voltage @ 2 mA | VOL | – | – | 0.40 | V |

Table 33. Recommended Operating Conditions and DC Characteristics (Cont.)

| Parameter | Symbol | Value | | | Unit |
|--|-----------------|-------------|---------|---------|------|
| | | Minimum | Typical | Maximum | |
| RF Switch Control Output Pins^c | | | | | |
| For VDDIO_RF = 3.3V: | | | | | |
| Output high voltage @ 2 mA | VOH | VDDIO – 0.4 | – | – | V |
| Output low voltage @ 2 mA | VOL | – | – | 0.40 | V |
| Input capacitance | C _{IN} | – | – | 5 | pF |

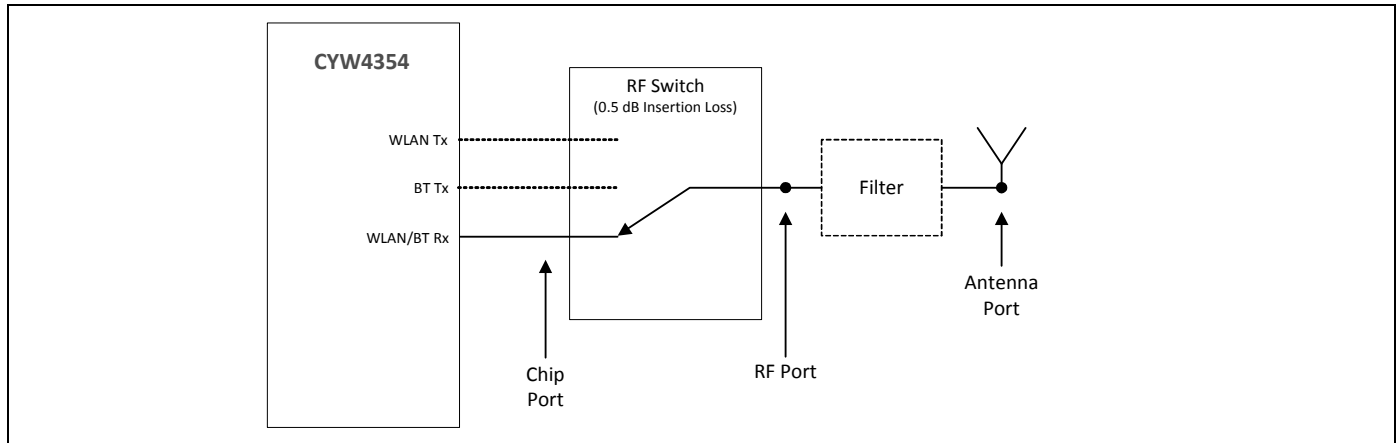
- a. The CYW4354 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 4.8V.
- b. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
- c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

15. Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 31 on page 103](#) and [Table 33 on page 104](#). Typical values apply for an ambient temperature of +25°C.

Figure 35. RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 34. Bluetooth Receiver RF Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--|-----------------------------------|---------|---------|---------|------|
| Note: The specifications in this table are measured at the chip port output unless otherwise specified. | | | | | |
| General | | | | | |
| Frequency range | – | 2402 | – | 2480 | MHz |
| RX sensitivity | GFSK, 0.1% BER, 1 Mbps | – | –93.5 | – | dBm |
| | $\pi/4$ -DQPSK, 0.01% BER, 2 Mbps | – | –95.5 | – | dBm |
| | 8-DPSK, 0.01% BER, 3 Mbps | – | –89.5 | – | dBm |
| Input IP3 | – | –16 | – | – | dBm |
| Maximum input at antenna | – | – | – | –20 | dBm |
| RX LO Leakage | | | | | |
| 2.4 GHz band | – | – | –90.0 | –80.0 | dBm |

Table 34. Bluetooth Receiver RF Specifications (Cont.)

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|--------------------------|---------|---------|---------|------|
| Interference Performance^a | | | | | |
| C/I co-channel | GFSK, 0.1% BER | – | 8 | 11 | dB |
| C/I 1 MHz adjacent channel | GFSK, 0.1% BER | – | –7 | 0 | dB |
| C/I 2 MHz adjacent channel | GFSK, 0.1% BER | – | –38 | –30 | dB |
| C/I ≥ 3 MHz adjacent channel | GFSK, 0.1% BER | – | –56 | –40 | dB |
| C/I image channel | GFSK, 0.1% BER | – | –31 | –9 | dB |
| C/I 1 MHz adjacent to image channel | GFSK, 0.1% BER | – | –46 | –20 | dB |
| C/I co-channel | $\pi/4$ -DQPSK, 0.1% BER | – | 9 | 13 | dB |
| C/I 1 MHz adjacent channel | $\pi/4$ -DQPSK, 0.1% BER | – | –11 | 0 | dB |
| C/I 2 MHz adjacent channel | $\pi/4$ -DQPSK, 0.1% BER | – | –39 | –30 | dB |
| C/I ≥ 3 MHz adjacent channel | $\pi/4$ -DQPSK, 0.1% BER | – | –55 | –40 | dB |
| C/I image channel | $\pi/4$ -DQPSK, 0.1% BER | – | –23 | –7 | dB |
| C/I 1 MHz adjacent to image channel | $\pi/4$ -DQPSK, 0.1% BER | – | –43 | –20 | dB |
| C/I co-channel | 8-DPSK, 0.1% BER | – | 17 | 21 | dB |
| C/I 1 MHz adjacent channel | 8-DPSK, 0.1% BER | – | –4 | 5 | dB |
| C/I 2 MHz adjacent channel | 8-DPSK, 0.1% BER | – | –37 | –25 | dB |
| C/I ≥ 3 MHz adjacent channel | 8-DPSK, 0.1% BER | – | –53 | –33 | dB |
| C/I Image channel | 8-DPSK, 0.1% BER | – | –16 | 0 | dB |
| C/I 1 MHz adjacent to image channel | 8-DPSK, 0.1% BER | – | –37 | –13 | dB |
| Out-of-Band Blocking Performance (CW) | | | | | |
| 30–2000 MHz | 0.1% BER | – | –10.0 | – | dBm |
| 2000–2399 MHz | 0.1% BER | – | –27 | – | dBm |
| 2498–3000 MHz | 0.1% BER | – | –27 | – | dBm |
| 3000 MHz–12.75 GHz | 0.1% BER | – | –10.0 | – | dBm |
| Out-of-Band Blocking Performance, Modulated Interferer | | | | | |
| GFSK (1 Mbps)^b | | | | | |
| 698–716 MHz | WCDMA | – | –13.5 | – | dBm |
| 776–849 MHz | WCDMA | – | –13.8 | – | dBm |
| 824–849 MHz | GSM850 | – | –13.5 | – | dBm |
| 824–849 MHz | WCDMA | – | –14.3 | – | dBm |
| 880–915 MHz | E-GSM | – | –13.1 | – | dBm |
| 880–915 MHz | WCDMA | – | –13.1 | – | dBm |
| 1710–1785 MHz | GSM1800 | – | –18.1 | – | dBm |
| 1710–1785 MHz | WCDMA | – | –17.4 | – | dBm |
| 1850–1910 MHz | GSM1900 | – | –19.4 | – | dBm |
| 1850–1910 MHz | WCDMA | – | –18.8 | – | dBm |
| 1880–1920 MHz | TD-SCDMA | – | –19.7 | – | dBm |
| 1920–1980 MHz | WCDMA | – | –19.6 | – | dBm |
| 2010–2025 MHz | TD-SCDMA | – | –20.4 | – | dBm |

Table 34. Bluetooth Receiver RF Specifications (Cont.)

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|------------|---------|---------|---------|------|
| 2500–2570 MHz | WCDMA | – | –20.4 | – | dBm |
| 2500–2570 MHz ^c | Band 7 | – | –30.5 | – | dBm |
| 2300–2400 MHz ^d | Band 40 | – | –34.0 | – | dBm |
| 2570–2620 MHz ^e | Band 38 | – | –30.8 | – | dBm |
| 2545–2575 MHz ^f | XGP Band | – | –29.5 | – | dBm |
| $\pi/4$ DPSK (2 Mbps)^b | | | | | |
| 698–716 MHz | WCDMA | – | –9.8 | – | dBm |
| 776–794 MHz | WCDMA | – | –9.7 | – | dBm |
| 824–849 MHz | GSM850 | – | –10.7 | – | dBm |
| 824–849 MHz | WCDMA | – | –11.4 | – | dBm |
| 880–915 MHz | E-GSM | – | –10.4 | – | dBm |
| 880–915 MHz | WCDMA | – | –10.2 | – | dBm |
| 1710–1785 MHz | GSM1800 | – | –15.8 | – | dBm |
| 1710–1785 MHz | WCDMA | – | –15.4 | – | dBm |
| 1850–1910 MHz | GSM1900 | – | –16.6 | – | dBm |
| 1850–1910 MHz | WCDMA | – | –16.4 | – | dBm |
| 1880–1920 MHz | TD-SCDMA | – | –17.9 | – | dBm |
| 1920–1980 MHz | WCDMA | – | –16.8 | – | dBm |
| 2010–2025 MHz | TD-SCDMA | – | –18.6 | – | dBm |
| 2500–2570 MHz | WCDMA | – | –20.4 | – | dBm |
| 2500–2570 MHz ^c | Band 7 | – | –31.9 | – | dBm |
| 2300–2400 MHz ^d | Band 40 | – | –35.3 | – | dBm |
| 2570–2620 MHz ^e | Band 38 | – | –31.8 | – | dBm |
| 2545–2575 MHz ^f | XGP Band | – | –31.1 | – | dBm |
| 8DPSK (3 Mbps)^b | | | | | |
| 698–716 MHz | WCDMA | – | –12.6 | – | dBm |
| 776–794 MHz | WCDMA | – | –12.6 | – | dBm |
| 824–849 MHz | GSM850 | – | –12.7 | – | dBm |
| 824–849 MHz | WCDMA | – | –13.7 | – | dBm |
| 880–915 MHz | E-GSM | – | –12.8 | – | dBm |
| 880–915 MHz | WCDMA | – | –12.6 | – | dBm |
| 1710–1785 MHz | GSM1800 | – | –18.1 | – | dBm |
| 1710–1785 MHz | WCDMA | – | –17.4 | – | dBm |
| 1850–1910 MHz | GSM1900 | – | –19.1 | – | dBm |
| 1850–1910 MHz | WCDMA | – | –18.6 | – | dBm |
| 1880–1920 MHz | TD-SCDMA | – | –19.3 | – | dBm |
| 1920–1980 MHz | WCDMA | – | –18.9 | – | dBm |
| 2010–2025 MHz | TD-SCDMA | – | –20.4 | – | dBm |
| 2500–2570 MHz | WCDMA | – | –21.4 | – | dBm |

Table 34. Bluetooth Receiver RF Specifications (Cont.)

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------------------|------------|---------|---------|---------|--------|
| 2500–2570 MHz ^c | Band 7 | – | –31.0 | – | dBm |
| 2300–2400 MHz ^d | Band 40 | – | –34.5 | – | dBm |
| 2570–2620 MHz ^e | Band 38 | – | –31.2 | – | dBm |
| 2545–2575 MHz ^f | XGP Band | – | –30.0 | – | dBm |
| Spurious Emissions | | | | | |
| 30 MHz–1 GHz | | – | –95 | –62 | dBm |
| 1–12.75 GHz | | – | –70 | –47 | dBm |
| 851–894 MHz | | – | –147 | – | dBm/Hz |
| 925–960 MHz | | – | –147 | – | dBm/Hz |
| 1805–1880 MHz | | – | –147 | – | dBm/Hz |
| 1930–1990 MHz | | – | –147 | – | dBm/Hz |
| 2110–2170 MHz | | – | –147 | – | dBm/Hz |

- a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.
- b. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = at 3 dB desense for each data rate.
- c. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
- d. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
- e. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
- f. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.

Table 35. Bluetooth Transmitter RF Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--|--|---------|---------|------------------------|--------|
| Note: The specifications in this table are measured at the Chip port output unless otherwise specified. | | | | | |
| General | | | | | |
| Frequency range | | 2402 | – | 2480 | MHz |
| Basic rate (GFSK) TX power at Bluetooth | | – | 13.0 | – | dBm |
| QPSK TX power at Bluetooth | | – | 10.0 | – | dBm |
| 8PSK TX power at Bluetooth | | – | 10.0 | – | dBm |
| Power control step | – | 2 | 4 | 8 | dB |
| Note: Output power is with TCA and TSSI enabled. | | | | | |
| GFSK In-Band Spurious Emissions | | | | | |
| –20 dBc BW | – | – | 0.93 | 1 | MHz |
| EDR In-Band Spurious Emissions | | | | | |
| 1.0 MHz < M – N < 1.5 MHz | M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency. | – | –38 | –26.0 | dBc |
| 1.5 MHz < M – N < 2.5 MHz | | – | –31 | –20.0 | dBm |
| M – N ≥ 2.5 MHz ^a | | – | –43 | –40.0 | dBm |
| Out-of-Band Spurious Emissions | | | | | |
| 30 MHz to 1 GHz | – | – | – | –36.0 ^{b,c} | dBm |
| 1 GHz to 12.75 GHz | – | – | – | –30.0 ^{b,d,e} | dBm |
| 1.8 GHz to 1.9 GHz | – | – | – | –47.0 | dBm |
| 5.15 GHz to 5.3 GHz | – | – | – | –47.0 | dBm |
| GPS Band Spurious Emissions | | | | | |
| Spurious emissions | – | – | –103 | – | dBm |
| Out-of-Band Noise Floor^f | | | | | |
| 65–108 MHz | FM RX | – | –147 | – | dBm/Hz |
| 776–794 MHz | CDMA2000 | – | –147 | – | dBm/Hz |
| 869–960 MHz | cdmaOne, GSM850 | – | –147 | – | dBm/Hz |
| 925–960 MHz | E-GSM | – | –147 | – | dBm/Hz |
| 1570–1580 MHz | GPS | – | –146 | – | dBm/Hz |
| 1805–1880 MHz | GSM1800 | – | –145 | – | dBm/Hz |
| 1930–1990 MHz | GSM1900, cdmaOne, WCDMA | – | –144 | – | dBm/Hz |
| 2110–2170 MHz | WCDMA | – | –141 | – | dBm/Hz |
| 2500–2570 MHz | Band 7 | – | –140 | – | dBm |
| 2300–2400 MHz | Band 40 | – | –140 | – | dBm |
| 2570–2620 MHz | Band 38 | – | –140 | – | dBm |
| 2545–2575 MHz | XGP Band | – | –140 | – | dBm |

- a. The typical number is measured at ± 3 MHz offset.
- b. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.
- c. The spurious emissions during Idle mode are the same as specified in [Table 35 on page 110](#).
- d. Specified at the Bluetooth Antenna port.
- e. Meets this specification using a front–end band–pass filter.
- f. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See [Figure 35 on page 106](#) for location of the port.

Table 36. Local Oscillator Performance

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---------|---------|---------|-----------|
| LO Performance | | | | |
| Lock time | – | 72 | – | μs |
| Initial carrier frequency tolerance | – | ±25 | ±75 | kHz |
| Frequency Drift | | | | |
| DH1 packet | – | ±8 | ±25 | kHz |
| DH3 packet | – | ±8 | ±40 | kHz |
| DH5 packet | – | ±8 | ±40 | kHz |
| Drift rate | – | 5 | 20 | kHz/50 μs |
| Frequency Deviation | | | | |
| 00001111 sequence in payload ^a | 140 | 155 | 175 | kHz |
| 10101010 sequence in payload ^b | 115 | 140 | – | kHz |
| Channel spacing | – | 1 | – | MHz |

- a. This pattern represents an average deviation in payload.
- b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 37. BLE RF Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--------------------------------------|------------------------|---------|---------|---------|------|
| Frequency range | – | 2402 | – | 2480 | MHz |
| RX sense ^a | GFSK, 0.1% BER, 1 Mbps | – | –95.5 | – | dBm |
| TX power ^b | – | – | 8.5 | – | dBm |
| Mod Char: delta F1 average | – | 225 | 255 | 275 | kHz |
| Mod Char: delta F2 max. ^c | – | 99.9 | – | – | % |
| Mod Char: ratio | – | 0.8 | 0.95 | – | % |

- a. Dirty TX is On.
- b. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm out. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.
- c. At least 99.9% of all delta F2 max. frequency values recorded over 10 packets must be greater than 185 kHz.

16. FM Receiver Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 31 on page 103](#) and [Table 33 on page 104](#). Typical values apply for an ambient temperature +25°C.

Table 38. FM Receiver Specifications

| Parameter | Conditions ^a | Minimum | Typical | Maximum | Units |
|--|--|---------|---------|---------|----------|
| RF Parameters | | | | | |
| Operating frequency ^b | Frequencies inclusive | 65 | – | 108 | MHz |
| Sensitivity ^c | FM only SNR ≥ 26 dB | – | 0 | – | dBμV EMF |
| | | – | 1 | – | μV EMF |
| | | – | –6 | – | dBuV |
| Receiver adjacent channel selectivity ^{c,d} | Measured for 30 dB SNR at the audio output. Wanted Signal: 23 dBμV EMF (14.1 μV EMF), at ± 200 kHz. | – | 51 | – | dB |
| | At ± 400 kHz | – | 62 | – | dB |
| Intermediate signal plus noise-to-noise ratio (S+N)/N, stereo ^c | Vin = 20 dBμV EMF (10 μV EMF) | 45 | 53 | – | dB |
| Intermodulation performance ^{c,d} | Blocker level increased until desired at 30 dB SNR Wanted Signal: 33 dBμV EMF (45 μV EMF) Modulated Interferer: At f _{Wanted} ±400 kHz and ±4 MHz CW Interferer: At f _{Wanted} ± 800 kHz and ±8 MHz | – | 55 | – | dBc |
| AM suppression, mono ^c | Vin = 23 dBμV EMF (14.1 μV EMF) AM at 400 Hz with m = 0.3 No A-weighted or any other filtering applied. | 40 | – | – | dB |
| RDS | | | | | |
| RDS sensitivity ^{e,f} | RDS deviation = 1.2 kHz | – | 16 | – | dBμV EMF |
| | | – | 6.3 | – | μV EMF |
| | | – | 10 | – | dBuV |
| | RDS deviation = 2 kHz | – | 12 | – | dBμV EMF |
| | | – | 4 | – | μV EMF |
| | | – | 6 | – | dBuV |
| RDS selectivity ^f | Wanted Signal: 33 dBμV EMF (45 μV EMF), 2 kHz RDS deviation Interferer: Δf = 40 kHz, f _{mod} = 1 kHz | | | | |
| | ± 200 kHz | – | 49 | – | dB |
| | ± 300 kHz | – | 52 | – | dB |
| | ± 400 kHz | – | 52 | – | dB |
| RF input impedance | – | 1.5 | – | – | kΩ |
| Antenna tuning capacitor | – | 2.5 | – | 30 | pF |
| Maximum input level ^c | SNR > 26 dB | – | – | 113 | dBμV EMF |
| | | – | – | 446 | mV EMF |
| | | – | – | 107 | dBuV |

Table 38. FM Receiver Specifications (Cont.)

| Parameter | Conditions ^a | Minimum | Typical | Maximum | Units |
|--|---|---------|---------|---------|-------|
| RF conducted emissions (measured into a 50Ω load) | Local oscillator breakthrough measured on the reference port | – | – | –55 | dBm |
| | 869–894 MHz, 925–960 MHz, 1805–1880 MHz, 1930–1990 MHz. GPS | – | – | –90 | dBm |
| RF blocking levels at the FM antenna input 40 dB SNR (assumes a 50Ω at the radio input and excludes spurs) | GSM850, E-GSM (std), BW = 0.2 MHz, 824–849 MHz 880–915 MHz | – | 7 | – | dBm |
| | GSM850, E-GSM (edge), BW = 0.2 MHz, 824–849 MHz 880–915 MHz | – | –1 | – | dBm |
| | GSM DCS 1800, PCS 1900 (std/edge), BW = 0.2 MHz, 1710–1785 MHz 1850–1910 MHz | – | 12 | – | dBm |
| | WCDMA: II(I), III(IV, X), BW = 5 MHz, 1850–1980 MHz (1920–1980 MHz), 1710–1785 MHz (1710–1755 MHz, 1710–1770 MHz) | – | 12 | – | dBm |
| | WCDMA: V(VI), VIII, XII, XIII, XIV, BW = 5 MHz, 824–849 MHz (830–840 MHz), 880–915 MHz | – | 5 | – | dBm |
| | CDMA2000, cdmaOne, BW = 1.25 MHz, 824–849 MHz, 887–925 MHz, 776–794 MHz | – | 0 | – | dBm |
| | CDMA2000, cdmaOne, BW = 1.25 MHz, 1850–1910 MHz, 1750–1780 MHz, 1920–1980 MHz | – | 12 | – | dBm |
| | Bluetooth, BW = 1 MHz, 2402–2480 MHz | – | 11 | – | dBm |
| | IEEE 802.11g/b, BW = 20 MHz, 2400–2483.5 MHz | – | 11 | – | dBm |
| | IEEE 802.11a, BW = 20 MHz, 4915–5825 MHz | – | 6 | – | dBm |
| 2500–2570 MHz | Band 7 | – | 11 | – | dBm |
| 2300–2400 MHz | Band 40 | – | 11 | – | dBm |
| 2570–2620 MHz | Band 38 | – | 11 | – | dBm |
| 2545–2575 MHz | XGP Band | – | 11 | – | dBm |
| Tuning | | | | | |
| Frequency step | – | 10 | – | – | kHz |
| Settling time | Single-frequency switch in any direction to a frequency within the bands 88–108 MHz or 76–90 MHz. Time measured to within 5 kHz of the final frequency. | – | 150 | – | μs |
| Search time | Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (and reverse direction) assuming no channels are found. | – | – | 8 | sec |

Table 38. FM Receiver Specifications (Cont.)

| Parameter | Conditions ^a | Minimum | Typical | Maximum | Units |
|---|--|---------|---------|---------|----------------|
| General Audio | | | | | |
| Audio output level ^g | – | –14.5 | – | –12.5 | dBFS |
| Maximum audio output level ^h | – | – | – | 0 | dBFS |
| Audio DAC output level ^g | – | 72 | – | 88 | mV rms |
| Maximum DAC audio output level ^h | – | – | 333 | – | mV rms |
| Audio DAC output level difference ⁱ | – | –1 | – | 1 | dB |
| Left and right AC mute | FM input signal fully muted with DAC enabled | 60 | – | – | dB |
| Left and right hard mute | FM input signal fully muted with DAC disabled | 80 | – | – | dB |
| Soft mute attenuation and start level | Muting is performed dynamically proportional to the FM wanted input signal C/N. The muting characteristic is fully programmable. Refer to “Audio Features” on page 45 for further details. | – | – | – | – |
| Maximum signal plus noise-to-noise ratio (S + N)/N, mono ⁱ | – | – | 69 | – | dB |
| Maximum signal plus noise-to-noise ratio (S + N)/N, stereo ^g | – | – | 64 | – | dB |
| Total harmonic distortion, mono | Vin = 66 dB μ V EMF (2 mV EMF), Δ f = 75 kHz, fmod = 400 Hz | – | – | 0.8 | % |
| | Δ f = 75 kHz, fmod = 1 kHz | – | – | 0.8 | % |
| | Δ f = 75 kHz, fmod = 3 kHz | – | – | 0.8 | % |
| | Δ f = 100 kHz, fmod = 1 kHz | – | – | 1.0 | % |
| Total harmonic distortion, stereo | Vin = 66 dB μ V EMF (2 mV EMF) Δ f = 67.5 kHz, fmod = 1 kHz, Δ f Pilot = 7.5 kHz, L = R | – | – | 1.5 | % |
| Audio spurious products ⁱ | Range from 300 Hz to 15 kHz, with respect to 1 kHz tone | – | – | –60 | dBc |
| Audio bandwidth, upper (–3 dB point) | Vin = 66 dB μ V EMF (2 mV EMF) Δ f = 8 kHz, for 50 μ s | 15 | – | – | kHz |
| Audio bandwidth, lower (–3 dB point) | | – | – | 20 | Hz |
| Audio in-band ripple | 100 Hz to 13 kHz, Vin = 66 dB μ V EMF (2 mV EMF) Δ f = 8 kHz, for 50 μ s | –0.5 | – | 0.5 | dB |
| De-emphasis time constant tolerance | With respect to 50 and 75 μ s | – | – | \pm 5 | % |
| RSSI range | With 1 dB resolution and \pm 5 dB accuracy at room temp | 3 | – | 83 | dB μ V EMF |
| | | 1.41 | – | 14.1m | μ V EMF |
| | | –3 | – | 77 | dBuV |
| Stereo Decoder | | | | | |
| Stereo channel separation | Forced Stereo mode Vin = 66 dB μ V EMF (2 mV EMF), Δ f = 67.5 kHz, fmod = 1 kHz, Δ f Pilot = 6.75 kHz R = 0, L = 1 | – | 48 | – | dB |

Table 38. FM Receiver Specifications (Cont.)

| Parameter | Conditions ^a | Minimum | Typical | Maximum | Units |
|--|--|---------|---------|---------|-------|
| Mono stereo blend and switching | Blending and switching is dynamically proportional to the FM wanted input signal C/N. The blending and switching characteristics are fully programmable. Refer to "Audio Features" on page 45 for further details. | | | | |
| Pilot suppression | Vin = 66 dBμV EMF (2 mV EMF), Δf = 75 kHz, fmod = 1 kHz | 46 | – | – | dB |
| Pause detection | | | | | |
| Audio level at which a pause is detected | Relative to 1 kHz tone, Δf = 22.5 kHz | – | – | – | – |
| | Four values in 3 dB steps | –21 | – | –12 | dB |
| Audio pause duration | Four values | 20 | – | 40 | ms |

- a. Following conditions are applied to all relevant tests unless otherwise indicated: Pre-emphasis and de-emphasis of 50 us, R = L for mono, DAC Load ≥ 20 kΩ, BAF = 300 Hz to 15 kHz, and A-weighted filtering applied.
- b. Contact Broadcom regarding applications that operate between 65 and 76 MHz.
- c. Wanted Signal: Δf = 22.5 kHz, and fmod = 1 kHz.
- d. Interferer: Δf = 22.5 kHz, and fmod = 1 kHz.
- e. RDS sensitivity numbers are for 87.5–108 MHz only.
- f. Vin = Δf = 32 kHz, fmod = 1 kHz, Δf Pilot = 7.5 kHz, and 95% of blocks decoded with no errors after correction.
- g. Vin = 66 dBμV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, and Δf Pilot = 6.75 kHz.
- h. Vin = 66 dBμV EMF (2 mV EMF), Δf = 100 kHz, fmod = 1 kHz, and Δf Pilot = 6.75 kHz.
- i. Vin = 66 dBμV EMF (2 mV EMF), Δf = 22.5 kHz, and fmod = 1 kHz.

17. WLAN RF Specifications

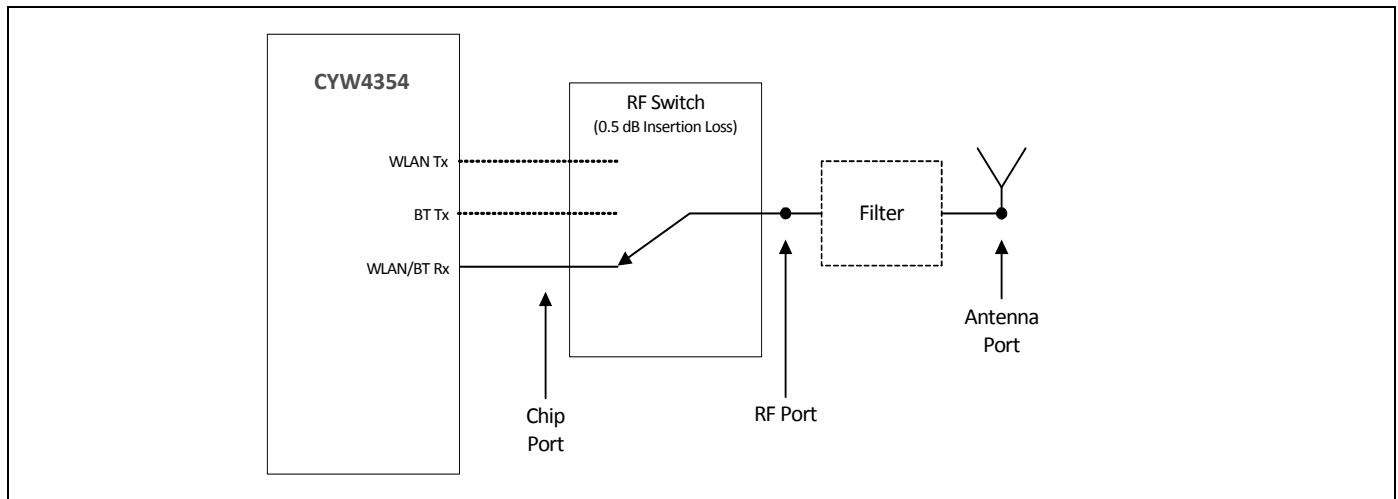
17.1 Introduction

The CYW4354 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

Note: Values in this section of the data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 31 on page 103](#) and [Table 33 on page 104](#). Typical values apply for an ambient temperature +25°C.

Figure 36. Port Locations (Applies to 2.4 GHz and 5 GHz)



17.2 2.4 GHz Band General RF Specifications

Table 39. 2.4 GHz Band General RF Specifications

| Item | Condition | Minimum | Typical | Maximum | Unit |
|-----------------------------------|------------------------|---------|---------|---------|------|
| TX/RX switch time | Including TX ramp down | – | – | 5 | μs |
| RX/TX switch time | Including TX ramp up | – | – | 2 | μs |
| Power-up and power-down ramp time | DSSS/CCK modulations | – | – | < 2 | μs |

17.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The values in Table 40 are specified at the RF port unless otherwise noted.

Table 40. WLAN 2.4 GHz Receiver Performance Specifications

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|---|--|------|-------|------|----------|
| Frequency range | – | 2400 | – | 2500 | MHz |
| RX sensitivity IEEE 802.11b ^a | 1 Mbps DSSS | – | –96.4 | – | dBm |
| | 2 Mbps DSSS | – | –94.5 | – | dBm |
| | 5.5 Mbps DSSS | – | –91.7 | – | dBm |
| | 11 Mbps DSSS | – | –89.4 | – | dBm |
| SISO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU) ^a | 6 Mbps OFDM | – | –93.5 | – | dBm |
| | 9 Mbps OFDM | – | –92.1 | – | dBm |
| | 12 Mbps OFDM | – | –91.2 | – | dBm |
| | 18 Mbps OFDM | – | –88.6 | – | dBm |
| | 24 Mbps OFDM | – | –85.3 | – | dBm |
| | 36 Mbps OFDM | – | –82 | – | dBm |
| | 48 Mbps OFDM | – | –77.3 | – | dBm |
| | 54 Mbps OFDM | – | –75.8 | – | dBm |
| MIMO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU) ^a | 6 Mbps OFDM | – | –94.5 | – | dBm/core |
| | 9 Mbps OFDM | – | –94 | – | dBm/core |
| | 12 Mbps OFDM | – | –93.2 | – | dBm/core |
| | 18 Mbps OFDM | – | –91.6 | – | dBm/core |
| | 24 Mbps OFDM | – | –88.3 | – | dBm/core |
| | 36 Mbps OFDM | – | –85 | – | dBm/core |
| | 48 Mbps OFDM | – | –80.3 | – | dBm/core |
| | 54 Mbps OFDM | – | –78.8 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –93 | – | dBm |
| | MCS1 | – | –90.7 | – | dBm |
| | MCS2 | – | –88.2 | – | dBm |
| | MCS3 | – | –85.1 | – | dBm |
| | MCS4 | – | –81.5 | – | dBm |
| | MCS5 | – | –76.9 | – | dBm |
| | MCS6 | – | –75.3 | – | dBm |
| | MCS7 | – | –73.7 | – | dBm |

Table 40. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|--|--|------|-------|------|----------|
| MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –94.5 | – | dBm/core |
| | MCS1 | – | –93.7 | – | dBm/core |
| | MCS2 | – | –91.2 | – | dBm/core |
| | MCS3 | – | –88.1 | – | dBm/core |
| | MCS4 | – | –84.5 | – | dBm/core |
| | MCS5 | – | –79.9 | – | dBm/core |
| | MCS6 | – | –78.3 | – | dBm/core |
| | MCS7 | – | –76.7 | – | dBm/core |
| | MCS8 | – | –93 | – | dBm/core |
| | MCS15 | – | –73.7 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –90.8 | – | dBm |
| | MCS1 | – | –87.9 | – | dBm |
| | MCS2 | – | –85.5 | – | dBm |
| | MCS3 | – | –82 | – | dBm |
| | MCS4 | – | –78.9 | – | dBm |
| | MCS5 | – | –74.2 | – | dBm |
| | MCS6 | – | –72.7 | – | dBm |
| | MCS7 | – | –71.3 | – | dBm |
| MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –92.3 | – | dBm/core |
| | MCS1 | – | –90.9 | – | dBm/core |
| | MCS2 | – | –88.5 | – | dBm/core |
| | MCS3 | – | –85 | – | dBm/core |
| | MCS4 | – | –81.9 | – | dBm/core |
| | MCS5 | – | –77.2 | – | dBm/core |
| | MCS6 | – | –75.7 | – | dBm/core |
| | MCS7 | – | –74.3 | – | dBm/core |
| | MCS8 | – | –90.8 | – | dBm/core |
| | MCS15 | – | –71.3 | – | dBm/core |

Table 40. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|--|--|-------|-------|------|----------|
| SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –92.3 | – | dBm |
| | MCS1, Nss 1 | – | –89.9 | – | dBm |
| | MCS2, Nss 1 | – | –88.1 | – | dBm |
| | MCS3, Nss 1 | – | –84.9 | – | dBm |
| | MCS4, Nss 1 | – | –81.4 | – | dBm |
| | MCS5, Nss 1 | – | –76.9 | – | dBm |
| | MCS6, Nss 1 | – | –75.3 | – | dBm |
| | MCS7, Nss 1 | – | –73.6 | – | dBm |
| | MCS8, Nss 1 | – | –69.2 | – | dBm |
| MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –93.8 | – | dBm/core |
| | MCS1, Nss 1 | – | –92.9 | – | dBm/core |
| | MCS2, Nss 1 | – | –91.1 | – | dBm/core |
| | MCS3, Nss 1 | – | –87.9 | – | dBm/core |
| | MCS4, Nss 1 | – | –84.4 | – | dBm/core |
| | MCS5, Nss 1 | – | –79.9 | – | dBm/core |
| | MCS6, Nss 1 | – | –78.3 | – | dBm/core |
| | MCS7, Nss 1 | – | –76.6 | – | dBm/core |
| | MCS8, Nss 1 | – | –72.2 | – | dBm/core |
| | MCS0, Nss 2 | – | –92 | – | dBm/core |
| | MCS8, Nss 2 | – | –68.1 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –89.5 | – | dBm |
| | MCS1, Nss 1 | – | –87 | – | dBm |
| | MCS2, Nss 1 | – | –85.2 | – | dBm |
| | MCS3, Nss 1 | – | –82 | – | dBm |
| | MCS4, Nss 1 | – | –78.8 | – | dBm |
| | MCS5, Nss 1 | – | –74.3 | – | dBm |
| | MCS6, Nss 1 | – | –72.7 | – | dBm |
| | MCS7, Nss 1 | – | –71.3 | – | dBm |
| | MCS8, Nss 1 | – | –66.9 | – | dBm |
| MCS9, Nss 1 | – | –65.6 | – | dBm | |

Table 40. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|---|--|----------|-------|-------|----------|----------|
| MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | | |
| | MCS0, Nss 1 | | – | –91 | – | dBm/core |
| | MCS1, Nss 1 | | – | –90 | – | dBm/core |
| | MCS2, Nss 1 | | – | –88.2 | – | dBm/core |
| | MCS3, Nss 1 | | – | –85 | – | dBm/core |
| | MCS4, Nss 1 | | – | –81.8 | – | dBm/core |
| | MCS5, Nss 1 | | – | –77.3 | – | dBm/core |
| | MCS6, Nss 1 | | – | –75.7 | – | dBm/core |
| | MCS7, Nss 1 | | – | –74.3 | – | dBm/core |
| | MCS8, Nss 1 | | – | –69.9 | – | dBm/core |
| | MCS9, Nss 1 | | – | –68.6 | – | dBm/core |
| | MCS0, Nss 2 | | – | –89 | – | dBm/core |
| MCS9, Nss 2 | | – | –64.2 | – | dBm/core | |
| SISO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) ^{a,b} at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC. | MCS7, Nss 1 | 20 MHz | – | –75.4 | – | dBm |
| | MCS8, Nss 1 | 20 MHz | – | –72.7 | – | dBm |
| | MCS9, Nss 1 | 20 MHz | – | –69.4 | – | dBm |
| | MCS7, Nss 1 | 40 MHz | – | –72.8 | – | dBm |
| | MCS8, Nss 1 | 40 MHz | – | –68.5 | – | dBm |
| | MCS9, Nss 1 | 40 MHz | – | –67.3 | – | dBm |
| MIMO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) ^{a,b} at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC. | MCS7, Nss 2 | 20 MHz | – | –74 | – | dBm/core |
| | MCS8, Nss 2 | 20 MHz | – | –71.2 | – | dBm/core |
| | MCS9, Nss 2 | 20 MHz | – | –68.0 | – | dBm/core |
| | MCS7, Nss 2 | 40 MHz | – | –71.8 | – | dBm/core |
| | MCS8, Nss 2 | 40 MHz | – | –67 | – | dBm/core |
| | MCS9, Nss 2 | 40 MHz | – | –65.5 | – | dBm/core |
| Blocking level for 3dB RX sensitivity degradation (without external filtering) ^c | 776–794 MHz | CDMA2000 | –8 | –24 | – | dBm |
| | 824–849 MHz ^d | cdmaOne | –24.5 | –25 | – | dBm |
| | 824–849 MHz ^d | GSM850 | –16.5 | –15 | – | dBm |
| | 880–915 MHz | E-GSM | –2 | –16 | – | dBm |
| | 1710–1785 MHz | GSM1800 | –17 | –18 | – | dBm |
| | 1850–1910 MHz | GSM1800 | –21 | –19 | – | dBm |
| | 1850–1910 MHz | cdmaOne | –32 | –26 | – | dBm |
| | 1850–1910 MHz | WCDMA | –29 | –26 | – | dBm |
| | 1920–1980 MHz | WCDMA | –32 | –28.5 | – | dBm |
| | 2500–2570 MHz | Band 7 | –45 | –45 | – | dBm |
| | 2300–2400 MHz | Band 40 | –50 | –50 | – | dBm |
| | 2570–2620 MHz | Band 38 | –45 | –45 | – | dBm |
| 2545–2575 MHz | XGP band | –45 | –45 | – | dBm | |

Table 40. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit | |
|--|--|---------|-------|------|------|----|
| In-band static CW jammer immunity ($f_c - 8 \text{ MHz} < f_{cw} < + 8 \text{ MHz}$) | RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSense + 23 dB < Rxlevel < max. input level) | -80 | - | - | dBm | |
| Input In-Band IP3 | Maximum LNA gain | - | -15.5 | - | dBm | |
| | Minimum LNA gain | - | -1.5 | - | dBm | |
| Maximum Receive Level @ 2.4 GHz | @ 1, 2 Mbps (8% PER, 1024 octets) | -3.5 | - | - | dBm | |
| | @ 5.5, 11 Mbps (8% PER, 1024 octets) | -9.5 | - | - | dBm | |
| | @ 6-54 Mbps (10% PER, 1024 octets) | -9.5 | - | - | dBm | |
| | @ MCS0-7 rates (10% PER, 4095 octets) | -9.5 | - | - | dBm | |
| | @ MCS8-9 rates (10% PER, 4095 octets) | -11.5 | - | - | dBm | |
| LPF 3 dB Bandwidth | - | 9 | - | 36 | MHz | |
| Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes) | Desired and interfering signal 30 MHz apart | | | | | |
| | 1 Mbps DSSS | -74 dBm | 35 | - | - | dB |
| | 2 Mbps DSSS | -74 dBm | 35 | - | - | dB |
| | Desired and interfering signal 25 MHz apart | | | | | |
| | 5.5 Mbps DSSS | -70 dBm | 35 | - | - | dB |
| Adjacent channel rejection-OFDM (difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes) | 6 Mbps OFDM | -79 dBm | 16 | - | - | dB |
| | 9 Mbps OFDM | -78 dBm | 15 | - | - | dB |
| | 12 Mbps OFDM | -76 dBm | 13 | - | - | dB |
| | 18 Mbps OFDM | -74 dBm | 11 | - | - | dB |
| | 24 Mbps OFDM | -71 dBm | 8 | - | - | dB |
| | 36 Mbps OFDM | -67 dBm | 4 | - | - | dB |
| | 48 Mbps OFDM | -63 dBm | 0 | - | - | dB |
| | 54 Mbps OFDM | -62 dBm | -1 | - | - | dB |
| Adjacent channel rejection MCS0-9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes) | MCS0 | -79 dBm | 16 | - | - | dB |
| | MCS1 | -76 dBm | 13 | - | - | dB |
| | MCS2 | -74 dBm | 11 | - | - | dB |
| | MCS3 | -71 dBm | 8 | - | - | dB |
| | MCS4 | -67 dBm | 4 | - | - | dB |
| | MCS5 | -63 dBm | 0 | - | - | dB |
| | MCS6 | -62 dBm | -1 | - | - | dB |
| | MCS7 | -61 dBm | -2 | - | - | dB |
| | MCS8 | -59 dBm | -4 | - | - | dB |
| | MCS9 | -57 dBm | -6 | - | - | dB |

Table 40. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|--|------------------------------------|---------|------|------|------|---------|
| IEEE 802.11ac Adjacent channel rejection MCS0–9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes) | MCS0 | –82 dBm | – | – | – | dB |
| | MCS1 | –80 dBm | – | – | – | dB |
| | MCS2 | –77 dBm | – | – | – | dB |
| | MCS3 | –74 dBm | – | – | – | dB |
| | MCS4 | –70 dBm | – | – | – | dB |
| | MCS5 | –66 dBm | – | – | – | dB |
| | MCS6 | –65 dBm | – | – | – | dB |
| | MCS7 | –64 dBm | – | – | – | dB |
| | MCS8 | –59 dBm | – | – | – | dB |
| | MCS9 | –57 dBm | – | – | – | dB |
| Maximum receiver gain | – | – | – | 95 | – | dB |
| Gain control step | – | – | – | 3 | – | dB |
| RSSI accuracy ^e | Range –90 dBm to –30 dBm | | –5 | – | 5 | dB |
| | Range above –30 dBm | | –8 | – | 8 | dB |
| Return loss | Zo = 50Ω, across the dynamic range | | 10 | 11.5 | 13 | dB |
| Receiver cascaded noise figure | At maximum gain | | – | 4 | – | dB |
| General spurs | 1–18 GHz | – | – | – | –60 | dBm/MHz |

- a. Derate by 1.5 dB for 55°C to 70°C.
- b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
- c. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- d. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
- e. The minimum and maximum values shown have a 95% confidence level.

17.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: The values in Table 41 are specified at the RF port unless otherwise noted.

Table 41. WLAN 2.4 GHz Transmitter Performance Specifications

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|--|--|---------------------------|------|------|--------|---------|
| Frequency range Transmitted power in cellular and FM bands at 18 dBm, 100% duty cycle, 1 Mbps CCK ^a | – | | 2400 | – | 2500 | MHz |
| | 76-108 MHz | FM RX | – | –149 | – | dBm/Hz |
| | 776-794 MHz | | – | –162 | – | dBm/Hz |
| | 869-960 MHz | cdmaOne, GSM850 | – | –162 | – | dBm/Hz |
| | 925-960 MHz | E-GSM | – | –162 | – | dBm/Hz |
| | 1570-1580 MHz | GPS | – | –152 | – | dBm/Hz |
| | 1805-1880 MHz | GSM1800 | – | –142 | – | dBm/Hz |
| | 1930-1990 MHz | GSM1900, cdmaOne, cdmaOne | – | –143 | – | dBm/Hz |
| | 2110-2170 MHz | WCDMA | – | –128 | – | dBm/Hz |
| | 2500-2570 MHz | Band 7 | – | –92 | – | dBm/Hz |
| | 2300-2400 MHz | Band 40 | – | –95 | – | dBm/Hz |
| | 2570-2620 MHz | Band 38 | – | –110 | – | dBm/Hz |
| 2545-2575 MHz | XGP Band | – | –110 | – | dBm/Hz | |
| Harmonic level (at 18 dBm with 100% duty cycle) | 4.8-5.0 GHz | 2 nd harmonic | – | –18 | – | dBm/Hz |
| | 7.2-7.5 GHz | 3 rd harmonic | – | –20 | – | dBm/Hz |
| General spurs (at 18 dBm with 100% duty cycle) | 1–18 GHz | – | – | – | –60 | dBm/MHz |
| – | EVM Does Not Exceed | | | | | |
| TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance ^b | 802.11b (DSSS/CCK) | –9 dB | 18 | 19.5 | – | dBm |
| | OFDM, BPSK | –8 dB | 18 | 19 | – | dBm |
| | OFDM, QPSK | –13 dB | 18 | 19 | – | dBm |
| | OFDM, 16-QAM | –19 dB | 16.5 | 18 | – | dBm |
| | OFDM, 64-QAM (R = 3/4) | –25 dB | 15.5 | 17 | – | dBm |
| | OFDM, 64-QAM (R = 5/6) | –28 dB | 14.5 | 16 | – | dBm |
| | OFDM, 256-QAM (R = 3/4, VHT20) | –30 dB | 13.5 | 15 | – | dBm |
| | OFDM, 256-QAM (R = 5/6, VHT20) | –32 dB | 12 | 13.5 | – | dBm |
| Phase noise | 37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz | | – | 0.45 | – | Degrees |
| TX power control dynamic range | – | | 10 | – | – | dB |
| Closed-loop TX power variation at highest power level setting | Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range. | | – | – | ±1.5 | dB |
| Carrier suppression | – | | 15 | – | – | dBc |

Table 41. WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|-----------------------------|----------------------|------|------|------|------|
| Gain control step | – | – | 0.25 | – | dB |
| Return loss at chip port TX | Z _o = 50Ω | – | 6 | – | dB |

- a. The cellular standards listed only indicate the typical usages of that band in some countries: other standards may also be used within those bands
- b. Derate by 1.5 dB for temperatures higher than 55°C, or supply voltages lower than 3.0V. Derate by 3.0 dB for supply voltages of lower than 2.7V, or supply voltages lower than 3.0V at temperatures higher than 55°C.

17.5 WLAN 5 GHz Receiver Performance Specifications

Note: The values in Table 42 on page 124 are specified at the RF port unless otherwise noted.

Table 42. WLAN 5 GHz Receiver Performance Specifications

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|---|--|------|-------|------|----------|
| Frequency range | – | 4900 | – | 5845 | MHz |
| SISO RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU) ^a | 6 Mbps OFDM | – | –92.5 | – | dBm |
| | 9 Mbps OFDM | – | –91.1 | – | dBm |
| | 12 Mbps OFDM | – | –90.2 | – | dBm |
| | 18 Mbps OFDM | – | –87.6 | – | dBm |
| | 24 Mbps OFDM | – | –84.3 | – | dBm |
| | 36 Mbps OFDM | – | –81 | – | dBm |
| | 48 Mbps OFDM | – | –76.3 | – | dBm |
| | 54 Mbps OFDM | – | –74.8 | – | dBm |
| MIMO RX sensitivity IEEE 802.11a (10% PER for 1024 octet PSDU) ^{a,b} | 6 Mbps OFDM | – | –93.5 | – | dBm/core |
| | 9 Mbps OFDM | – | –93 | – | dBm/core |
| | 12 Mbps OFDM | – | –92.2 | – | dBm/core |
| | 18 Mbps OFDM | – | –90.6 | – | dBm/core |
| | 24 Mbps OFDM | – | –87.3 | – | dBm/core |
| | 36 Mbps OFDM | – | –84 | – | dBm/core |
| | 48 Mbps OFDM | – | –79.3 | – | dBm/core |
| | 54 Mbps OFDM | – | –75.8 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –92 | – | dBm |
| | MCS1 | – | –89.7 | – | dBm |
| | MCS2 | – | –87.2 | – | dBm |
| | MCS3 | – | –84.1 | – | dBm |
| | MCS4 | – | –80.5 | – | dBm |
| | MCS5 | – | –75.9 | – | dBm |
| | MCS6 | – | –74.3 | – | dBm |
| | MCS7 | – | –72.7 | – | dBm |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|---|--|-------|-------|----------|----------|
| MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –93.5 | – | dBm/core |
| | MCS1 | – | –92.7 | – | dBm/core |
| | MCS2 | – | –90.2 | – | dBm/core |
| | MCS3 | – | –87.1 | – | dBm/core |
| | MCS4 | – | –83.5 | – | dBm/core |
| | MCS5 | – | –78.9 | – | dBm/core |
| | MCS6 | – | –77.3 | – | dBm/core |
| | MCS7 | – | –75.7 | – | dBm/core |
| | MCS8 | – | –92 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –89.8 | – | dBm |
| | MCS1 | – | –86.9 | – | dBm |
| | MCS2 | – | –84.5 | – | dBm |
| | MCS3 | – | –81 | – | dBm |
| | MCS4 | – | –77.9 | – | dBm |
| | MCS5 | – | –73.2 | – | dBm |
| | MCS6 | – | –71.7 | – | dBm |
| | MCS7 | – | –70.3 | – | dBm |
| MIMO RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0 | – | –91.3 | – | dBm/core |
| | MCS1 | – | –89.9 | – | dBm/core |
| | MCS2 | – | –87.5 | – | dBm/core |
| | MCS3 | – | –84 | – | dBm/core |
| | MCS4 | – | –80.9 | – | dBm/core |
| | MCS5 | – | –76.2 | – | dBm/core |
| | MCS6 | – | –74.7 | – | dBm/core |
| | MCS7 | – | –73.3 | – | dBm/core |
| | MCS8 | – | –89.8 | – | dBm/core |
| MCS15 | – | –70.3 | – | dBm/core | |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|--|--|-------|-------|----------|----------|
| SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –91.3 | – | dBm |
| | MCS1, Nss 1 | – | –88.3 | – | dBm |
| | MCS2, Nss 1 | – | –86 | – | dBm |
| | MCS3, Nss 1 | – | –83 | – | dBm |
| | MCS4, Nss 1 | – | –79.4 | – | dBm |
| | MCS5, Nss 1 | – | –74.9 | – | dBm |
| | MCS6, Nss 1 | – | –73.3 | – | dBm |
| | MCS7, Nss 1 | – | –72.6 | – | dBm |
| MCS8, Nss 1 | – | –68.2 | – | dBm | |
| MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC | 20 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –92.8 | – | dBm/core |
| | MCS1, Nss 1 | – | –91.3 | – | dBm/core |
| | MCS2, Nss 1 | – | –89 | – | dBm/core |
| | MCS3, Nss 1 | – | –86 | – | dBm/core |
| | MCS4, Nss 1 | – | –82.4 | – | dBm/core |
| | MCS5, Nss 1 | – | –77.9 | – | dBm/core |
| | MCS6, Nss 1 | – | –76.3 | – | dBm/core |
| | MCS7, Nss 1 | – | –75.6 | – | dBm/core |
| | MCS8, Nss 1 | – | –71.2 | – | dBm/core |
| | MCS0, Nss 2 | – | –91 | – | dBm/core |
| MCS8, Nss 2 | – | –67.1 | – | dBm/core | |
| SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –88.5 | – | dBm |
| | MCS1, Nss 1 | – | –85.5 | – | dBm |
| | MCS2, Nss 1 | – | –83.7 | – | dBm |
| | MCS3, Nss 1 | – | –80.5 | – | dBm |
| | MCS4, Nss 1 | – | –77.5 | – | dBm |
| | MCS5, Nss 1 | – | –72.5 | – | dBm |
| | MCS6, Nss 1 | – | –71.7 | – | dBm |
| | MCS7, Nss 1 | – | –70.3 | – | dBm |
| MCS8, Nss 1 | – | –65.9 | – | dBm | |
| MCS9, Nss 1 | – | –64.6 | – | dBm | |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|--|--|------|-------|------|----------|
| MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 40 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –90 | – | dBm/core |
| | MCS1, Nss 1 | – | –88.5 | – | dBm/core |
| | MCS2, Nss 1 | – | –86.7 | – | dBm/core |
| | MCS3, Nss 1 | – | –83.5 | – | dBm/core |
| | MCS4, Nss 1 | – | –80.5 | – | dBm/core |
| | MCS5, Nss 1 | – | –75.5 | – | dBm/core |
| | MCS6, Nss 1 | – | –74.7 | – | dBm/core |
| | MCS7, Nss 1 | – | –73.3 | – | dBm/core |
| | MCS8, Nss 1 | – | –68.9 | – | dBm/core |
| | MCS9, Nss 1 | – | –67.6 | – | dBm/core |
| | MCS0, Nss 2 | – | –88 | – | dBm/core |
| | MCS9, Nss 2 | – | –63.2 | – | dBm/core |
| SISO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 80 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –85 | – | dBm |
| | MCS1, Nss 1 | – | –82 | – | dBm |
| | MCS2, Nss 1 | – | –80 | – | dBm |
| | MCS3, Nss 1 | – | –76.7 | – | dBm |
| | MCS4, Nss 1 | – | –73.7 | – | dBm |
| | MCS5, Nss 1 | – | –70.5 | – | dBm |
| | MCS6, Nss 1 | – | –68 | – | dBm |
| | MCS7, Nss 1 | – | –66.5 | – | dBm |
| | MCS8, Nss 1 | – | –62.3 | – | dBm |
| | MCS9, Nss 1 | – | –60.5 | – | dBm |
| MIMO RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) ^{a,b} Defined for default parameters: GF, 800 ns GI, and non-STBC. | 80 MHz channel spacing for all MCS rates | | | | |
| | MCS0, Nss 1 | – | –86.5 | – | dBm/core |
| | MCS1, Nss 1 | – | –85 | – | dBm/core |
| | MCS2, Nss 1 | – | –83 | – | dBm/core |
| | MCS3, Nss 1 | – | –79.7 | – | dBm/core |
| | MCS4, Nss 1 | – | –76.7 | – | dBm/core |
| | MCS5, Nss 1 | – | –73.5 | – | dBm/core |
| | MCS6, Nss 1 | – | –71 | – | dBm/core |
| | MCS7, Nss 1 | – | –69.5 | – | dBm/core |
| | MCS8, Nss 1 | – | –65.3 | – | dBm/core |
| | MCS9, Nss 1 | – | –63.5 | – | dBm/core |
| | MCS0, Nss 2 | – | –84.3 | – | dBm/core |
| | MCS9, Nss 2 | – | –59.5 | – | dBm/core |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|--|-----------------|--------|------|-------|------|----------|
| SISO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) ^{a,b} at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC. | MCS7, Nss 1 | 20 MHz | – | –74.4 | – | dBm |
| – | MCS8, Nss 1 | 20 MHz | – | –71.7 | – | dBm |
| – | MCS9, Nss 1 | 20 MHz | – | –71.4 | – | dBm |
| – | MCS7, Nss 1 | 40 MHz | – | –71.8 | – | dBm |
| – | MCS8, Nss 1 | 40 MHz | – | –67.5 | – | dBm |
| – | MCS9, Nss 1 | 40 MHz | – | –66.5 | – | dBm |
| – | MCS7, Nss 1 | 80 MHz | – | –68 | – | dBm |
| – | MCS8, Nss 1 | 80 MHz | – | –64.3 | – | dBm |
| – | MCS9, Nss 1 | 80 MHz | – | –62.5 | – | dBm |
| MIMO RX sensitivity IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) ^{a,b} at WLAN RF port. Defined for default parameters: GF, 800 ns GI, LDPC coding, and non-STBC. | MCS7, Nss 2 | 20 MHz | – | –73 | – | dBm/core |
| – | MCS8, Nss 2 | 20 MHz | – | –70.2 | – | dBm/core |
| – | MCS9, Nss 2 | 20 MHz | – | –66.5 | – | dBm/core |
| – | MCS7, Nss 2 | 40 MHz | – | –70.8 | – | dBm/core |
| – | MCS8, Nss 2 | 40 MHz | – | –66 | – | dBm/core |
| – | MCS9, Nss 2 | 40 MHz | – | –64.7 | – | dBm/core |
| – | MCS7, Nss 2 | 80 MHz | – | –67 | – | dBm/core |
| – | MCS8, Nss 2 | 80 MHz | – | –62.8 | – | dBm/core |
| – | MCS9, Nss 2 | 80 MHz | – | –60.5 | – | dBm/core |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|--|---------------------------|-----------|-------|-------|------|------|
| Alternate adjacent channel rejection Blocking level for 3 dB RX sensitivity degradation ^c (without external filtering) | 776–794 MHz | CDMA2000 | -21 | - | - | dBm |
| | 824–849 MHz ^d | cdmaOne | -20 | - | - | dBm |
| | 824–849 MHz ^d | GSM850 | -12 | - | - | dBm |
| | 880–915 MHz | E-GSM | -12 | - | - | dBm |
| | 1710–1785 MHz | GSM1800 | -15 | - | - | dBm |
| | 1850–1910 MHz | GSM1800 | -15 | - | - | dBm |
| | 1850–1910 MHz | cdmaOne | -20 | - | - | dBm |
| | 1850–1910 MHz | WCDMA | -21 | - | - | dBm |
| | 1920–1980 MHz | WCDMA | -21 | - | - | dBm |
| | 2500–2570 MHz | Band 7 | -21 | - | - | dBm |
| | 2300–2400 MHz | Band 40 | -21 | - | - | dBm |
| | 2570–2620 MHz | Band 38 | -21 | - | - | dBm |
| | 2545–2575 MHz | XGP Band | -21 | - | - | dBm |
| Input In-Band IP3 | Maximum LNA gain | | - | -15.5 | - | dBm |
| | Minimum LNA gain | | - | -1.5 | - | dBm |
| Maximum receive level @ 5.24 GHz | @ 6, 9, 12 Mbps | | -9.5 | - | - | dBm |
| | @ 18, 24, 36, 48, 54 Mbps | | -14.5 | - | - | dBm |
| LPF 3 dB bandwidth | - | | 9 | - | 36 | MHz |
| Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes) | 6 Mbps OFDM | -79 dBm | 16 | - | - | dB |
| | 9 Mbps OFDM | -78 dBm | 15 | - | - | dB |
| | 12 Mbps OFDM | -76 dBm | 13 | - | - | dB |
| | 18 Mbps OFDM | -74 dBm | 11 | - | - | dB |
| | 24 Mbps OFDM | -71 dBm | 8 | - | - | dB |
| | 36 Mbps OFDM | -67 dBm | 4 | - | - | dB |
| | 48 Mbps OFDM | -63 dBm | 0 | - | - | dB |
| | 54 Mbps OFDM | -62 dBm | -1 | - | - | dB |
| | 65 Mbps OFDM | -61 dBm | -2 | - | - | dB |
| (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000 ^e octet PSDU with desired signal level as specified in Condition/Notes) | 6 Mbps OFDM | -78.5 dBm | 32 | - | - | dB |
| | 9 Mbps OFDM | -77.5 dBm | 31 | - | - | dB |
| | 12 Mbps OFDM | -75.5 dBm | 29 | - | - | dB |
| | 18 Mbps OFDM | -73.5 dBm | 27 | - | - | dB |
| | 24 Mbps OFDM | -70.5 dBm | 24 | - | - | dB |
| | 36 Mbps OFDM | -66.5 dBm | 20 | - | - | dB |
| | 48 Mbps OFDM | -62.5 dBm | 16 | - | - | dB |
| | 54 Mbps OFDM | -61.5 dBm | 15 | - | - | dB |
| | 65 Mbps OFDM | -60.5 dBm | 14 | - | - | dB |
| Maximum receiver gain | - | | - | 95 | - | dB |
| Gain control step | - | | - | 3 | - | dB |
| RSSI accuracy ^f | Range -90 dBm to -30 dBm | | -5 | - | 5 | dB |
| | Range above -30 dBm | | -8 | - | 8 | dB |

Table 42. WLAN 5 GHz Receiver Performance Specifications (Cont.)

| Parameter | Condition/Notes | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------------------------|------|------|------|---------|
| Return loss | Zo = 50Ω, across the dynamic range | 10 | – | 13 | dB |
| Receiver cascaded noise figure | At maximum gain | – | 5 | – | dB |
| General spurs | 1–18 GHz | – | – | –65 | dBm/MHz |

- a. Derate by 1.5 dB for 55°C to 70°C.
- b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- c. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- d. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
- e. For 65 Mbps, the size is 4096.
- f. The minimum and maximum values shown have a 95% confidence level.

17.6 WLAN 5 GHz Transmitter Performance Specifications

Note: The values in Table 43 are specified at the RF port unless otherwise noted.

Table 43. WLAN 5 GHz Transmitter Performance Specifications

| Parameter | Condition/Notes | | Min. | Typ. | Max. | Unit |
|--|--|--------------------------|------|------|--------|---------|
| Frequency range | – | | 4900 | – | 5845 | MHz |
| Transmitted power in cellular and FM bands (at 18 dBm) ^a | 76-108 MHz | FMRX | – | –162 | – | dBm/Hz |
| | 776-794 MHz | – | – | –168 | – | dBm/Hz |
| | 869-960 MHz | cdmaOne, GSM850 | – | –167 | – | dBm/Hz |
| | 1570-1580 MHz | GPS | – | –170 | – | dBm/Hz |
| | 1592-1610 MHz | GLONASS | – | –162 | – | dBm/Hz |
| | 1805-1880 MHz | GSM1800 | – | –169 | – | dBm/Hz |
| | 1850-1910 MHz | GSM1900 | – | –169 | – | dBm/Hz |
| | 1910-1930 MHz | Band 37 | – | –168 | – | dBm/Hz |
| | 1930-1990 MHz | GSM1900, cdmaOne, WCDMA | – | –168 | – | dBm/Hz |
| | 2010-2075 MHz | TDSCDMA | – | –168 | – | dBm/Hz |
| | 2110-2170 MHz | WCDMA | – | –160 | – | dBm/Hz |
| | 2300-2370 MHz | Band 40 | – | –166 | – | dBm/Hz |
| | 2370-2400 MHz | Band 40 | – | –162 | – | dBm/Hz |
| | 2496-2530 MHz | Band 41 | – | –165 | – | dBm/Hz |
| 2530-2560 MHz | Band 41 | – | –165 | – | dBm/Hz | |
| 2570-2690 MHz | Band 41 | – | –158 | – | dBm/Hz | |
| Harmonic level (at 17 dBm) | 9.8-11.570 GHz | 2 nd harmonic | – | –30 | – | dBm/MHz |
| General spurs | 1-18 GHz | – | – | – | –57 | dBm/MHz |
| TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance ^b | OFDM, QPSK | –13 dB | 17.5 | 18.5 | – | dBm |
| | OFDM, 16-QAM | –19 dB | 16 | 17.5 | – | dBm |
| | OFDM, 64-QAM | | – | – | – | – |
| | (R = 3/4) | –25 dB | 15 | 16.5 | – | dBm |
| | OFDM, 64-QAM | | – | – | – | – |
| | (R = 5/6) | –28 dB | 14 | 15.5 | – | dBm |
| | OFDM, 256-QAM (R = 3/4, VHT) | –30 dB | 13 | 14.5 | – | dBm |
| OFDM, 256-QAM (R = 5/6, VHT) | –32 dB | 11 | 12.5 | – | dBm | |
| Phase noise | 37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz | | – | 0.5 | – | Degrees |
| TX power control dynamic range | – | | 10 | – | – | dB |
| Closed loop TX power variation at highest power level setting | Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range. | | – | – | ±2.0 | dB |
| Carrier suppression | – | | 15 | – | – | dBc |
| Gain control step | – | | – | 0.25 | – | dB |
| Return loss | Zo = 50Ω | | – | 6 | – | dB |

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. Derate by 1.5 dB for temperatures higher than 55°C, or supply voltages lower than 3.0V. Derate by 3.0 dB for supply voltages of lower than 2.7V, or supply voltages lower than 3.0V at temperatures higher than 55°C.

18. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Functional operation is not guaranteed outside of the specification limits provided in this section.

18.1 Core Buck Switching Regulator

Table 44. Core Buck Switching Regulator (CBUCK) Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|-----------------------------------|--|-------------------|------|-------------------|-------|
| Input supply voltage (DC) | DC voltage range inclusive of disturbances. | 3.0 | 3.6 | 5.25 ^a | V |
| PWM mode switching frequency | CCM, Load > 100 mA VBAT = 3.6V | 2.8 | 4 | 5.2 | MHz |
| PWM output current | – | – | – | 600 | mA |
| Output current limit | – | – | 1400 | – | mA |
| Output voltage range | Programmable, 30 mV steps Default = 1.35V | 1.2 | 1.35 | 1.5 | V |
| PWM output voltage DC accuracy | Includes load and line regulation. Forced PWM mode | –4 | – | 4 | % |
| PWM ripple voltage, static | Measure with 20 MHz bandwidth limit. Static Load. Max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 μH inductor L > 1.05 μH, Cap + Board total-ESR < 20 mΩ, C _{out} > 1.9 μF, ESL < 200pH | – | 7 | 20 | mVpp |
| PWM mode peak efficiency | Peak Efficiency at 200 mA load | 78 | 86 | – | % |
| PFM mode efficiency | 10 mA load current | 70 | 81 | – | % |
| Start-up time from power down | VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V | – | – | 850 | μs |
| External inductor | 0806 size, ± 30%, 0.11 ± 25% Ohms | – | 2.2 | – | μH |
| External output capacitor | Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V | 2.0 ^b | 4.7 | 10 ^c | μF |
| External input capacitor | For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 μF | 0.67 ^b | 4.7 | – | μF |
| Input supply voltage ramp-up time | 0 to 4.3V | 40 | – | – | μs |

- The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
- Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
- Total capacitance includes those connected at the far end of the active load.

18.2 3.3V LDO (LDO3P3)
Table 45. LDO3P3 Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|----------------------------------|---|------------------|------|-------------------|-------|
| Input supply voltage, V_{in} | Min. = $V_o + 0.2V = 3.5V$ dropout voltage requirement must be met under maximum load for performance specifications. | 2.3 | 3.6 | 5.25 ^a | V |
| Output current | – | 0.2 | – | 600 | mA |
| Nominal output voltage, V_o | Default = 3.3V | – | 3.3 | – | V |
| Dropout voltage | At max. load. | – | – | 200 | mV |
| Output voltage DC accuracy | Includes line/load regulation. | –5 | – | +5 | % |
| Quiescent current | No load | – | 100 | 120 | μA |
| | Maximum load (600 mA) | – | 5.8 | 6 | mA |
| Leakage current | Power-Down mode, junction temperature = 85°C | – | 1.5 | 5 | μA |
| Line regulation | V_{in} from ($V_o + 0.2V$) to 4.8V, max. load | – | – | 3.5 | mV/V |
| Load regulation | load from 1 mA to 450 mA | – | – | 0.25 | mV/mA |
| PSRR | $V_{in} \geq V_o + 0.2V$, $V_o = 3.3V$, $C_o = 4.7 \mu F$, Max. load, 100 Hz to 100 kHz | 20 | – | – | dB |
| LDO turn-on time | Chip already powered up. | – | 160 | 250 | μs |
| External output capacitor, C_o | Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V | 1.0 ^b | 4.7 | – | μF |
| External input capacitor | For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 μF with SR_VDDBATP5V. | – | 4.7 | – | μF |

- a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
- b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

18.3 3.3V LDO (LDO3P3_B)
Table 46. LDO3P3_B Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|----------------------------------|---|------------------|------|-------------------|---------|
| Input supply voltage, V_{in} | Min. = $V_o + 0.2V = 3.5V$ dropout voltage requirement must be met under maximum load for performance specifications. | 2.3 | 3.6 | 5.25 ^a | V |
| Output current | – | 0.1 | – | 150 | mA |
| Nominal output voltage, V_o | Default = 3.3V | – | 3.3 | – | V |
| Dropout voltage | At max. load. | – | – | 200 | mV |
| Output voltage DC accuracy | Includes line/load regulation. | –5 | – | +5 | % |
| Quiescent current | No load | – | 10 | 16 | μA |
| Maximum load (150 mA) | – | – | 1.38 | 1.4 | mA |
| Leakage current | Power-Down mode, junction temperature = 85°C | – | 1.5 | 5 | μA |
| Line regulation | V_{in} from ($V_o + 0.2V$) to 4.8V, max. load | – | – | 3.5 | mV/V |
| Load regulation | load from 1 mA to 450 mA | – | – | 0.25 | mV/mA |
| PSRR | $V_{in} \geq V_o + 0.2V$, $V_o = 3.3V$, $C_o = 4.7 \mu F$, Max. load, 100 Hz to 100 kHz | 20 | – | – | dB |
| LDO turn-on time | Chip already powered up. | – | – | 150 | μs |
| External output capacitor, C_o | Ceramic, X5R, 0402, (ESR: 5 m Ω –240 m Ω), $\pm 10\%$, 10V | 0.7 ^b | 2.2 | – | μF |
| External input capacitor | For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402 | – | 4.7 | – | μF |

- a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
- b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

18.4 2.5V LDO (BTLDO2P5)
Table 47. BTLDO2P5 Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|---|--|------------------|------|-------------------|-------|
| Input supply voltage | Min. = 2.5V + 0.2V = 2.7V. Dropout voltage requirement must be met under maximum load for performance specifications. | 3.0 | 3.6 | 5.25 ^a | V |
| Nominal output voltage | Default = 2.5V. | – | 2.5 | – | V |
| Output voltage programmability | Range | 2.2 | 2.5 | 2.8 | V |
| | Accuracy at any step (including line/load regulation), load > 0.1 mA. | –5 | – | 5 | % |
| Dropout voltage | At maximum load. | – | – | 200 | mV |
| Output current | – | 0.1 | – | 70 | mA |
| Quiescent current | No load. | – | 8 | 16 | μA |
| | Maximum load at 70 mA. | – | 660 | 700 | μA |
| Leakage current | Power-down mode. | – | 1.5 | 5 | μA |
| Line regulation | V _{in} from (V _o + 0.2V) to 4.8V, maximum load. | – | – | 3.5 | mV/V |
| Load regulation | Load from 1 mA to 70 mA, V _{in} = 3.6V. | – | – | 0.3 | mV/mA |
| PSRR | V _{in} ≥ V _o + 0.2V, V _o = 2.5V, C _o = 2.2 μF, maximum load, 100 Hz to 100 kHz. | 20 | – | – | dB |
| LDO turn-on time | Chip already powered up. | – | – | 150 | μs |
| In-rush current | V _{in} = V _o + 0.15V to 4.8V, C _o = 2.2 μF, No load. | – | – | 250 | mA |
| External output capacitor, C _o | Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V | 0.7 ^b | 2.2 | 2.64 | μF |
| External input capacitor | For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 μF capacitor with SR_VDDBATP5V. | – | 4.7 | – | μF |

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

b. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

18.5 CLDO
Table 48. CLDO Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|----------------------------------|--|-------------------|------|-------|---------|
| Input supply voltage, V_{in} | Min. = $1.2 + 0.15V = 1.35V$ dropout voltage requirement must be met under maximum load. | 1.3 | 1.35 | 1.5 | V |
| Output current | – | 0.2 | – | 300 | mA |
| Output voltage, V_o | Programmable in 25 mV steps. Default = 1.2.V | 1.1 | 1.2 | 1.275 | V |
| Dropout voltage | At max. load | – | – | 150 | mV |
| Output voltage DC accuracy | Includes line/load regulation | –4 | – | +4 | % |
| Quiescent current | No load | – | 24 | – | μA |
| | 300 mA load | – | 2.1 | – | mA |
| Line Regulation | V_{in} from ($V_o + 0.15V$) to 1.5V, maximum load | – | – | 5 | mV/V |
| Load Regulation | Load from 1 mA to 300 mA | – | 0.02 | 0.05 | mV/mA |
| Leakage Current | Power down | – | – | 20 | μA |
| | Bypass mode | – | 1 | 3 | μA |
| PSRR | @1 kHz, $V_{in} \geq 1.35V$, $C_o = 4.7 \mu F$ | 20 | – | – | dB |
| Start-up Time of PMU | VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V. | – | – | 700 | μs |
| LDO Turn-on Time | LDO turn-on time when rest of the chip is up | – | 140 | 180 | μs |
| External Output Capacitor, C_o | Total ESR: 5 m Ω –240 m Ω | 1.32 ^a | 4.7 | – | μF |
| External Input Capacitor | Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. | – | 1 | 2.2 | μF |

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

18.6 LNLDO
Table 49. LNLDO Specifications

| Specification | Notes | Min. | Typ. | Max. | Units |
|----------------------------------|--|------------------|------|----------|--------------------------|
| Input supply voltage, V_{in} | Min. = $1.2V_o + 0.15V = 1.35V$ dropout voltage requirement must be met under maximum load. | 1.3 | 1.35 | 1.5 | V |
| Output Current | – | 0.1 | – | 150 | mA |
| Output Voltage, V_o | Programmable in 25 mV steps. Default = 1.2V | 1.1 | 1.2 | 1.275 | V |
| Dropout Voltage | At maximum load | – | – | 150 | mV |
| Output Voltage DC Accuracy | Includes line/load regulation | –4 | – | +4 | % |
| Quiescent current | No load | – | 44 | – | μA |
| | Max. load | – | 970 | 990 | μA |
| Line Regulation | V_{in} from ($V_o + 0.1V$) to 1.5V, max. load | – | – | 5 | mV/V |
| Load Regulation | Load from 1 mA to 150 mA | – | 0.02 | 0.05 | mV/mA |
| Leakage Current | Power-down | – | – | 10 | μA |
| Output Noise | @30 kHz, 60–150 mA load $C_o = 2.2 \mu F$ @100 kHz, 60–150 mA load $C_o = 2.2 \mu F$ | – | – | 60 35 | nV/rt Hz nV/ rt Hz |
| PSRR | @ 1kHz, Input > 1.35V, $C_o = 2.2 \mu F$, $V_o = 1.2V$ | 20 | – | – | dB |
| LDO Turn-on Time | LDO turn-on time when rest of chip is up | – | 140 | 180 | μs |
| External Output Capacitor, C_o | Total ESR (trace/capacitor): 5 m Ω –240 m Ω | 0.5 ^a | 2.2 | 4.7 | μF |
| External Input Capacitor | Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 m Ω –200 m Ω | – | 1 | 2.2 | μF |

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

19. System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, these values apply for the conditions specified in Table 33: “Recommended Operating Conditions and DC Characteristics,” on page 113.

19.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 50.

All values in Table 50 are with the Bluetooth core in reset (that is, Bluetooth and FM are OFF).

Table 50. Typical WLAN Power Consumption

| Mode | Bandwidth (MHz) | Band (GHz) | Vbat = 3.6V mA | Vio = 1.8V uA ^a |
|--|-----------------|------------|-------------------|-------------------------------|
| Sleep Modes | | | | |
| OFF^b | – | – | 0.003 | 5.5 |
| Sleep^c | – | – | 0.005 | 260 |
| IEEE power save, DTIM 1 1 RX core ^d | 20 | 2.4 | 1.2 | 260 |
| IEEE power save, DTIM 3 1 RX core ^d | 20 | 2.4 | 0.4 | 260 |
| IEEE power save, DTIM 1 1 RX core ^d | 20 | 5 | 1.2 | 260 |
| IEEE power save, DTIM 3 1 RX core ^d | 20 | 5 | 0.4 | 260 |
| IEEE power save, DTIM 1 1 RX core ^d | 40 | 5 | 1.5 | 260 |
| IEEE power save, DTIM 3 1 RX core ^d | 40 | 5 | 0.5 | 260 |
| IEEE power save, DTIM 1 1 RX core ^d | 80 | 5 | 2.0 | 260 |
| IEEE power save, DTIM 3 1 RX core ^d | 80 | 5 | 0.7 | 260 |
| Active Modes | | | | |
| Transmit | | | | |
| CCK 1 chain ^e | 20 | 2.4 | 350 | 60 |
| MCS8, Nss 1, HT20, SGI ^{f,g,h} | 20 | 2.4 | 270 | 60 |
| TMCS8, Nss 2, HT20, SGI ^{f,g,h} | 20 | 2.4 | 540 | 60 |
| MCS7, SGI ^{f,g,i} | 20 | 5 | 310 | 60 |
| MCS15, SGI ^{f,g,i} | 20 | 5 | 620 | 60 |
| MCS7 ^{f,g,i} | 40 | 5 | 315 | 60 |
| MCS9, Nss 1, SGI ^{f,g,j} | 40 | 5 | 295 | 60 |
| MCS9, Nss 2, SGI ^{f,g,j} | 40 | 5 | 590 | 60 |
| MCS9, Nss 1, SGI ^{f,g,j} | 80 | 5 | 305 | 60 |
| MCS9, Nss 2, SGI ^{f,g,j} | 80 | 5 | 610 | 60 |
| Receive | | | | |
| 1 Mbps, 1 RX core | 20 | 2.4 | 59 | 60 |
| 1 Mbps, 2 RX cores | 20 | 2.4 | 75 | 60 |
| MCS7, HT20 1 RX core ^k | 20 | 2.4 | 62 | 60 |
| MCS7, HT20 2 RX cores ^k | 20 | 2.4 | 81 | 60 |
| MCS15, HT20 ^k | 20 | 2.4 | 86 | 60 |
| CRS 1 RX core ^l | 20 | 2.4 | 57 | 60 |
| CRS 2 RX cores ^l | 20 | 2.4 | 76 | 60 |
| Receive MCS7, SGI 1 RX core ^k | 20 | 5 | 71 | 60 |

Table 50. Typical WLAN Power Consumption (Cont.)

| Mode | Bandwidth (MHz) | Band (GHz) | Vbat = 3.6V) mA | Vio = 1.8V uA ^a |
|--|-----------------|------------|-----------------|----------------------------|
| Receive MCS7, SGI 2 RX cores ^k | 20 | 5 | 102 | 60 |
| Receiver MCS15, SGI ^k | 20 | 5 | 106 | 60 |
| CRS 1 RX core ^l | 20 | 5 | 67 | 60 |
| CRS 2 RX cores ^l | 20 | 5 | 96 | 60 |
| Receive MCS 7, SGI 1 RX core ^k | 40 | 5 | 91 | 60 |
| Receive MCS 7, SGI 2 RX cores ^k | 40 | 5 | 135 | 60 |
| Receive MCS 15, SGI ^k | 40 | 5 | 141 | 60 |
| CRS 1 RX core ^l | 40 | 5 | 80 | 60 |
| CRS 2 RX cores ^l | 40 | 5 | 121 | 60 |
| Receive MCS9, Nss 1, SGI ^k | 80 | 5 | 123 | 60 |
| Receive MCS9, Nss 1, SGI 2 RX cores ^k | 80 | 5 | 189 | 60 |
| Receive MCS9, Nss 2, SGI ^k | 80 | 5 | 206 | 60 |
| CRS 1 RX core ^l | 80 | 5 | 102 | 60 |
| CRS 2 RX cores ^l | 80 | 5 | 163 | 60 |

- a. Specified with all pins idle (not switching) and not driving any loads.
- b. WL_REG_ON, BT_REG_ON low, no VDDIO.
- c. Idle, not associated, or inter-beacon.
- d. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over 3 DTIM intervals.
- e. Output power per core at RF port = 21 dBm
- f. Duty cycle is 100%
- g. Measured using packet engine test mode.
- h. Output power per core at RF port = 17 dBm.
- i. Output power per core at RF port = 17.5 dBm.
- j. Output power per core at RF port = 14 dBm.
- k. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
- l. Carrier sense (CCA) when no carrier present.

19.2 Bluetooth and FM Current Consumption

The Bluetooth, BLE, and FM current consumption measurements are shown in [Table 51](#).

Note:

- The WLAN core is in reset (WLAN_REG_ON = low) for all measurements provided in [Table 51](#).
- For FM measurements, the Bluetooth core is in Sleep mode.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 51. Bluetooth BLE and FM Current Consumption

| Operating Mode | VBAT (VBAT = 3.6V) Typical | VDDIO (VDDIO = 1.8V) Typical | Units |
|-----------------------------------|----------------------------|------------------------------|-------|
| Sleep | 13 | 198 | μA |
| Standard 1.28s Inquiry Scan | 0.217 | 0.197 | mA |
| P and I Scan ^b | 440 | 194 | μA |
| 500 ms Sniff Master | 0.168 | 0.195 | mA |
| 500 ms Sniff Slave | 0.124 | 0.190 | mA |
| DM1/DH1 Master | 25.3 | 0.024 | mA |
| DM3/DH3 Master | 30.6 | 0.035 | mA |
| DM5/DH5 Master | 31.4 | 0.037 | mA |
| 3DH5 Master | 29.2 | 0.094 | mA |
| SCO HV3 Master | 11.45 | 0.089 | mA |
| HV3 + Sniff + Scan ^a | 11.7 | 0.090 | mA |
| FMRX I ² S Audio | 8.0 | – | mA |
| FMRX Analog Audio only | 8.6 | – | mA |
| FMRX I ² S Audio + RDS | 8.0 | – | mA |
| FMRX Analog Audio + RDS | 8.6 | – | mA |
| BLE Scan ^b | 244 | 196 | μA |
| BLE Scan 10 ms | 21.34 | 0.013 | mA |
| BLE Adv—Unconnectable 1.00 sec | 67 | 199 | μA |
| BLE Adv—Unconnectable 1.28 sec | 55 | 199 | μA |
| BLE Adv—Unconnectable 2.00 sec | 58 | 199 | μA |
| BLE Connected 7.5 ms | 3.95 | 0.013 | mA |
| BLE Connected 1 sec. | 57 | 198 | μA |
| BLE Connected 1.28 sec. | 52 | 197 | μA |

a. At maximum class 1 TX power, 500 ms sniff, four attempts (slave), P = 1.28s, and I = 2.56s.

b. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

20. Interface Timing and AC Characteristics

20.1 SDIO Timing

20.1.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of [Figure 37](#) and [Table 52](#).

Figure 37. SDIO Bus Timing (Default Mode)

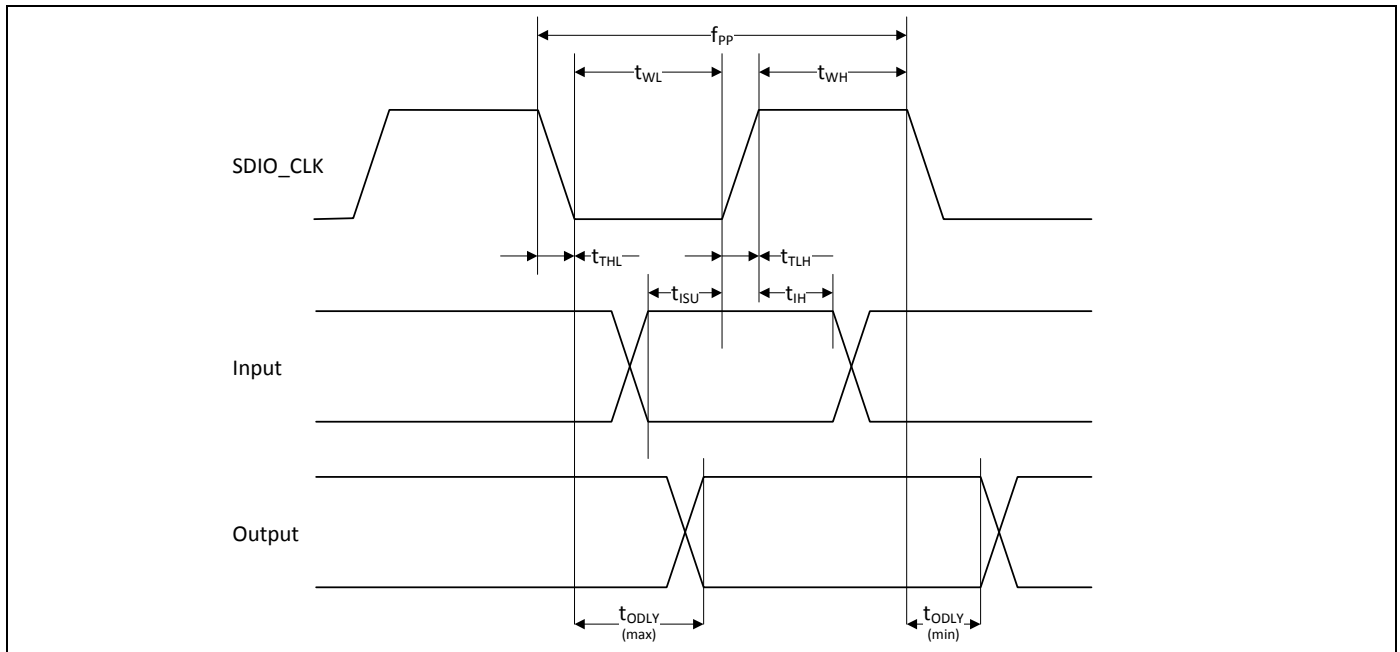


Table 52. SDIO Bus Timing^a Parameters (Default Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|--------|---------|---------|---------|------|
| SDIO CLK (All values are referred to minimum VIH and maximum VIL^b) | | | | | |
| Frequency – Data Transfer mode | fPP | 0 | – | 25 | MHz |
| Frequency – Identification mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 10 | – | – | ns |
| Clock high time | tWH | 10 | – | – | ns |
| Clock rise time | tTLH | – | – | 10 | ns |
| Clock low time | tTHL | – | – | 10 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup time | tISU | 5 | – | – | ns |
| Input hold time | tIH | 5 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer mode | tODLY | 0 | – | 14 | ns |
| Output delay time – Identification mode | tODLY | 0 | – | 50 | ns |

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. Min. (Vih) = $0.7 \times VDDIO$ and max. (Vil) = $0.2 \times VDDIO$.

20.1.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 38 and Table 53.

Figure 38. SDIO Bus Timing (High-Speed Mode)

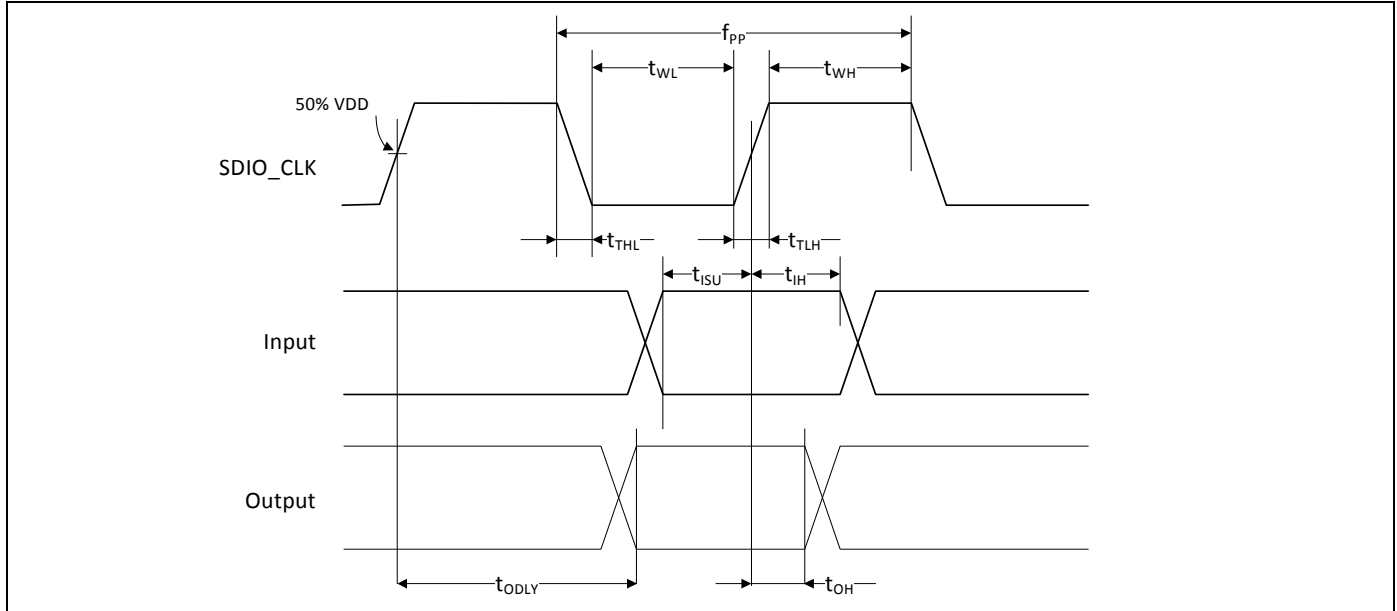


Table 53. SDIO Bus Timing^a Parameters (High-Speed Mode)

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|-------------------|---------|---------|---------|------|
| SDIO CLK (all values are referred to minimum VIH and maximum VIL^b) | | | | | |
| Frequency – Data Transfer Mode | f _{PP} | 0 | – | 50 | MHz |
| Frequency – Identification Mode | f _{OD} | 0 | – | 400 | kHz |
| Clock low time | t _{WL} | 7 | – | – | ns |
| Clock high time | t _{WH} | 7 | – | – | ns |
| Clock rise time | t _{TLH} | – | – | 3 | ns |
| Clock low time | t _{THL} | – | – | 3 | ns |
| Inputs: CMD, DAT (referenced to CLK) | | | | | |
| Input setup Time | t _{ISU} | 6 | – | – | ns |
| Input hold Time | t _{IH} | 2 | – | – | ns |
| Outputs: CMD, DAT (referenced to CLK) | | | | | |
| Output delay time – Data Transfer Mode | t _{ODLY} | – | – | 14 | ns |
| Output hold time | t _{OH} | 2.5 | – | – | ns |
| Total system capacitance (each line) | CL | – | – | 40 | pF |

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. Min. (V_{Ih}) = 0.7 × V_{DDIO} and max. (V_{Il}) = 0.2 × V_{DDIO}.

20.1.3 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 39. SDIO Clock Timing (SDR Modes)

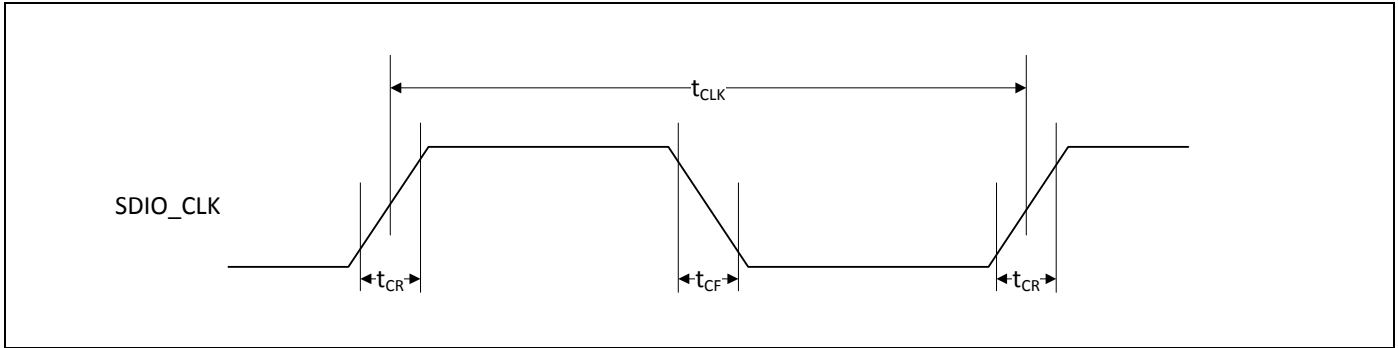


Table 54. SDIO Bus Clock Timing Parameters (SDR Modes)

| Parameter | Symbol | Minimum | Maximum | Unit | Comments |
|------------|------------------|---------|----------------------|------|--|
| - | t_{CLK} | 40 | - | ns | SDR12 mode |
| | | 20 | - | ns | SDR25 mode |
| | | 10 | - | ns | SDR50 mode |
| | | 4.8 | - | ns | SDR104 mode |
| - | t_{CR}, t_{CF} | - | $0.2 \times t_{CLK}$ | ns | $t_{CR}, t_{CF} < 2.00$ ns (max.) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max.) @208 MHz, $C_{CARD} = 10$ pF |
| Clock duty | - | 30 | 70 | % | - |

Device Input Timing

Figure 40. SDIO Bus Input Timing (SDR Modes)

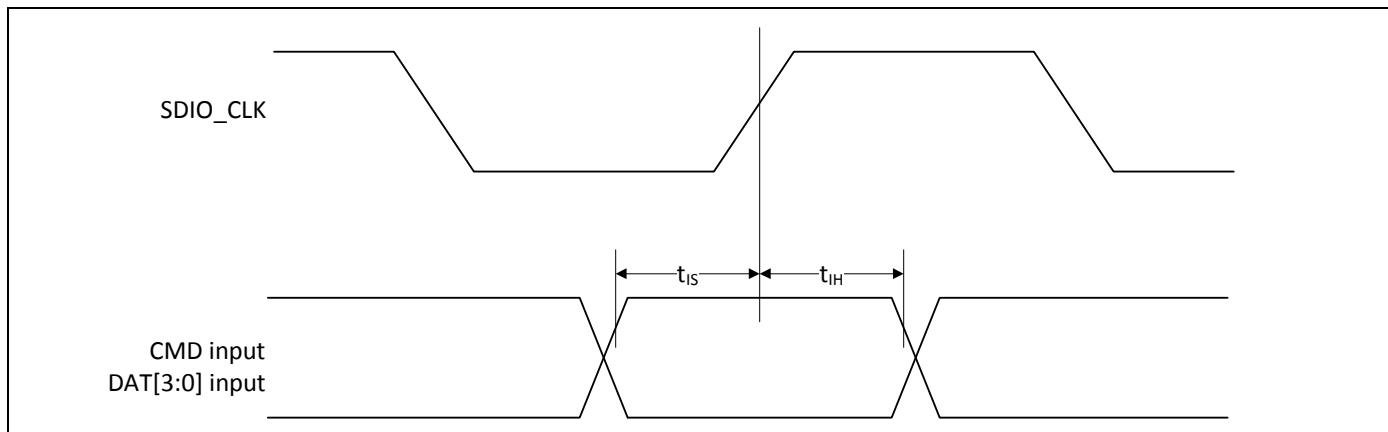


Table 55. SDIO Bus Input Timing Parameters (SDR Modes)

| Symbol | Minimum | Maximum | Unit | Comments |
|--------------------|---------|---------|------|---|
| SDR104 Mode | | | | |
| t_{IS} | 1.4 | – | ns | $C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$ |
| t_{IH} | 0.80 | – | ns | $C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$ |
| SDR50 Mode | | | | |
| t_{IS} | 3.00 | – | ns | $C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975\text{V}$ |
| t_{IH} | 0.80 | – | ns | $C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975\text{V}$ |

Device Output Timing

Figure 41. SDIO Bus Output Timing (SDR Modes up to 100 MHz)

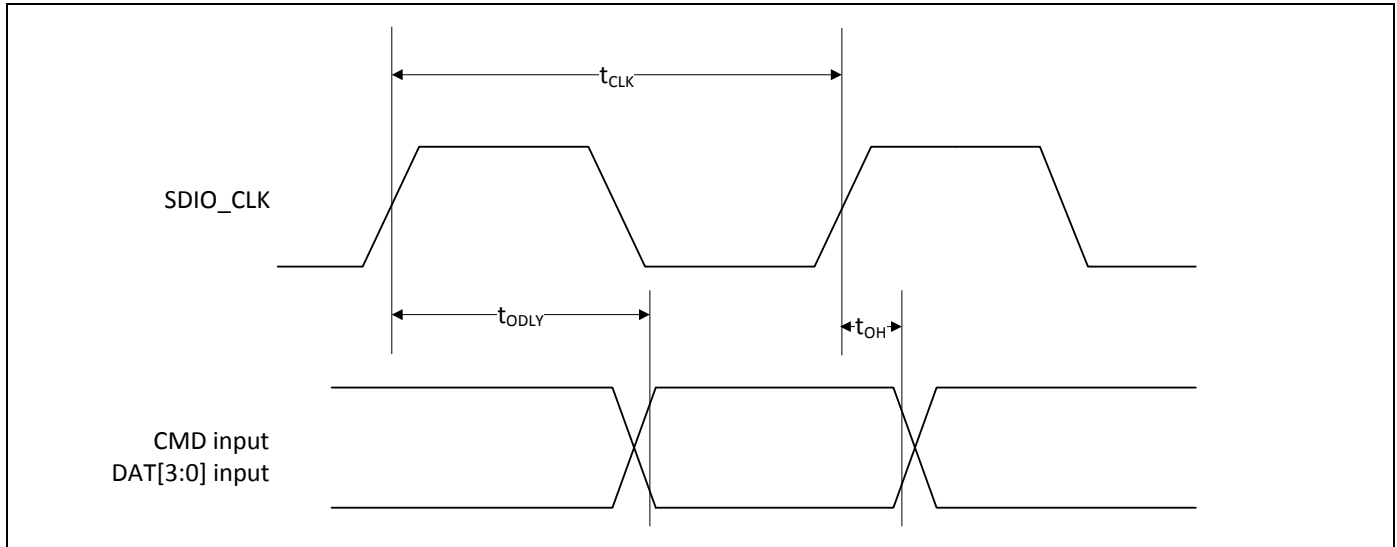


Table 56. SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

| Symbol | Minimum | Maximum | Unit | Comments |
|------------|---------|---------|------|--|
| t_{ODLY} | – | 7.5 | ns | $t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50 |
| t_{ODLY} | – | 14.0 | ns | $t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25 |
| t_{OH} | 1.5 | – | ns | Hold time at the t_{ODLY} (min.) $C_L = 15$ pF |

Figure 42. SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

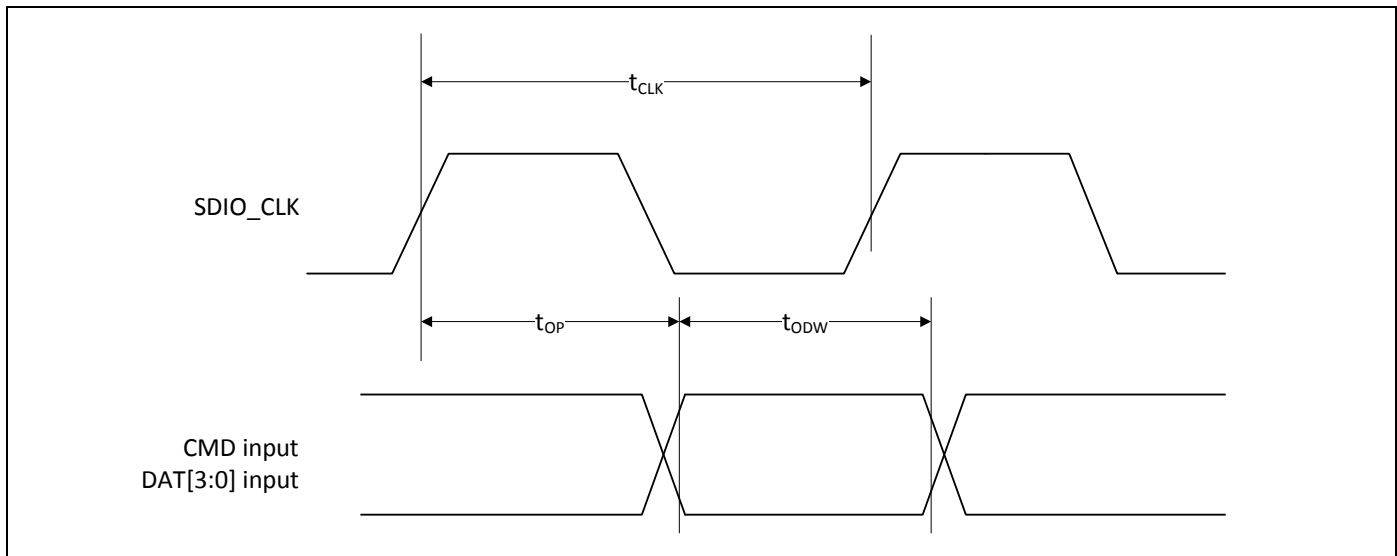
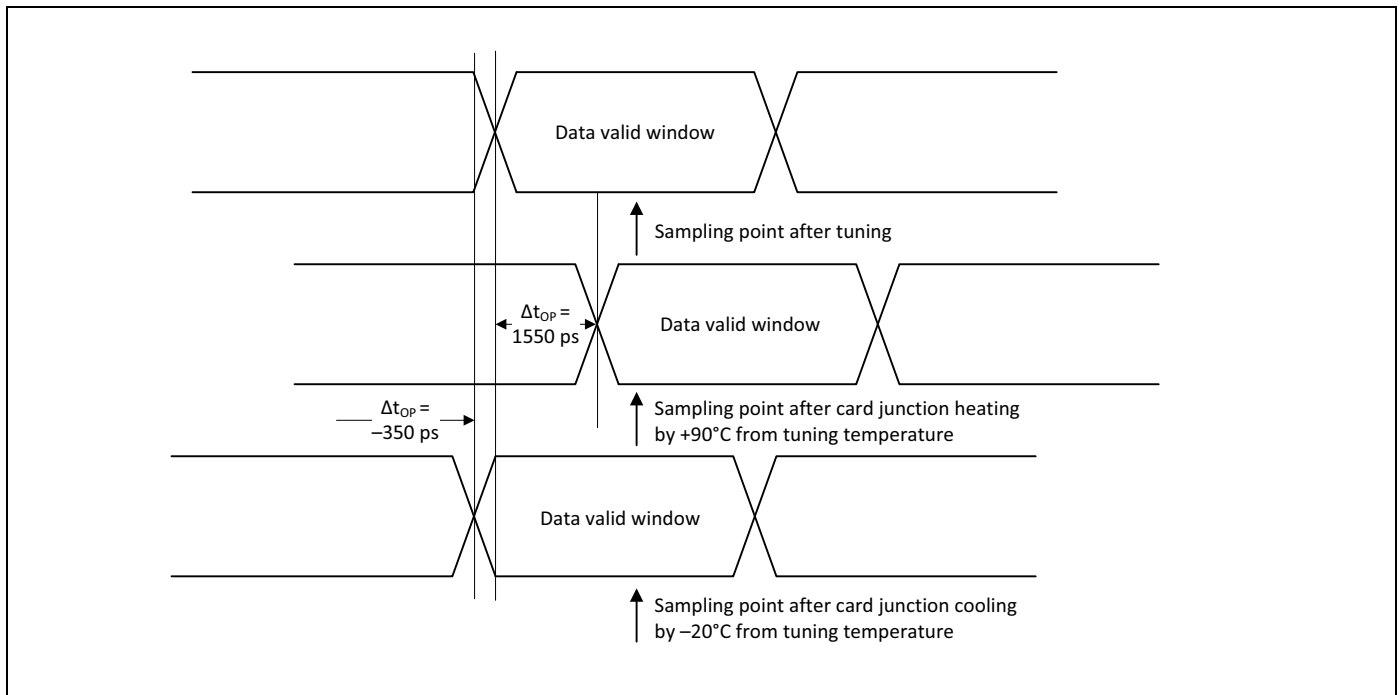


Table 57. SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

| Symbol | Minimum | Maximum | Unit | Comments |
|-----------------|---------|---------|------|---|
| t_{OP} | 0 | 2 | UI | Card output phase |
| Δt_{OP} | -350 | +1550 | ps | Delay variation due to temp change after tuning |
| t_{ODW} | 0.60 | - | UI | $t_{ODW}=2.88$ ns @208 MHz |

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Figure 43. Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



20.1.4 SDIO Bus Timing Specifications in DDR50 Mode

Figure 44. SDIO Clock Timing (DDR50 Mode)

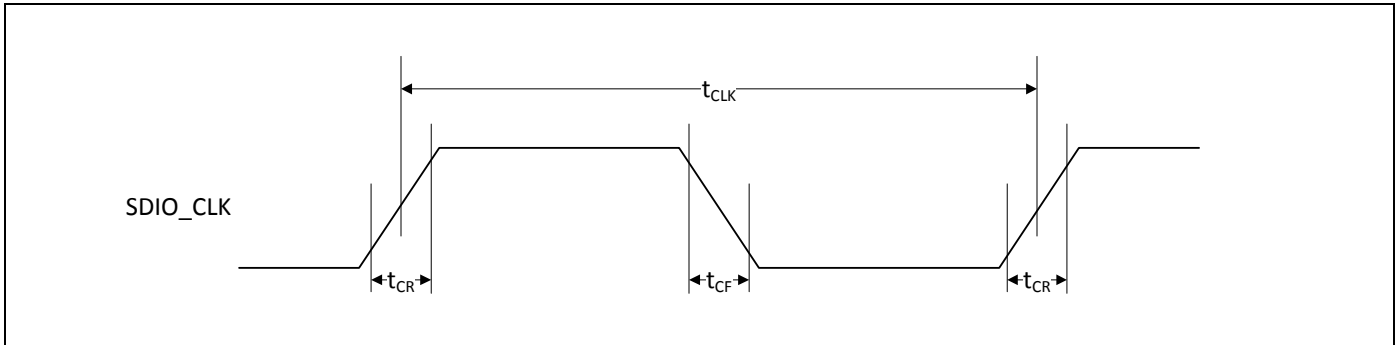


Table 58. SDIO Bus Clock Timing Parameters (DDR50 Mode)

| Parameter | Symbol | Minimum | Maximum | Unit | Comments |
|------------|------------------|---------|----------------------|------|--|
| – | t_{CLK} | 20 | – | ns | DDR50 mode |
| – | t_{CR}, t_{CF} | – | $0.2 \times t_{CLK}$ | ns | $t_{CR}, t_{CF} < 4.00$ ns (max.) @50 MHz, $C_{CARD} = 10$ pF |
| Clock duty | – | 45 | 55 | % | – |

Data Timing, DDR50 Mode

Figure 45. SDIO Data Timing (DDR50 Mode)

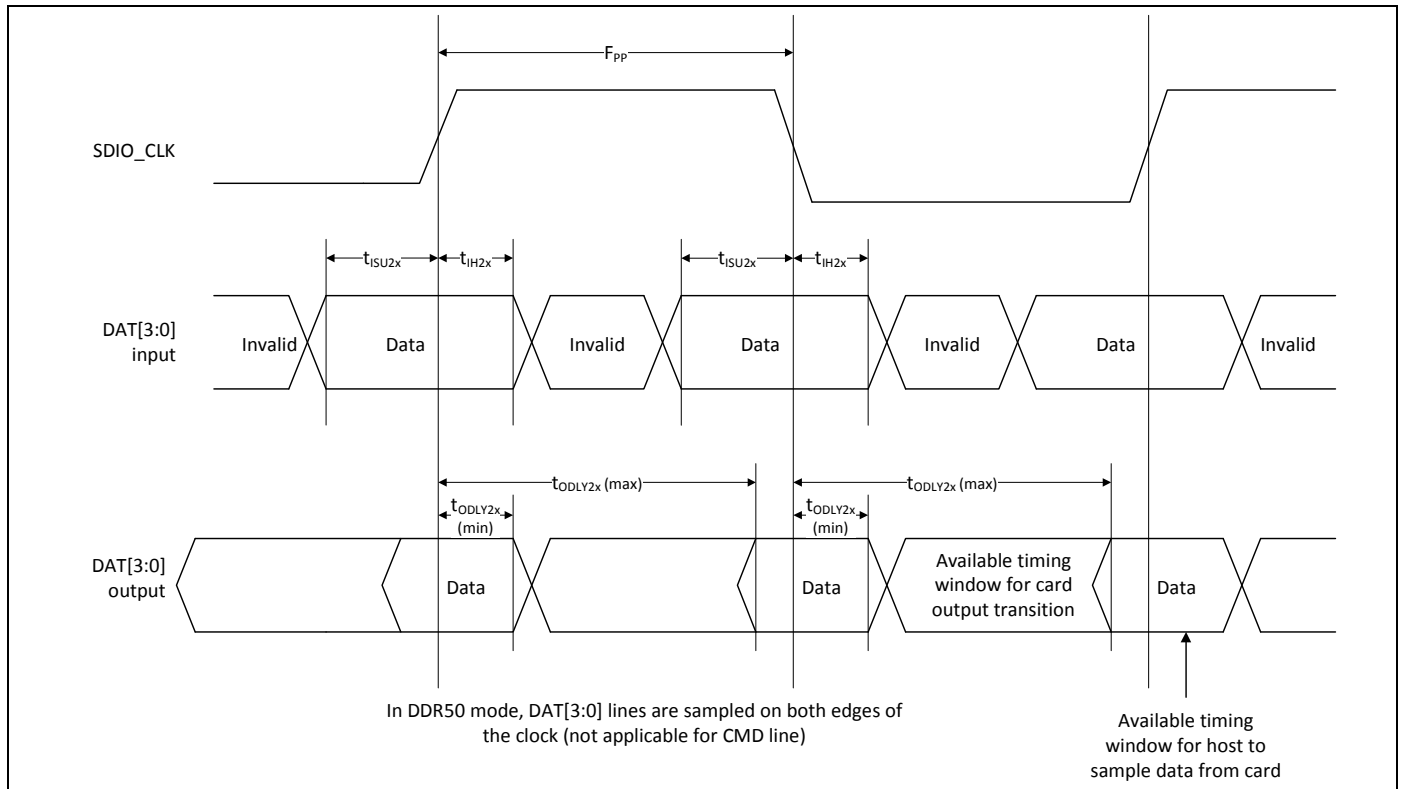


Table 59. SDIO Bus Timing Parameters (DDR50 Mode)

| Parameter | Symbol | Minimum | Maximum | Unit | Comments |
|-------------------|--------------|---------|---------|------|-------------------------------------|
| Input CMD | | | | | |
| Input setup time | t_{ISU} | 6 | – | ns | $C_{CARD} < 10 \text{ pF}$ (1 Card) |
| Input hold time | t_{IH} | 0.8 | – | ns | $C_{CARD} < 10 \text{ pF}$ (1 Card) |
| Output CMD | | | | | |
| Output delay time | t_{ODLY} | – | 13.7 | ns | $C_{CARD} < 30 \text{ pF}$ (1 Card) |
| Output hold time | t_{OH} | 1.5 | – | ns | $C_{CARD} < 15 \text{ pF}$ (1 Card) |
| Input DAT | | | | | |
| Input setup time | t_{ISU2x} | 3 | – | ns | $C_{CARD} < 10 \text{ pF}$ (1 Card) |
| Input hold time | t_{IH2x} | 0.8 | – | ns | $C_{CARD} < 10 \text{ pF}$ (1 Card) |
| Output DAT | | | | | |
| Output delay time | t_{ODLY2x} | – | 7.5 | ns | $C_{CARD} < 25 \text{ pF}$ (1 Card) |
| Output hold time | t_{ODLY2x} | 1.5 | – | ns | $C_{CARD} < 15 \text{ pF}$ (1 Card) |

20.2 HSIC Interface Specifications

Table 60. HSIC Interface Parameters

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Comments |
|--|--------------|----------------------|---------|----------------------|------------|------------------------------------|
| HSIC signaling voltage | V_{DD} | 1.1 | 1.2 | 1.3 | V | – |
| I/O voltage input low | V_{IL} | -0.3 | – | $0.35 \times V_{DD}$ | V | – |
| I/O Voltage input high | V_{IH} | $0.65 \times V_{DD}$ | – | $V_{DD} + 0.3$ | V | – |
| I/O voltage output low | V_{OL} | – | – | $0.25 \times V_{DD}$ | V | – |
| I/O voltage output high | V_{OH} | $0.75 \times V_{DD}$ | – | – | V | – |
| I/O pad drive strength | O_D | 40 | – | 60 | Ω | Controlled output impedance driver |
| I/O weak keepers | I_L | 20 | – | 70 | mA | – |
| I/O input impedance | Z_I | 100 | – | – | k Ω | – |
| Total capacitive load ^a | C_L | 3 | – | 14 | pF | – |
| Characteristic trace impedance | T_I | 45 | 50 | 55 | Ω | – |
| Circuit board trace length | T_L | – | – | 10 | cm | – |
| Circuit board trace propagation skew ^b | T_S | – | – | 15 | ps | – |
| STROBE frequency ^c | F_{STROBE} | 239.988 | 240 | 240.012 | MHz | ± 500 ppm |
| Slew rate (rise and fall) STROBE and DATA ^c | T_{slew} | $0.60 \times V_{DD}$ | 1.0 | 1.2 | V/ns | Averaged from 30% ~ 70% points |
| Receiver data setup time (with respect to STROBE) ^c | T_s | 300 | – | – | ps | Measured at the 50% point |
| Receiver data hold time (with respect to STROBE) ^c | T_b | 300 | – | – | ps | Measured at the 50% point |

- a. Total Capacitive Load (C_L), includes device Input/Output capacitance, and capacitance of a 50 Ω PCB trace with a length of 10 cm.
- b. Maximum propagation delay skew in STROBE or DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that the signal timing is within specification limits at the receiver.
- c. Jitter and duty cycle are not separately specified parameters, they are incorporated into the values in the [Table 60](#).

20.3 PCI Express Interface Parameters

Table 61. PCI Express Interface Parameters

| Parameter | Symbol | Comments | Minimum | Typical | Maximum | Unit |
|--|-----------------------------|---|---|---------|---------|-------|
| General | | | | | | |
| Baud rate | BPS | – | – | 5 | – | Gbaud |
| Reference clock amplitude | Vref | LVPECL | 1 | – | – | V |
| Receiver | | | | | | |
| Differential termination | ZRX-DIFF-DC | Differential termination | 80 | 100 | 120 | Ω |
| DC impedance | ZRX-DC | DC common-mode impedance | 40 | 50 | 60 | Ω |
| Powered down termination (POS) | ZRX-HIGH-IMP-DC-POS | Power-down or RESET high impedance | 100k | – | – | Ω |
| Powered down termination (NEG) | ZRX-HIGH-IMP-DC-NEG | Power-down or RESET high impedance | 1k | – | – | Ω |
| Input voltage | VRX-DIFFp-p | AC coupled, differential p-p | 175 | – | – | mV |
| Jitter tolerance | TRX-EYE | Minimum receiver eye width | 0.4 | – | – | UI |
| Differential return loss | RLRX-DIFF | Differential return loss | 10 | – | – | dB |
| Common-mode return loss | RLRX-CM | Common-mode return loss | 6 | – | – | dB |
| Unexpected electrical idle enter detect threshold integration time | TRX-IDEL-DET-DIFF-ENTERTIME | An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition. | – | – | 10 | ms |
| Signal detect threshold | VRX-IDLE-DET-DIFFp-p | Electrical idle detect threshold | 65 | – | 175 | mV |
| Transmitter | | | | | | |
| Output voltage | VTX-DIFFp-p | Differential p-p, programmable in 16 steps | 0.8 | – | 1200 | mV |
| Output voltage rise time | VTX-RISE | 20% to 80% | 0.125 (2.5 GT/s) 0.15 (5 GT/s) | – | – | UI |
| Output voltage fall time | VTX-FALL | 80% to 20% | 0.125 (2.5 GT/s) 0.15 (5 GT/s) | – | – | UI |
| RX detection voltage swing | VTX-RCV-DETECT | The amount of voltage change allowed during receiver detection. | – | – | 600 | mV |
| TX AC peak common-mode voltage (5 GT/s) | VTX-CM-AC-PP | TX AC common mode voltage (5 GT/s) | – | – | 100 | mV |
| TX AC peak common-mode voltage (2.5 GT/s) | VTX-CM-AC-P | TX AC common mode voltage (2.5 GT/s) | – | – | 20 | mV |

Table 61. PCI Express Interface Parameters (Cont.)

| Parameter | Symbol | Comments | Minimum | Typical | Maximum | Unit |
|--|-----------------------------|---|------------------------------|---------|---------|------|
| Absolute delta of DC common-mode voltage during L0 and electrical idle | VTX-CM-DC-ACTIVE-IDLE-DELTA | Absolute delta of DC common-mode voltage during L0 and electrical idle. | 0 | – | 100 | mV |
| Absolute delta of DC common-mode voltage between D+ and D- | VTX-CM-DC-LINE-DELTA | DC offset between D+ and D- | 0 | – | 25 | mV |
| Electrical idle differential peak output voltage | VTX-IDLE-DIFF-AC-p | Peak-to-peak voltage | 0 | – | 20 | mV |
| TX short circuit current | ITX-SHORT | Current limit when TX output is shorted to ground. | – | – | 90 | mA |
| DC differential TX termination | ZTX-DIFF-DC | Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF) | 80 | – | 120 | Ω |
| Differential return loss | RLTX-DIFF | Differential return loss | 10 (min.) for 0.05: 1.25 GHz | – | – | dB |
| Common-mode return loss | RLTX-CM | Common-mode return loss | 6 | – | – | dB |
| TX eye width | TTX-EYE | Minimum TX eye width | 0.75 | – | – | UI |

20.4 JTAG Timing

Table 62. JTAG Timing Characteristics

| Signal Name | Period | Output Maximum | Output Minimum | Setup | Hold |
|-------------|--------|----------------|----------------|-------|------|
| TCK | 125 ns | – | – | – | – |
| TDI | – | – | – | 20 ns | 0 ns |
| TMS | – | – | – | 20 ns | 0 ns |
| TDO | – | 100 ns | 0 ns | – | – |
| JTAG_TRST | 250 ns | – | – | – | – |

21. Power-Up Sequence and Timing

21.1 Sequencing of Reset and Regulator Control Signals

The CYW4354 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see [Figure 46](#), [Figure 47 on page 154](#), and [Figure 48](#) and [Figure 49 on page 155](#)). The timing values indicated are minimum required values; longer delays are also acceptable.

21.1.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4354 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW4354 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note:

- For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.
- The reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.
- The CYW4354 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.
- VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

21.1.2 Control Signal Timing Diagrams

Figure 46. WLAN = ON, Bluetooth = ON

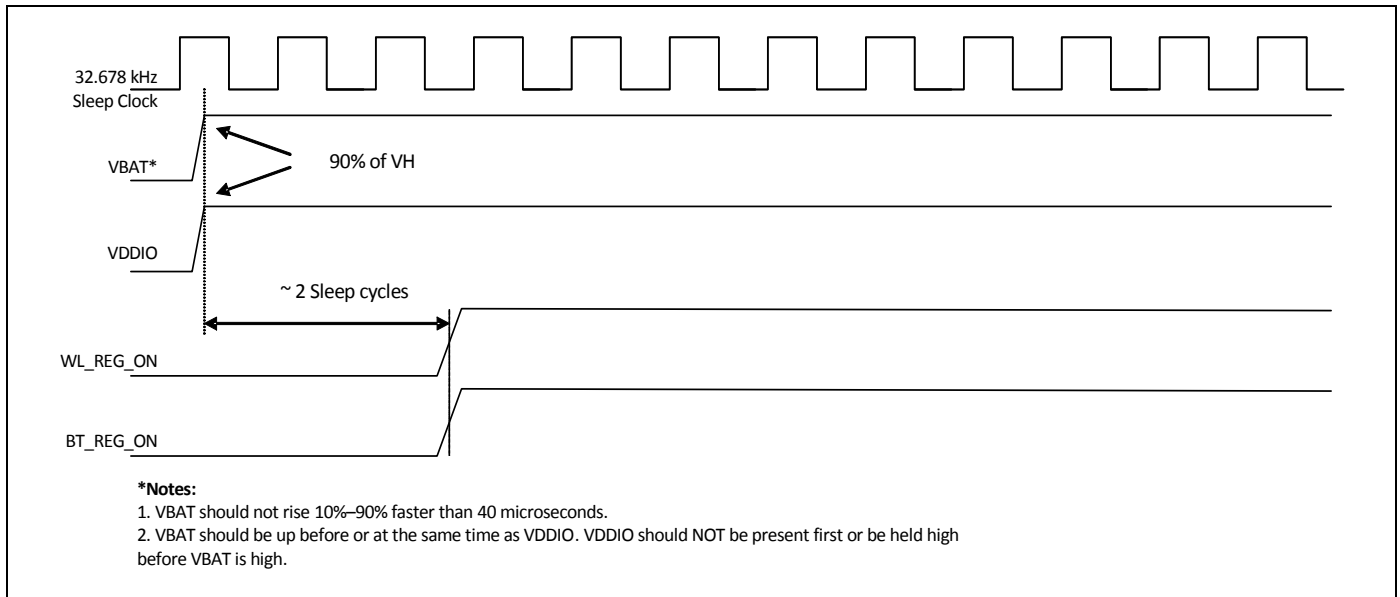


Figure 47. WLAN = OFF, Bluetooth = OFF

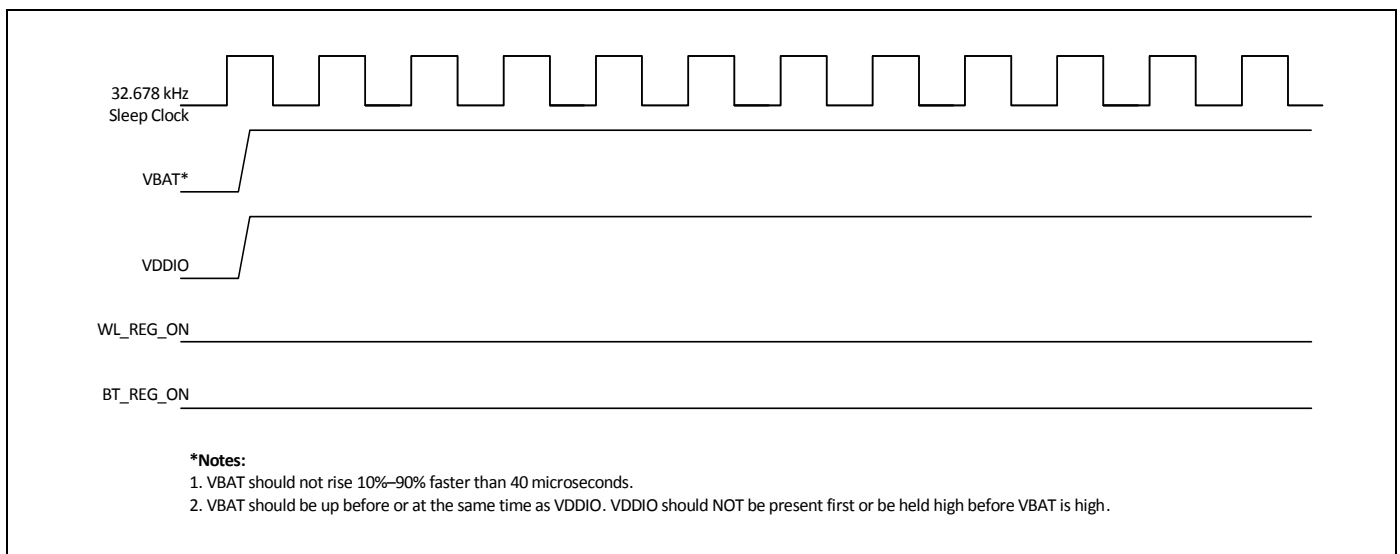


Figure 48. WLAN = ON, Bluetooth = OFF

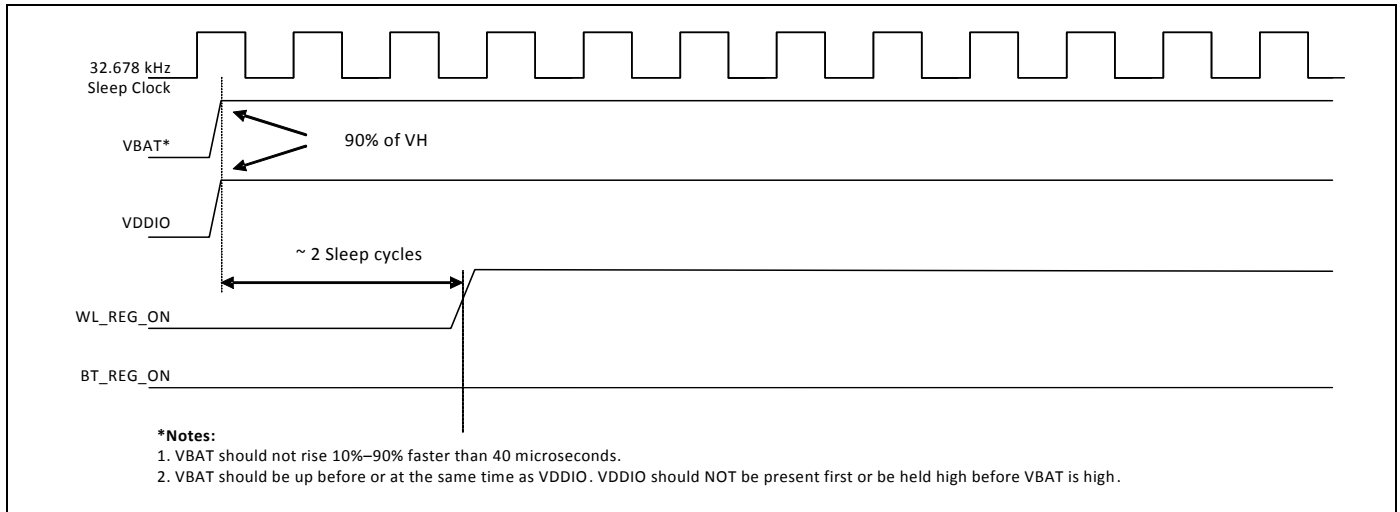


Figure 49. WLAN = OFF, Bluetooth = ON

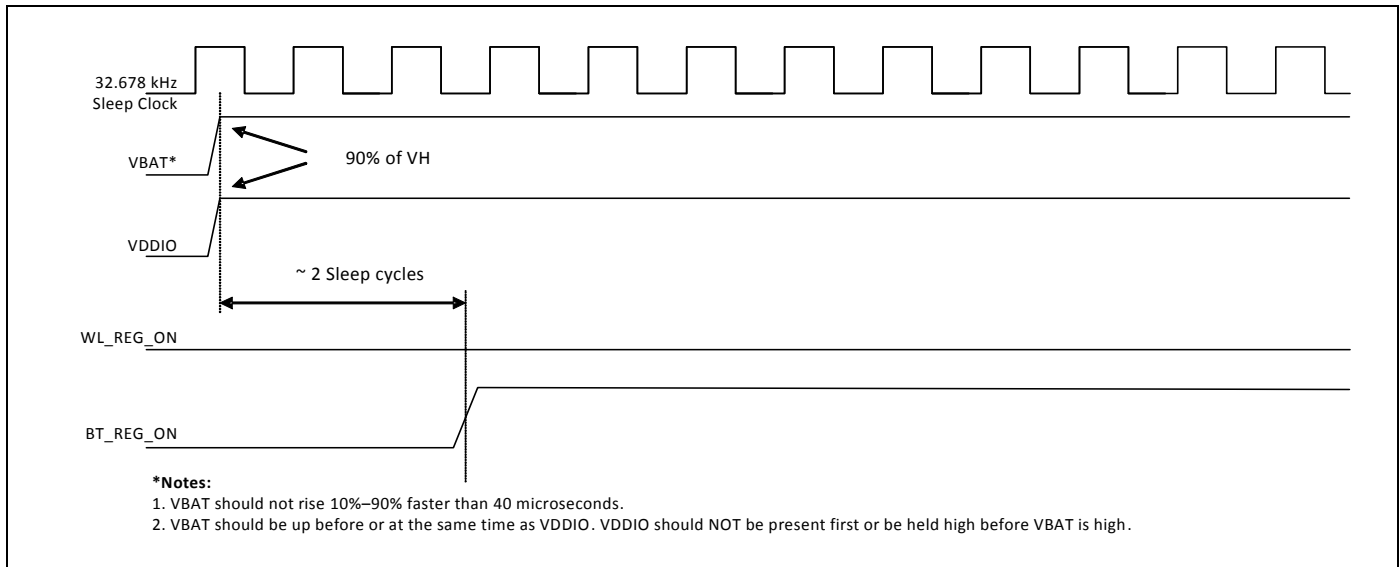
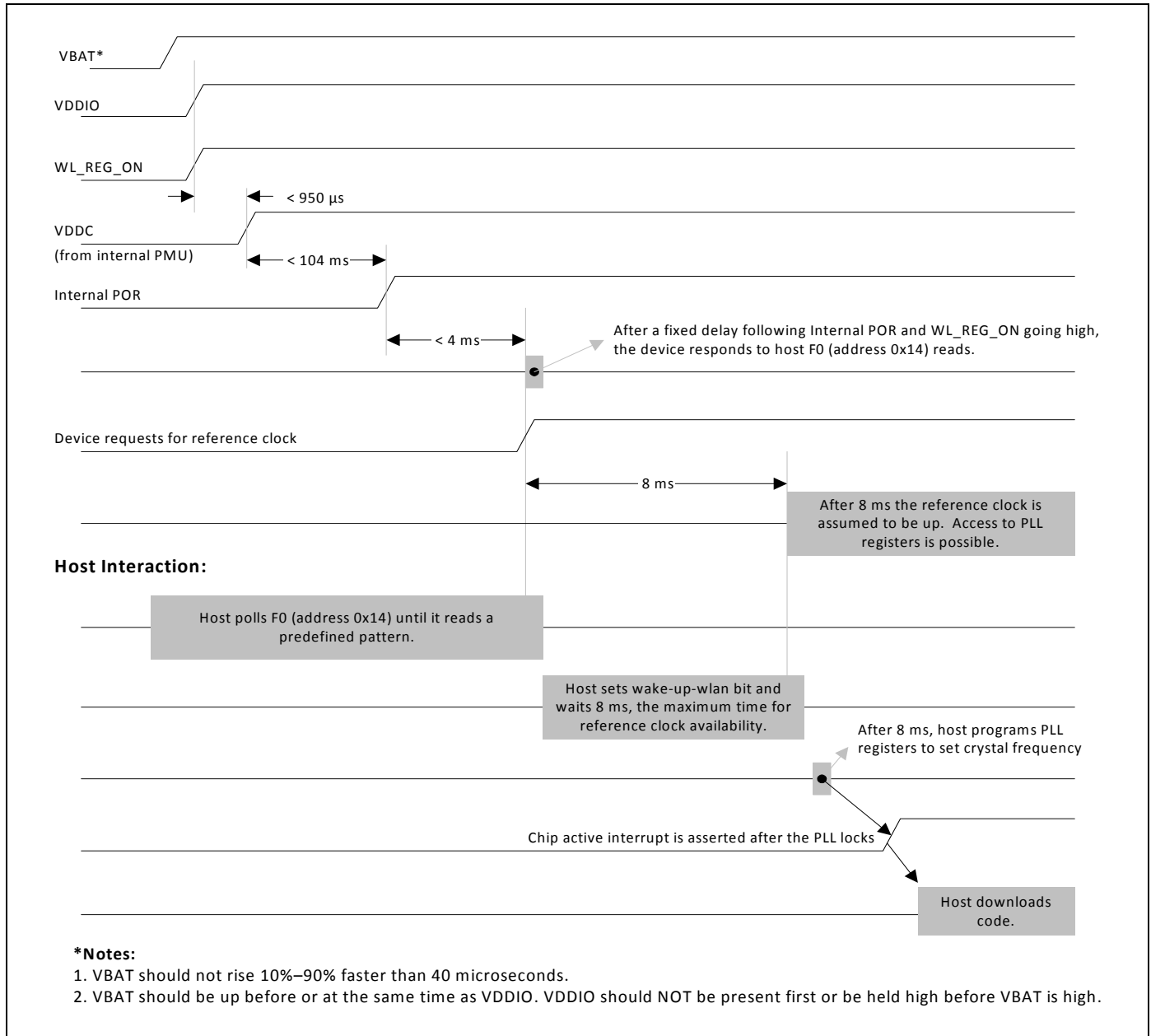


Figure 50 shows the WLAN boot-up sequence from power-up to firmware download.

Figure 50. WLAN Boot-Up Sequence



22. Package Information

22.1 Package Thermal Characteristics

The information in [Table 63](#) and [Table 64](#) is based on the following conditions:

- No heat sink, $T_A = 70^\circ\text{C}$. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51-7 (101.6 mm × 101.6 mm × 1.6 mm) and $P = 1.53\text{W}$ continuous dissipation.
- Absolute junction temperature limits are maintained through active thermal monitoring and driver-based techniques that may include duty-cycle limiting or turning off one of the TX chains, or both.

Table 63. WLCSP Package Thermal Characteristics

| Characteristic | WLCSP |
|--|-------|
| θ_{JA} ($^\circ\text{C}/\text{W}$) (value in still air) | 26.86 |
| θ_{JB} ($^\circ\text{C}/\text{W}$) | 2.23 |
| θ_{JC} ($^\circ\text{C}/\text{W}$) | 1.09 |
| ψ_{JT} ($^\circ\text{C}/\text{W}$) | 2.48 |
| ψ_{JB} ($^\circ\text{C}/\text{W}$) | 11.61 |
| Maximum Junction Temperature T_j ($^\circ\text{C}$) | 125 |
| Maximum Power Dissipation (W) | 1.53 |

Table 64. WLBGA Package Thermal Characteristics

| Characteristic | WLBGA |
|--|-------|
| θ_{JA} ($^\circ\text{C}/\text{W}$) (value in still air) | 26.80 |
| θ_{JB} ($^\circ\text{C}/\text{W}$) | 1.66 |
| θ_{JC} ($^\circ\text{C}/\text{W}$) | 1.16 |
| ψ_{JT} ($^\circ\text{C}/\text{W}$) | 1.85 |
| ψ_{JB} ($^\circ\text{C}/\text{W}$) | 7.93 |
| Maximum Junction Temperature T_j ($^\circ\text{C}$) | 125 |
| Maximum Power Dissipation (W) | 1.53 |

22.2 Junction Temperature Estimation and ψ_{JT} Versus θ_{JC}

The package thermal characterization parameter ψ_{JT} (ψ_{JT}) yields a better estimation of actual junction temperature (T_j) than using the junction-to-case thermal resistance parameter θ_{JC} (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_j = T_T + P \times \psi_{JT}$$

Where:

- T_j = Junction temperature at steady-state condition ($^\circ\text{C}$)
- T_T = Package case top center temperature at steady-state condition ($^\circ\text{C}$)
- P = Device power dissipation (Watts)
- ψ_{JT} = Package thermal characteristics; no airflow ($^\circ\text{C}/\text{W}$)

22.3 Environmental Characteristics

For environmental characteristics data, see [Table 31 on page 103](#).

23. Mechanical Information

Figure 51. 192-Ball WLBGA Package Mechanical Information

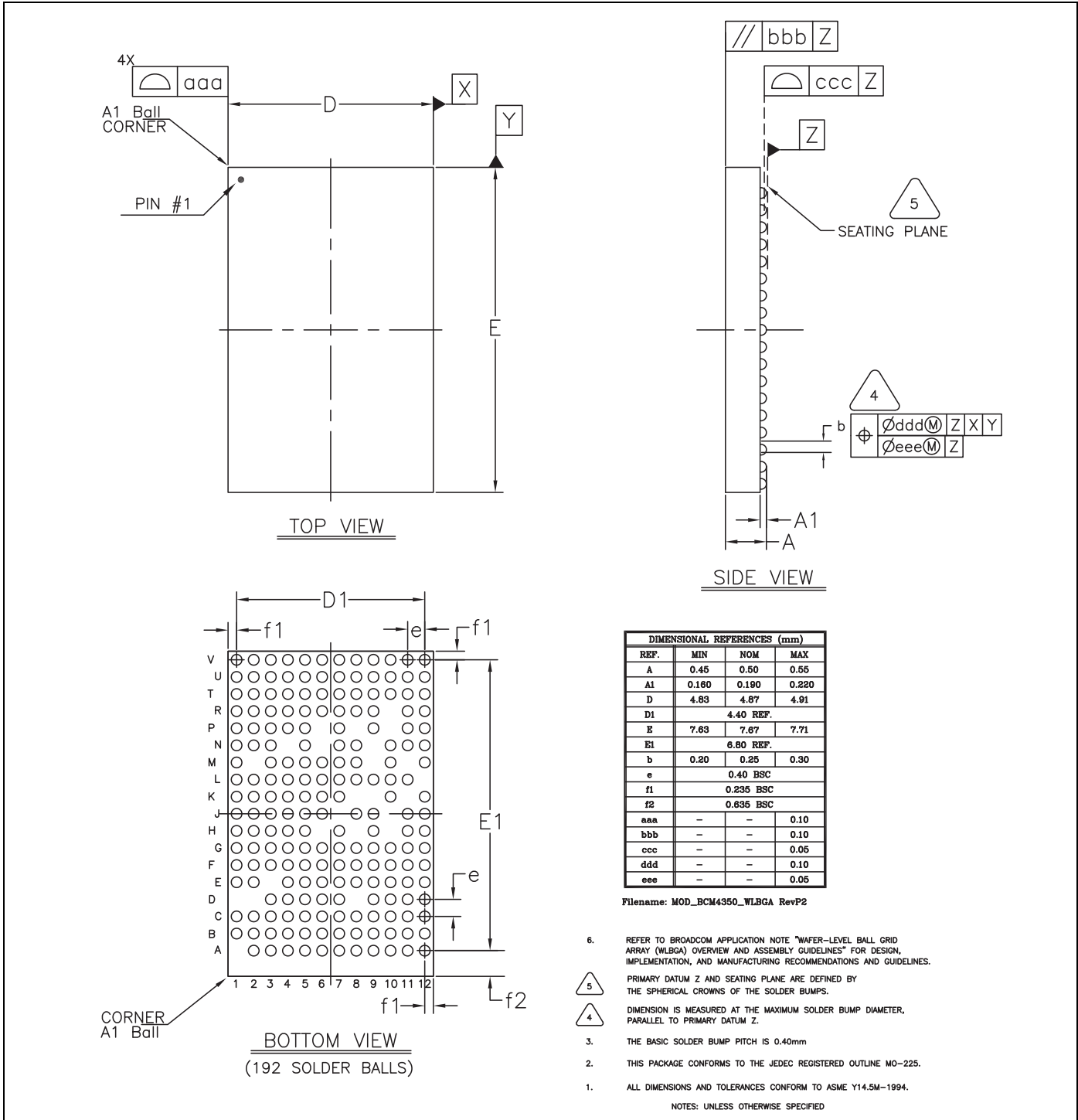


Figure 52. WLBGA Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)

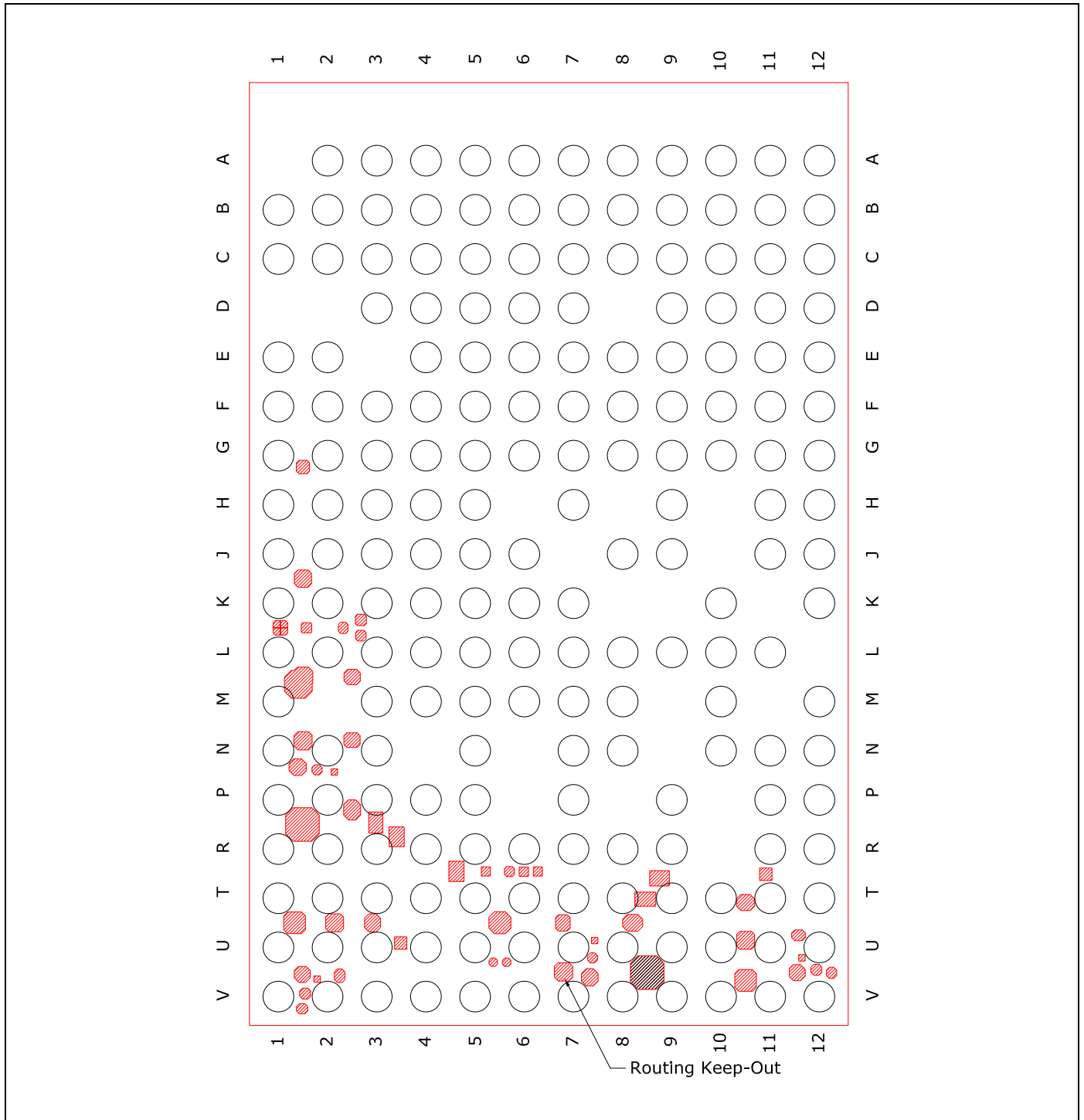


Figure 53. 395-Bump WLCSP Package

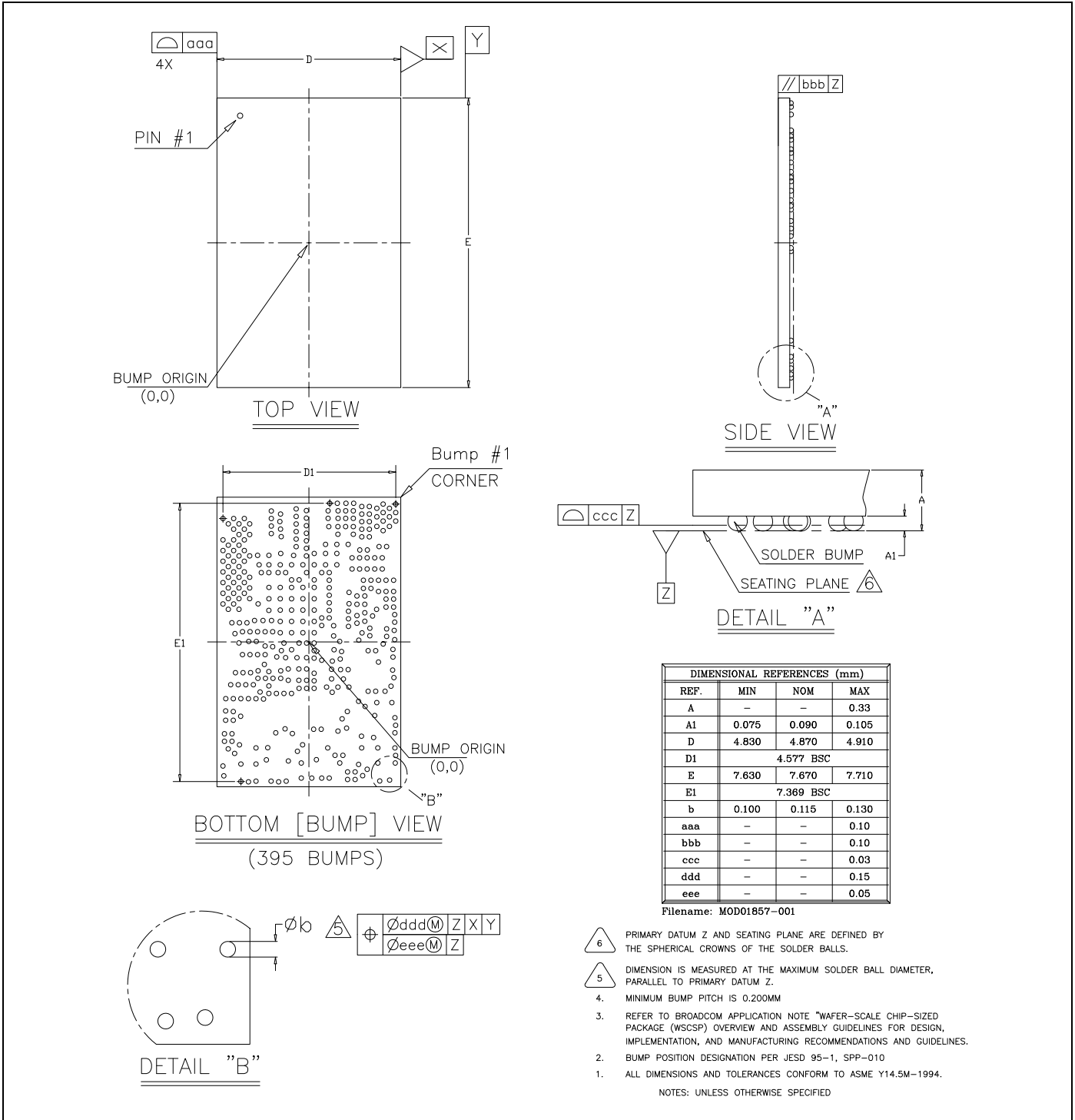
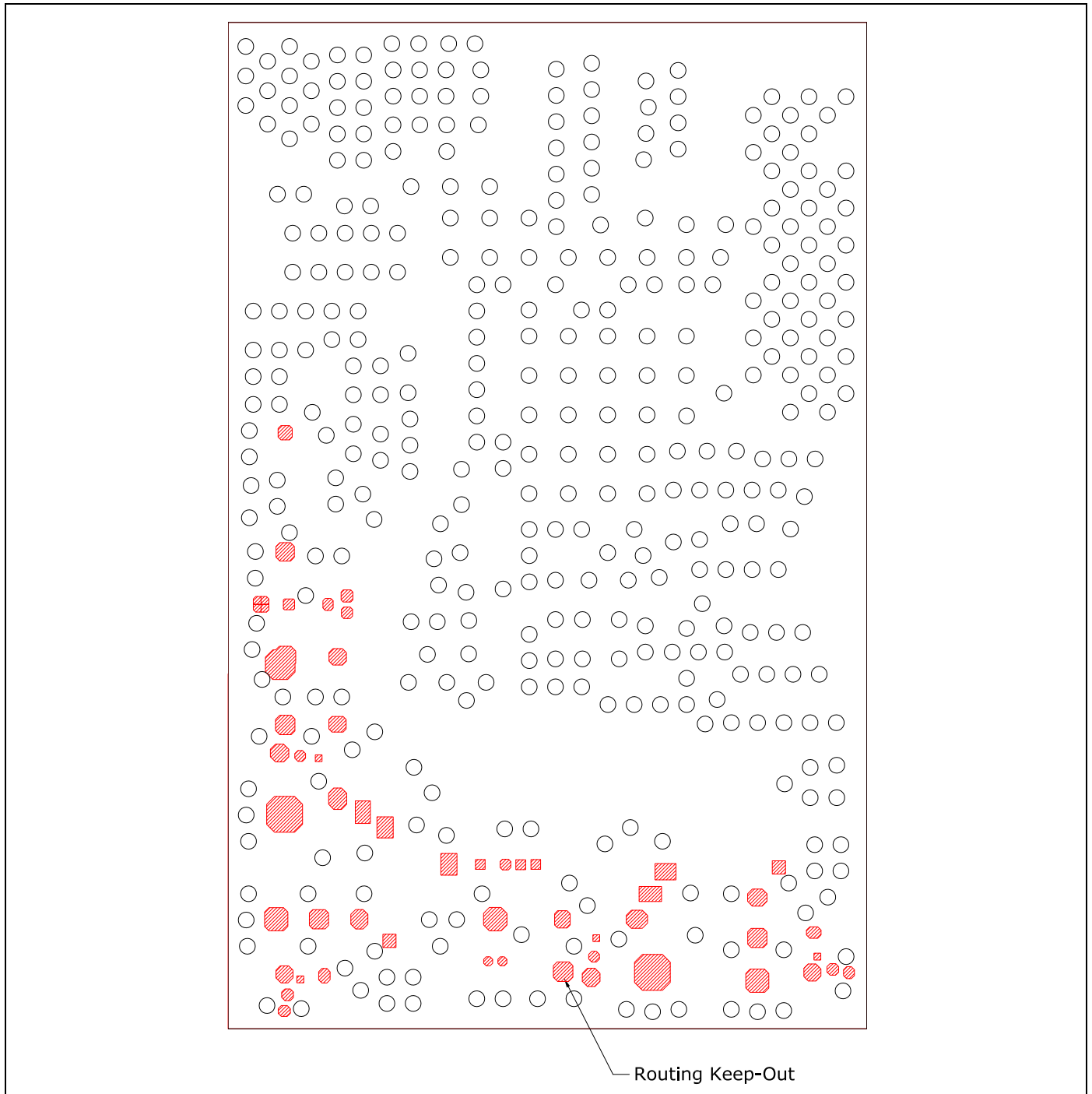


Figure 54. WLCSP Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)



24. Ordering Information

| Part Number | Package | Description | Operating Ambient Temperature |
|--------------------|--|---|--------------------------------------|
| CYW4354XKUBG | 192-ball WLBGA (4.87 mm × 7.67 mm, 0.4 mm pitch) | Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FMRX | -30°C to +85°C (-22°F to 185°F) |
| CYW4354XKWBG | 395-bump WLCSP (4.87 mm × 7.67 mm, 0.2 mm pitch) | Dual-band 2.4 GHz and 5 GHz WLAN + BT 4.0 + FMRX | -30°C to +85°C (-22°F to 185°F) |
| CYW4354ZKUBG | 192-ball WLBGA (4.87 mm × 7.67 mm, 0.4 mm pitch) | Dual-band 2.4 GHz and 5 GHz WLAN | -30°C to +85°C (-22°F to 185°F) |

Document History

| Document Title: CYW4354 Single-Chip 5G Wi-Fi IEEE 802.11ac 2x2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and FM Receiver | | | | |
|---|-----|-----------------|-----------------|--|
| Document Number: 002-14809 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | - | - | 07/31/13 | 4354-DS100-R Initial Release |
| *A | - | - | 11/06/13 | 4354-DS101-R Updated: <ul style="list-style-type: none"> Section 2: "Power Supplies and Power Management," on page 27. "WLAN Power Management" on page 29. "Crystal Interface and Clock Generation" on page 32. Table 4: "Crystal Oscillator and External Clock — Requirements and Performance," on page 33: Frequency conditions. Figure 7: "Startup Signaling Sequence," on page 43. "Receiver Path" on page 88. "Transmit Path" on page 88. Section 13: "Pinout and Signal Descriptions," on page 89. Table 29: "GPIO Alternative Signal Functions," on page 135. Table 34: "Recommended Operating Conditions and DC Characteristics," on page 142: DC supply voltage for digital I/O (minimum value). Table 42: "WLAN 2.4 GHz Receiver Performance Specifications," on page 163: SISO/MIMO RX sensitivity. Table 46: "WLAN 5 GHz Receiver Performance Specifications," on page 180: SISO/MIMO RX sensitivity. Table 51: "LDO3P3 Specifications," on page 192. Table 57: "Typical WLAN Power Consumption," on page 199. Table 58: "Bluetooth BLE and FM Current Consumption," on page 201. Section 22: "Package Information," on page 219. Section 23: "Mechanical Information," on page 221. Section 24: "Ordering Information," on page 226. Added: <ul style="list-style-type: none"> Figure 4: "Typical Power Topology for the CYW435X," on page 28. "External 32.768 kHz Low-Power Oscillator" on page 35. Table 30: "GPIO Status Vs. Test Modes," on page 136. Table 52: "LDO3P3_B Specifications," on page 193. |
| *B | - | - | 12/12/13 | 4354-DS102-R Updated: <ul style="list-style-type: none"> The CYW4354 now supports PCI Express base specification v3.0 running at Gen1 speeds. "WLAN 2.4 GHz Receiver Performance Specifications" on page 158: Note update. "WLAN 2.4 GHz Transmitter Performance Specifications" on page 170: Note update. "WLAN 5 GHz Receiver Performance Specifications" on page 174: Note update. "WLAN 5 GHz Transmitter Performance Specifications" on page 187: Note update. "Package Thermal Characteristics" on page 219: Note update. ■ Section 24: "Ordering Information," on page 227. |
| *C | - | - | 12/20/13 | 4354-DS103-R Updated: <ul style="list-style-type: none"> Table 33: "Environmental Ratings," on page 141: Ambient temperature range for functional operation is now -30°C to +85°C. |

| Document Title: CYW4354 Single-Chip 5G Wi-Fi IEEE 802.11ac 2x2 MAC/Baseband/Radio with Integrated Bluetooth 4.1 and FM Receiver | | | | |
|---|---------|------|----------|--|
| Document Number: 002-14809 | | | | |
| *D | - | - | 03/24/14 | <p>4354-DS104-R</p> <p>Updated:</p> <ul style="list-style-type: none"> Table 4: "External 32.768 kHz Sleep Clock Specifications," on page 28 Figure 33: "WLBGA Ball Map, 4.87 × 7.67 Array, 192-Balls, A7-V12 (Bottom View — Balls Facing Up)," on page 83 Table 20: "395-Bump WLCSP Coordinates," on page 90 (Modified Bump 230, see note at end of the Table 20.) Table 32: "Bluetooth Receiver RF Specifications," on page 129 (footnotes modified) <p>Table 50: "Bluetooth BLE and FM Current Consumption," on page 167</p> |
| *E | - | - | 04/02/14 | <p>4354-DS105-R</p> <p>Updated:</p> <ul style="list-style-type: none"> Table 4: "External 32.768 kHz Sleep Clock Specifications," on page 28 Figure 34: "WLBGA Ball Map, 4.87 × 7.67 Array, 192-Ball, A7-V12 (Bottom View — Balls Facing Up)," on page 84 Table 49: "Bluetooth BLE and FM Current Consumption," on page 164 "Receiver Path" on page 80 Figure 32: "Radio Functional Block Diagram (core 0)," on page 81 Table 38: "WLAN 2.4 GHz Receiver Performance Specifications," on page 139 Table 39: "WLAN 2.4 GHz Transmitter Performance Specifications," on page 145 Table 40: "WLAN 5 GHz Receiver Performance Specifications," on page 147 Table 41: "WLAN 5 GHz Transmitter Performance Specifications," on page 154 General Spurious Emissions Specifications (deleted) |
| *F | - | - | 05/20/14 | <p>4354-DS106-R</p> <p>Updated:</p> <p>Section 24: "Ordering Information," on page 189.</p> |
| *G | - | - | 06/30/14 | <p>4354-DS107-R</p> <p>Updated:</p> <ul style="list-style-type: none"> "CYW4354 PMU Features" on page 22 Figure 3: "Typical Power Topology for the CYW4354," on page 23 Table 18: "Pin List by Pin Number (192-Pin WLBGA Package)," on page 85 Table 19: "Pin List by Pin Name (192-Pin WLBGA Package)," on page 88 Table 20: "395-Bump WLCSP Coordinates," on page 91 Table 21: "WLCSP Signal Descriptions," on page 102 Table 60: "PCI Express Interface Parameters," on page 175 <p>Added:</p> <ul style="list-style-type: none"> "Electrostatic Discharge Specifications" on page 124 |
| *H | - | - | 08/08/14 | <p>4354-DS108-R</p> <p>Updated:</p> <p>Changed document type from "Preliminary Data Sheet" to "Data Sheet".</p> |
| *I | - | - | 10/15/14 | <p>4354-DS109-R</p> <p>Updated:</p> <ul style="list-style-type: none"> "I/O States" on page 99. <p><Cross-Ref>Figure 52: "WLBGA Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)," on page 159.</p> |
| *J | 5451155 | UTSV | 09/28/16 | Converted to Cypress Template |

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