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Single Chip IEEE 802.11™ a/b/g/n MAC/Baseband/Radio with Integrated Bluetooth 2.1 + EDR and FM Transceiver

GENERAL DESCRIPTION

The Broadcom® BCM4329 family of single chip devices provides for the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11™ a/b/g and handheld device class 802.11n (MAC/baseband/radio), Bluetooth® 2.1 + EDR (Enhanced Data Rate), and FM radio receiver and transmitter. It also integrates 2.4 GHz and 5 GHz WLAN CMOS power amplifiers to meet the requirements of most handheld systems while permitting an external power amplifier for even high power applications. The BCM4329 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size.

Utilizing advanced design techniques and process technology to reduce active and idle power, the BCM4329 extends the system battery life while maintaining robust connectivity and still provides a rich set of features.

The BCM4329 implements the highly sophisticated Enhanced Collaborative Coexistence radio coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative Bluetooth coexistence scheme along with coexistence support for external radios (such as GPS, WiMax, or Ultra Wide-Band radio technologies, as well as cellular radios) and a single shared antenna (2.4-GHz antenna for Bluetooth and WLAN). As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

In addition, the BCM4329 integrates a power management unit, simplifying the power topology on a system, and allowing for operation directly from the mobile platform battery.

Along with integrated power amplifiers, the BCM4329 also includes integrated transmit and receive baluns, further reducing the overall solution cost.

FEATURES

General Features

- Programmable dynamic power management
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices
- Supports battery voltage range from 2.3V to 5.5V supplies with internal switching regulator
- Integrated WLAN CMOS power amplifiers
- Flip-chip 182-ball WLBGA package (5.62 mm x 6.57 mm, 0.4 mm pitch)

IEEE 802.11x Key Features

- Single-band 2.4 GHz 802.11 b/g/n or dual-band 2.4 GHz and 5 GHz 802.11 a/b/g/n
- Provides the smallest form-factor solution with ultra low-power consumption to support low-cost requirements
- Supports IEEE 802.11d, e (WMM®, QoS, WMM-PS), h, i, j (upgradable to support k, r, and w in the future)
- Supports IEEE 802.15.2 external three-wire coexistence scheme to support additional wireless technologies such as GPS, WiMax, or UWB
- Supports standard interfaces SDIO v1.2 (50 MHz, 4-bit and 1-bit), SPI (48 MHz), and high-speed UART
- Integrated CPU with on-chip memory to allow running 802.11 firmware that provides the capability to field-upgrade with future features
- A complete reference WLAN subsystem optimized for power consumption that can also be field-upgraded with future features
- Internal fractional nPLL allows support for a wide range of reference clock frequencies
- Security:
  - WPA™- and WPA2™- (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extension- (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0) certified
  - Reference WLAN subsystem provides Wi-Fi Protected Setup™ (WPS)

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FEATURES

IEEE 802.11x Key Features *(cont.)*

- Worldwide regulatory support: Global products supported with worldwide homologated design
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.

Bluetooth and FM Key Features

- Bluetooth Core Specification Version 2.1 + EDR (up to 3 Mbps) compliant with provisions for supporting future specifications
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference

FEATURES

Bluetooth and FM Key Features (*cont.*)

- Interface support — Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data
- The FM unit supports I^2C or HCI for communication, stereo analog input and output, as well as bidirectional I^2S and PCM interfaces
- Low-power consumption improves battery life of handheld devices
- FM receiver: 76 MHz to 108 MHz FM bands and supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards
- Supports two simultaneous Advanced Audio Distribution Profile (A2DP) for stereo sound
- Automatic frequency detection for standard crystal and TCXO values
- FM transmitter: 76 MHz to 108 MHz bands, supports both RDS and the RBDS standards, and programmable output power

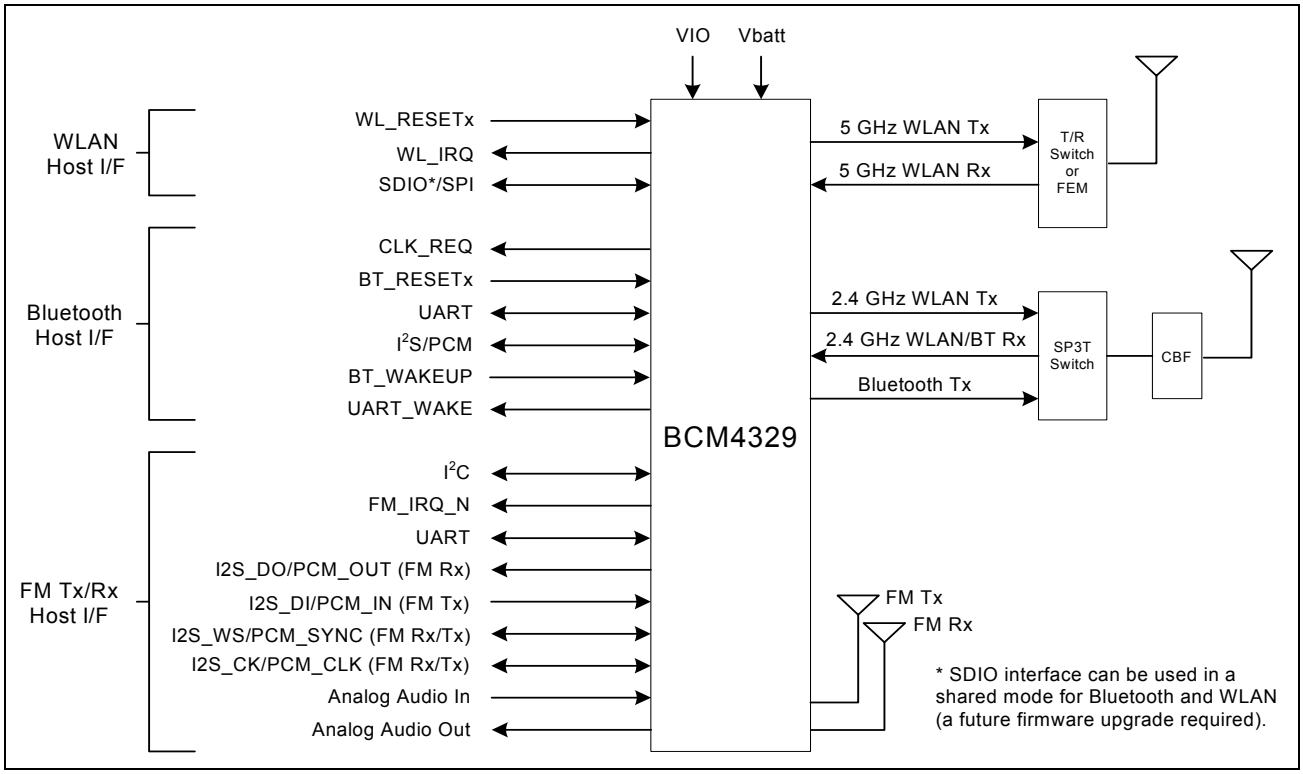

Figure 1: BCM4329 System Block Diagram

Revision History

Revision	*Date*	*Description*
002-14927 *F	09/19/16	Parts in this datasheet are not recommended for new designs.
4329-DS105-R	12/3/10	**Updated:** • Table 24: "FM Receiver Specifications," on page 101.
4329-DS104-R	04/07/10	**Updated:** • Document type to "Preliminary Data Sheet" • Table 9: "Crystal Oscillator and External Clock Performance," on page 71 • Table 12: "WLBGA Signal Descriptions," on page 79 • Table 16: "BCM4329 During and After Reset," on page 92 **Deleted:** • Chips from "Ordering Information" on page 145
4329-DS103-R	01/26/10	**Updated:** • "Features" on page 2. • "UART Interface" on page 16. • "I2S Interface" on page 17. • "FM Radio" on page 19. • "Digital FM Audio Interfaces" on page 19. • "SDIO v1.2" on page 33. • Table 4, "SDIO Bus Timing Parameters (Default Mode)," on page 35. • Figure 14, "SDIO Bus Timing (High-Speed Mode)," on page 36. • Table 5, "SDIO Bus Timing Parameters (High-Speed Mode)," on page 36. • Table 6, "SPI Timing," on page 38. • "Boot-Up Sequence" on page 43. • Figure 24, "Power Topology," on page 48. • "Crystal Interface and Clock Generation" on page 50. • Table 9, "Crystal Oscillator and External Clock Performance," on page 50. • Table 10, "LPO Signal Characteristics," on page 52. • Table 21, "ESD Specifications," on page 72. • "Recommended Operating Conditions and DC Characteristics" on page 72. • Table 23, "Bluetooth Receiver RF Specifications," on page 74. • Table 24, "Bluetooth Transmitter RF Specifications," on page 76. • Table 26, "FM Transmitter Specifications," on page 78. • Table 27, "FM Receiver Specifications," on page 80. • Table 30, "WLAN 5-GHz Receiver Performance Specifications," on page 87. • Table 31, "WLAN 2.4-GHz Transmitter Performance Specifications," on page 89. • Table 32, "WLAN 5-GHz Transmitter Performance Specifications," on page 91. • Table 33, "General Spurious Emissions Specifications," on page 92.

Revision	*Date*	*Description*
4329-DS103-R	01/26/10	**Updated:** • Table 40, ”WLAN Power Consumption (lvbat+lvio),” on page 97. • “Bluetooth and FM Current Consumption” on page 99. • “Package Thermal Characteristics” on page 112. **Added:** • Table 16, ”BCM4329 During and After Reset,” on page 67.
4329-DS102-R	06/01/09	**Added:** • “SDIO Default Mode Timing” on page 35. • “SDIO High-Speed Mode Timing” on page 36. • Updated: • FM unit support for HCI or I2C on the cover page and in “Features” on page 2. • Figure 3, ”Mobile Phone Block System Diagram,” on page 7. • “Host Controller Power Management” on page 11 including Table 1. • “BBC Power Management” on page 12. • “FM Power Management” on page 13. • “Slot Mapping” on page 16. • “PCM Interface for FM Rx and Tx Audio” on page 16. • “I2S Interface” on page 17 by changing I2S_SCK to I2S in one sentence. • “FM Radio” on page 19 and “Digital FM Audio Interfaces” on page 19. • “SDIO v1.2” on page 33. • Table 4, ”SDIO Bus Timing Parameters (Default Mode),” on page 35 footnote. • “SDIO High-Speed Mode Timing” on page 36. • Table 5, ”SDIO Bus Timing Parameters (High-Speed Mode),” on page 36 footnote. • “Power Supply Topology” on page 48. • Table 9, ”Crystal Oscillator and External Clock Performance,” on page 51. • Table 10, ”LPO Signal Characteristics,” on page 53. • Table 12, ”WLBGA Signal Descriptions,” on page 58. • Table 14, ”BCM4329 During and After Reset,” on page 65. • Table 15, ”BCM4329 During Sleep,” on page 67. • Table 20, ”ESD Specifications,” on page 72. • Table 21, ”Recommended Operating Conditions and DC Characteristics,” on page 72. • Table 22, ”Bluetooth Receiver RF Specifications,” on page 74. • Table 23, ”Bluetooth Transmitter RF Specifications,” on page 76. • Table 25, ”FM Transmitter Specifications,” on page 78, by changing kHz to Hz for the lower 3 dB point associated with stereo separation. • Table 26, ”FM Receiver Specifications,” on page 80.

Revision	*Date*	*Description*
4329-DS102-R	06/01/09	**Added:** • Table 27, ”2.4-GHz Band General RF Specifications,” on page 85. • Table 28, ”WLAN 2.4-GHz Receiver Performance Specifications,” on page 86. • Table 29, ”WLAN 5-GHz Receiver Performance Specifications,” on page 88. • Table 30, ”WLAN 2.4-GHz Transmitter Performance Specifications,” on page 90. • Table 31, ”WLAN 5-GHz Transmitter Performance Specifications,” on page 92. • Table 32, ”General Spurious Emissions Specifications,” on page 93. • “PMU Total Quiescent Currents in Each Mode” on page 97. • Section 23 ”System Power Consumption” on page 98. • Section 27 ”Ordering Information” on page 115. • Table 46, ”Package Thermal Characteristics,” on page 113.

Revision	*Date*	*Description*
4329-DS101-R	01/22/09	**Added:** • Figure 23, ”182-Ball WLBGA Ball Map (Bottom view),” on page 54. • “Sequencing of Reset and Regulator Control Signals” on page 102. **Updated:** • “Features” on page 2 in Section 1: BCM4329 Overview. • “Features” on page 5 in Section 2: Bluetooth + FM Subsystem Overview. • “Power Amplifier” on page 8 and “Link Control Layer” on page 9. • “I2C-Compatible Bus” on page 19. • ”SDIO v1.2” and Table 3, ”SDIO Pin Description,” on page 33. • Figure 21, ”Power Topology,” on page 46. • Table 6, ”SPI Registers,” on page 41. • Figure 21, ”Power Topology,” on page 46. • Table 7, ”Crystal Oscillator and External Clock Performance,” on page 48. • Table 8, ”LPO Signal Characteristics,” on page 50. • Table 9, ”182-Ball WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates (Units = mm),” on page 52. • Table 10, ”WLBGA Signal Descriptions,” on page 55. • Table 14, ”GPIO Multiplexing Matrix,” on page 64. • “Absolute Maximum Ratings” on page 66. • Table 19, ”Recommended Operating Conditions and DC Characteristics,” on page 67. • Section 18 ”Bluetooth RF Specifications” on page 68. • Table 20, ”Bluetooth Receiver RF Specifications,” on page 69. • Table 21, ”Bluetooth Transmitter RF Specifications,” on page 71. • Section 19 ”FM Transmitter Specifications” on page 73. • Section 20 ”FM Receiver Specifications” on page 75. • Section 21 ”WLAN RF Specifications” on page 79. • Table 26, ”WLAN 2.4-GHz Receiver Performance Specifications,” on page 81.

Revision	*Date*	*Description*
4329-DS101-R	01/22/09	**Updated:** • Table 27, ”WLAN 5-GHz Receiver Performance Specifications,” on page 83. • Table 29, ”WLAN 5-GHz Transmitter Performance Specifications,” on page 86. • Section 22 ”Internal Regulator Electrical Specifications” on page 88. • Section 23 ”System Power Consumption” on page 92. • Section 24 ”Interface Timing and AC Characteristics” on page 93 introductory text. • Table 42, ”Package Thermal Characteristics,” on page 106. • Table 43, ”Environmental Characteristics,” on page 106 and renamed table. • Figure 33, ”182-Ball WLBGA Mechanical Information (5.62 mm x 6.57 mm, 0.4 mm Pitch),” on page 108. • Section 27 ”Ordering Information” on page 109. **Removed:** • Sections previously entitled “PALD0 with External PNP”, “Bandgap Reference Block (HVBG)”, “LDO Bandgap Reference (LDOBG)”, and “PMU4329”.
4329-DS100-R	05/15/08	Initial release.

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Section 1: BCM4329 Overview

Overview

The Broadcom® BCM4329 family of single chip devices provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11™ a/b/g/n (MAC/baseband/radio), Bluetooth 2.1 + EDR (Enhanced Data Rate), and FM transceiver. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The BCM4329 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM4329 and their associated external interfaces, which are described in greater detail in the following sections.

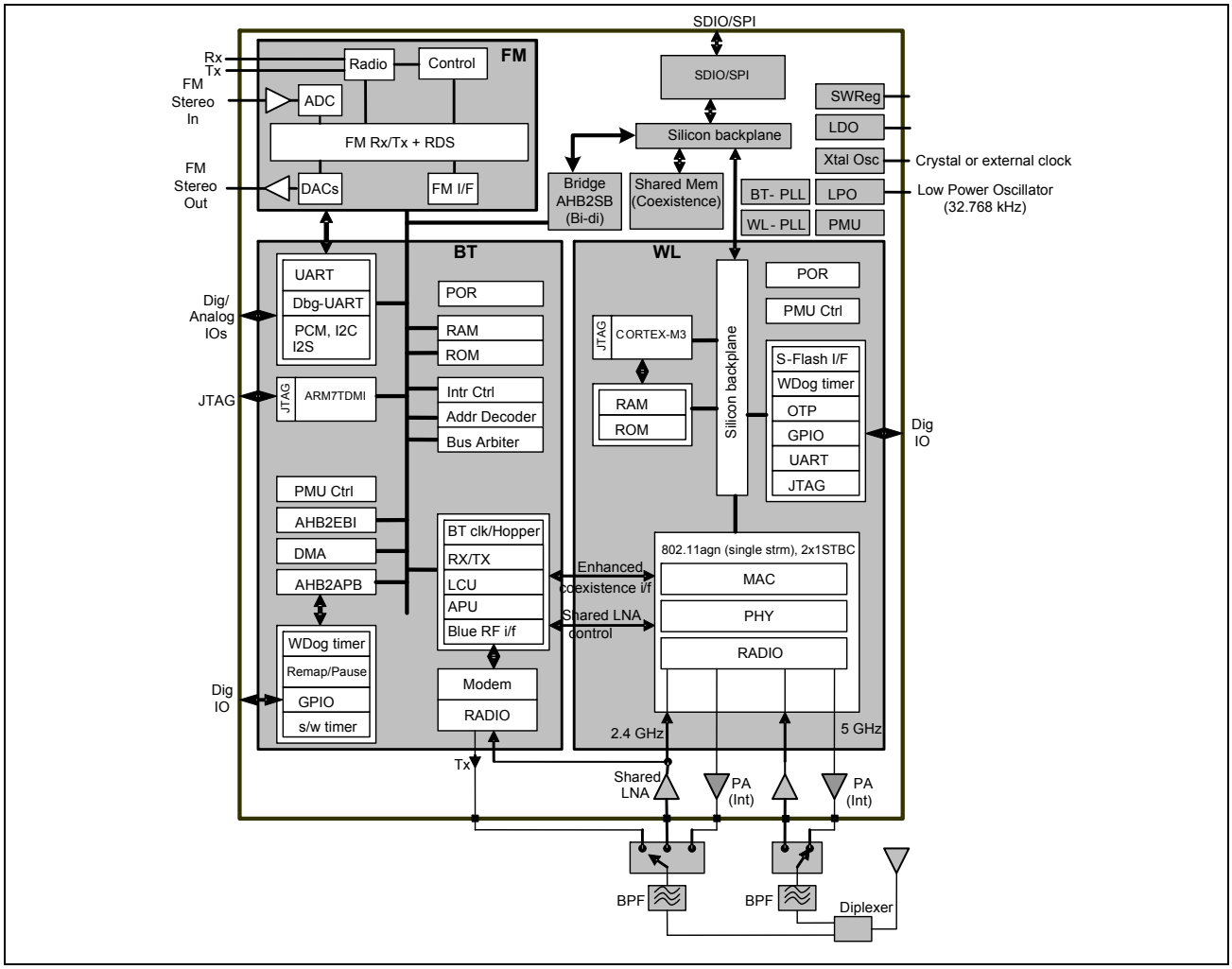

Figure 2: BCM4329 Block Diagram

Features

The BCM4329 supports the following features:

- 802.11a/b/g/n dual-band radio — non-simultaneous dual-band operations
- Bluetooth v2.1 + EDR with integrated Class 1 PA
- FM RDS TX/RX
- On-chip WLAN driver execution capable of supporting 802.11 functionality
- Single- and dual-antenna support
  - Single antenna without external switch (shared LNA)
  - Simultaneous BT/WLAN receive with single antenna
  - Support for a 2×1 dual receiver system
- WLAN host interface
  - SPI — up to 48 MHz clock rate
  - SDIO v1.2x (1-bit/4-bit) — up to 50 MHz clock rate
- BT only digital Interface (can be used concurrently with above interfaces):
  - UART (up to 4 Mbps)
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I^2S/PCM for FM/BT audio
- I^2C/HCI for FM block control
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)

Standards Compliance

The BCM4329 supports the following standards:

- Bluetooth 2.1 + EDR
- 76 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n — Handheld Device Class (Section 11)
- 802.11a
- 802.11b
- 802.11g
- 802.11d
- 802.11h
- 802.11i
- 802.11j

The BCM4329 will support the following future drafts/standards:

- 802.11r — Fast Roaming (between APs)
- 802.11k — resource management
- 802.11w — Secure Management Frames
- 802.11 Extensions:
  - 802.11e QoS Enhancements (as per the WMM® specification is already supported)
  - 802.11h 5 GHz Extensions
  - 802.11i MAC Enhancements
  - 802.11r Fast Roaming Support
  - 802.11k Radio Resource Measurement
- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC
- 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3 wire requirements

Section 2: Bluetooth + FM Subsystem Overview

The Broadcom BCM4329 is a Bluetooth 2.1 + EDR-compliant, baseband processor/ 2.4 GHz transceiver with an integrated FM/ RDS/RBDS receiver and FM/RDS transmitter. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus FM radio solution.

The BCM4329 is the optimal solution for any Bluetooth voice and/or data application that also requires an FM radio receiver and transmitter. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM for audio. The FM subsystem supports I^2C-compatible and HCI control interfaces, analog input and output, as well as I^2S and PCM interfaces. The BCM4329 incorporates all Bluetooth 2.1 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The BCM4329 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

Features

Major Bluetooth features of the BCM4329 include:

- Supports key features of upcoming Bluetooth standards
- Class 1 support with Power Amplifier (PA) bias adjust
- Fully supports Bluetooth Core Specification version 2.1 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO) — Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 2.1 + EDR packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_WAKE and UART_WAKE signaling (see "Host Controller Power Management" on page 29)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

Major FM Radio features include:

- 76 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- FM subsystem control using I^2C-compatible bus or through Bluetooth HCI interface
- FM subsystem operates from 32.768-kHz low-power oscillator (LPO) or reference clock inputs
- Improved audio interface capabilities with full-featured bidirectional PCM, I^2S, and analog stereo DAC and ADC
- I^2S can be master or slave for FMRX. I^2S slave mode is supported for FMTX.

FM Receiver-Specific Features Include:

- Excellent FM radio performance with 1-µV sensitivity for 26 dB (S+N)/N
- Signal-dependent stereo/mono blending
- Signal dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RSSI, IF frequency, status indicators
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump

FM Transmitter-Specific Features Include:

- Programmable output power with +117 dBµV maximum output power and 24 dB range
- RDS and RBDS encoder and modulator with intelligent frame encoding and programmable scroll rate
- Programmable audio swing to FM modulation deviation
- Programmable mono or stereo transmission
- Concurrent Bluetooth v2.1 + EDR and FM transmit functionality
- Digital audio input from I^2S or PCM
- Host programmable frequency from 76 MHz to 108 MHz in 50 kHz channel steps
- Digitally programmable audio level and mute control

Mobile Phone Usage Model

The BCM4329 has flexible PCM and UART interfaces, enabling it to transparently connect with existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to minimize the size, power, and cost of a complete system.

The BCM4329 incorporates a number of unique features to accommodate the integration into mobile phone platforms.

- The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid interfacing to single or multiple external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- The TCXO interface accommodates any of the typical reference frequencies used by cell phones.
- The I^2C-compatible and analog FM interface is available for legacy systems.
- FM digital interfaces can use either I^2S or PCM.
- The highly linear design of the radio transceiver ensures that the device has the lowest spurious emissions output regardless of the state of operation. It has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of a any cellular transmission (GSM®, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The BCM4329 is designed to provide direct interface with new and existing handset designs as shown in Figure 3.

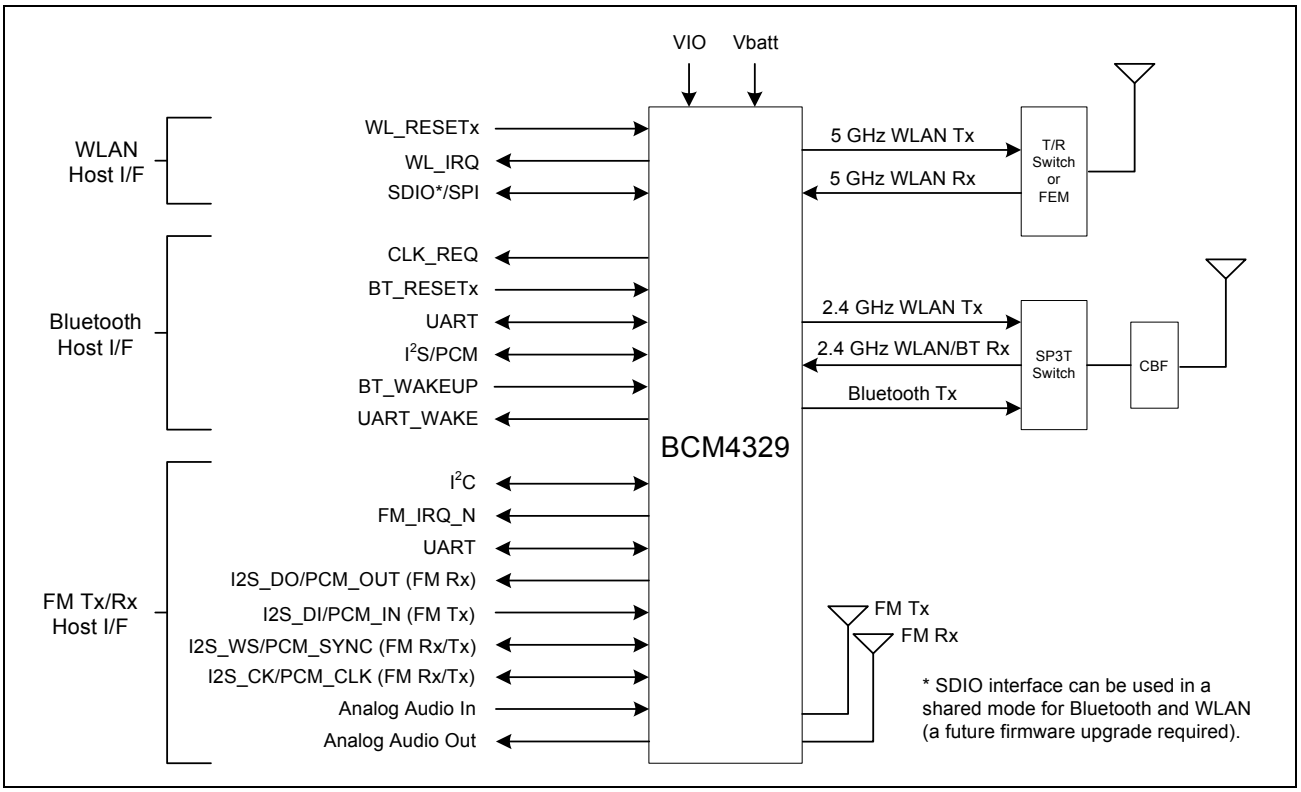

Figure 3: Mobile Phone Block System Diagram

Bluetooth Radio

The BCM4329 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The BCM4329 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates $\pi/4$-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter PA bias can also be adjusted to provide Bluetooth Class 1 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications where the Bluetooth is integrated next to the cellular radio, minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM4329 to be used in most applications with no off-chip filtering. For integrated handset operation, where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Receiver Signal Strength Indicator

The radio portion of the BCM4329 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM4329 uses an internal RF and IF loop filter.

Calibration

The BCM4329 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 3: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 2.1 Features

The BBC supports all Bluetooth 2.1 features, including:

- Extended Inquiry Response (EIR): Shortens the time to retrieve device name, specific profile, and mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Simple Pairing (SP): Reduces the number of steps with minimal or no user interaction when connecting two devices.
- Link Supervision Timeout (LST)

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page

- Page Scan
- Inquiry
- Inquiry Scan
- Sniff

Test Mode Support

The BCM4329 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 2.1*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM4329 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM4329 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management
- FM Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

When running in UART mode, the BCM4329 may be configured so that dedicated signals are used for power management hand-shaking between the BCM4329 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Table 1 describes the power-control hand-shake signals used with the UART interface.

Table 1: Power Control Pin Description

Signal	*Mapped to Pin*	*Type*	*Description*
BT_WAKE	BT_GPIO_0	I	Bluetooth device wake-up: Signal from the host to the BCM4329 indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deasserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
UART_WAKE	BT_GPIO_1	O	Host wake up. Signal from the BCM4329 to the host indicating that the BCM4329 requires attention. • Asserted: Host device must wake-up or remain awake. • Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	XTAL_PU	O	The BCM4329 asserts XTAL_PU when it wants the host to turn on the reference clock. The polarity of this signal is programmable based on BT_TM0. If BT_TM0 is connected to ground, then XTAL_PU asserts high, and the BCM4329 drives XTAL_PU high when it wants the clock turned on. (It is pulled low-otherwise.) If BT_TM0 is connected to VDDIO, then XTAL_PU asserts low. Add an external 100 kΩ pull-down or pull-up resistor, depending on the state of BT_TM0, to keep the signal deasserted during BCM4329 power-up or reset when VDDIO is present.

Note: Pad function Control Register is set to 0 for these pins. See "Muxed Bluetooth GPIO Signals" on page 88 for more details.

BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection modes are sniff, hold, and park. While in these modes, the BCM4329 runs on the low-power oscillator and wakes up after a predefined time period. See Table 9 on page 69 for LPO clock requirement details.

FM Power Management

The BCM4329 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems. The FM block does not have a low power state, it is either on or off.

Adaptive Frequency Hopping

The BCM4329 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

Advanced Bluetooth/WLAN Coexistence

The BCM4329 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and 802.11g. Dual-antenna applications are also supported. The BCM4329 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM4329 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM4329 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

Fast Connection (Interlaced Page and Inquiry Scans)

The BCM4329 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 4: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on ARM7TDMIS® 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM® core is paired with a memory unit that contains 256 KB of ROM memory for program storage and boot ROM, 56 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM4329 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM2045 and BCM2048 device.

RAM, ROM, and Patch Memory

The BCM4329 Bluetooth core has 56 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 256 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Reset

The BCM4329 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The reset can also be driven by an active-low, external reset signal, BT_RST_N, that can be used to externally control the device, forcing it into a power-on reset state. (Note that the BT_RST_N signal is independent of the POR reset.)

Section 5: Bluetooth Peripheral Transport Unit

PCM Interface for Bluetooth and SCO Audio

The PCM Interface on the BCM4329 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM4329 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM4329.

The BCM4329 supports up to three SCO or eSCO channels through the PCM Interface and each channel can be independently mapped to any of the available slots in a frame.

The configuration of the PCM interface may be adjusted by the host through the use of Vendor Specific HCI Commands.

Figure 4 shows three options for connecting a BCM4329 to a PCM codec device as either a master or slave connection.

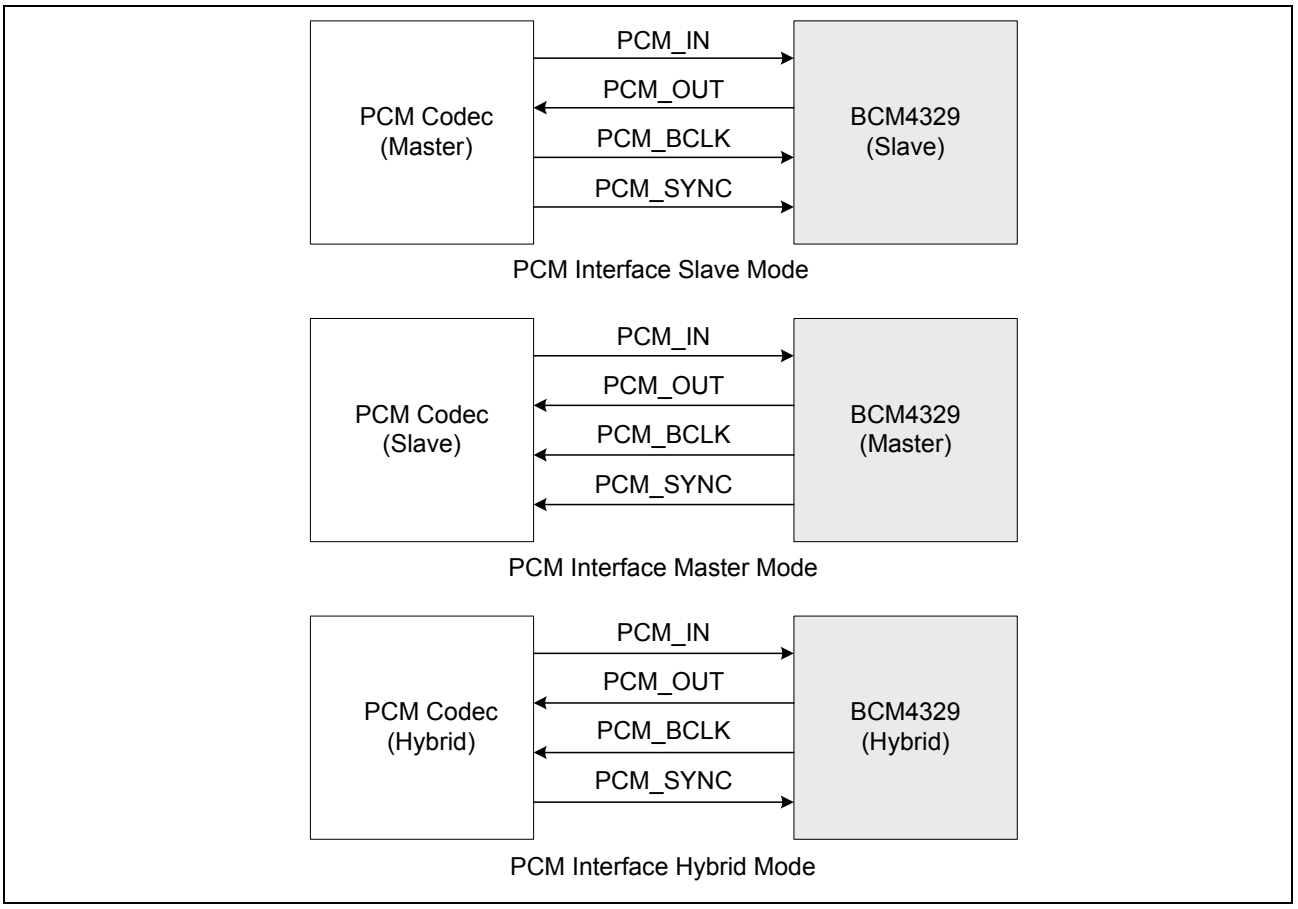

Figure 4: BCM4329 PCM Interface with Linear PCM Codec

Slot Mapping

The BCM4329 supports up to three simultaneous full-duplex SCO or eSCO channels. These three channels are time-multiplexed onto the single PCM interface by using a time slotting scheme where the 8-kHz audio sample interval is divided into up to 16 slots. The number of slots is dependant on the selected interface rate of 128 kHz, 256 kHz, 512 kHz, 1024 kHz, or 2048 kHz. The corresponding number of slots for these interface rates is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot. The PCM data output has an internal pull-down resistor that is enabled during the allocated time slot.

Frame Sync

The BCM4329 supports both short and long frame sync types in both master and slave configurations. In the short frame sync mode, the frame sync signal is an active-high pulse at the 8-kHz audio frame rate that is a single-bit period in width and synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In the long frame sync mode, the frame sync signal is again an active-high pulse at the 8-kHz audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The BCM4329 may be configured to generate and accept several different data formats. The BCM4329 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with 0s, 1s, sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left-justified, and clocked MSB first.

PCM Interface for FM Rx and Tx Audio

The BCM4329 also supports a mode where the FM stereo audio is output over the PCM interface in master or slave mode. A PCM_SYNC sample rate of 48 kHz is supported with associated PCM_CLK rate of 1.536 MHz. The PCM_SYNC signal follows the short frame sync format. In this FM audio mode, PCM_IN is used for FM Tx, and PCM_OUT is used for FM Rx. The ordering of stereo audio data on PCM_OUT and PCM_IN is 16 bits of left-channel data followed by the 16 bits of right-channel data with the most significant bit presented first.

UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface defaults to a baud rate of 115.2 Kbps coming out of reset. The desired high-speed baud rate may be selected via a vendor-specific UART HCI command. The BCM4329 has a 480-byte receive FIFO and a 480-byte transmit FIFO to support EDR. The interface supports the Bluetooth 2.1 UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

In order to support both high and low baud rates efficiently, the UART clock can be selected as either 24 or 48 MHz. Generally, the higher speed clock is needed for baud rates over 3 Mbaud, however a lower speed clock may be used to achieve a more accurate baud rate under 3 Mbaud.

The legacy method of programming the high-speed baud rate of the BCM4329 UART using DHBR and DLBR values is also supported for backward compatibility with previous-generation BCM20xx Bluetooth devices.

Normally, the UART baud rate is set by a configuration record downloaded after reset, or by automatic baud rate detection and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The BCM4329 UART operates correctly with the host UART, provided the combined baud rate error of the two devices is within 2%.

I²S Interface

The I²S interface for FM audio supports both master and slave modes for FMRX. The I²S interface for FM audio supports only slave mode for FMTX. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. I²S data input is used for FM Tx. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the BCM4329 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider. When the input/output clk frequency divide ratio (for example, 26 Mhz/1.536 Mhz) is not an integer, there is a clock cycle jitter (1/26 Mhz).

In slave mode, any clock rate is supported to a maximum of 6 MHz. The I²S interface is available as multiplexed signals onto the following:

- PCM interface
- Class 1 control signals

The I²S interface for FMTX can only support a 48 kHz data sampling rate. The bit clock frequency has to be 1.536 MHz unless the interface can support clock gating.

Section 6: FM Transceiver Subsystem

FM Radio

The BCM4329 includes a completely integrated FM radio receiver and transmitter with RDS/RBDS covering all FM bands from 76 MHz to 108 MHz. The transceiver is controlled through commands on the I^{2}C-compatible bus or the HCI. FM received audio is available as stereo analog output or in digital form through I^{2}S or PCM. The FM audio to be transmitted can be delivered via stereo analog audio input or in digital form via the I^{2}S or PCM interface. The FM radio is running from the 32.768 kHz LPO clock.

Digital FM Audio Interfaces

The FM audio can be received or transmitted via the shared PCM and I^{2}S pins, and the sampling rate is nominally at 48 kHz. The BCM4329 supports a three-wire PCM or I^{2}S audio interface in either master or slave configuration. The master or slave configuration is selected using vendor specific commands over the HCI interface. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks. In master mode, the clock rate is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

In slave mode, any clock rate is supported to a maximum of 6 MHz.

Analog FM Audio Interfaces

The demodulated FM audio signal is available as line-level analog stereo output, generated by twin internal high SNR audio DACs. The FM transmitted audio can be delivered via analog stereo high SNR audio ADCs.

I^{2}C-Compatible Bus

The BCM4329 implements a slave I^{2}C-compatible bus interface for control of the FM subsystem. The interface supports a clock rate up to 400 kHz. The I^{2}C-compatible slave address is programmable using the UART HCI interface and requires a configuration download over the UART HCI interface in order to be operable. The default slave address is 0x22. The interface supports seven-bit addressing mode. The I^{2}C-compatible bus interface is dependent upon the reference clock input being active. Pull-ups on the external bus may be required.

Initial I^{2}C communication has to be conducted at 100 kHz.

RDS/RBDS

The BCM4329 integrates a RDS/RBDS modem and codec, the decoder includes programmable filtering and buffering functions, and the encoder includes the option to encode messages to PS or RT frame format with programmable scrolling in PS mode. The RDS/RBDS data can be read out in receive mode or delivered in transmit mode through either the HCI or I^2C-compatible interface.

In addition, the RDS/RBDS functionality supports the following:

Receive

- Block decoding, error correction and synchronization
- Flywheel synchronization feature, allowing the host to set parameters for acquisition, maintenance, and loss of sync. (It is possible to set up the BCM4329 such that synch is achieved when a minimum of two good blocks (error free) are decoded in sequence. The number of good blocks required for sync is programmable.)
- Storage capability up to 126 blocks of RDS data
- Full or partial block B match detect and interrupt to host
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection and interrupt to host
- Automatic frequency jump
- Block E filtering
- Soft mute
- Signal dependent mono/stereo blend
- Programmable pre-emphasis

Transmit

- Support simple block encoding or RT/PS message to frame encoding (RT/PS mode minimizes host communication for improved system power saving)
- Programmable scroll rate in PS mode
- 256 bytes of storage for either RT/PS message or simple RDS/RBDS blocks
- Programmable de-emphasis

Other Features

- Single-ended or differential FM RF input
- Auto search and tuning
- Digital-level indicator (RSSI, IF Frequency)
- Low current consumption

Section 7: Wireless LAN Functional Description

Introduction to IEEE Std 802.11

IEEE Std 802.11 defines two different ways to configure a wireless network: *ad hoc* mode and *infrastructure* mode. In ad hoc mode, nodes are brought together to form a network on the fly, whereas infrastructure mode uses fixed access points through which mobile nodes can communicate. These network access points are sometimes connected to wired networks through bridging or routing functions.

The medium access control (MAC) layer is a contention-resolution protocol that is responsible for maintaining order in the use of a shared wireless medium. IEEE 802.11 specifies both contention-based and contention-free channel access mechanisms. The contention-based scheme is also called the distributed coordination function (DCF) and the contention-free scheme is also called the point coordination function (PCF).

The DCF employs a carrier sense multiple access with collision avoidance (CSMA/CA) protocol. In this protocol, when the MAC receives a packet to be transmitted from its higher layer, the MAC first listens to ensure that no other node is transmitting. If the channel is clear, it then transmits the packet. Otherwise, it chooses a random *backoff factor* that determines the amount of time the node must wait until it is allowed to transmit its packet. During periods in which the channel is clear, the MAC waiting to transmit decrements its backoff counter, and when the channel is busy, it does not decrement its backoff counter. When the backoff counter reaches zero, the MAC transmits the packet. Because the probability that two nodes will choose the same backoff factor is low, collisions between packets are minimized. Collision detection, as employed in Ethernet, cannot be used for the radio frequency transmissions of devices following IEEE 802.11. The IEEE 802.11™ nodes are half-duplex—when a node is transmitting, it cannot hear any other node in the system that is transmitting because its own signal drowns out any others arriving at the node.

Optionally, when a packet is to be transmitted, the transmitting node can first send out a short request to send (RTS) packet containing information on the length of the packet. If the receiving node hears the RTS, it responds with a short clear to send (CTS) packet. After this exchange, the transmitting node sends its packet. When the packet is received successfully, as determined by a cyclic redundancy check (CRC), the receiving node transmits an acknowledgment (ACK) packet. This back-and-forth exchange is necessary to avoid the *hidden node* problem. Hidden node is a situation where node A can communicate with node B, node B can communicate with node C, but node A cannot communicate with node C. For instance, although node A can sense that the channel is clear, node C can be transmitting to node B. This protocol alerts node A that node B is busy, and that it must wait before transmitting its packet.

MAC Features

The BCM4329 WLAN MAC supports features specified in the 802.11 base standard, and amended by 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multi-phase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, and support for key management
- Support for co-existence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The 4329 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising on Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes, that have been implemented, allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 5.

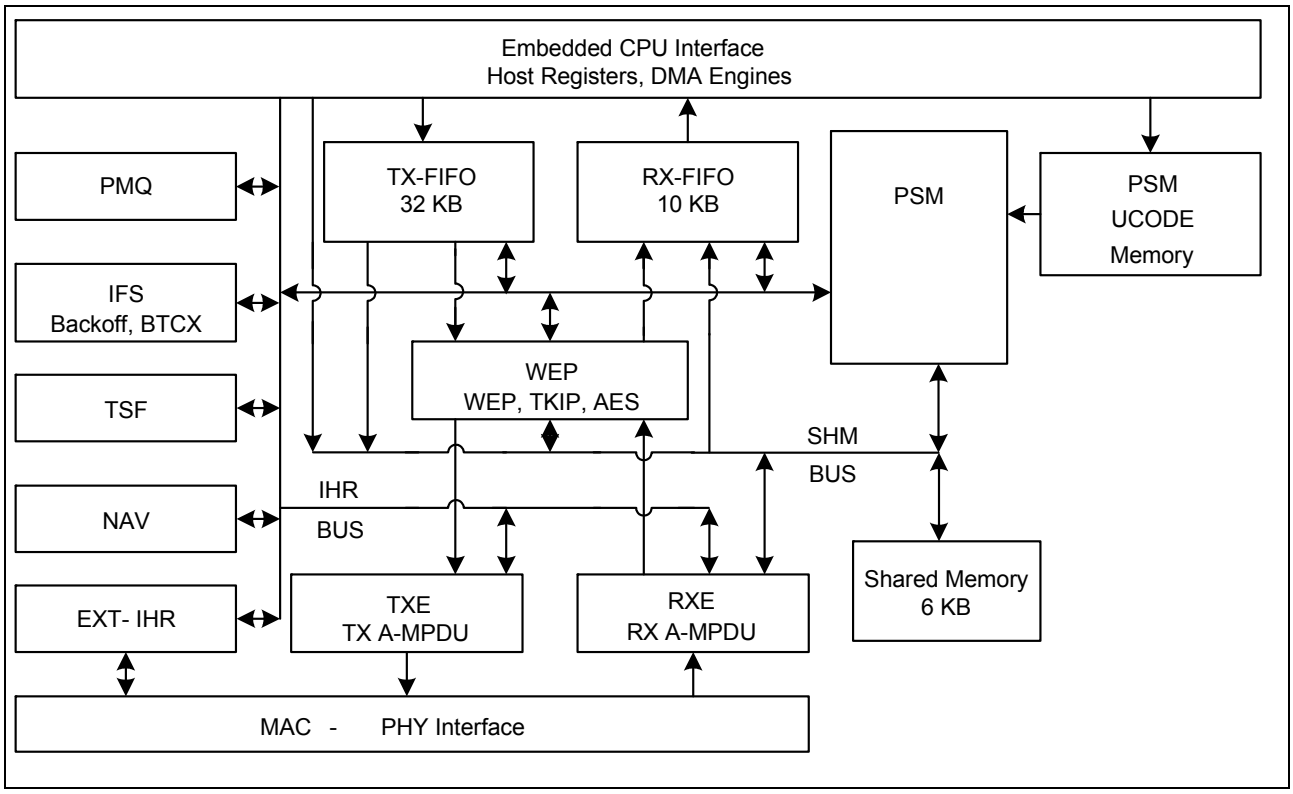

Figure 5: WLAN MAC Architecture

The following sections provide an overview of the important modules in the MAC.

PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the 802.11 specification. It is a micro-controller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit datapath of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive datapath of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a datapath interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

PHY Features

- Supports IEEE 802.11a, 11b, 11g, 11n single stream and 11j PHY standards
- Supports Optional Short GI and Green Field modes in Tx and Rx. Supports optional STBC receive of two space-time stream.
- Supports 802.11h/k for worldwide operation
- Algorithms achieving low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Simultaneous Rx-Rx (WL-BT) architecture
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications.
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle non-idealities of direct conversion CMOS RF chip On-the-fly channel frequency and transmit power selection
- Supports per packet Rx Antenna diversity
- Designed to meet FCC and other regulatory requirements

PHY Description

The BCM4329 WLAN Digital PHY is designed to comply with IEEE 802.11a/b/g/j/n single stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 72.2 Mbps for low power, high performance handheld applications.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the Filters, FFT and Viterbi-decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust 11b demodulator. The PHY carrier sense has been tuned to provide high-throughput for 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous Rx-Rx.

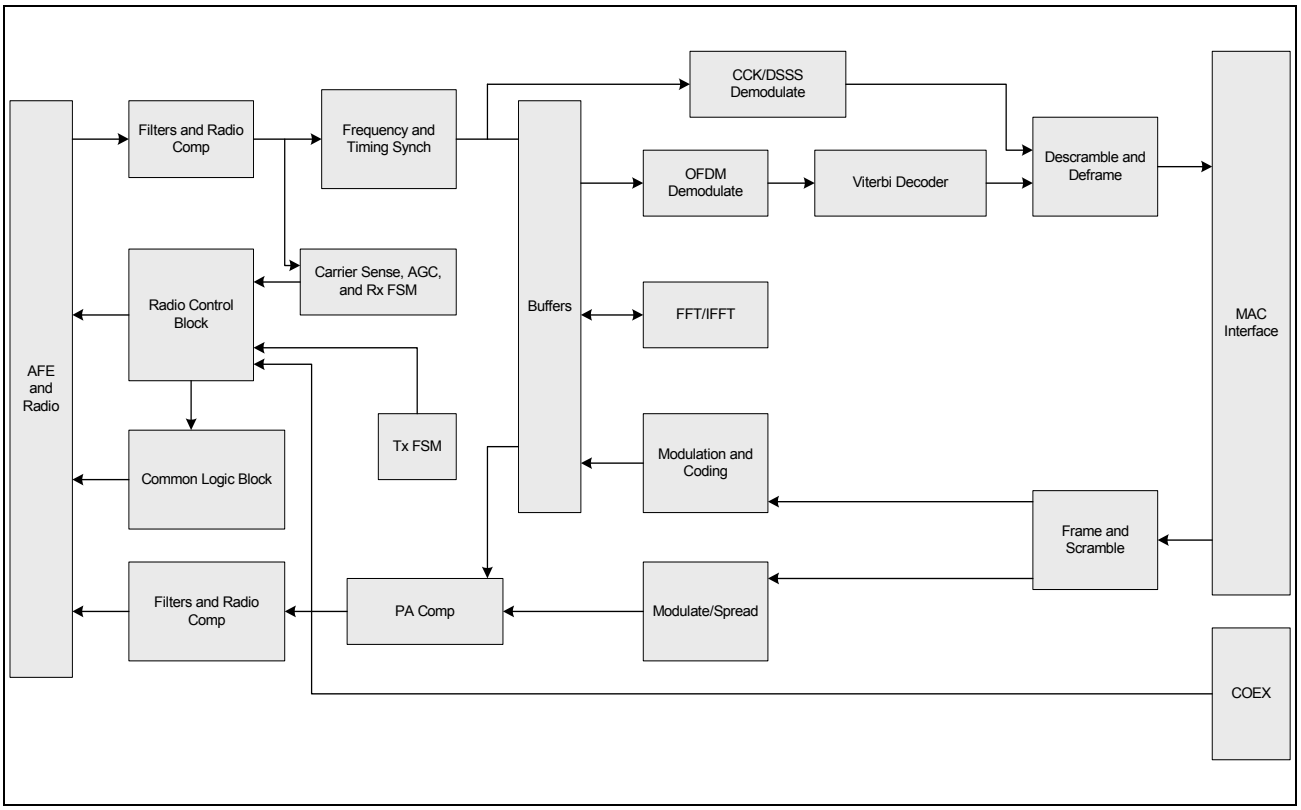

Figure 6: WLAN PHY Block Diagram

The PHY is capable of fully calibrating the RF front-end to extract the highest performance. On power-up, the PHY performs a full-suite of calibration to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift thus maintaining high-performance over time. A closed loop transmit control algorithm maintains the output power to required level with capability control Tx power on a per packet basis.

One of the key feature of the PHY is two space-time stream receive capability. The STBC scheme can obtain diversity gains by using multiple transmit antennas in AP (Access Point) in a fading channel environment, without increasing the complexity at the STA. Details of the STBC receive is shown in the block diagram shown in Figure 7 on page 44.

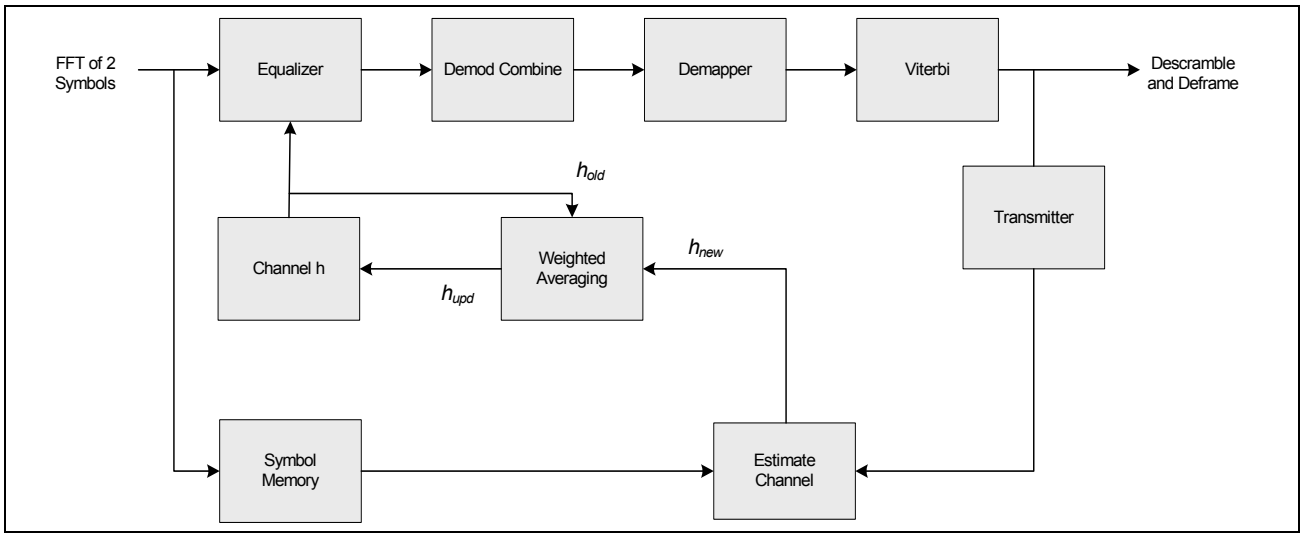

Figure 7: STBC Receive Block Diagram

In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 8:WLAN Radio Subsystem

The BCM4329 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz or 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

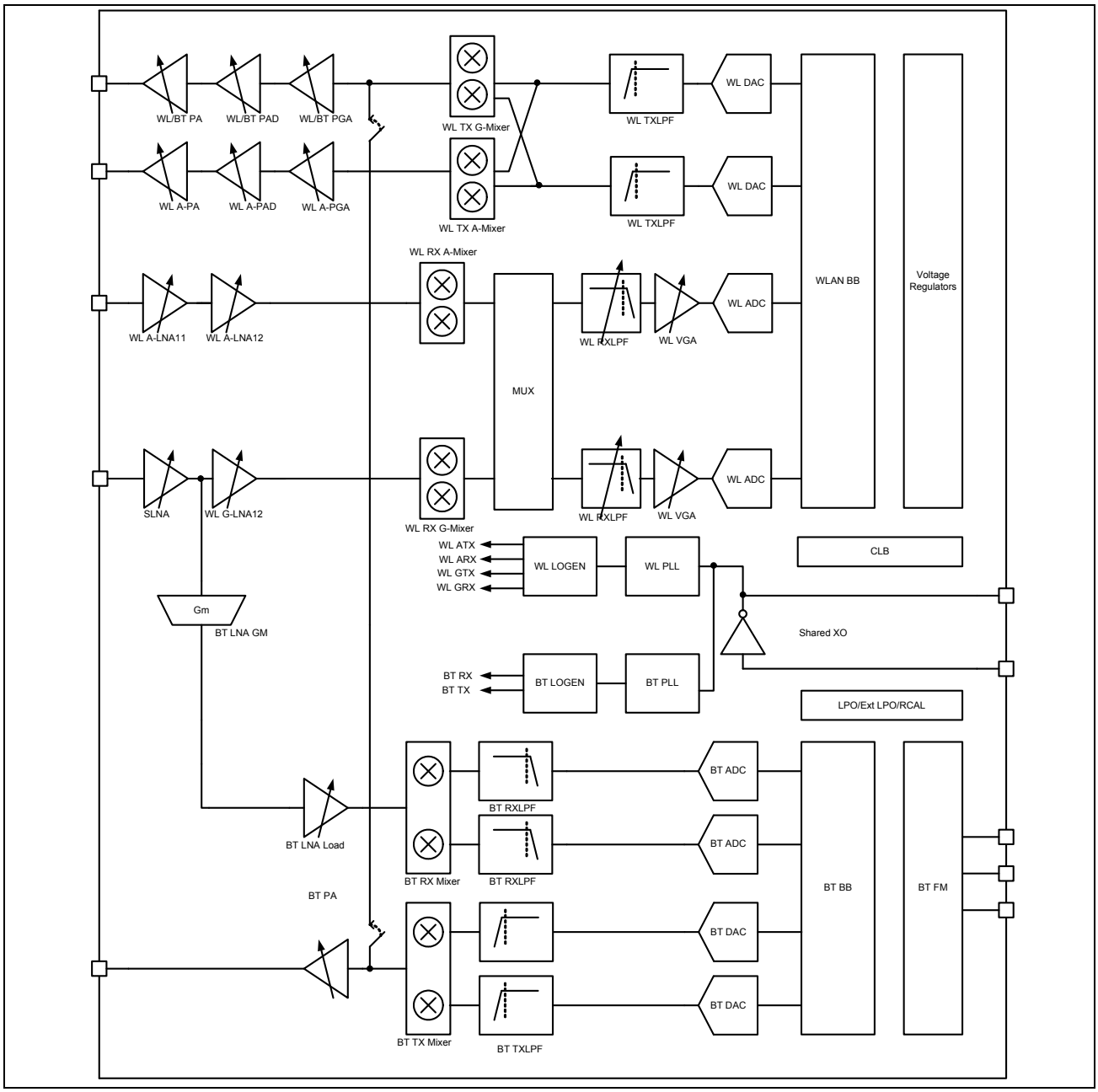

Figure 8: Radio Functional Block Diagram

Receiver Path

The BCM4329 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band.

Transmit Path

Linear transmitters are included, which are capable of delivering high output powers while meeting 802.11a/b/g/n specifications without the need for external PAs. Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively.

Calibration

The BCM4329 features dynamic on-chip calibration, eliminating process variation across components. This enables the BCM4329 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of this automatic calibration are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip as well.

Section 9: WLAN CPU and Memory Subsystem

The BCM4329 includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19uW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/uW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for Code and Data access (ICode/DCode and System buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

Section 10: WLAN Power Management

The BCM4329 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM4329 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only.

Additionally, the BCM4329 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM4329 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768-kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM4329 WLAN power states are described as follows:

- Active mode — All components in the BCM4329 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode (PWM or Burst) based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode — The radio, AFE, PLLs, and the ROMs are powered down. The rest of the BCM4329 remains powered up in an IDLE state. All main clocks are shut down. The 32.768-kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current. The external switcher and internal baseband switcher are put into Burst mode (for better efficiency at low load currents).
- Power-down Mode — The BCM4329 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic reenabling the internal regulators.

Section 11: WLAN Interfaces

SDIO v1.2

The BCM4329 supports SDIO version 1.2. for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks — 200 Mbps). It has the ability to map the interrupt signal onto a GPIO pin. This "out-of-band" interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

Note: Per section 6 of the SDIO specification, pull-ups in the 10–100 kΩ range are required on the four data lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of internal pull-ups in the BCM4329 or the SDIO host.

Note: The SDIO host must wait a minimum of 110 ms before initiating access to the BCM4329 after the VDDC (1.25V DC supply for the core) ramps up and settles. The specifics of this requirement depend on the power supply topology being used. For example, if the topology shown in Figure 22 on page 65 is being used, reset and host access timing depends on the CLDO and CBUCK outputs and the VDDC bypass capacitors. For an additional safety margin, a longer delay should be used.

Three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

SDIO Pin Description

Table 2: SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode		SPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait	NC	Not used
DATA3	Data line 3	N/C	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

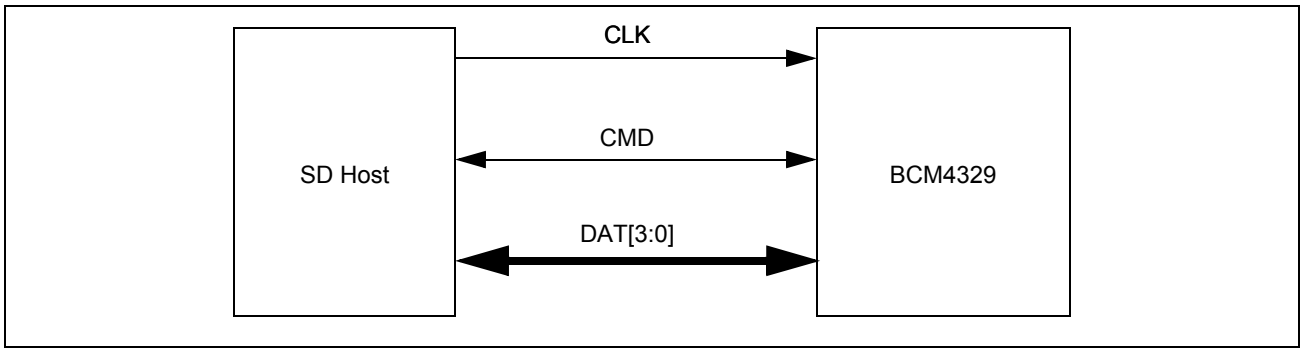

Figure 9: Signal Connections to SDIO Card (SD 4-Bit Mode)

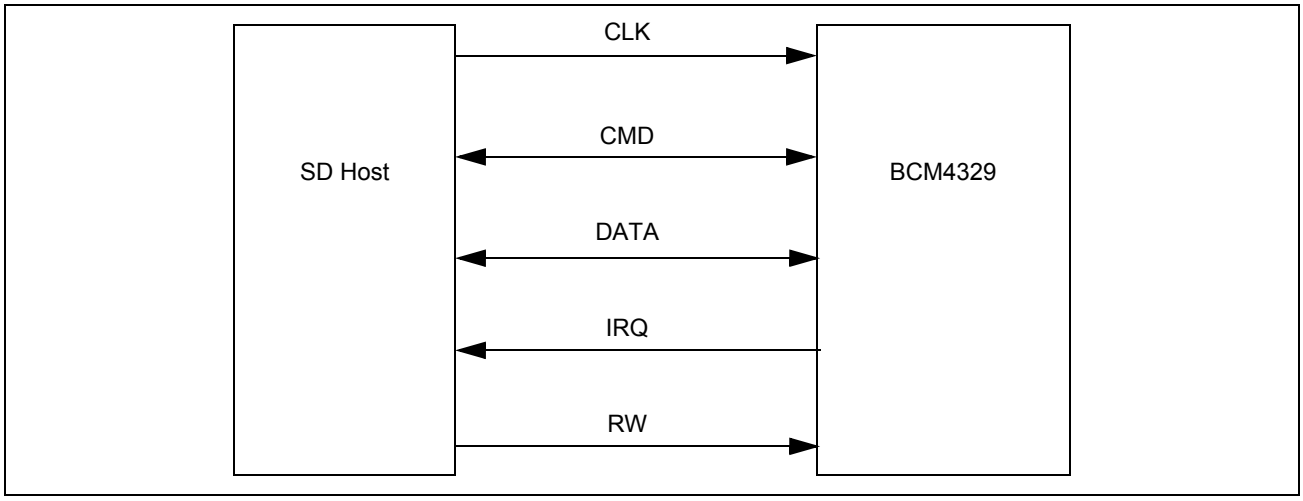

Figure 10: Signal Connections to SDIO Card (SD 1-Bit Mode)

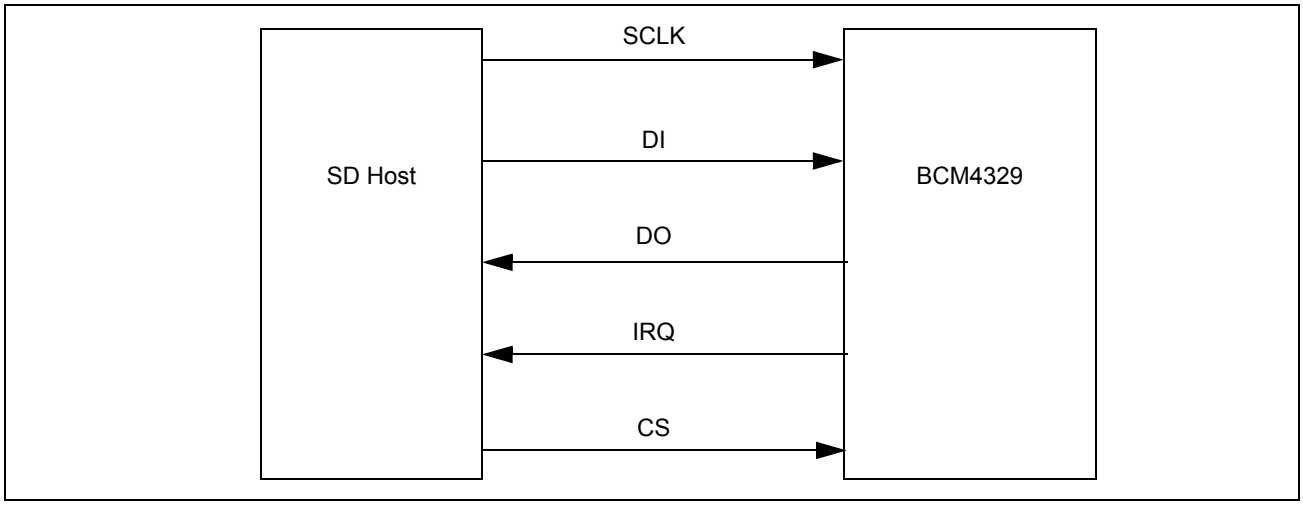

Figure 11: Signal Connections to SDIO Card (SPI Mode)

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 12 and Table 3.

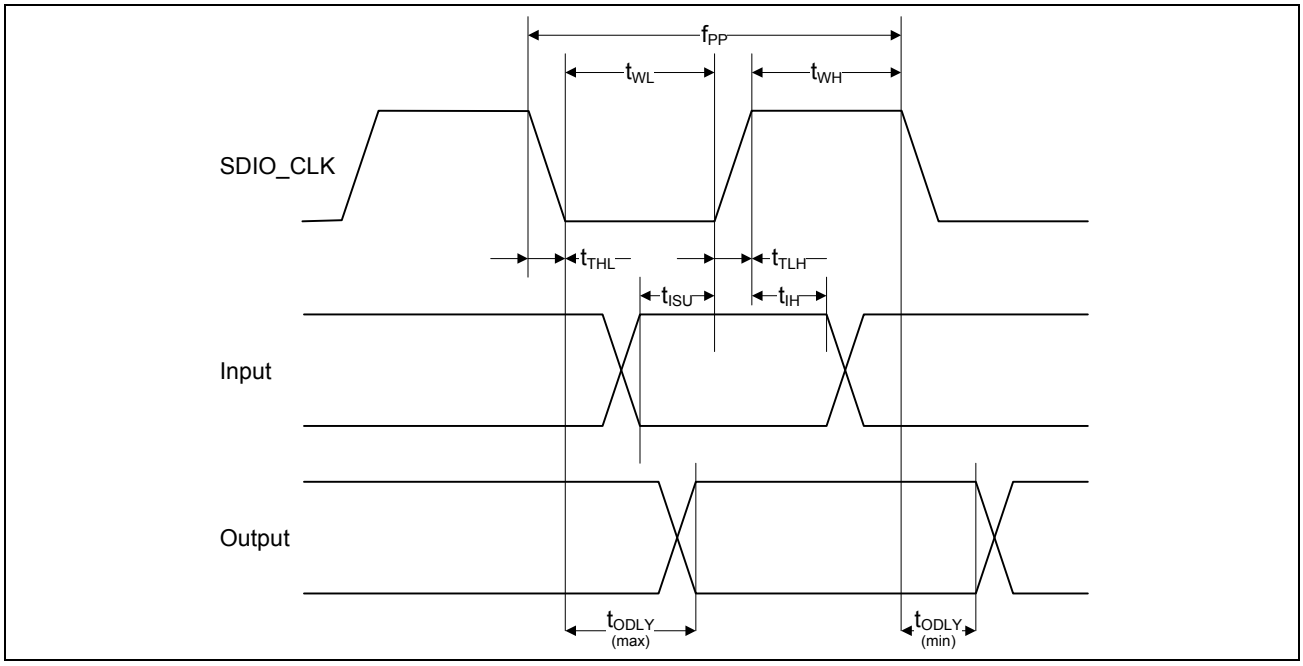

Figure 12: SDIO Bus Timing (Default Mode)

Table 3: SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency — Data Transfer mode	fPP	0	–	25	MHz
Frequency — Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time — Data Transfer mode	tODLY	0	–	14	ns
Output delay time — Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 13 and Table 4.

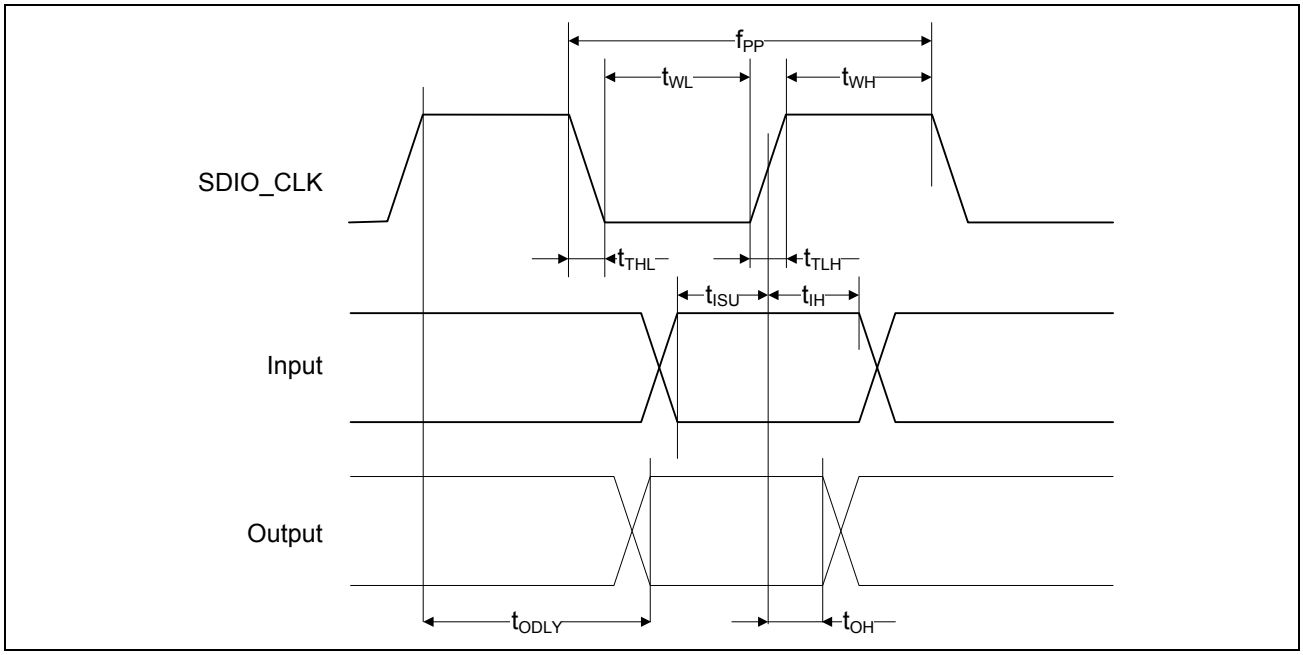

Figure 13: SDIO Bus Timing (High-Speed Mode)

Table 4: SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency — Data Transfer Mode	fPP	0	–	50	MHz
Frequency — Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time — Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SPI

The BCM4329 also includes SPI interface/protocol functionality. Characteristics of the BCM4329 interface include:

- Supports up to 48 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host SPI frames (16- or 32-bits)
- Supports up to 2-KB frame size per transfer
- Supports little endian and big endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

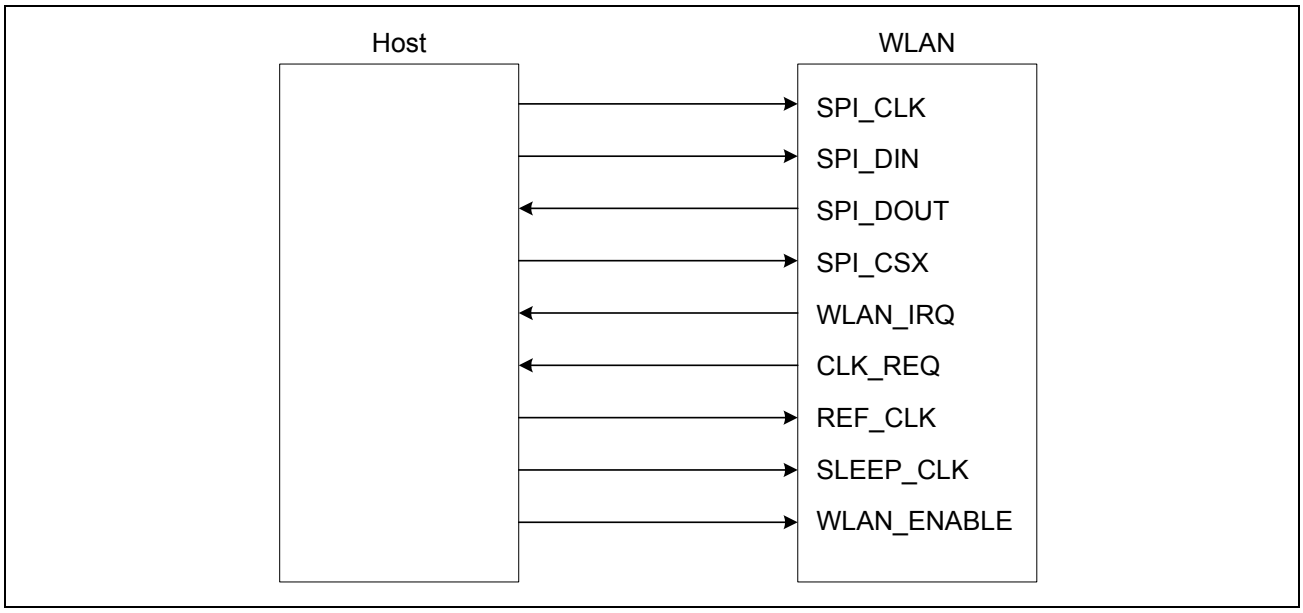

Figure 14: Host Interface

Signal Timing

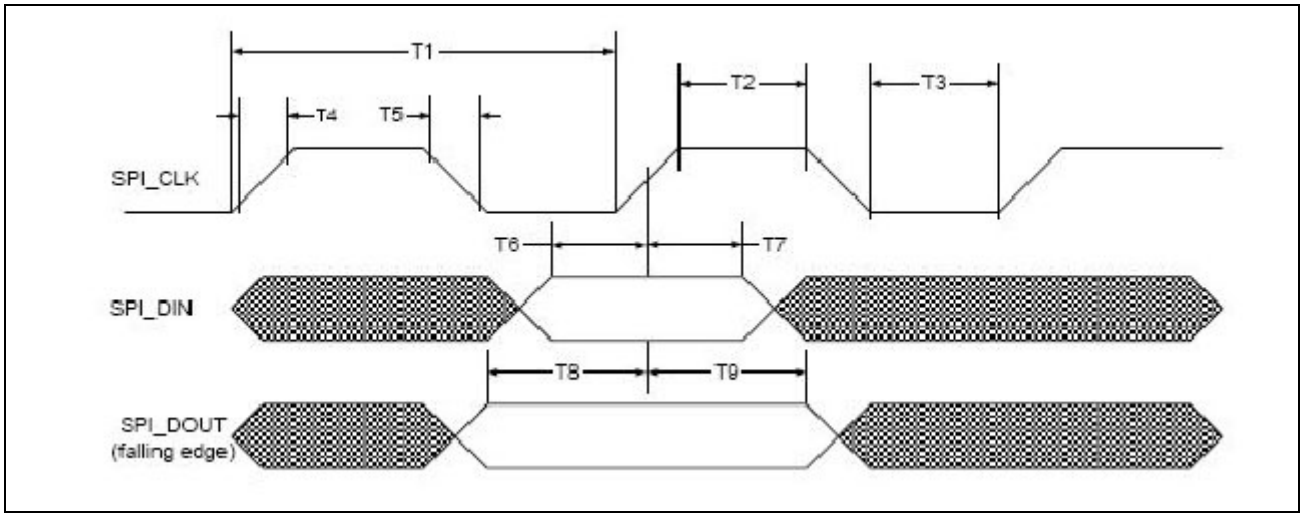

Figure 15: SPI Timing

Table 5: SPI Timing

Parameter	*Symbol*	*Minimum*	*Maximum*	*Units*	*Note*
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time	T4/T5	–	2.5	ns	–
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	2.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[a]	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX[a]	–	–	–	ns	Last falling edge to CSX high

a. SPI_CSx remains active for entire duration of SPI read/write/write_read transaction (i.e., overall words for multiple word transaction)

The SPI host and device always use the rising edge of clock to sample data.

SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianess is supported in both modes. Figure 16 and Figure 17 show the basic write and write-read commands.

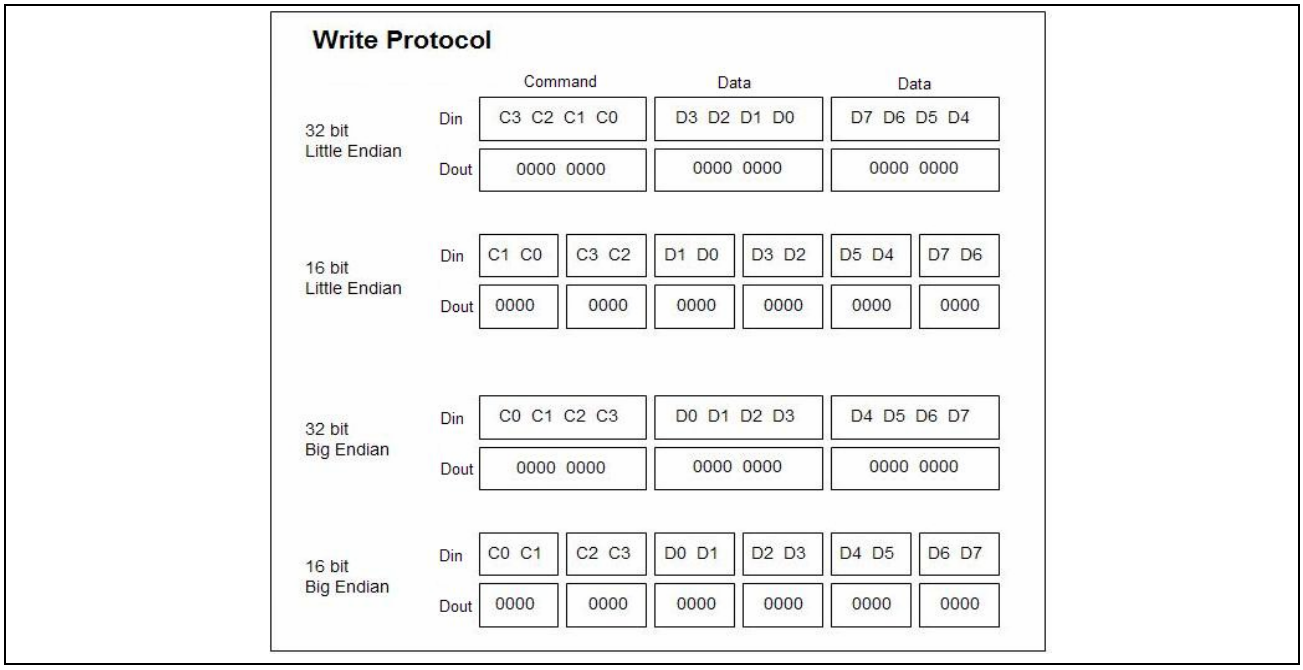

Figure 16: SPI Write Protocol

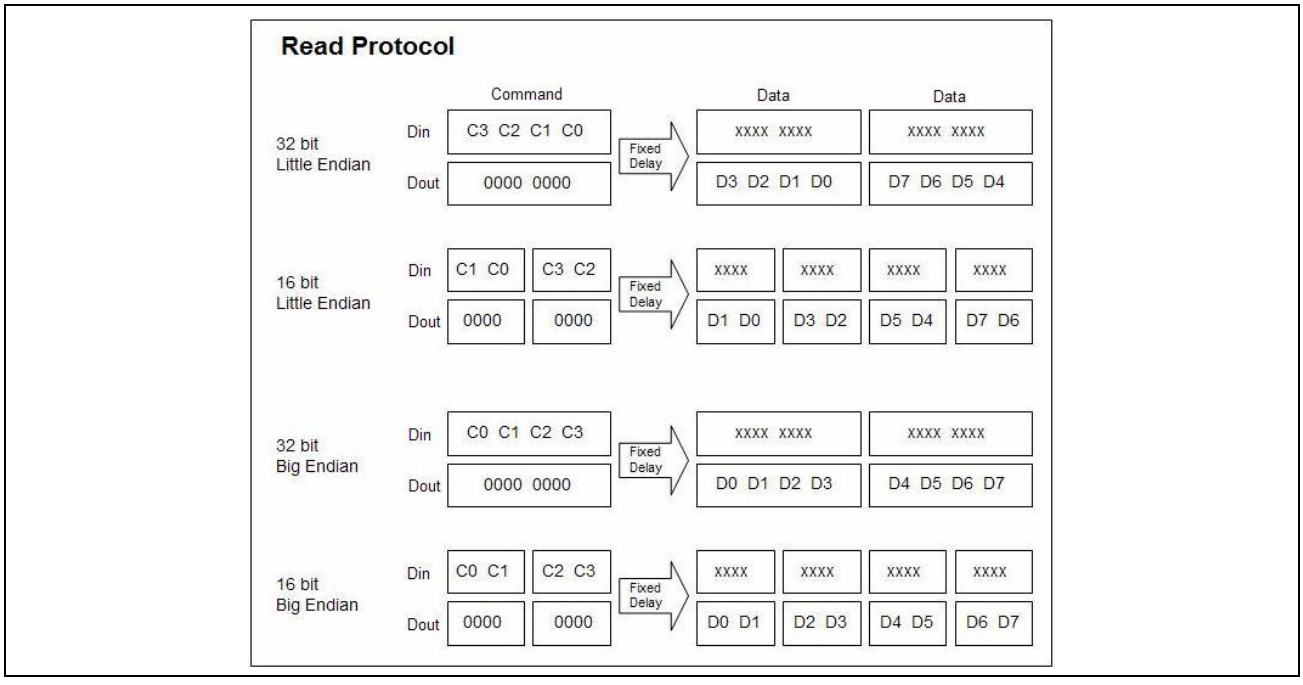

Figure 17: SPI Read Protocol

Command Structure

The SPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 18.

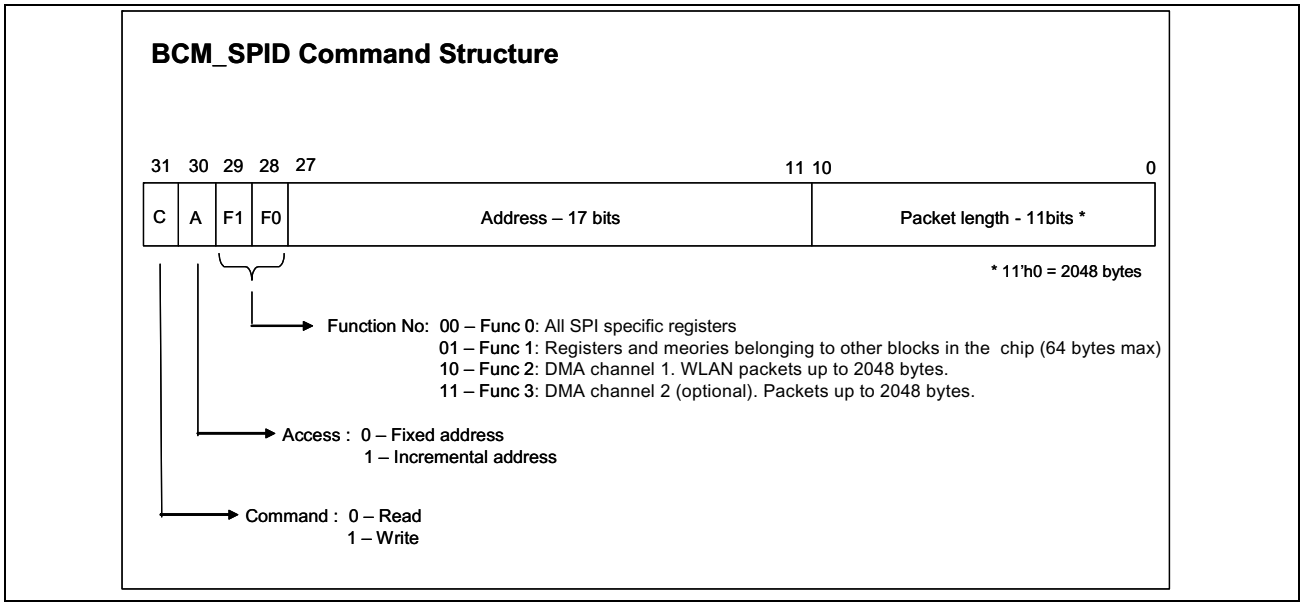

Figure 18: SPI Command Structure

Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the SPI clock. The device samples the data on the active edge.

Write-Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write-read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The SPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the Host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The SPI bus timing for read/write transactions with and without status notification are as shown in Figure 19 on page 57 and Figure 20 on page 58. See Table 6 on page 58 for information on status field details.

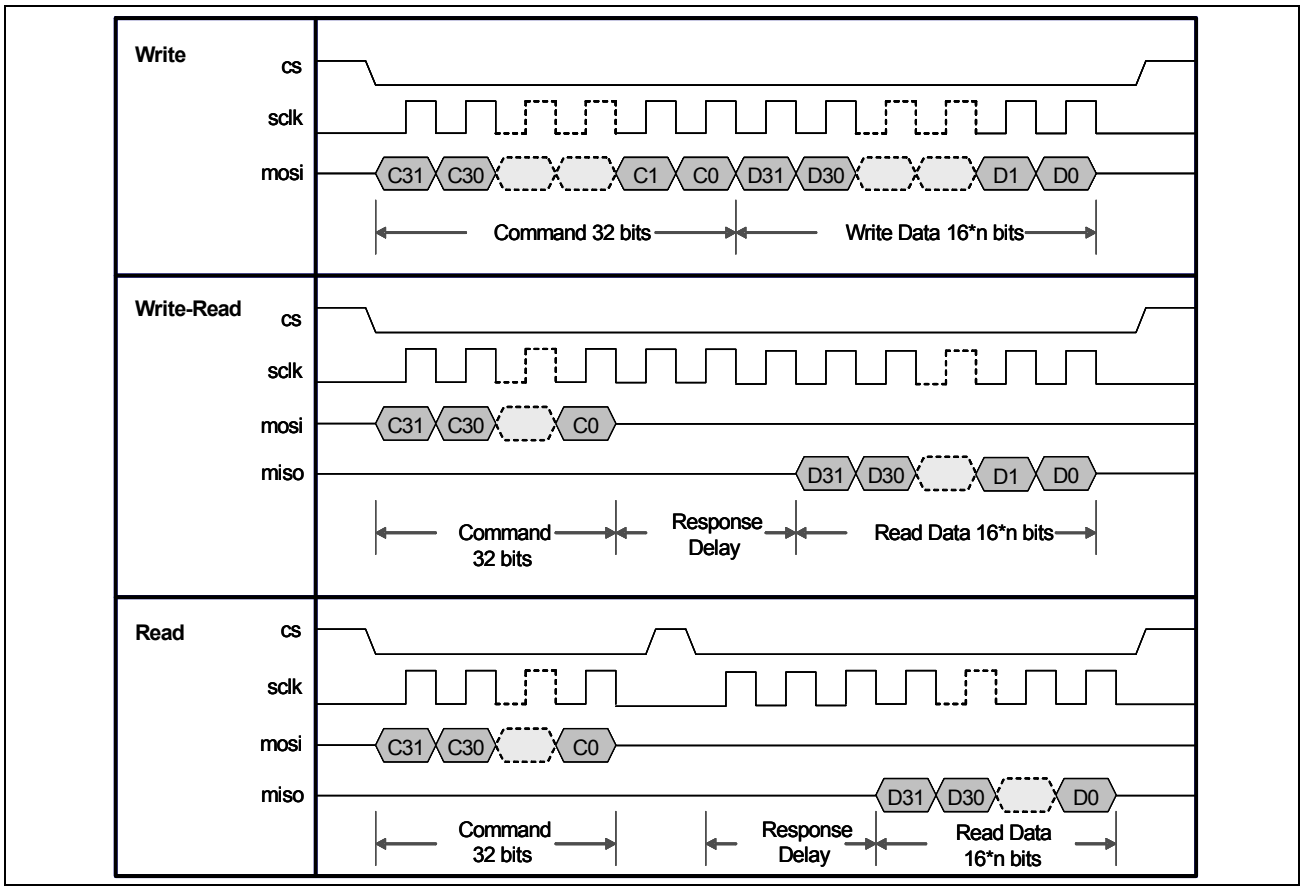

Figure 19: SPI Signal Timing Without Status

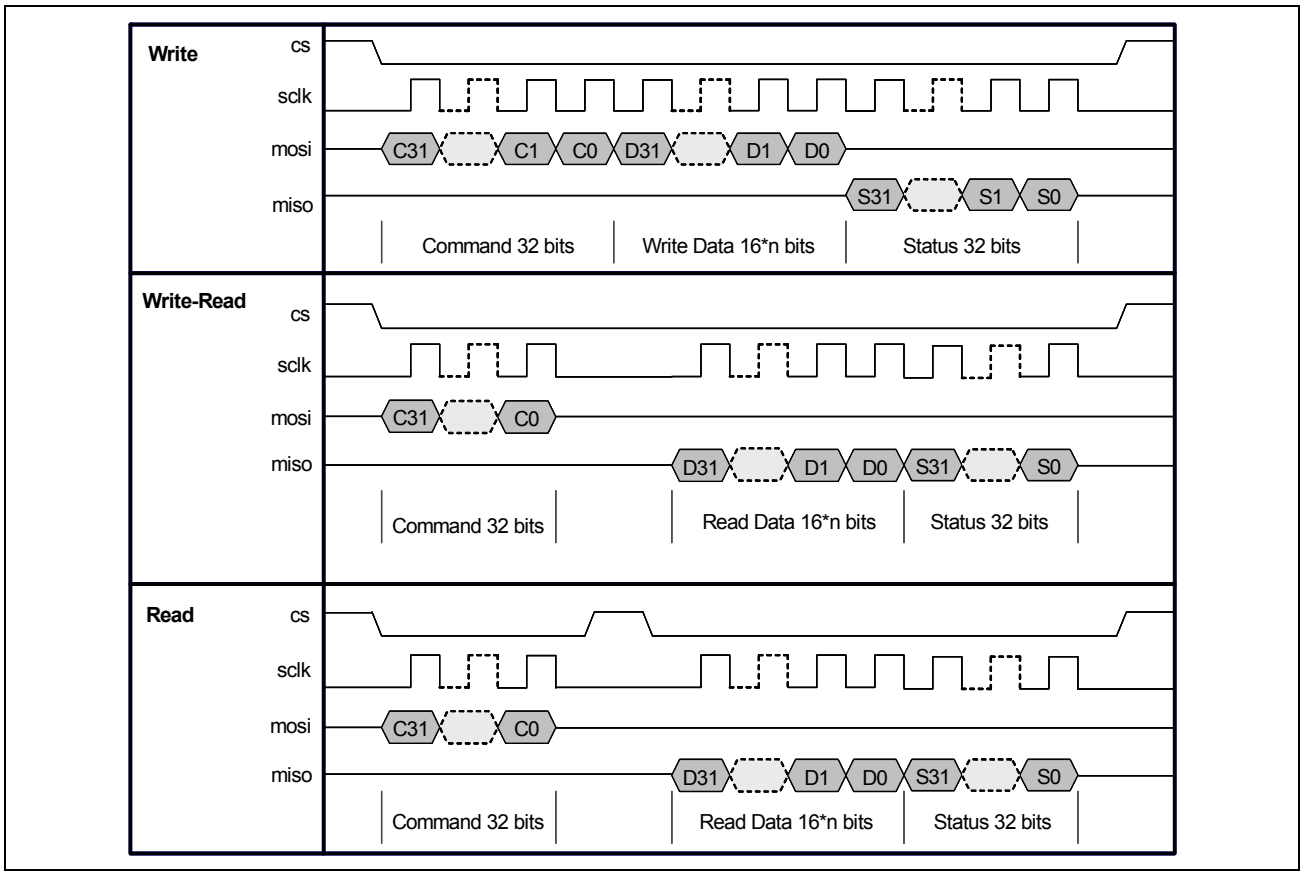

Figure 20: SPI Signal Timing with Status (Response Delay = 0)

Table 6: SPI Status Field Details

Bit	*Name*	*Description*
0	Data not available	The requested read data is not available
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
4	F3 interrupt	F3 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty)
6	F3 RX Ready	F3 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO
9:19	F2 Packet Length	Length of packet available in F2 FIFO
20	F3 Packet Available	Packet is available/ready in F3 TX FIFO
21:31	F3 Packet Length	Length of packet available in F3 FIFO

SPI Host-Device Handshake

To initiate communication through the SPI after power-up, the Host needs to bring up the WLAN/Chip by writing to the Wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM4329 is ready for data transfer. The device can signal an interrupt to the Host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the Host using the WLAN IRQ line whenever it has any information to pass to the Host. On getting an interrupt, the Host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

Boot-Up Sequence

After power-up, the SPI Host needs to wait for the device to be out of reset. For this, the Host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the Host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the Host needs to set wakeup-wlan bit (F0 reg 0x00 bit 7). Wakeup-wlan issues a clock request to the PMU.

The wake WLAN bit locks the PLL. However, since the crystal frequency is not known to the device at power up, the PLL is not turned ON. The host must write the crystal frequency into the internal registers of the device once, at power-up. To write to these registers, the host must first wait until the crystal clock is provided to the device. At power-up the device asserts the XTAL_PU pin and assumes that the crystal clock is stable by 8 ms. So, at power-up, the host must wait for a little over 8 ms after the host obtains the predefined bit pattern from the 0x14 register and then write the crystal frequency into the internal registers of the device. After the PLL is locked, the chipActive interrupt is issued to the host. This indicates that the device is awake and ready. See Table 7 for information about SPI registers.

In Table 7, the following notation is used for register access:

- R: Readable from Host and CPU
- W: Writable from Host
- U: Writable from CPU

Table 7: SPI Registers

Address	*Register*	*Bit*	*Access*	*Default*	*Description*
x0000	Word length	0	R/W/U	0	0–16 bit word length 1–32 bit word length
	Endianess	1	R/W/U	0	0 = Little Endian 1 = Big Endian
	High speed mode	4	R/W/U	1	0 = Normal mode. RX and TX at different edges. 1 = High speed mode. RX and TX on same edge (default).
	Interrupt polarity	5	R/W/U	1	0 = Interrupt active polarity is low 1 = Interrupt active polarity is high (default)
	Wake-up	7	R/W	0	A write of 1 will denote wake-up command from Host to device. This will be followed by a F2 Interrupt from SPI device to Host, indicating device awake status.
x0001	Response delay	7:0	R/W/U	8‘h04	Configurable read response delay in multiples of 8 bits
x0002	Status enable	0	R/W	1	0 = No status sent to host after read/write 1 = Status sent to host after read/write
	Interrupt with status	1	R/W	0	0 = Do not interrupt if status is sent 1 = Interrupt host even if status is sent
	Response delay for all	2	R/W	0	0 = Response delay applicable to F1 read only 1 = Response delay applicable to all function read
x0003	Reserved				
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006–x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008–x000B	Status register	31:0	R	32'h0000	Same as status bit definitions

Table 7: SPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x000C–x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E–x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0010–x0011	F3 info register	0	R/U	1	F3 enabled
		1	R	0	F3 ready for data transfer
		15:2	R/U	14'h800	F3 max packet size
x0014–x0017	Test–Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read and determine if the SPI interface is working properly.
x0018–x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the SPI interface is working properly.

Section 12:WLAN Software Architecture

Host Software Architecture

The host driver (DHD) provides a transparent connection between the host operating system and the BCM4329 media (for example, WLAN) by presenting a network driver interface to the host operating system and communicating with the BCM4329 over an interface-specific bus (SPI, SDIO, and so on) to:

- Forward transmit and receive frames between the host network stack and the BCM4329 device, and
- Pass control requests from the host to the BCM4329 device, returning the BCM4329 device responses

The driver communicates with the BCM4329 over the bus using a control channel and a data channel to pass control messages and data messages. The actual message format is based on the BDC protocol.

Device Software Architecture

The wireless device, protocol, and bus drivers are run on the embedded ARM® processor and Broadcom-defined operating system called HNDRTE that transfers data over a propriety Broadcom format over the SDIO/SPI interface between the host and device (BDC/LMAC). The data portion of the format consists of 802.11 frames wrapped in a Broadcom encapsulation. The host side architecture provides all missing functionality between a network device and the Broadcom device interface. The host can also be customized to provide functionality between the Broadcom device interface and a full network device interface.

This transfer requires a message-oriented (framed) interconnect between the host and device. The SDIO bus is an addressed bus—each host-initiated bus operation contains an explicit device target address—and does not natively support a higher-level data frame concept. Broadcom has implemented a hardware/software message encapsulation scheme that ignores the bus operation code address and prefixes each frame with a 4-byte length tag for framing. The device presents a packet-level interface over which data, control and asynchronous event (from the device) packets are supported.

The data and control packets received from the bus are initially processed by the bus driver and then passed on to the protocol driver. If the packets are data packets, they are transferred to the wireless device driver (and out through its medium), and a data packet received from the device medium follows the same path in the reverse direction. If the packets are control packets, the protocol header is decoded by the protocol driver. If the packets are wireless IOCTL packets, the IOCTL API of the wireless driver is called to configure the wireless device. The microcode running in the D11 core processes all time-critical tasks.

Remote Downloader

When the BCM4329 powers up, the DHD initializes and downloads the firmware to run in the device.

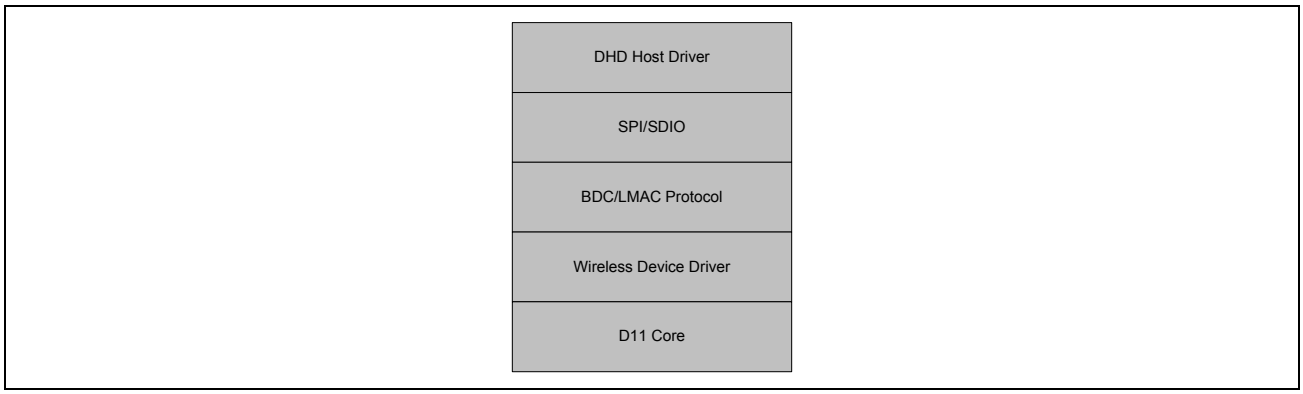

Figure 21: WLAN Software Architecture

Wireless Configuration Utility

The device driver that supports the Broadcom IEEE 802.11 family of wireless solutions provides an input/output control (IOCTL) interface for making advanced configuration settings. The IOCTL interface makes it possible to make settings that are normally not possible when using just the native operating system-specific IEEE 802.11 configuration mechanisms. The utility uses IOCTLs to query or set a number of different driver/chip operating properties.

Section 13: Power Supplies and Power Management

Power Supply Topology

The BCM4329 contains power supply building blocks, including a switcher, three low noise LDOs, and a power amplifier LDO. These blocks simplify power supply design for Bluetooth, WLAN, and FM functions in embedded designs. All regulator inputs and outputs are brought out to pins on the BCM4329. This allows maximum flexibility to the system designer who can choose which of the BCM4329's integrated regulators to use.

A single host power supply can be used (including VBATT ranging from 2.3V to 5.5V) with all additional voltages being provided by the regulators in the BCM4329. Alternately, if specific rails such as 3.3V, 2.5V, and 1.25V already exist in the system, appropriate regulators in the BCM4329 can be bypassed, thereby reducing the cost and board space associated with external components for the regulators, such as inductors and large capacitors.

BT_REG_ON and WL_REG_ON are used to power-up the regulators. The CBuck and CLDO get powered whenever any of the reset signals is de-asserted. Optionally LNLDO1 may also be powered. All regulators are powered down only when both the resets are asserted. The PA-LDO, LNLDO1 and LNLDO2 may be turned off/on based on need by the digital baseband.

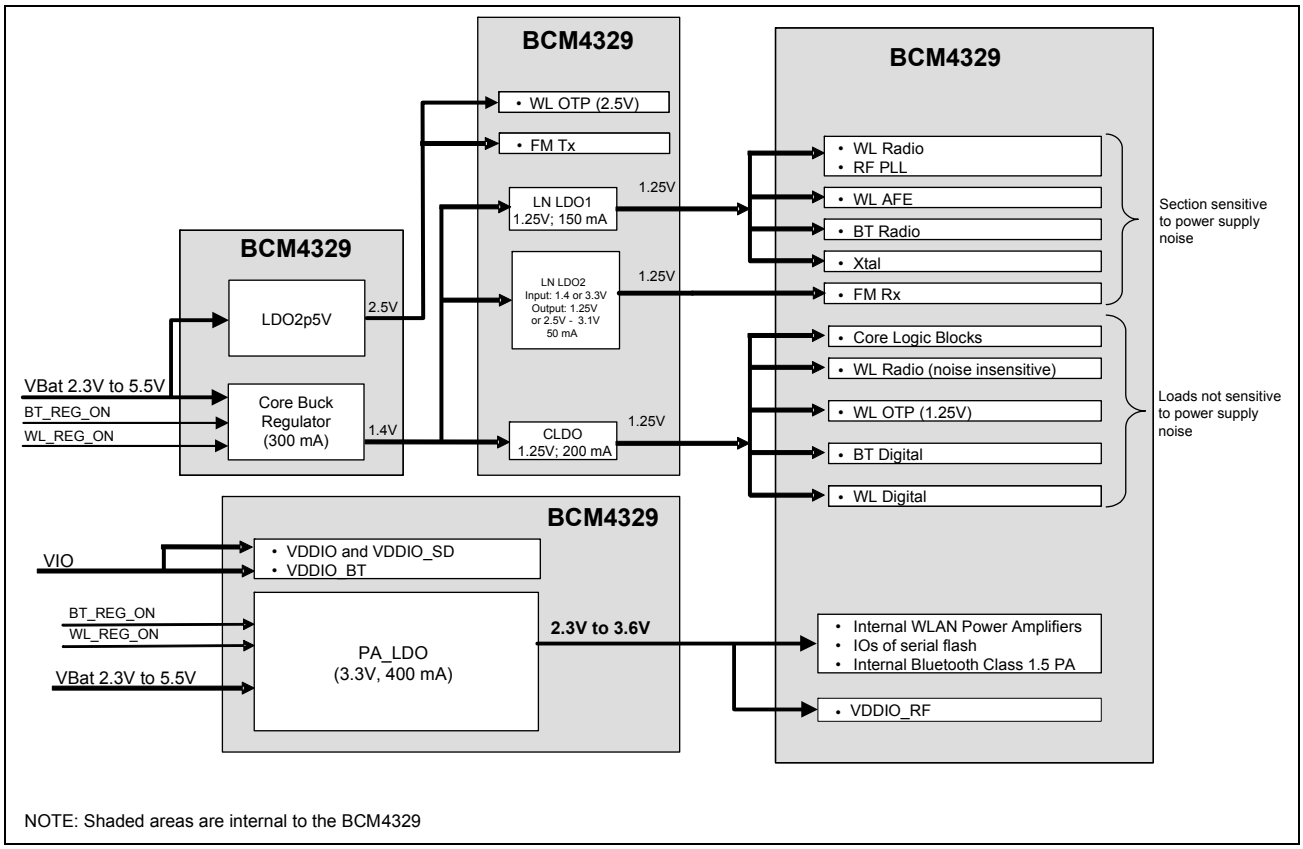

Figure 22: Power Topology

PMU Sequencing

WLAN PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off. Each resource has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the resource's time_on or time_off value when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768-kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. computes the required resource set based on requests and the resource dependency table.
2. decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. compares the request with the current resource status and determines which resources must be enabled or disabled.
4. initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
5. initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Low-Power Shutdown

The BCM4329 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM4329 is not needed in the system, VDDRF and VDDC are shut down while VDDO remains powered. This allows the BCM4329 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDO remains applied to the BCM4329, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM4329 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

Two signals on the BCM4329, the frequency reference input (OSCIN) and LPO input (WRF_EXTREFIN), are designed to be high-impedance inputs that do not load down the driving signal even if the chip does not have VDDO power applied to it.

When the BCM4329 is powered on from this state, it is the same as a normal power-up and the device does not contain any information about its state from before it was powered down.

Section 14: Frequency References

The BCM4329 uses the following external frequency references for normal and low-power operational modes:

- An external crystal or external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal is used for the generating all radio frequencies and normal operation clocking.
- Either an external 32.768-kHz or fully integrated internal low power oscillator (LPO) for lower power mode timing.

Crystal Interface and Clock Generation

The BCM4329 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing. This enables it to operate using numerous frequency references. This may either be an external source such as a TCXO or a crystal interfaced directly to the BCM4329.

The default frequency reference setting is a 38.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are shown in Table 8.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added to the driver, and also require additional, extensive system testing. Contact your Broadcom technical representative for further details.

Table 8: Crystal Oscillator and External Clock Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference[a]			Units
		Min	Typ	Max	Min	Typ	Max	
Frequency	–	Between 12 MHz and 52 MHz[b,c]						
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input impedance	Resistive				1M	–	–	Ω
	Capacitive				–	–	4.7	pF
Input voltage	AC-coupled analog signal				400[d]	–	1200	mV_{p-p}
Output low level	DC-coupled digital signal				0	–	–	V
Output high level	DC-coupled digital signal				1.0	–	1.36	V
Frequency tolerance Initial + over temperature	Without trimming	–20	–	20	–20	–	20	Ppm

Table 8: Crystal Oscillator and External Clock Performance (Cont.)

Parameter	Conditions/Notes	Crystal			External Frequency Reference[a]			Units
		Min	Typ	Max	Min	Typ	Max	
Initial frequency tolerance trimming range	–	–50	–	50	–50	–	50	Ppm
Duty cycle	38.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[e] (802.11b/g)	38.4 MHz clock at 1 kHz offset	–	–	–	–	–	–115	dBc/Hz
	38.4 MHz clock at 10 kHz offset	–	–	–	–	–	–125	dBc/Hz
	38.4 MHz clock at 100 kHz offset	–	–	–	–	–	–130	dBc/Hz
	38.4 MHz clock at 1 MHz offset	–	–	–	–	–	–135	dBc/Hz
Phase Noise[e] (802.11a)	38.4 MHz clock at 1 kHz offset	–	–	–	–	–	–123	dBc/Hz
	38.4 MHz clock at 10 kHz offset	–	–	–	–	–	–133	dBc/Hz
	38.4 MHz clock at 100 kHz offset	–	–	–	–	–	–138	dBc/Hz
	38.4 MHz clock at 1 MHz offset	–	–	–	–	–	–143	dBc/Hz
Phase Noise[e] (802.11n, 2.4 GHz)	38.4 MHz clock at 1 kHz offset	–	–	–	–	–	–120	dBc/Hz
	38.4 MHz clock at 10 kHz offset	–	–	–	–	–	–130	dBc/Hz
	38.4 MHz clock at 100 kHz offset	–	–	–	–	–	–135	dBc/Hz
	38.4 MHz clock at 1 MHz offset	–	–	–	–	–	–140	dBc/Hz
Phase Noise[e] (802.11n, 5 GHz)	38.4 MHz clock at 1 kHz offset	–	–	–	–	–	–128	dBc/Hz
	38.4 MHz clock at 10 kHz offset	–	–	–	–	–	–138	dBc/Hz
	38.4 MHz clock at 100 kHz offset	–	–	–	–	–	–143	dBc/Hz
	38.4 MHz clock at 1 MHz offset	–	–	–	–	–	–148	dBc/Hz
Auto-detection frequencies when using external LPO[f]	–	12, 13, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8, 20, 26, 38.4, and 52			12, 13, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8, 20, 26, 38.4, and 52			MHz

a. For a clock reference other than 38.4 MHz, 20 × log10(f/ 38.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
b. BT_TM6 should be tied low for a 52 MHz clock reference. For other frequencies, BT_TM6 should be tied high. Note that 52 MHz is not an auto-detected frequency using the LPO clock unless BT_TM6 is tied low.
c. The frequency step size is approximately 80 Hz resolution.
d. Applies to 2.4 GHz band. 5 GHz band = TBD.
e. If the selected clock has a flat phase noise response above 100 kHz, that is, the phase noise at and above 100 kHz is constant, then subtract 1dB from all 1 kHz, 10 kHz, and 100 kHz values shown. For example, for the 2.4 GHz 802.11b/g values, the phase noise requirements change from –115, –125, and –130 dBc/Hz to –116, –126, and –131 dBc/Hz respectively. Ignore the 1 MHz requirements when the phase noise is flat above 100 kHz.
f. Bluetooth/FM auto-detection of frequencies requires that the crystal or external frequency reference have < ±50 ppm of variation, and the external LPO frequency have < ±250 ppm of variation at the time of auto-detection. WLAN does not auto-detect the reference clock frequency.

Crystal Oscillator

The BCM4329 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 23. Consult the reference schematics for the latest configuration.

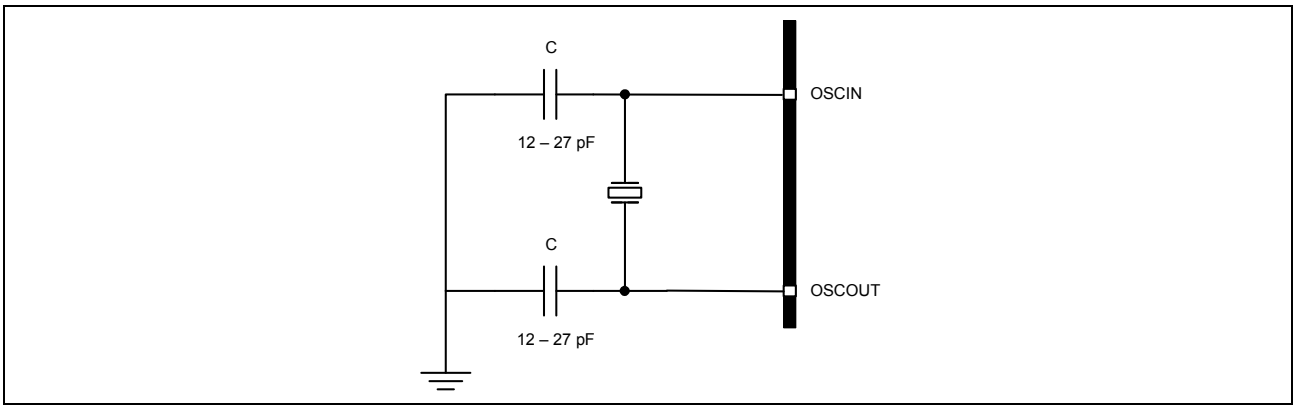

Figure 23: Recommended Oscillator Configuration

Low Power Oscillator

The second frequency reference is the LPO clock that the BCM4329 uses to provide low power mode timing. The LPO clock is provided externally to the device from a 32.768 kHz source.

Table 9: LPO Signal Characteristics

Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200[a, b]	ppm
Duty cycle	30–70	%
Input signal amplitude	200 to 1800[c]	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[d]	>100k < 5	Ω pF
Clock jitter (integrated over 300 Hz – 15 kHz)	<1	Hz
Clock jitter (during initial start-up)	<1000	ppm

a. If FM Rx is used: ±150 ppm maximum with frequency error indication, ± 50ppm without frequency error indication.
b. If FM Tx is used: ±100 ppm maximum with frequency error indication, ±50 ppm without frequency error indication.
c. 200–1800 mVp-p to avoid additional current consumption and degradation in FM SNR. 3.3 Vp-p maximum.
d. When power is applied or switched off.

Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset references frequencies of 12, 13, 14.4, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8, 20, 26, 38.4, and 52 MHz, but any other frequency in-between these as desired by the system designer. The BCM4329 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

The reference frequency for the BCM4329 may be set in one of two ways.

- Use the default frequency of 38.4 MHz
- Auto-detect the standard handset reference frequencies using an external LPO clock

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM4329 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto frequency detection to work correctly, the BCM4329 must have a valid and stable 32.768-kHz LPO clock present during power-on reset.

Note: When the BCM4329 goes into power-on reset, the external LPO clock must be stable and accurate for correct operation of the auto-frequency detection. The BCM4329 tolerates a duty cycle of up to +/- 15% for the reference frequency.

Section 15: Pinout and Signal Descriptions

Signal Assignments

182-Ball WLBGA Pinout

Note: The X- and Y-coordinate orientation is looking at the solder balls on the bottom of the package as opposed to top down. Refer to Figure 34 on page 136 for X- and Y-coordinate origin information.

Table 10: 182-Ball WLBGA Signal Assignments by Pin Number and X- and Y-Coordinates (Units = ìm)

Ball Pad	Signal Name	X-Coord	Y-Coord
A1	WRF_VDDPAA_3P3	-3014.8	2549.9
A2	WRF_GNDPAA_3P3	-2966.755	2152.48
A3	WRF_VDDTX_1P2	-2826.025	1774.125
A4	WRF_RFINP_A1	-2981.95	1400.535
A5	WRF_RFINN_A1_XFMR	-3004.96	946.685
A7	WRF_RFINP_G1	-3010.84	276.485
A8	WRF_RFINN_G1_XFMR	-3007.73	-153.575
A9	WRF_GNDCAB_1P2	-2953.695	-550
A10	BT_VSSRF	-3025	-950
A11	BT_RFOP	-3025	-1444
A12	BT_VDDTF	-3025	-1844
A13	BT_VDDVCO	-3025	-2244
B5	WRF_VDDRX_1P2	-2530.785	925.875
B6	WRF_GNDRX_1P2	-2774.355	601.71
B8	WRF_GNDD_1P2	-2605.665	-152.685
B9	WRF_RES_EXT	-2550.98	-550
B11	BT_RFON	-2625	-1307
B14	FM_VDDRX	-2713	-2550
C1	WRF_RFOUTP_A	-2214.8	2549.9
C2	WRF_GNDPAA_3P3	-2364.065	2170.495
C3	WRF_GNDTX_1P2	-2191.66	1761.185
C5	WRF_VDDLO_1P2	-2082.43	961.065
C7	WRF_VDDA_1P2	-2066.785	227.09
C8	WRF_VDDD_1P2	-2203.525	-152.825
C9	WRF_VDDPFDCP_1P2	-2149.895	-550.005
C10	BT_VDDRF	-2313	-950
C11	BT_VDDIF	-2113	-1350

Ball Pad	Signal Name	X-Coord	Y-Coord
C12	BT_VSSVCO	-2313	-1750
C13	FM_TXN	-2313	-2150
C14	FM_RXN	-2313	-2550
D1	WRF_VDDPAG_3P3	-1814.8	2549.9
D2	WRF_GNDPAG_3P3	-1963.8	2178.495
D4	WRF_EXTCOUPLE_AIN	-1760.47	1357.67
D5	WRF_GNDLO_1P2	-1677.115	965.365
D6	WRF_VDDVCO_1P2	-1713.505	565.275
D8	WRF_GNDA_1P2	-1832.585	-303.85
D9	WRF_GNDPFDCP_1P2	-1512.295	-550
D10	BT_VSSIF	-1913	-950
D11	BT_VSSIFP	-1713	-1350
D12	FM_VSSRX	-1913	-1750
D13	FM_TXP	-1913	-2150
D14	FM_RXP	-1913	-2550
E1	WRF_RFOUTP_G	-1414.8	2549.9
E2	WRF_GNDPAG_3P3	-1414.8	2149.9
E3	WRF_AFE_TSSI_G	-1414.8	1749.9
E4	WRF_GPIO_OUT1	-1355.995	1349.9
E5	WRF_GPIO_OUT2	-1275.045	952.96
E6	WRF_GNDVCO_1P2	-1275.045	546.615
E7	WRF_VDDCAB_1P2	-1395.265	162.16
E8	WRF_EXTREFIN	-1275.045	-222.135
E10	FM_VDDPLL	-1513	-950
E12	FM_VSSVCO	-1513	-1750
E13	FM_VDDVCO	-1513	-2150
E14	FM_CVAR	-1513	-2550
F1	WRF_AFE_TEST_IP	-1014.8	2549.9
F2	WRF_AFE_TEST_IN	-1014.8	2149.9
F3	WRF_AFE_IQADC_VREF	-1014.8	1749.9
F4	WRF_BBPLL_VDD_1P2	-814.48	1402.28
F10	FM_VSSPLL	-1113	-950
F11	VSS_XTAL	-1113	-1350
F12	VDD_XTAL	-1113	-1750
F13	OSCOUT	-1113	-2150
F14	OSCIN	-1113	-2550
G1	WRF_AFE_AVSS_RXADC	-614.8	2549.9
G2	WRF_AFE_AVDD_RXADC	-614.8	2149.9
G3	WRF_AFE_AVDD_AUX	-614.8	1749.9
G6	BT_TM3	-575	650
G7	BT_GPIO_0	-575	250
G8	VDD	-575	-150

Ball Pad	Signal Name	X-Coord	Y-Coord
G10	FM_BGNDLF	-713	-950
G11	FM_TXADCVCM	-713	-1350
G12	FM_ADOUT2	-713	-1750
G13	FM_ANAVSS	-713	-2150
G14	FM_TXADCIN2	-713	-2550
H1	WRF_AFE_TEST_OP	-214.8	2549.9
H2	WRF_AFE_TEST_ON	-214.8	2149.9
H3	WRF_AFE_TSSI_A	-214.8	1749.9
H4	WRF_BBPLL_GND_1P2	-214.8	1349.9
H6	RF_SW_CTRL_N_0	-175	650
H7	BT_VDDO	-175	250
H8	BT_GPIO_1	-175	-150
H9	BT_RST_N	-175	-550
H12	FM_ADOUT1	-313	-1750
H13	FM_ANAVDD	-313	-2150
H14	FM_TXADCIN1	-313	-2550
J5	RF_SW_CTRL_P_0	225	1050
J6	BT_VDDO	225	650
J7	VSS	225	250
J8	BT_GPIO_2	225	-150
J9	BT_TM0	225	-550
J10	BT_COEX_OUT0	225	-950
K1	AMODE_TX_PU	625	2550
K2	RF_SW_CTRL_N_3	625	2150
K4	GMODE_TX_PU	625	1450
K5	RF_SW_CTRL_P_1	625	1050
K6	RF_SW_CTRL_N_1	625	650
K7	VDDIO_RF	625	250
K8	BT_TM1	625	-150
K9	BT_GPIO_4	625	-550
K10	BT_VSSC	625	-950
K11	BT_GPIO_7	625	-1350
K12	BT_COEX_OUT1	625	-1750
K13	BT_GPIO_5	625	-2150
K14	BT_GPIO_6	625	-2550
L1	VDD	1025	2550
L2	TMS	1025	2150
L4	TCK	1025	1450
L5	JTAG_TRST_L	1025	1050
L6	RF_SW_CTRL_P_3	1025	650
L7	VDDIO_RF	1025	250
L8	BT_TM6	1025	-150

Ball Pad	Signal Name	X-Coord	Y-Coord
L9	BT_GPIO_3	1025	-550
L10	BT_PCM_SYNC	1025	-950
L11	BT_PCM_IN	1025	-1350
L12	BT_VDDC	1025	-1750
L13	BT_VSSC	1025	-2150
L14	BT_PCM_CLK	1025	-2550
M1	AMODE_EXT_LNA_GAIN	1425	2550
M2	GMODE_EXT_LNA_GAIN	1425	2150
M4	VSS	1425	1450
M5	WL_RST_N	1425	1050
M6	TDO	1425	650
M7	BT_SDA	1425	250
M8	BT_SCL	1425	-150
M9	BT_PCM_OUT	1425	-550
M10	BT_VDDC	1425	-950
M11	BT_UART_CTS_N	1425	-1350
M12	BT_UART_RTS_N	1425	-1750
M13	BT_UART_TXD	1425	-2150
M14	BT_UART_RXD	1425	-2550
N1	WL_GPIO_3	1825	2550
N2	WL_GPIO_2	1825	2150
N4	WL_GPIO_1	1825	1450
N5	WL_GPIO_0	1825	1050
N6	TDI	1825	650
N7	TAP_SEL_0	1825	250
N8	BT_REG_ON	1825	-150
N9	WL_REG_ON	1825	-550
N10	VDD_LNLDO2	1825	-950
N11	VOUT_LDO2	1825	-1350
N12	SR_TESTSWG	1825	-1750
N13	SR_VDDBAT1	1825	-2150
N14	SR_VDDBAT1	1825	-2550
P1	WL_GPIO_8	2225	2550
P2	VDDIO	2225	2150
P4	OTP_VDD25	2225	1450
P5	VSS	2225	1050
P6	SDIO_CMD	2225	650
P7	TAP_SEL_1	2225	250
P8	AVSS_LDO	2225	-150
P9	VREF_LDO	2225	-550
P10	SR_PNPO	2225	-950
P11	SR_PAVSS	2225	-1350
P12	SR_AVSS	2225	-1750
P13	SR_PVSS	2225	-2150
P14	SR_VLX1	2225	-2550
R1	XTAL_PU	2625	2550
R2	UART_TX_0	2625	2150
R4	UART_RX_0	2625	1450
R5	VDDIO	2625	1050
R6	SDIO_DATA_2	2625	650
R7	SDIO_DATA_3	2625	250
R8	VDD_CLDO	2625	-150
R9	VDD_LNLDO1	2625	-550
R10	SR_PALDO	2625	-950
R11	SR_VDDBAT3	2625	-1350
R12	SR_VDDBAT2	2625	-1750
R13	SR_PVSS	2625	-2150
R14	SR_VLX1	2625	-2550
T1	SDIO_DATA_0	3025	2550
T2	SDIO_CLK	3025	2150
T4	VDD	3025	1450
T5	VDDIO_SD	3025	1050
T6	VDDIO_SD	3025	650
T7	SDIO_DATA_1	3025	250
T8	VOUT_CLDO	3025	-150
T9	VOUT_LNLDO1	3025	-550
T10	SR_PALDO	3025	-950
T11	SR_VDDBAT3	3025	-1350
T12	SR_AVDD2P5	3025	-1750
T13	SR_VDDNLDO	3025	-2150
T14	SR_VSSPLDO	3025	-2550

182-Ball WLBGA Ball Map (Bottom View)

Figure 24 shows a bottom view of the 182-Ball WLBGA ball map. This view is looking at the solder balls on the bottom of the package as opposed to top down. The X and Y coordinate information is provided in Table 10 on page 71.

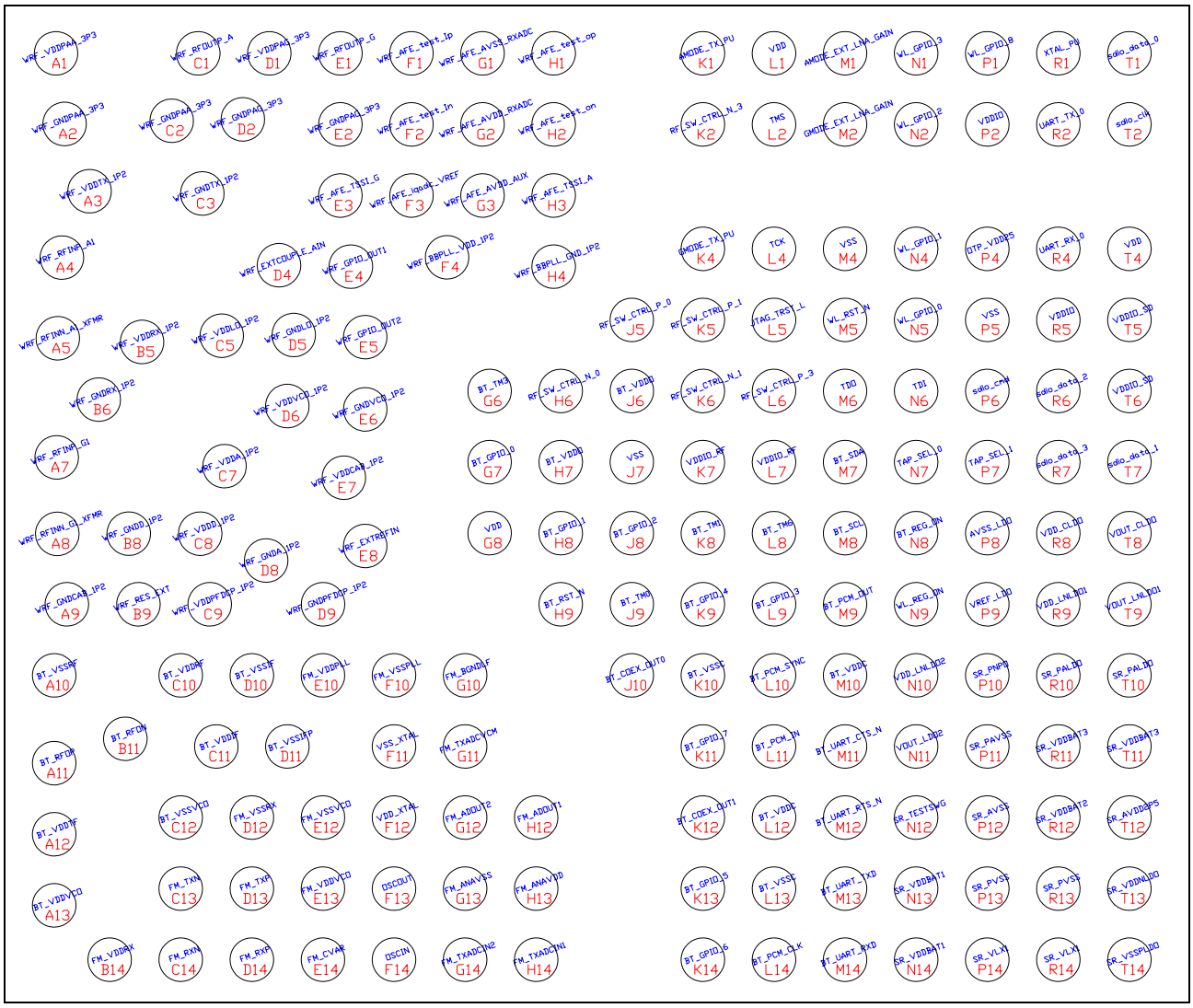

Figure 24: 182-Ball WLBGA Ball Map (Bottom view)

Signal Descriptions

182-Ball WLBGA Package

Table 11: WLBGA Signal Descriptions

Ball Pad	Signal Name	Type	Description
WLAN RF			
B9	WRF_RES_EXT	I	Connect to external 15 kΩ resistor to ground
A5	WRF_RFINN_A1_XFMR	I	WLAN 802.11a internal LNA RX input (50Ω)
A4	WRF_RFINP_A1	I	WLAN 802.11a Internal LNA RX input (50Ω)
D4	WRF_EXTCOUPLE_AIN	I	WLAN directional coupler input for 802.11a (50Ω)
C1	WRF_RFOUTP_A	O	WLAN 802.11a internal power amplifier output (50Ω)
A7	WRF_RFINP_G1	I	WLAN 802.11g and BT shared LNA RX input (50Ω)
E1	WRF_RFOUTP_G	O	WLAN 802.11g internal power amplifier output (50Ω)
A8	WRF_RFINN_G1_XFMR	O	Ground of the primary side of the shared RX transformer. Need short and solid ground.
M1	AMODE_EXT_LNA_GAIN	O	WLAN external LNA gain control (5 GHz)
M2	GMODE_EXT_LNA_GAIN	O	BT and WLAN external LNA gain control (2.4 GHz)
Integrated LDOs			
R8	VDD_CLDO	I	Input supply pin for CLDO
R9	VDD_LNLDO1	I	Input supply pin for LNLDO1
N10	VDD_LNLDO2	I	Input supply pin for LNLDO2 (backup linear regulator)
T8	VOUT_CLDO	O	1.25V output for core LDO, 200 mA
N11	VOUT_LDO2	O	1.25V/2.5V–3.1V programmable output for low noise LDO2, 50 mA
T9	VOUT_LNLDO1	O	1.25V output for low noise LDO1, 150 mA
P9	VREF_LDO	O	Vref bypass. Connect to external capacitor.
Integrated Switching Regulators			
T12	SR_AVDD2P5	O	2.5V LDO output
R10	SR_PALDO	O	internal PALDO output
T10	SR_PALDO	O	internal PALDO output
P10	SR_PNPO	O	No connect
N12	SR_TESTSWG	O	Test output for switcher/LDOs. Internally tied to SR_AVSS through a 2 MΩ resistor.
N13	SR_VDDBAT1	I	Buck regulator: Battery voltage Input
N14	SR_VDDBAT1	I	
R12	SR_VDDBAT2	I	

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
R11	SR_VDDBAT3	I	Battery supply input for PALDO
T11	SR_VDDBAT3	I	
T13	SR_VDDNLDO	O	NLDO output — connect to 220 nF external capacitor to ground
P14	SR_VLX1	O	Core buck regulator: Output to inductor
R14	SR_VLX1	O	Core buck regulator: Output to inductor
T14	SR_VSSPLDO	I	Tracks battery voltage — connect to 220 nF external capacitor to battery
SDIO Bus Interface			
T7	SDIO_DATA_1	I/O	SDIO data line 1. This pin has an internal weak pull-up resistor. The resistor is enabled by default but can be disabled by software. The value of the pull-up depends on the VDDIO_SD supply voltage. For 1.8V, the resistance range is 30–82 kΩ. For 2.6V, it ranges from 21–41 kΩ. For 3.3V, it ranges from 15–35 kΩ.
T2	SDIO_CLK	I	SDIO clock.
P6	SDIO_CMD	I/O	SDIO command line. This pin has an internal weak pull-up resistor. The resistor is enabled by default but can be disabled by software. The value of the pull-up depends on the VDDIO_SD supply voltage. For 1.8V, the resistance range is 30–82 kΩ. For 2.6V, it ranges from 21–41 kΩ. For 3.3V, it ranges from 15–35 kΩ.
T1	SDIO_DATA_0	I/O	SDIO data line 0. This pin has an internal weak pull-up resistor. The resistor is enabled by default but can be disabled by software. The value of the pull-up depends on the VDDIO_SD supply voltage. For 1.8V, the resistance range is 30–82 kΩ. For 2.6V, it ranges from 21–41 kΩ. For 3.3V, it ranges from 15–35 kΩ.
R6	SDIO_DATA_2	I/O	SDIO data line 2. This pin has an internal weak pull-up resistor. The resistor is enabled by default but can be disabled by software. The value of the pull-up depends on the VDDIO_SD supply voltage. For 1.8V, the resistance range is 30–82 kΩ. For 2.6V, it ranges from 21–41 kΩ. For 3.3V, it ranges from 15–35 kΩ.
R7	SDIO_DATA_3	I/O	SDIO data line 3. This pin has an internal weak pull-up resistor. The resistor is enabled by default but can be disabled by software. The value of the pull-up depends on the VDDIO_SD supply voltage. For 1.8V, the resistance range is 30–82 kΩ. For 2.6V, it ranges from 21–41 kΩ. For 3.3V, it ranges from 15–35 kΩ.

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
JTAG			
N7	TAP_SEL_0	I	TAP Select Pin — used in conjunction with TAP_SEL_1 to select JTAG tap: 00= Select chip tap (in functional mode.) 01= Selects WLAN core ARM tap (in functional mode) 10= Selects BT core ARM tap (in functional mode) 11= Selects chip tap (strict JTAG compliance mode for boundary scan only). In this mode, all of the internal pull-up / pull-down resistors in the BCM4329 are disabled. Because of this, the power up state of the chip may be different from that during functional mode. This setting is used for board level boundary scan. **Note:** There are internal pull-downs on the TAP_SEL_0 and TAP_SEL_1 pins, making the default state 00 if the pins are left floating.
P7	TAP_SEL_1	I	TAP Select Pin — used in conjunction with TAP_SEL_0 to select JTAG tap: 00= Select chip tap (in functional mode.) 01= Selects WLAN core ARM tap (in functional mode) 10= Selects BT core ARM tap (in functional mode) 11= Selects chip tap (strict JTAG compliance mode for boundary scan only). In this mode, all of the internal pull-up / pull-down resistors in the BCM4329 are disabled. Because of this, the power up state of the chip may be different from that during functional mode. This setting is used for board level boundary scan. **Note:** There are internal pull-downs on the TAP_SEL_0 and TAP_SEL_1 pins, making the default state 00 if the pins are left floating.
L4	TCK	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left unconnected (NC) as they have internal pull-up resistors.
N6	TDI	I	
L5	JTAG_TRST_L	I	
L2	TMS	I	
M6	TDO	O	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC).
RF Control Lines *(see Table 12 on page 84) for details)*			
H6	RF_SW_CTRL_N_0	O	Programmable RF switch control line. Default at this pin is low.
K6	RF_SW_CTRL_N_1	O	
K2	RF_SW_CTRL_N_3	O	
J5	RF_SW_CTRL_P_0	O	
K5	RF_SW_CTRL_P_1	O	
L6	RF_SW_CTRL_P_3	O	

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
K1	AMODE_TX_PU	O	802.11a external PA control
K4	GMODE_TX_PU	O	802.11g external PA control
Clocks			
E8	WRF_EXTREFIN	I	Low Power Clock input (32.768 kHz)
R1	XTAL_PU	O	The BCM4329 asserts XTAL_PU when it wants the host to turn on the reference clock. The polarity of this signal is programmable based on BT_TM0. If BT_TM0 is connected to ground, then XTAL_PU is high asserting, and the BCM4329 drives XTAL_PU high when it wants the clock turned on. (It is pulled low-otherwise.) If BT_TM0 is connected to VDDIO, then XTAL_PU is low asserting. Add an external 100 kΩ pull-resistor, pull down or pull up depending on the state of BT_TM0, to keep the signal deasserted during power-up or reset of the BCM4329 when VDDIO is present.
F14	OSCIN	I	XTAL amplifier input
F13	OSCOUT	O	XTAL amplifier output
WLAN GPIO			
N5	WL_GPIO_0	I/O	WLAN general purpose interface pins. These pins are high-impedance on power up and reset. Subsequently, they become inputs or outputs through software control. These pins have programmable pull-up/down. **Note:** WL_GPIO_8 is initially used as a strapping option to select between SPI and SDIO mode. Tie high for SPI; tie low for SDIO. Default is SPI mode.
N4	WL_GPIO_1	I/O	
N2	WL_GPIO_2	I/O	
N1	WL_GPIO_3	I/O	
P1	WL_GPIO_8	I/O	
FM Transceiver			
H12	FM_ADOUT1	O	FM analog audio output channel 1
G12	FM_ADOUT2	O	FM analog audio output channel 2
H13	FM_ANAVDD	I	FM audio ADC/DAC supply
E14	FM_CVAR	I	Bypass node for FM VCO
C14	FM_RXN	I	FM radio RF antenna port
D14	FM_RXP	I	FM radio RF antenna port
H14	FM_TXADCIN1	I	FM audio ADC input 1
G14	FM_TXADCIN2	I	FM audio ADC input 2
G11	FM_TXADCVCM		FM audio ADC common mode (terminate with external 220 nF–1 μF cap to ground)
C13	FM_TXN	O	No Connect floating pad. May be connected to D13 to enhance ESD protection.
D13	FM_TXP	O	FM radio RF antenna port

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
Bluetooth UART			
M11	BT_UART_CTS_N	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
M12	BT_UART_RTS_N	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
M14	BT_UART_RXD	I/O	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface.
M13	BT_UART_TXD	I/O	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
Bluetooth Test Mode			
J9	BT_TM0	I	Bluetooth test mode pin. Used to select polarity of XTAL_PU signal. If low, then XTAL_PU will be high asserting. If high, then XTAL_PU will be low asserting.
K8	BT_TM1	I	Bluetooth test mode pin. Tie low for normal operation
G6	BT_TM3	I	Tie high (VDDIO) for normal operation.
L8	BT_TM6	I	Tie high to disable the crystal divider; tie low to divide crystal clock by 2.
Bluetooth			
B11	BT_RFON	O	BT-PA negative output. For single-ended configuration with BT_RFOP (A11) as PA output port, B11 may be connected directly to the ground plane. Trace lengths from the ball to the ground plane must then be kept short (parasitic inductance < 0.5 nH). If trace lengths need to be longer due to board constraints, a series tuning capacitor (1 pF–2.7 pF) may be needed (total trace parasitic inductance < 2 nH).
A11	BT_RFOP	O	BT-PA positive output. For single-ended configuration with BT_RFON (B11) as PA output port, A11 may be connected directly to the ground plane. Trace lengths from the ball to the ground plane must then be kept short (parasitic inductance < 0.5 nH). If trace lengths need to be longer due to board constraints, a series tuning capacitor (1 pF–2.7 pF) may be needed (total trace parasitic inductance < 2 nH).
M8	BT_SCL	I/O	Bluetooth I^2C clock
M7	BT_SDA	I/O	Bluetooth I^2C data
Bluetooth PCM			
L14	BT_PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
L11	BT_PCM_IN	I/O	PCM data input
M9	BT_PCM_OUT	I/O	PCM data output
L10	BT_PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input)
Bluetooth GPIO			

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
G7	BT_GPIO_0	I/O	Bluetooth general purpose interface pin. These pins are high-impedance on power up and reset. Subsequently, they become inputs or outputs through software control
H8	BT_GPIO_1	I/O	
J8	BT_GPIO_2	I/O	
L9	BT_GPIO_3	I/O	
K9	BT_GPIO_4	I/O	
K13	BT_GPIO_5	I/O	
K14	BT_GPIO_6	I/O	
K11	BT_GPIO_7	I/O	
Miscellaneous			
R4	UART_RX_0	I	RX pin of debug UART
R2	UART_TX_0	O	TX pin of debug UART
N8	BT_REG_ON	I	Used by PMU (along with WL_REG_ON) to decide whether or not to power down internal BCM4329 regulators. If both BT_REG_ON and WL_REG_ON are low then the regulators will be disabled. This signal has an internal 200 kΩ pull-down resistor. This pin detects a high for the voltage range from 1.6V to 3.6V. It detects a low for voltages < 0.4V (i.e., leakage 2 uA max * 200k).
N9	WL_REG_ON	I	Used by PMU (along with BT_REG_ON) to decide whether or not to power down the internal BCM4329 regulators. If both BT_REG_ON and WL_REG_ON are low, then the regulators will be disabled. This signal has an internal 200 kΩ pull-down resistor. This pin detect a high for the voltage range from 1.6V to 3.6V. It detects a low for voltages < 0.4V (i.e., leakage 2 uA max * 200k).
H9	BT_RST_N	I	Low asserting reset for Bluetooth core
M5	WL_RST_N	I	Low asserting reset for WLAN core
Bluetooth Supplies			
M10	BT_VDDC	I	1.25V Bluetooth baseband core supply
C11	BT_VDDIF	I	1.25V Bluetooth IF block power supply
L12	BT_VDDC	I	1.25V Bluetooth baseband core supply
H7	BT_VDDO	I	Bluetooth digital I/O supply (1.8V to 3.3V)
J6	BT_VDDO	I	Bluetooth digital I/O supply (1.8V to 3.3V)
C10	BT_VDDRF	I	1.25V Bluetooth RF power supply
A12	BT_VDDTF	I	3.3V Bluetooth Internal PA power supply
A13	BT_VDDVCO	I	1.25V Bluetooth VCO power supply
WLAN Supplies			
G3	WRF_AFE_AVDD_AUX	I	1.25V supply for aux ADC
G2	WRF_AFE_AVDD_RXADC	I	1.25V supply for AVDD_AFE
F4	WRF_BBPLL_VDD_1P2	I	1.25V supply for WLAN baseband PLL

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
C5	WRF_VDDLO_1P2	I	1.25V supply for WLAN LO Generator
C7	WRF_VDDA_1P2	I	1.25V supply for WLAN PLL
C8	WRF_VDDD_1P2	I	1.25V supply for WLAN PLL
C9	WRF_VDDPFDCP_1P2	I	1.25V supply for WLAN PLL
D6	WRF_VDDVCO_1P2	I	1.25V supply for WLAN PLL
B5	WRF_VDDRX_1P2	I	1.25V supply tor WLAN receivers
A3	WRF_VDDTX_1P2	I	1.25V supply for WLAN transmitters
A1	WRF_VDDPAA_3P3	I	3.3V for the internal power amplifiers
D1	WRF_VDDPAG_3P3	I	3.3V for the internal power amplifiers
Miscellaneous Supplies			
P4	OTP_VDD25	I	2.5V OTP power supply
G8	VDD	I	1.25V digital supply
L1	VDD	I	1.25V digital supply
T4	VDD	I	1.25V digital supply
F12	VDD_XTAL	I	1.25V XTAL power supply
P2	VDDIO	I	Digital I/O supply (1.8V to 3.3V)
R5	VDDIO	I	Digital I/O supply (1.8V to 3.3V)
K7	VDDIO_RF	I	RF I/O supply (3.3V)
L7	VDDIO_RF	I	RF I/O supply (3.3V)
T5	VDDIO_SD	I	SDIO/SPI I/O supply (1.8V to 3.3V)
T6	VDDIO_SD	I	SDIO/SPI I/O supply (1.8V to 3.3V)
E7	WRF_VDDCAB_1P2	I	Common analog block 1.25V supply
FM Transceiver Supplies			
E10	FM_VDDPLL	I	1.25V FM receiver PLL power supply
B14	FM_VDDRX	I	FM receiver power supply
E13	FM_VDDVCO	I	FM receiver VCO 1.25V supply
Ground			
P8	AVSS_LDO	I	Ground
K10	BT_VSSC	I	Ground
L13	BT_VSSC	I	Ground
D10	BT_VSSIF	I	Bluetooth IF block ground
D11	BT_VSSIFP	I	Bluetooth IF PLL ground
A10	BT_VSSRF	I	Bluetooth ground
C12	BT_VSSVCO	I	Bluetooth VCO ground
G13	FM_ANAVSS	I	FM audio ADC/DAC ground

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
G10	FM_BGNDLF	I	FM PLL loop filter ground
F10	FM_VSSPLL	I	FM receiver PLL ground
D12	FM_VSSRX	I	FM receiver ground
E12	FM_VSSVCO	I	FM receiver VCO ground
P12	SR_AVSS	I	Analog ground
P11	SR_PAVSS	I	Analog ground
P13	SR_PVSS	I	Buck Regulator: power switch ground
R13	SR_PVSS	I	Buck Regulator: power switch ground
J7	VSS	I	Ground
M4	VSS	I	Ground
P5	VSS	I	Ground
F11	VSS_XTAL	I	XTAL ground
G1	WRF_AFE_AVSS_RXADC	I	AVSS_AFE: AFE ground
H4	WRF_BBPLL_GND_1P2	I	Ground for WLAN baseband PLL
D8	WRF_GNDA_1P2	I	WLAN PLL ground
A9	WRF_GNDCAB_1P2	I	Common analog block ground
B8	WRF_GNDD_1P2	I	WLAN PLL ground
D5	WRF_GNDLO_1P2	I	WLAN LO generator ground
A2	WRF_GNDPAA_3P3	I	Internal power amplifier ground
C2	WRF_GNDPAA_3P3	I	Internal power amplifier ground
D2	WRF_GNDPAG_3P3	I	Internal power amplifier ground
E2	WRF_GNDPAG_3P3	I	Internal power amplifier ground
D9	WRF_GNDPFDCP_1P2	I	WLAN PLL ground
B6	WRF_GNDRX_1P2	I	WLAN RX ground
C3	WRF_GNDTX_1P2	I	Radio transmitter ground
E6	WRF_GNDVCO_1P2	I	WLAN PLL ground

Table 11: WLBGA Signal Descriptions (Cont.)

Ball Pad	Signal Name	Type	Description
No Connect			
J10	BT_COEX_OUT0	I/O	No connect
K12	BT_COEX_OUT1	I/O	No connect
F3	WRF_AFE_IQADC_VREF	I	iqadc_VREF: No connect
F2	WRF_AFE_TEST_IN	I	Test_In: No connect
F1	WRF_AFE_TEST_IP	I	Test_Ip: No connect
H2	WRF_AFE_TEST_ON	I	Test_On: No connect
H1	WRF_AFE_TEST_OP	I	Test_Op: No connect
H3	WRF_AFE_TSSI_A	I	TSSI_A: No connect
E3	WRF_AFE_TSSI_G	I	TSSI_G: No connect
E4	WRF_GPIO_OUT1	O	No connect
E5	WRF_GPIO_OUT2	I/O	No connect

Table 12: RF Switch Control Lines

	Index to LUT					Output to RF Switch		
Function	BT Priority	BT TX	WL TX	T/R Switch	Antenna	Rf_sw_ctrl_p_0	Rf_sw_ctrl_n_0	Rf_sw_ctrl_n_1
WL RX	0	0	0	0	0	1	0	0
WL RX with attenuation	0	0	0	1	0	0	0	1
WL TX	0	0	1	0	0	0	0	1
BT TX	0	1	0	0	0	0	1	0
BT RX	1	0	0	0	0	1	0	0

Strapping Options and GPIO Functions

The SPI signals and SDIO signals are muxed on the same pins. SPI/SDIO mode is determined by the strapping option on WL_GPIO_8 when WL_RST_N is deasserted. If WL_GPIO_8 is left floating or pulled high, then SPI mode is selected. If WL_GPIO_8 is pulled low, then SDIO mode is selected.

I/O States

In Table 13, BT_RST_N is associated with all BT_* signals and WL_RST_N is associated with all SPI_* signals.

Notation used in Table 13:

- PU = Pulled up
- PD = Pulled down
- None = Neither pulled up nor pulled down

Table 13: BCM4329 During and After Reset

Signal Name/Group	I/O	Keeper[a]	Active Mode		Low-Power/Sleep Mode[b]		Power-Down Mode[c]		Out of Reset[d, e, f]		In
			I/O	Pull	I/O	Pull	I/O	Pull	I/O	Pull	I/O
WL_REG_ON	I	N	Input	PD (pull-down can be disabled)	Input	PD (pull-down can be disabled)	Input	PD (200 KΩ)	Input	PD (200 KΩ)	Inp
WL_RST_N	I	Y	Input	None	Input	None	Input	None	Input	None	Inp
BT_RST_N	I	Y	Input	None	Input	None	Input	None	Input	None	Inp
BT_REG_ON	I	N	Input	PD (pull-down can be disabled)	Input	PD (pull-down can be disabled)	Input	PD (200 KΩ)	Input	PD (200 KΩ)	Inp
BT_GPIO 0, 2, 3, 4, 6, and 7	I/O	Y	I/O	PU, PD, none (programmable)	I/O	PU, PD, none (programmable)	High-Z	None	Input	None	Inp
BT_GPIO_1, 5	I/O	Y	I/O	PU, PD, none (programmable)	I/O	PU, PD, none (programmable)	High-Z	None	Output	None	Ou
BT_UART_CTS	I	Y	Input	None	Input	None	High-Z	None	Input	None	Inp
BT_UART_RTS	O	Y	Output	None	Output	None	High-Z	None	Output	None	Inp
BT_UART_RXD	I	Y	Input	None	Input	None	High-Z	None	Input	None	Inp
BT_UART_TXD	O	Y	Output	None	Output	None	High-Z	None	Output	None	Inp
SDIO Data	I/O	N	I/O	PU	Input	PU	High-Z	None	Input	PU	Dis Inp
SDIO CMD	I/O	N	I/O	PU	Input	PU	High-Z	None	Input	PU	Dis Inp
SDIO_CLK	I	N	Input	None	Input	None	High-Z	None	Input	None	Dis Inp
BT_PCM_CLK	I/O	Y	Input[h]	None	Input[h]	None	High-Z	None	Input	None	Inp
BT_PCM_IN	I/O	Y	Input[h]	None	Input[h]	None	High-Z	None	Input	None	Inp
BT_PCM_OUT	I/O	Y	Input[h]	None	Input[h]	None	High-Z	None	Input	None	Inp
BT_PCM_SYNC	I/O	Y	Input[h]	None	Input[h]	None	High-Z	None	Input	None	Inp
WL_GPIO_0 (N5)	I/O	Y	I/O	PU, PD, or none (programmable; default = PD)	I/O	PU, PD, or none (programmable; default = PD)	High-Z	None	Input	PD	Inp
WL_GPIO_1 (N4)	I/O	Y	I/O	PU, PD, or none (programmable; default = PU)	I/O	PU, PD, or none (programmable; default = PD)	High-Z	None	Input	PU	Inp
WL_GPIO_2 (N2)	I/O	Y	I/O	PU, PD, none (programmable default = PD)	I/O	PU, PD, or none (programmable; default = PD)	High-Z	None	Input	PD	Inp
WL_GPIO_3 (N1)	I/O	Y	I/O	PU, PD, none (programmable; default = PU)	I/O	PU, PD, none (programmable; default = PU)	High-Z	None	Input	PU	Inp
WL_GPIO_8 (P1)	I/O	Y	I/O	PU, PD, none (programmable; default = PU)	I/O	PU, PD, none (programmable; default = PU)	High-Z	None	Input	PU	Inp
UART_RX_0 (R4)	I	Y	Input	PU	Input	PU	High-Z	None	Input	PU	Inp
UART_TX_0 (R2)	O	Y	Output	None	Output	None	High-Z	None	Output	None	Ou
BT_SCL (M8)	I/O	Y	Input	None[i]	Input	None[i]	High-Z	None	Input	None	Inp
BT_SDA (M7)	I/O	Y	Input	None[i]	Input	None[i]	High-Z	None	Input	None	Inp

a. Keeper column: N = pad has no keeper. Y = pad has a keeper. The keeper is always active except in Power-Down mode.

b. Power is enabled on all rails.
c. BT_REG_ON and WL_REG_ON are held low. In the case of High-Z/none, the pad is disabled because power is not being supplied.
d. Software has not yet been downloaded; WL_RST_N, BT_RST_N, and REG_ON are high.
e. When only WLAN is out of reset (WL_RST_N = high; BT_RST_N = Low; REG_ON = high), the state of the chip will be same as *Out o*
f. When only BT is out of reset (WL_RST_N = low; BT_RST_N = high; REG_ON = high) the state of the chip will be same as *In Reset*.
g. BT_REG_ON or WL_REG_ON are high; BT_RST_N and WL_RST_N = 0; VDDIOs are present.
h. Can be either an input or an output depending on whether the PCM interface is enabled and PCM is configured for master or sla
i. If the I^2C interface is used for FM, the pin is configured to open drain with the internal pull up enabled.

Muxed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Bluetooth interface signals such as I^2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control Register for that specific pin. Table 14 shows the possible options for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control Register Setting is independent (i.e. BT_GPIO_1 can be set to Pad Function 7 at the same time that BT_GPIO_3 is set to PAD Function 0). When the Pad Function Control Register is set to 0 the BT_GPIOs do not have specific functions assigned to them and behave as generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the BCM4329's PCM and I^2C interface pins.

Table 14: GPIO Multiplexing Matrix

	Pad Function Control Register Setting							
Pin Name	***0***	***1***	***2***	***3***	***4***	***5***	***6***	***7***
BT_GPIO_7	BT_GPIO_7	DEBUG_TXD	–	I2S_MSCK	I2S_SSCK	–	–	CLASS1[2][a]
BT_GPIO_6	BT_GPIO_6	I2C_CK	–	–	–	–	–	FM_IRQ_N
BT_GPIO_5	BT_GPIO_5	I2C_DA	–	–	–	–	–	CLK_REQ[a]
BT_GPIO_4	BT_GPIO_4	–	–	I2S_MSDO	I2S_SSDO	–	–	CLASS1[1][a]
BT_GPIO_3	BT_GPIO_3	DEBUG_TXD	–	I2S_MWS	I2S_SWS	–	–	CLASS1[0][a]
BT_GPIO_2	BT_GPIO_2	–	–	–	I2S_SSDI	–	–	–
BT_GPIO_1	BT_GPIO_1[b]	–	–	–	–	–	–	CLK_REQ[a]
BT_GPIO_0	BT_GPIO_0[b]	–	–	–	–	–	–	–
BT_SCL	A_GPIO7	–	–	–	–	–	–	I2C_CK
BT_SDA	A_GPIO6	–	–	–	INT_LPO	–	–	I2C_DA
BT_PCM_IN	A_GPIO3	PCM_IN	–	–	–	–	–	I2S_SSDI
BT_PCM_OUT	A_GPIO2	PCM_OUT	–	–	INT_LPO	I2S_MSDO	–	I2S_SSDO
BT_PCM_SYNC	A_GPIO1	PCM_SYNC	–	–	–	I2S_MWS	–	I2S_SWS
BT_PCM_CLK	A_GPIO0	PCM_CLK	–	–	–	I2S_MSCK	–	I2S_SSCK

a. For internal Bluetooth debug only.
b. When set to function as generic GPIOs (Pad Control Register = 0), BT_GPIO_0 AND BT_GPIO_1 are often used for out of band power control signals BT_WAKE and UART_WAKE. See Table 1 on page 29 for more details.

The multiplexed GPIO signals are described in Table 15.

Table 15: Multiplexed GPIO Signals

Pin Name	*Type*	*Description*
PCM_IN	I	PCM data input
PCM_OUT	O	PCM data output
PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input)
PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
I2S_MSDO	O	I^2S master data output
I2S_MWS	O	I^2S master word select
I2S_MSCK	O	I^2S master clock
I2S_SSDI	I	I^2S slave data input
I2S_SSDO	O	I^2S slave data output
I2S_SWS	I	I^2S slave word select
I2S_SSCK	I	I^2S slave clock
CLASS1[2]	O	PA_VCTL power control for external PA
CLASS1[1]	O	TDD_P external T/R switch control
CLASS1[0]	O	TDD_N external T/R switch control
INT_LPO	O	Test signal for internal LPO
FM_IRQ_N	O	FM subsystem interrupt request
CLK_REQ	O	Reference clock (REFCLK) request (for internal Bluetooth debug only)
I2C_CK	I	I^2C-compatible clock
I2C_DA	I/O	I^2C-compatible bidirectional data
DEBUG_TXD	O	Debug serial transmit

Section 16: DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 16 indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 16: Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply voltage for RF	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
DC supply voltage for I/O	VDDIO	–0.5 to 4.1	V
DC supply for VBATT	VBATT	–0.5 to 6.5	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum Junction Temperature	T_j	125	°C

The environmental ratings are shown in Table 17.

Table 17: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85°C	°C	Operation
Storage Temperature	–40 to +105°C	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 18: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/ JESD22-A114	1500	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	50	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/ JESD22-C101	500 (300 for RF pins)	V

Recommended Operating Conditions and DC Characteristics

Functional operation is not guaranteed outside of the limits shown in Table 19. Operation outside these limits for extended periods can adversely affect the long-term reliability of the device.

Table 19: Recommended Operating Conditions and DC Characteristics

		Value			
Element	Symbol	Minimum	Typical	Maximum	Unit
DC supply voltage for VBATT	VBATT	2.3	–	5.5	V
DC supply voltage for I/O	VDDO	1.62	1.8V to 3.3V	3.63	V
Input low voltage (VDDO = 3.3V)[a]	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)[b]	V_{IH}	2.0	–	–	V

Table 19: Recommended Operating Conditions and DC Characteristics

		Value			
Element	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
Input low voltage (VDDO = 1.8V)[c]	V_{IL}	–	–	0.6	V
Input high voltage (VDDO = 1.8V)[d]	V_{IH}	1.1	–	–	V
Output low voltage (100 µA load)	V_{OL}	–	–	0.2	V
Output high voltage (–100 µA load)	V_{OH}	VDDIO – 0.2V		–	V
Input low current	I_{IL}	–	0.3	–	µA
Input high current	I_{IH}	–	0.3	–	µA
Output low current (VDDO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	3.0[e]	mA
Output high current (VDDO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	3.0[e]	mA
Input capacitance	C_{IN}	–	–	5	pF

a. 3.3V IO Undershoot: the absolute maximum undershoot limit is 500 mV below ground for no more than 25% of the duty cycle.
b. 3.3V IO Overshoot: the absolute maximum overshoot limit is 500 mV above supply for no more than 25% of the duty cycle.
c. 1.8V IO Undershoot: the absolute maximum undershoot limit is 300 mV below ground for no more than 25% of the duty cycle.
d. 1.8V IO Overshoot: the absolute maximum overshoot limit is 300 mV above supply for no more than 25% of the duty cycle.
e. For SDIO interface outputs, the drive level is programmable from 2–12 mA (default is 10 mA).

Section 17: Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 17 on page 90 and Table 19 on page 91. Functional operation outside of these limits is not guaranteed.

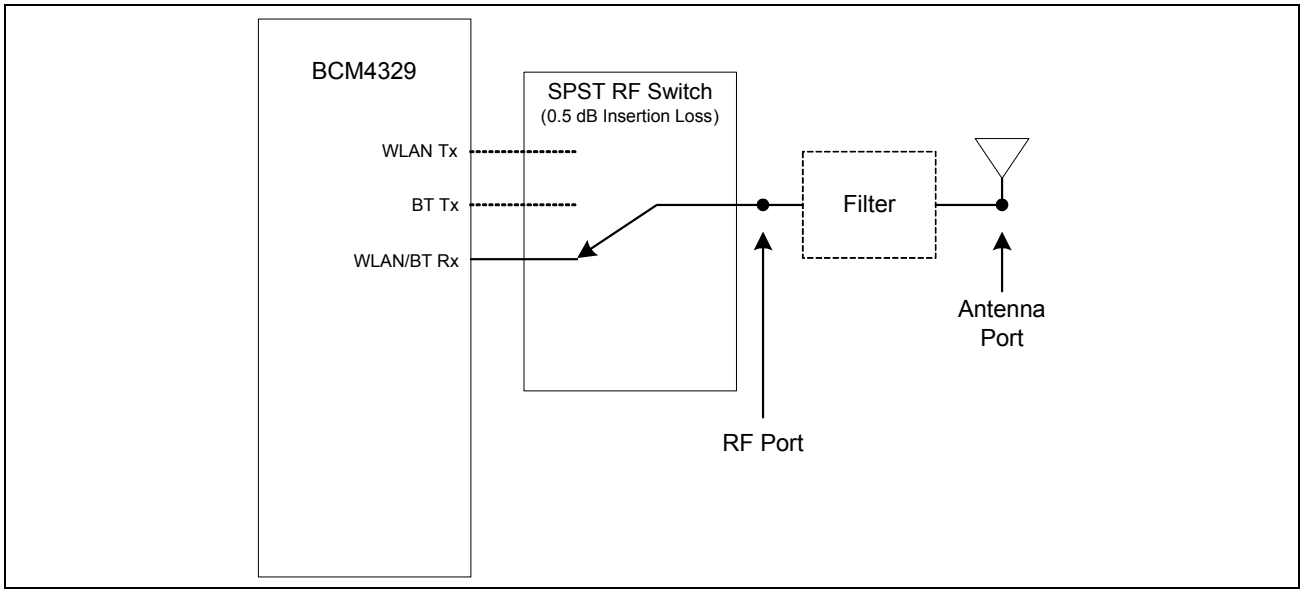

Figure 25: RF Port Location

Note: All specifications are measured at the RF port unless otherwise specified.

Table 20: Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–89	–84	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–91	–87.5	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–85	–82.5	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Return loss of BT Rx and Tx pins	50Ω port	10	–	–	dB
Interference Performance[1]					
C/I cochannel	GFSK, 0.1% BER	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	–	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0.0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB

Table 20: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer [2]					
776–794 MHz	CDMA2000	–	+10	–	dBm
824–849 MHz	cdmaOne	–	+8	–	dBm
824–849 MHz	GSM850	–	+13	–	dBm
880–915 MHz	E-GSM	–	+14	–	dBm
1710–1785 MHz	GSM1800	–	+4	–	dBm
1850–1910 MHz	GSM1900	–	0	–	dBm
1850–1910 MHz	cdmaOne	–	–8	–	dBm
1850–1910 MHz	WCDMA	–	–16	–	dBm
1920–1980 MHz	WCDMA	–	–19	–	dBm
Spurious Emissions					
30 MHz–1 GHz		–	–	–62	dBm
1–12.75 GHz		–	–	–47	dBm
Out-of-Band Noise Floor					
851–894 MHz		–	–145	–	dBm/Hz
925–960 MHz		–	–145	–	dBm/Hz
1805–1880 MHz		–	–145	–	dBm/Hz
1930–1990 MHz		–	–145	–	dBm/Hz
2110–2170 MHz		–	–145	–	dBm/Hz
Rx LO Leakage					
2.4 GHz band		–	–	–54.0	dBm

1. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 2.1 specification.

2. Bluetooth reference level for wanted signal at the Bluetooth RF port = –82.5 dBm + 3 dB = –79.5 dBm.

Table 21: Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) Tx power at Bluetooth RF port		–	11	–	dBm
QPSK Tx Power at Bluetooth RF Port		–	11	–	dBm
8PSK Tx Power at Bluetooth RF Port		–	8	–	dBm
Relative Power (EDR)		–1	0	+1	dB
Power control step		2	4	6	dB
In-Band Spurious Emissions					
±500 kHz		–	–	–20.0	dBc
1.0 MHz < |M–N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–	–26.0	dBc
1.5 MHz < |M–N| < 2.5 MHz[a]		–	–	–40.0	dBm
|M–N| ≥ 2.5 MHz		–	–	–60.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz		–	–	–36.0 [b, c]	dBm
1 GHz to 12.75 GHz		–	–	–30.0 [b, c]	dBm
1.8 GHz to 1.9 GHz		–	–	–37.0	dBm
5.15 GHz to 5.3 GHz		–	–	–37.0	dBm
GPS Band Spurious Emissions					
Spurious emissions		–	–150	–124	dBm/Hz
Out-of-Band Noise Floor[d]					
76–108 MHz	FM Rx	–	–145	–	dBm/Hz
746–764 MHz	CDMA2000	–	–145	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–145	–	dBm/Hz
925–960 MHz	E-GSM	–	–145	–	dBm/Hz
1570–1580 MHz	GPS	–	–140	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–140	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–140	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–135	–	dBm/Hz

a. In-band spurious emissions fail at ±2 MHz offset if battery voltage falls below 2.7V.
b. The maximum value represents the value required for Bluetooth qualification as defined in the v2.1 specification.
c. The spurious emissions during Idle mode are the same as specified in Table 21 on page 96.
d. Transmitted power in cellular and FM bands at BT RF port. See Figure 25 on page 93 for location of BT RF port.

Table 22: Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	130	180	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±20	±25	kHz
DH3 packet	–	±20	±40	kHz
DH5 packet	–	±20	±40	kHz
Drift rate	–	10	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	–	175	kHz
10101010 sequence in payload[b]	115	–	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Section 18: FM Transmitter Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 17 on page 90 and Table 19 on page 91. Functional operation outside of these limits is not guaranteed.

Table 23: FM Transmitter Specifications

Parameter	Conditions	Min	Typ	Max	Units
Synthesizer RF Parameters					
Operating frequency	Frequencies inclusive	76	–	108	MHz
Frequency step	Channel resolution		50		kHz
Settling time	Single frequency switch in any direction to a frequency within the bands 88–108 MHz or 76–95 MHz. Time measured to within 5 kHz of the final frequency.	25	–	40	ms
FM Rx/Tx antenna switching time		–	5	–	ms/ channel
Frequency accuracy	Over temperature and voltage using available reference clocks	–10	–	10	kHz
Transmitter Output					
Maximum transmit output level	Driving from a current source output into a resonated loop antenna for which L = 120 nH nominal, with a $Q \geq 30$, all Tx frequencies ON, L= R = 0 (that is, no modulation), 0 dB internal attenuation/ gain, and a 1.8V supply.	+114[a]	+120	–	dBuV
	Driving from current source output into coil load, with a $Q \geq 30$, all frequencies, Tx attenuation set to 24 dB	–	+96	–	dBuV
FM antenna port impedance	–	500	1k	–	Ω
Tuning Capacitance range	76 to 108 MHz Based on tuning inductance of 120 to 150 nH	0	0	3	pF
Transmitter output accuracy[b, c]	Over entire output range	–2	–	2	dB
Gain step accuracy	25 levels in normal 1 dB steps, one of those being 0 dB	–0.5	1	1.5	dB
Pilot deviation	Relative to maximum peak deviation	8	–	10	%

Table 23: FM Transmitter Specifications (Cont.)

Parameter	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Transmitted spectrum for maximum deviation	Total peak deviation set to 75 kHz. Audio tone of 1 kHz, pilot = 6.75 kHz.	–	–	–	–
	0 kHz offset from carrier	–	–	0	dBc
	+/- 50 kHz offset	–	–	0	dBc
	+/- 75 kHz offset	–	–	0	dBc
	+/- 120 kHz offset	–	–	–12.2	dBc
Occupied BW	+/- 100 kHz offset from nominal channel freq	–	–	–20	dBc
Transmitter noise floor	From 850 MHz to 2.4 GHz	–	–	–140	dBm/ Hz
Composite transmitted deviation	L = R set to 75-mV rms, stereo enabled	–	–	+/- 75	kHZ peak
Transmitter spurious	RL = 500Ω in parallel with 120 nH Q = 30 and resonant capacitance at transmitter tuned frequency driven from current source output	–	–	–	–
	746–764 MHz	–	–	–102	dBm
	869–894 MHz, 925–960 MHz, 1805–1880 MHz, 1930–1990 MHz	–	–	–109	dBm
	2110–2170 MHz	–	–	–96	dBm
	1570–1580 MHz	–	–	–106	dBm
Analog audio input level for rated deviation, range setting 1	AC- coupled, 1 kHz tone for 75 kHz carrier deviation	80	100	125	mVp
Analog audio input level for rated deviation, range setting 2	AC- coupled, 1 kHz tone for 75 kHz carrier deviation	160	200	250	mVp
Analog audio input level for rated deviation, range setting 3	AC- coupled, 1 kHz tone for 75 kHz carrier deviation	240	300	375	mVp
Analog inputs-impedance	–	30K	–	–	Ω
Transmitted deviation flatness	Change in audio level for 75 kHz deviation over 76–108 MHz	–	–	+/-1	dB
Channel balance	1 kHz tone for 22.5 kHz audio deviation L = R, pilot 6.75 kHz	–1	–	1	dB
Stereo separation	1 kHz tone for 22.5 kHz audio deviation L ≠ R , pilot 6.75 kHz	27	40		dB
	Lower 3 dB point[d] (measured with receiver set to correct de-emphasis)	–	–	50	Hz
	Upper 3 dB point[a]	15	–	–	kHz
Pre-emphasis time constant	High	–	75	–	Us
	Low	–	50	–	Us
	Tolerance	–	–	+/-5	%
Distortion	75 kHz total deviation including 6.75 kHz pilot, 1 kHz modulation rate	–	0.1	1	%

Table 23: FM Transmitter Specifications (Cont.)

Parameter	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Transmitted S/N depends on the 32.768 kHz sleep clock phase noise performance	Deviation set to 22.5 kHz with 6.75 kHz pilot deviation. Measured with 50 μS de-emphasis and A-weighted filter. Forced Mono	57	–	–	dB
	As above in Stereo	54	–	–	dB
Audio spurious products	Δf = 22.5 kHz, fmod = 1 kHz, de-emphasis = 50 μs, L = R, BAF = 300 Hz to 15 kHz, fTX = 76 to 108 MHz	–	–	–60	dBc[a]

a. The +114 dBuV occurs between 76–88 MHz, and 105–108 MHz when using external filter to optimize out of band spurious performance.
b. Relative to mean power in the band.
c. Valid for U.S. and European bands only
d. With respect to a 1 kHz tone.

Section 19: FM Receiver Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 17 on page 90 and Table 19 on page 91. Functional operation outside of these limits is not guaranteed.

Table 24: FM Receiver Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
RF Parameters					
Operating frequency	Frequencies inclusive	76	–	108	MHz
Sensitivity[a], V_{RF}	FM only, fmod = 1 kHz, Δf = 22.5 kHz (S+N)/N = 26 dB, BAF = 300 Hz to 15 kHz, A-weighted de-emphasis = 50 µs, f_{IN} = 76 to 108 MHz	–	–107	–102	dBm
	RDS. For an RDS deviation of 1.2 kHz. 95% of blocks decoded with no errors, over a sample of 5000 blocks.	–	–83	–78	dBm
	RDS. For an RDS deviation of 2 kHz. 95% of blocks decoded with no errors, over a sample of 5000 blocks.	–	–88	–85	dBm
RDS selectivity	Wanted RF level = RDS sensitivity + 3 dB, 2 kHz deviation. Interferer 40 kHz deviation 1 kHz tone.				
	Interferer level for 5% BLER				
	±200 kHz	S + 16	–	–	dBm
	±300 kHz	S + 25	–	–	dBm
	±400 kHz	S + 35	–	–	dBm
Receiver adjacent channel selectivity	At ±200 kHz. f_{IN} = 76 to 108 MHz. Measured for 40 dB S/I at the audio output according to EN55020 (mono & stereo).	16	–	–	dB
	At ±300 kHz (as above)	25	–	–	dB

Table 24: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Image response (assuming image frequency ≥ ±300 kHz), mono	At f_{wanted} ±2fIF, depending on LO injection relative to F_{wanted}. Measured for 40-dB S/I at the audio output according to EN55020. Image frequency = ±325 kHz and ±375 kHz.	25	–	–	dB
Image response (assuming image frequency ≥ ±300 kHz), stereo		40[b]	–	–	dB
Min S/N for in band blocking for offsets ≥ 400 kHz, mono	Wanted level set to –90 dBm, Δf = 75 kHz. Interferer level set to –55 dBm, Δf = 40 kHz, 1-kHz tone, AGC on.	40	–	–	dB
Min S/N for in band blocking for offsets ≥ 400 kHz, stereo	Wanted level set to –72 dBm, Δf = 75 kHz, 1-kHz tone. Interferer level set to –37 dBm.	40	–	–	dB
Intermediate S/N in the presence of intermodulation	Overall third-order intercept point, for tones ±400 and ±800 kHz, ±4 and ±8 MHz. Reference level is –82 dBm, tone levels set at –50 dBm. f_{IN} = 76 to 108 MHz. AGC enabled.	40	–	–	dB
AM suppression, mono	Vin = –90 dBm, fmod = 1 kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz, L = R, de-emphasis = 75 µs	40	–	–	dB
AM suppression, stereo	Vin = –47 dBm, fmod = 1 kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz, L = R, de-emphasis = 75 µs	40	–	–	dB
Intermediate S/N	Vin = –93 dBm (Vin 10 µV emf), fmod = 1kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz A-weighted, mono, de-emphasis = 50 µs	45	–	–	dB
RF Input					
RF input impedance	Single-ended input with external matching circuitry (see Figure 26 on page 105)	–	50	–	Ω
RF input level	Maximum on-channel input level 76–108 MHz.	–	–	–2	dBm
RF input impedance return loss	With external matching circuitry	–	–	10	dB
RF conducted emissions	Local oscillator breakthrough measured on the reference port	–	–	–55	dBm
	925–960 MHz, 1805–1880 MHz, and 1930–1990 MHz	–	–	–90	dBm

Table 24: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
RF blocking levels at the FM antenna input. (Assumes presence of an external matching circuit, see Figure 26 on page 105.)	824–915 MHz, GSM 200 kHz BW, CDMA 1.2 MHz BW	–	–	0	dBm
	1710–1980 MHz, GSM 200 kHz BW, CDMA 1.2 MHz BW, WCDMA 4 MHz BW	–	–	–5	dBm
	2.4–2.4835 GHz, BT 1 MHz BW, WLAN 20 MHz BW	–	–	–20	dBm
PLL					
Frequency step	Channel offset	–	–	50	kHz
Settling time	Single frequency switch in any direction to a frequency within the bands 88–108 MHz or 76–90 MHz. Time measured to within 5 kHz of the final frequency.	–	–	5	ms
Sweep time	Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (and reverse direction) assuming no channels found.	–	–	8	sec
Soft Mute					
Soft mute start level	Mute attenuation = 3 dB	–	2.8	–	uV
Soft mute attenuation	Vin = 1 µV, Δf = 22.5 kHz, L = R fmod = 1 kHz, BAF = 300 Hz to 15 kHz, de-emphasis = 75 µs	–	6	–	dB
General Audio					
Audio output level	Vin = 1 mV, Δf = 22.5 kHz_p fmod = 1 kHz, L = R, de-emphasis = 75 µs. Δf Pilot = 6.75 kHz_p, Rload > 30Ω	60	75	90	mV, rms
Maximum audio output level	Vin = 1 mV, Δf = 100 kHz_p fmod = 1 kHz, L = R, de-emphasis = 75 µs. Δf Pilot = 6.75 kHz_p, Rload > 30Ω	–	–	360	mV, rms
Audio output level difference	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, L = R, de-emphasis = 75 µs	–1	–	1	dB
Max signal plus noise to noise ratio (S+N)/N, mono	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, de-emphasis = 50 µs, L = R, BAF = 300 Hz to 15 kHz (A-Weighted) f_{IN} = 76 to 108 MHz	56	60	–	dB
Max signal plus noise to noise ratio (S+N)/N, stereo		53	56	–	dB

Table 24: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Total harmonic distortion, mono	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 400 Hz, de-emphasis = 50 µs	–	0.4	0.8	%
	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 1 kHz, de-emphasis = 50 µs	–	0.4	0.8	%
	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 3 kHz, de-emphasis = 50 µs	–	0.4	0.8	%
	Vin = 1 mV, Δf = 100 kHz, L = R, fmod = 1 kHz, de-emphasis = 50 µs	–	0.5	0.8	%
Total harmonic distortion, stereo	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 3 kHz, de-emphasis = 50 µs	–	0.9	1.5	%
Audio spurious products	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, de-emphasis = 50 µs, L = R, BAF = 300 Hz to 15 kHz (A-Weighted), f_{IN} = 76 to 108 MHz, With respect to 1 kHz tone	–	–	–60	dBC
Audio bandwidth, upper (–3-dB point)	Vin = 1 mV, Δf = 22.5 kHz, for both 50- and 75-µs de-emphasis, pre-emphasis applied. Lower audio bandwidth (–3-dB point) measured at application circuit with AC coupling capacitor.	15 K	–	–	Hz
Audio bandwidth, lower (–3-dB point)		–	–	20	Hz
Deviation of the audio response from an ideal de-emphasis curve	100 Hz to 13 kHz, Vin = 1 mV, Δf = 22.5 kHz, for both 50- and 75-µs de-emphasis, pre-emphasis applied	–	–	±0.5	dB
De-emphasis time constant tolerance	With respect to 50 and 75 µs	–	–	±5	%
Audio output impedance	When FM function is disabled, or when left or right channels are hard-muted via the bus	50	–	–	kΩ
Audio output impedance	When FM function is enabled and in any of the following modes: autosearch, AC-muted by software, or RF soft-mute is active	–	–	50	Ω
Left and right AC_mute		60	–	–	dB
Right audio output hard muting attenuation		80	–	–	dB
Left audio output hard muting attenuation		80	–	–	dB
RSSI range	±3 dB accuracy with 1 dB resolution	–110	–	–30	dBm
Pause Detection					
Audio level at which a pause is detected	Relative to 1 kHz tone, 22.5 kHz deviation, 50-µs de-emphasis	–	–	–	–
	4 values in 3 dB steps	–21	–	–12	dB
Audio pause duration	4 values	20	–	40	ms

Table 24: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Stereo Decoder					
Stereo channel separation	SNC = OFF, increasing RF input, switched from mono to stereo Δf = 75 kHz, fmod = 1 kHz, 30-µV input level, R = 0, L = 1 including 9% pilot	27	30	–	dB
Mono/stereo blend start level[b]	Stereo channel separation = 1 dB, SNC ON (additional to nominal channel imbalance)	10	15	20	µV
Mono/stereo switching hysteresis	SNC = OFF, Δf = 75 kHz, fmod = 1 kHz, R = 0, L = 1 including 9% pilot	2	3	4	dB
Pilot suppression	Measured at audio outputs. Δf = 75 kHz, fmod = 1 kHz, de-emphasis = 75 µs	46	–	–	dB
Mono/Stereo switching level	SNC = OFF, Δf = 75 kHz, fmod = 1 kHz, R = 0, L = 1 including 9% pilot	60	80	110	µV emf

a. Sensitivity numbers are specified in potential difference and RDS sensitivity numbers are for 87.5–108 MHz only.
b. Performance trade off exists between SNR and blending profile with SNC = ON.

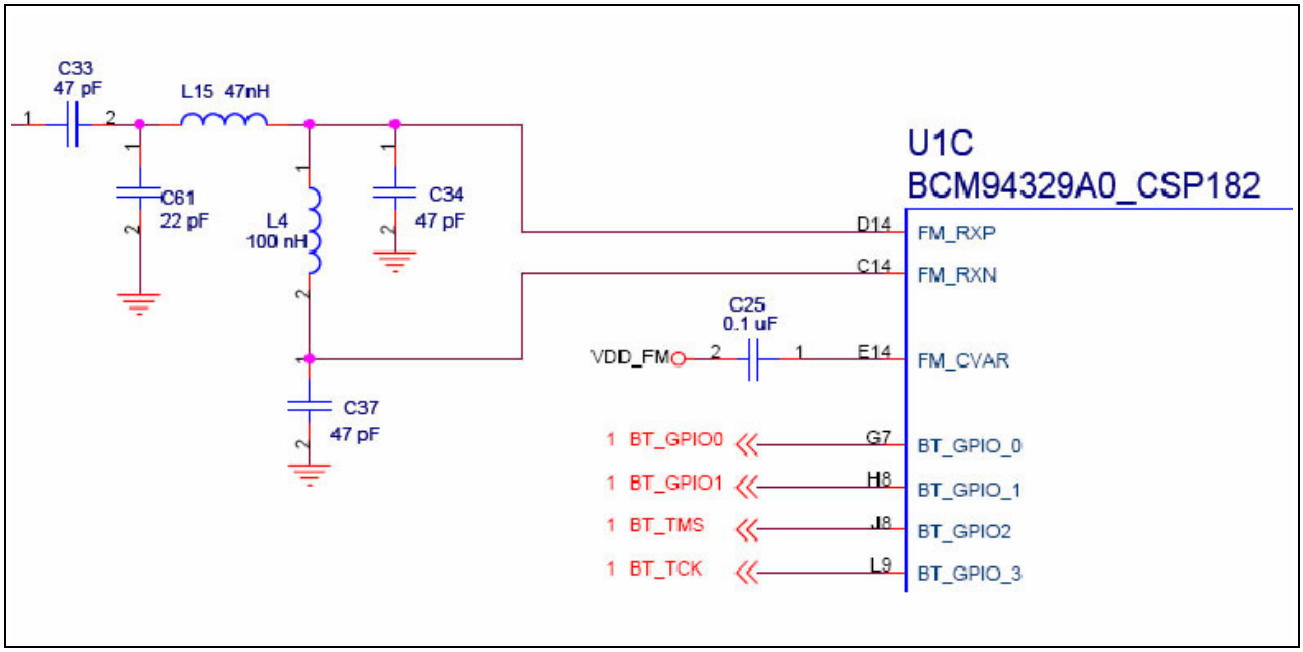

Figure 26: FM Receiver Circuit with External Balun and Cellular Band Blocking Filter

Section 20: WLAN RF Specifications

Introduction

The BCM4329 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. The BCM4329 does not provide simultaneous 2.4 GHz and 5 GHz operation. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 17 on page 90 and Table 19 on page 91. Functional operation outside of these limits is not guaranteed.

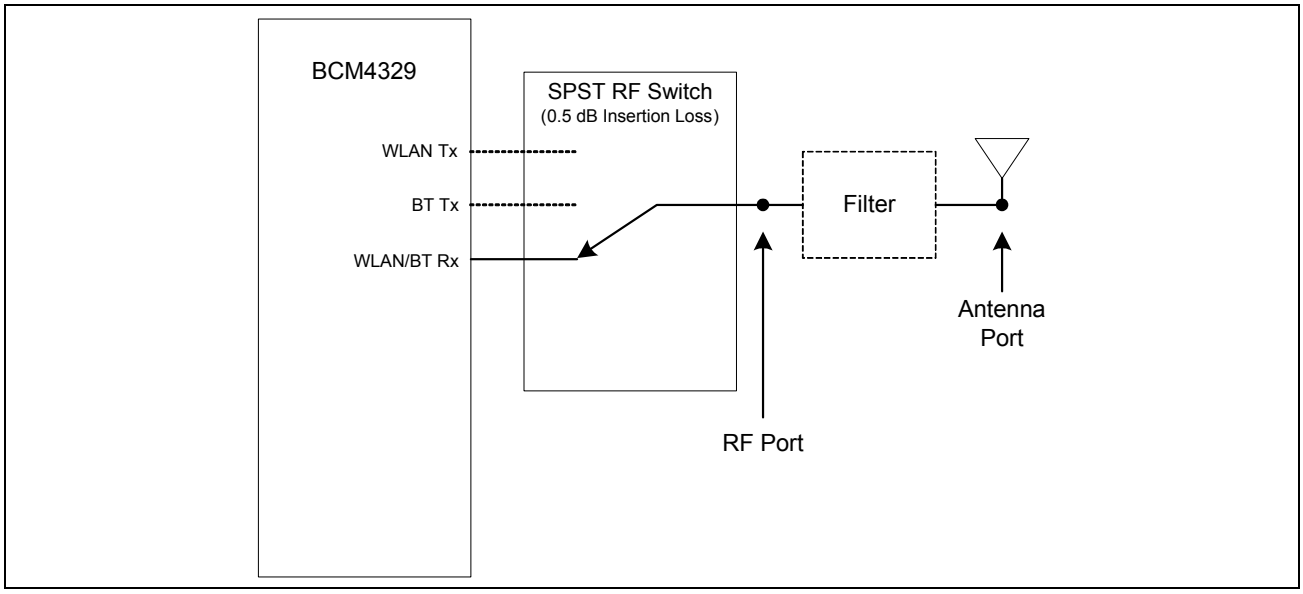

Figure 27: RF Port Location

Note: All specifications are measured at the RF port unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 25: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 26 are measured at the RF port.

Table 26: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
Operating temperature	–	–30	25	85	°C
RX sensitivity (8% PER for 1024 octet PSDU) at WLAN RF port[a]	1 Mbps DSSS	–94	–97	–	dBm
	2 Mbps DSSS	–91	–94	–	dBm
	5.5 Mbps DSSS	–90	–92	–	dBm
	11 Mbps DSSS	–88	–90	–	dBm
RX sensitivity (10% PER for 1024 octet PSDU) at WLAN RF port[a]	6 Mbps OFDM	–90	–91.5	–	dBm
	9 Mbps OFDM	–89	–90.5	–	dBm
	12 Mbps OFDM	–88	–90	–	dBm
	18 Mbps OFDM	–86	–88	–	dBm
	24 Mbps OFDM	–84	–86	–	dBm
	36 Mbps OFDM	–80	–82	–	dBm
	48 Mbps OFDM	–76	–78	–	dBm
	54 Mbps OFDM	–74	–76	–	dBm

Table 26: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity (10% PER for 4096 octet PSDU) at WLAN RF port[a,b]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS 7		–71	–73	–	dBm
	MCS 6		–72.5	–74.5	–	dBm
	MCS 5		–74.5	–76.5	–	dBm
	MCS 4		–78.5	–80.5	–	dBm
	MCS 3		–82	–84	–	dBm
	MCS 2		–84.5	–86.5	–	dBm
	MCS 1		–86.5	–88.5	–	dBm
	MCS0		–88	–90	–	dBm
Blocking level @ WLAN RF port for 1dB Rx sensitivity degradation (without external filtering)	776–794 MHz	CDMA2000	–8	–	–	dBm
	824–849 MHz[c]	cdmaOne	–24.5	–	–	dBm
	824–849 MHz	GSM850	–16.5	–	–	dBm
	880–915 MHz	E-GSM	–2	–	–	dBm
	1710–1785 MHz	GSM1800	–17	–	–	dBm
	1850–1910 MHz	GSM1800	–21	–	–	dBm
	1850–1910 MHz	cdmaOne	–32	–	–	dBm
	1850–1910 MHz	WCDMA	–29	–	–	dBm
	1920–1980 MHz	WCDMA	–32	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–	–	–3.5	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–	–	–9.5	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–	–	–9.5	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–	–	–9.5	dBm
LPF 3-dB Bandwidth	–		9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	11 Mbps DSSS	–70 dBm	35	–	–	dB

Table 26: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[d]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range		10	11.5	13	dB

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
d. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 27 are measured at the RF port input.

Note: The switch insertion loss at 5 GHz is approximately 1dB.

Table 27: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
RX sensitivity (10% PER for 1000 octet PSDU) at WLAN RF port[a]	6 Mbps OFDM		–87.5	–89	–	dBm
	9 Mbps OFDM		–86.5	–88	–	dBm
	12 Mbps OFDM		–86.5	–88	–	dBm
	18 Mbps OFDM		–85.5	–87	–	dBm
	24 Mbps OFDM		–82.5	–84	–	dBm
	36 Mbps OFDM		–79.5	–81	–	dBm
	48 Mbps OFDM		–73.5	–75	–	dBm
	54 Mbps OFDM		–71.5	–73	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU) at WLAN RF port[a]	MCS0		–87	–89	–	dBm
	MCS7 (64 QAM, R = 5/6, 20 MHz channel spacing)		–69.5	–71	–	dBm
Blocking level @ WLAN RF port for 1 dB Rx sensitivity degradation	776–794 MHz	CDMA2000	–21	–	–	dBm
	824–849 MHz	cdmaOne	–20	> +10	–	dBm
	824–849 MHz	GSM850	–12	> +10	–	dBm
	880–915 MHz	E-GSM	–12	–	–	dBm
	1710–1785 MHz	GSM1800	–15	+8.5	–	dBm
	1850–1910 MHz	GSM1800	–15	+7.5	–	dBm
	1850–1910 MHz	cdmaOne	–20	+8.5	–	dBm
	1850–1910 MHz	WCDMA	–21	–	–	dBm
	1920–1980 MHz	WCDMA	–21	+1	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps		–14.5	–	–	dBm
LPF 3-dB bandwidth	–		9	–	10	MHz

Table 27: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[b] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	100	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[c]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Zo = 50Ω		10	14	–	dB

a. Derate by 1.5 dB for -30 °C to -10°C and 55°C to 85°C.
b. For 65 Mbps, the size is 4096.
c. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 28 are measured at the RF port output.

Table 28: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands at RF port across rates and channels at Tx power specified in this table (see below).	76–108 MHz	FM Rx	–	–149	–	dBm/Hz
	776–794 MHz	CDMA2000	–	–127	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–147	–	dBm/Hz
	925–960 MHz	E-GSM	–	–145	–	dBm/Hz
	1570–1580 MHz	GPS	–	–145	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–144	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–140	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–127	–123	dBm/Hz
Harmonic level at RF port (at 20.5 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–	–10	dBm/ 1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–	–28	dBm/ 1 MHz
Tx power at RF port for highest power level setting at 25°C, VBATT = 3.6V and spectral mask and EVM compliance[a, b]		***EVM Does Not Exceed***				
	802.11b (DSSS/CCK)	–9 dB	19	20.5	–	dBm
	OFDM, BPSK	–8 dB	18.5	20	–	dBm
	OFDM, QPSK	–13 dB	18.5	20	–	dBm
	OFDM, 16-QAM	–19 dB	16	17.5[c]	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	16	17.5[e]	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	14	15.5	–	dBm
Tx power control dynamic range	–		10	–	–	dB
Closed-loop Tx power variation	Across full temperature and voltage range. Power accuracy of ±1.5 dB for 10–20 dBm and ±3 dB for 5–10 dBm.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB

Table 28: WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Return loss	Zo = 50Ω		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	2:1	EVM degradation	–	3.5	–	dB
		Output power variation	–	±2.0	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. Derate by 1.5 dB for −30 °C to −10°C and 55°C to 85°C.
b. Tx power for Ch 1 and Ch 11 is specified by non-volatile memory parameters.
c. Tx power for OFDM 16 QAM and 64 QAM is 16.5 dBm at the RF port when VBATT = 2.7V.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 29 are measured at the RF port. The switch insertion loss at 5 GHz is approximately 1dB.

Table 29: WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands at RF port (at 18 dBm)	76–108 MHz	FM Rx	–	–162	–110.5	dBm/Hz
	776–794 MHz	CDMA2000	–	–162	–114.5	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–162	–114.5	dBm/Hz
	925–960 MHz	E-GSM	–	–162	–113.5	dBm/Hz
	1570–1580 MHz	GPS	–	–162	–124.5	dBm/Hz
	1805–1880 MHz	GSM1800	–	–162	–118.5	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–162	–119.5	dBm/Hz
	2010–2170 MHz	WCDMA	–	–162	–129.5	dBm/Hz
	2400–2483 MHz	BT/WLAN	–	–162	–148.5	dBm/Hz
Harmonic level at RF port (at 18 dBm)	9.8–11.570 GHz	2nd harmonic	–	–31	–27	dBm/1 MHz
Tx power at RF port for highest power level setting at 25°C, VBATT = 3.6V and spectral mask and EVM compliance[a]		***EVM Does Not Exceed***				
	OFDM, BPSK	–8 dB	–	14	–	dBm
	OFDM, QPSK	–13 dB	–	14	–	dBm
	OFDM, 16-QAM	–19 dB	–	14	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	14	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	–	12	–	dBm
Tx power control dynamic range	–		10	–	–	dB
Tx power control resolution	–		0.5	–	–	dB
Closed loop Tx power variation at highest power level setting	Across full temperature and voltage range		–	–	±2	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB

Table 29: WLAN 5 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Return loss	Zo = 50Ω		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	2:1	EVM degradation	–	3.5	–	dB
		Output power variation	–	±1.5	–	dB
		ACPR-compliant power level	–	15	–	dBm
	3:1	EVM degradation	–	3.5	–	dB
		Output power variation	–	±1.5	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. Derate by 1.5 dB for -30 °C to -10°C and 55°C to 85°C.

General Spurious Emissions Specifications

Table 30: General Spurious Emissions Specifications

Parameter	Condition/Notes		Min	Typ	Max[a]	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–	–62	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–	–41.2	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–	–53	dBm
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–78	–63	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–68.5[b]	–53	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–96	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–96	–53	dBm

a. Using conducted measurement at the antenna port for Tx powers as given in Table 28. Measurements were taken with the Murata® LFB2H2G45CC1D005 blocking filter in place.
b. For frequencies other than 3.2 GHz, the emissions value is –96 dBm. The value presented in table is the result of LO leakage at 3.2 GHz.

Section 21: Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

Core Buck Regulator (CBuck)

Table 31: Core Buck Regulator (CBUCK)

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Units*
Input supply voltage	–	2.3	–	5.5	V
PWM mode switching frequency	–	2.24	2.8	3.36	MHz
PWM output current	–	–	–	300	mA
Output voltage range	Programmable, 25 mV steps	1.0	1.45	1.75	V
Output voltage accuracy	–	–5	–	5	%
PWM ripple voltage, static load	Measured with a 20 MHz bandwidth limit.	–	7	20	mVpp
PWM ripple voltage, dynamic load	200 mA, 1 µs rise/fall current step	–	70	100	mV
Burst mode ripple voltage, static	<30 mA load current, measured with a 20 MHz bandwidth limit.	–	–	80	mVpp
PWM mode efficiency	200 mA load current	80	90	–	%
Burst mode efficiency	10 mA load current	70	80	–	%
Low power mode efficiency	200 µA load current	–	60	–	%
	5 mA load current	–	75		
Quiescent current	Burst Mode	–	30	–	µA
	Low Power Mode	–	20		
	Power Down	–	1		
Output current limit	–	–	600	–	mA
Output capacitor[a]	–	3.76	4.7	5.64	µF
Output inductor[a]	–	2.64	3.3	3.96	µH
Start-up time from power down	–	–	500	1000	µs
Settling time: LPOM to burst	Ensure load current < 5 mA during mode change.	–	–	200	µs

Table 31: Core Buck Regulator (CBUCK)

Specification	Notes	Minimum	Typical	Maximum	Units
Settling time: Burst To PWM mode	Ensure load current < 30 mA during mode-change.	–	–	400	µs

a. Refer to Broadcom document 4329-AN2XX-R for component recommendations.

PALDO

Table 32: PALDO [a]

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.3	–	5.5	V
Output current	–	–	–	400	mA
Output voltage range	Programmable, 100 mV steps	2.3	3.3	4.0	V
Output voltage accuracy	–	–5	–	5	%
Quiescent current	No load Max load		40 8		µA mA
Output noise	@30 kHz, 100 mA	–	–	500	nV/rt Hz
Output capacitor (ESR: 30m–200 mΩ)	–	–	3.3	–	µF
Output current limit	–	–	700	–	mA
Drop-out voltage	300 mA load	–	–	200	mV
Start-up time from power down	–	–	30	60	µs
Settling time for voltage step change[b]	2.5 to 3.3V(10–90%)	–	20	–	µs

a. PALDO has a programmable overvoltage protection setting. It can be enabled (default) or disabled and can be set to 3.6V or 4.4V.
b. Settling time for ΔV high to low voltage change will depend on load current: Tset ~ Cout ΔV/Iload

2.5V LDO (LDO2p5V)

Table 33: 2.5V LDO (LDO2p5V)

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.3	–	5.5	V
Output current	–	–	–	50	mA
Output voltage	–	2.25	2.5	2.75	V

Table 33: 2.5V LDO (LDO2p5V)

Specification	Notes	Minimum	Typical	Maximum	Units
Quiescent current	No load	–	6	–	µA
	Max load	–	1.5	–	mA
Output capacitor (ESR: 30–200 mΩ)	–	0.7	1	5	µF
Start-up time from power-down	–	–	500	1000	µs

CLDO

Table 34: CLDO

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	1.35	1.4	2.0	V
Output voltage	Programmable in 25 mV steps	1.10	1.25	1.35	V
Absolute accuracy	–	–	–	+/-4	%
Output current	–	–	–	200	mA
LDO quiescent current	–	–	10	15	µA
Leakage current through output transistor	CLDO_pu = 0		0.1	10	µA
Output noise	@30 kHz 200 mA load		80	–	nV/rt Hz
Power supply rejection (PSR)	@1 kHz, 150 mV dropout	–	40	–	dB
Output capacitor	Output capacitor (ESR: 30–200 mΩ)	–	4.7	–	µF
Dropout voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

LNLDO1, LNLDO2

Table 35: LNLDO1, LNLDO2

Specification	Notes	Minimum	Typical	Maximum	Units
Input Supply Voltage	LNLDOi_vo_sel = 0	1.35	1.4	2.0	V
	LNLDOi_vo_sel = 1	3.0	3.3	3.6	
Output Voltage	LNLDOi_vo_sel = 0	1.10	1.25	1.35	V
	LNLDOi_vo_sel = 1	2.5	2.5	3.1	
Absolute Accuracy	–	–	–	+/-4	%
Output Current For LNLDO1	–	–	–	150	mA
Output Current For LNLDO2	–	–	–	50	mA
Quiescent Current for LNLDO1	LNLDOi_vo_sel = 0		31	44	µA
	LNLDOi_vo_sel = 1		110	206	
Quiescent Current for LNLDO2,3,4	LNLDOi_vo_sel = 0		29	42	µA
	LNLDOi_vo_sel = 1		108	202	
Leakage Current for LNLDO1 (LNLDO1_pu = 0)	LNLDOi_vo_sel = 0 (1.25V)		0.1	5	µA
	LNLDOi_vo_sel = 1 (2.5V)		0.1	9	
Leakage Current for LNLDO2,3,4 (LNLDO1_pu = 0)	LNLDOi_vo_sel = 0 (1.25V)		0.1	2	µA
	LNLDOi_vo_sel = 1 (2.5V)		0.1	4	
Output Noise	@30 kHz, 50 mA load				
	LNLDOi_vo_sel = 0		20		nV/rt Hz
	LNLDOi_vo_sel = 1		31		
PSR for LNLDO	@1 kHz, 150 mV dropout	–	50	–	dB
Dropout Voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

PMU Total Quiescent Currents in Each Mode

Table 36: PMU Total Quiescent Currents in Each Mode

Specification	Notes	Minimum	Typical	Maximum	Units
Total quiescent current from VBATT	Burst mode[a]	–	100	–	µA
	Low Power Burst mode[a]	–	50	–	µA
	Power-down	–	11	–	µA

a. Assumes that the CBUCK load current = 0uA. Also, PALDO, CLDO, and LNLDOs are powered down.

Section 22: System Power Consumption

WLAN Power Consumption

The WLAN current consumption measurements are shown in Table 37.

Note: Table 37 shows device measurement values.

All values in Table 37 are with the Bluetooth core in reset (that is, Bluetooth and FM are off).

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Table 37: WLAN Power Consumption (Ivbat+Ivio)

	VBATT @ 3.6V, VIO = 1.8V, 25°C	
WLAN	***Typical Total***	***Unit***
OFF[a]	16	µA
Rx (Listen)[b]	68	mA
Rx (Active)[c, d]	82	mA
SLEEP[e]	180	µA
Power Save[f, g]	1.2	mA
Tx 11b (21 dBm @ chip)[h]	345	mA
Tx OFDM, 6 Mbps (20.5 dBm @ chip)[h]	335	mA
Tx OFDM, 54 Mbps (18 dBm @ chip)[h]	310	mA
Tx MCS7 (16 dBm @ chip)[h]	255	mA

a. WL_REG_ON = Low, VIO present or absent.
b. Carrier sense (CCA) when no carrier present.
c. Carrier sense (CS) detect/packet Rx.
d. Applicable to all supported rates.
e. Intra-beacon Sleep.
f. Beacon Interval = 102.4 ms, DTIM = 1, Beacon duration = 1 ms @1 Mbps. Integrated Sleep + wakeup + Beacon Rx current over 1 DTIM interval.
g. In WLAN power save mode, the following blocks are powered down: Crystal oscillator, Baseband PLL, AFE, RF PLL, and the Radio.
The above blocks are turned on in the required order with sufficient time for them to settle. This sequencing is done by the PMU controller that contains the settling time for each of the blocks. It also has information to determine the order in which the blocks should be turned on. The settling times and the dependency order are programmable in the PMU controller. The default CLK settling time is set to 8 ms at power-up. It can be reduced after power-up.
h. Duty cycle is 100%. Includes PA contribution at 3.6V.

Bluetooth and FM Current Consumption

The Bluetooth and FM current consumption measurements are shown in Table 38.

Note: The WLAN core is in reset (WLAN_RST_N = low) for all measurements provided in Table 38.

Note: For FM measurements, the Bluetooth core is in Sleep mode. The current consumption numbers are measured based on the typical output power as specified in Table 21 on page 96.

Table 38: Bluetooth and FM Current Consumption

Operating Mode	*VBATT (VBATT = 3.6V)*	*VDDIO (VDDIO = 1.8V)*	*Units*
Sleep	0.15	0.15	mA
Standard 1.28s Inquiry Scan	0.35	–	mA
3DH5/3DH1 Master	28	–	mA
3DH5/3DH1 Slave	28	–	mA
HV3 + Sniff + Scan[a]	14.5	–	mA
P & I Scan[b]	550	5	µA
500 ms Sniff Master	0.35	–	mA
500 ms Sniff Slave	0.35	–	mA
DM1/DH1 Master	37	–	mA
DM3/DH3 Master	42	–	mA
DM5/DH5 Master	42.5	–	mA
FMRX I^2S Audio	9	–	mA
FMRX Analog Audio	10.5	–	mA
FMTX I^2S Audio	11.5	–	mA
FMTX Analog Audio	13.2	–	mA

a. At maximum class 1 Tx power, 500 ms sniff, four attempts (slave), P = 1.28s, and I = 2.56s.
b. 1.28 s page/inquiry scan interval.

Section 23: Interface Timing and AC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

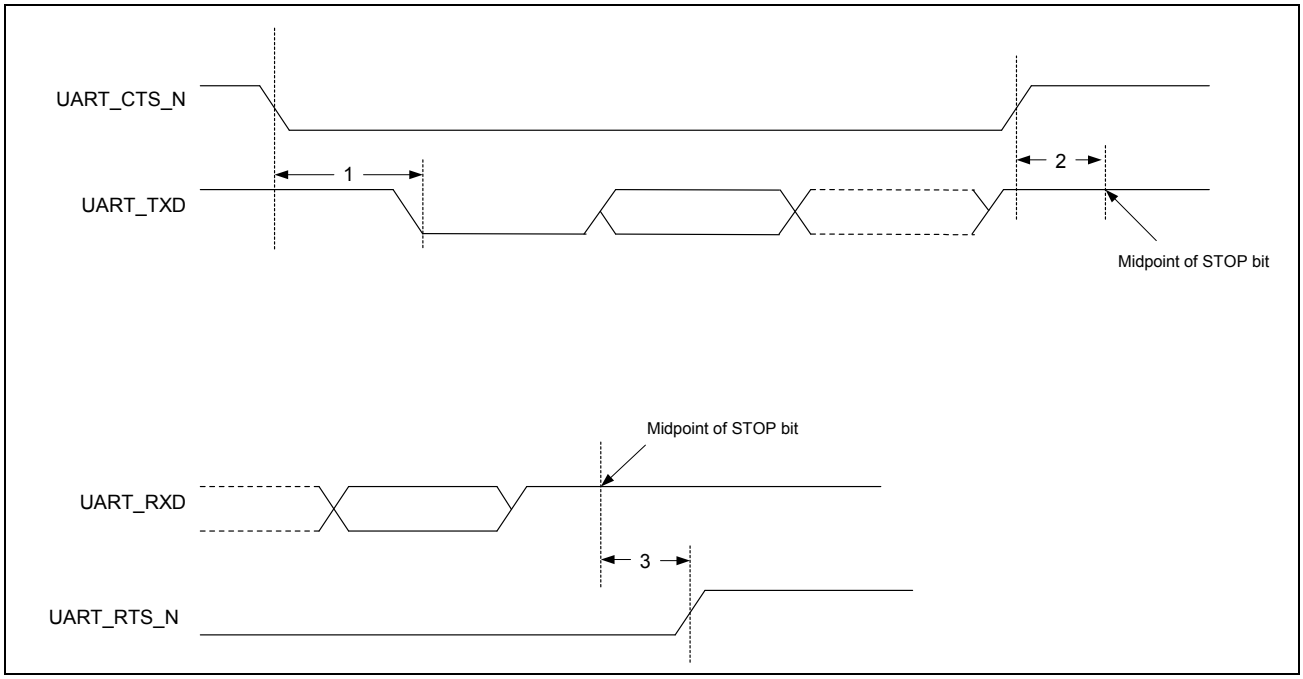
Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 17 on page 90 and Table 19 on page 91. Functional operation outside of these limits is not guaranteed.

Bluetooth Peripheral Transport Unit Timing Specifications

This section describes the Peripheral Transport Unit (PTU) timing. The following conditions apply:

V_{DD} = 3.3V, V_{SS} = 0V, T_A = 0 to 85 °C

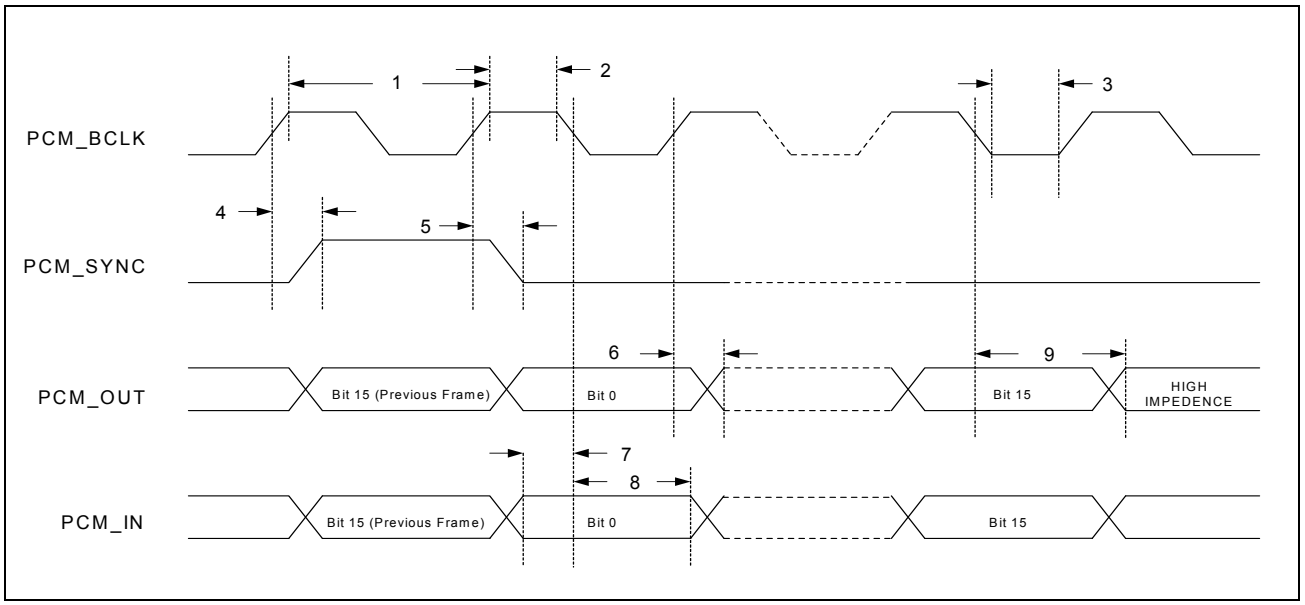
UART Timing



Reference	Description	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to UART_TXD valid	–	–	24	Baudout cycles
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	10	ns
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	2	Baudout cycles

PCM Interface Timing

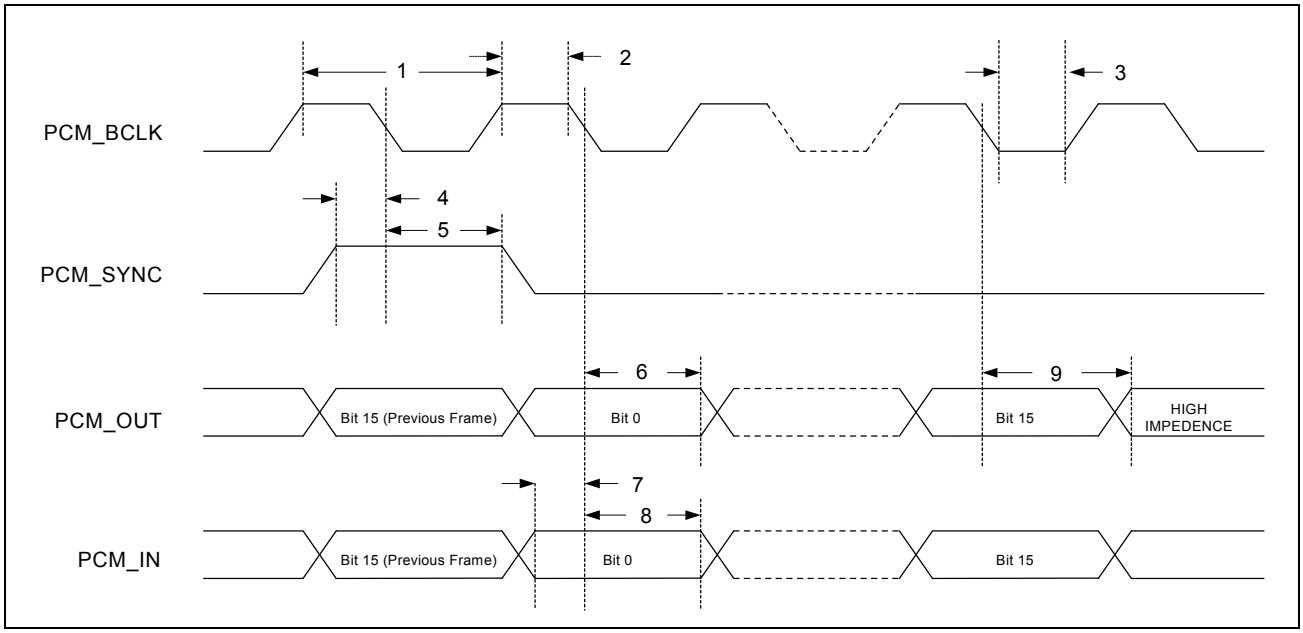
Short Frame Sync, Master Mode



Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	128	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high	–	–	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low	–	–	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	–	–	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns

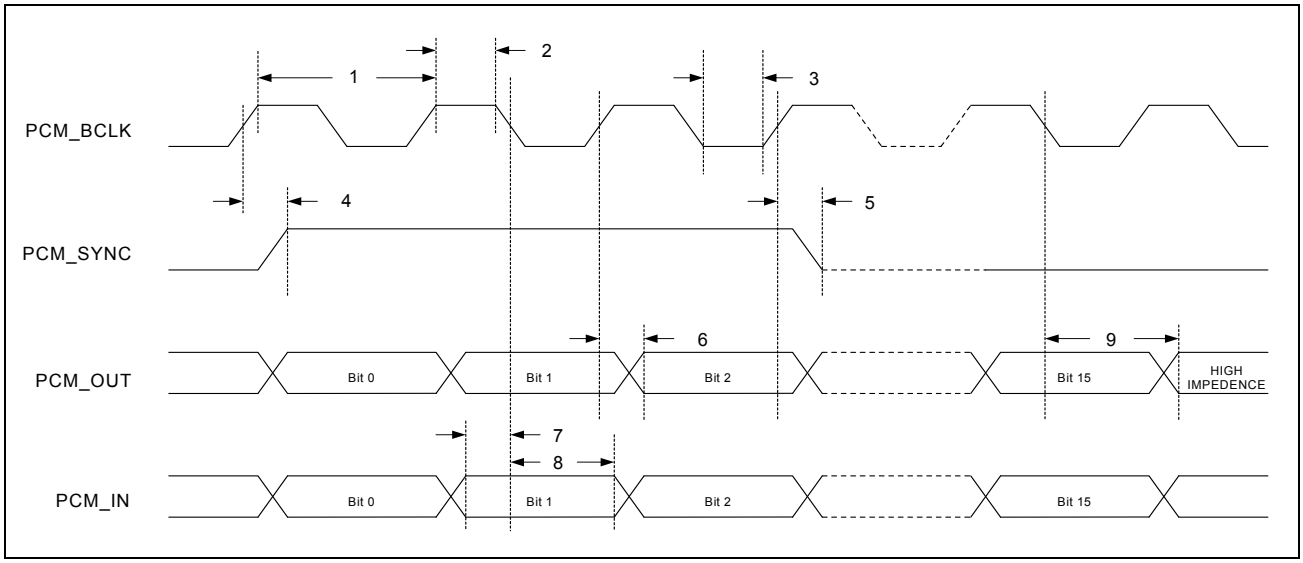
Reference	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	50	ns

Short Frame Sync, Slave Mode



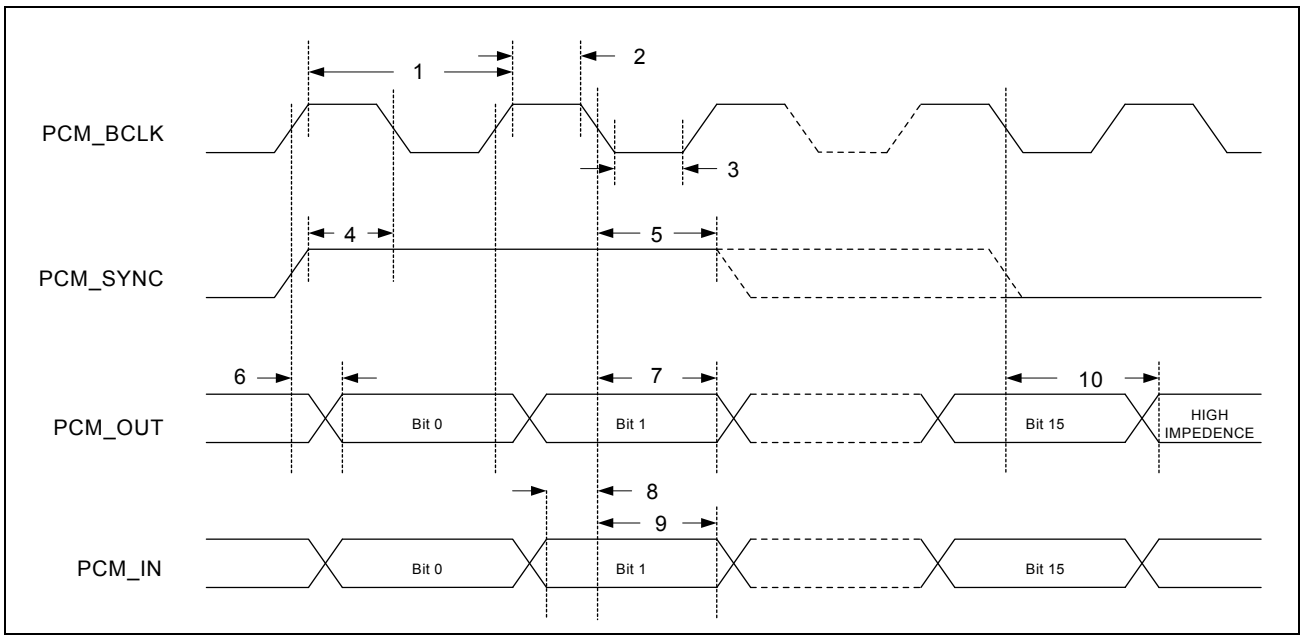
Reference	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_BCLK	50	–	–	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK	10	–	–	ns
6	Hold time of BT_PCM_OUT after BT_PCM_CLK falling edge	–	–	175	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	100	ns

Long Frame Sync, Master Mode



Reference	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high during first bit time	–	–	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low during third bit time	–	–	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	–	–	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	50	ns

Long Frame Sync, Slave Mode

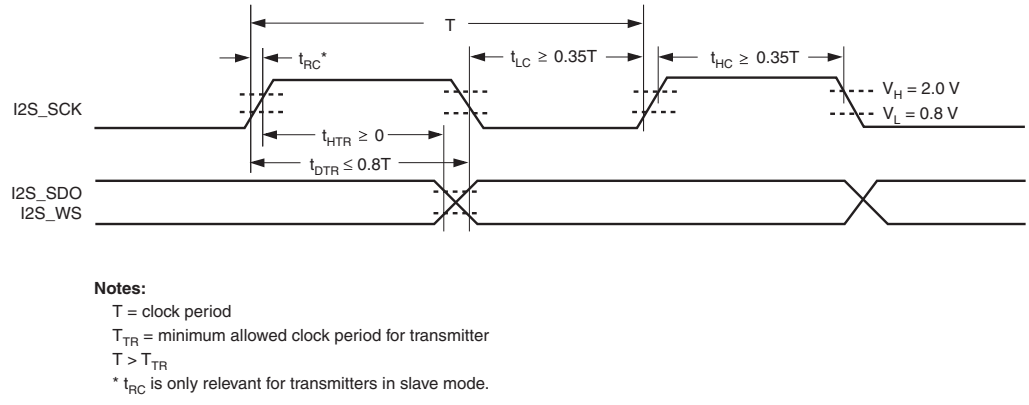


Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_CLK during first bit time	50	–	–	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK during second bit period. (BT_PCM_SYNC may go low any time from second bit period to last bit period)	10	–	–	ns
6	Delay from rising edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) to data valid for first bit on BT_PCM_OUT	–	–	50	ns
7	Hold time of BT_PCM_OUT after BT_PCM_CLK falling edge	–	–	175	ns
8	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
9	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
10	Delay from falling edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) during last bit in slot to BT_PCM_OUT becoming high impedance	–	–	100	ns

FM I²S Timing

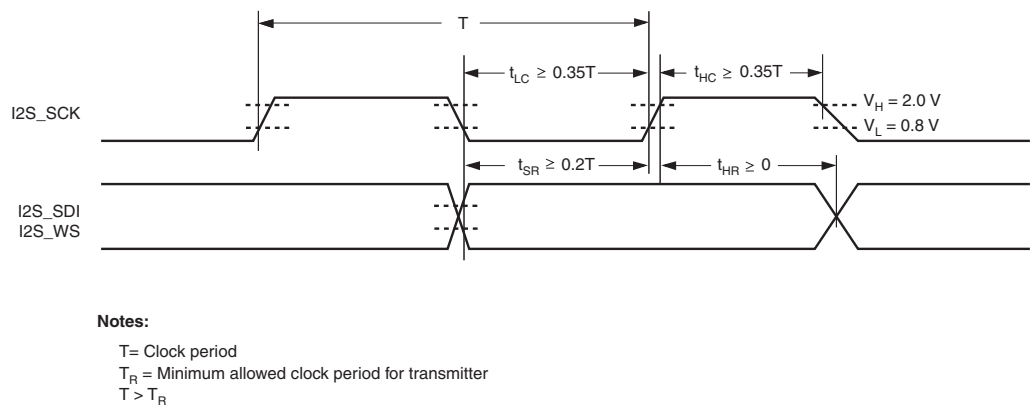
The timing illustrated in Figures 28 and 29 are further described in Table 39 on page 129.

Note: The times given in Figure 28 and Figure 29 are determined by the transmitter speed. The specification of the receiver must be capable of matching the performance of the transmitter.



Notes:
T = clock period
T_{TR} = minimum allowed clock period for transmitter
$T > T_{TR}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 28: I²S Transmitter Timing



Notes:
T= Clock period
T_R = Minimum allowed clock period for transmitter
$T > T_R$

Figure 29: I²S Receiver Timing

Note: The data in Table 39 on page 129 refer to the chip input for Rx and chip output for Tx.

Table 39: Timing for I²S Transmitters and Receivers[a]

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
Clock Period T[b]	T_{TR}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver[c]									
High t_{HC}	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	–	b
Low t_{LC}	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver[d]									
High t_{HC}	–	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	c
Low t_{LC}	–	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	c
Rise-time t_{RC}	–	–	$0.15T_{TR}$	–	–	–		–	d
Transmitter									
Delay t_{DTR}[e]	–	–	–	0.8T	–	–	–	–	e
Hold time t_{HTR}	0	–	–	–	–	–	–	–	d
Receiver[f]									
Set-up time t_{SR}	–	–	–	–	–	$0.2T_R$	–	–	f
Hold time t_{HR}	–	–	–	–	–	0	–	–	f

a. All timing values are specified with respect to high and low threshold levels.
b. The system clock period T must be greater than T_{TR} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
c. The transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason t_{HC} and t_{LC} are specified with respect to T.
d. The transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_R$, any clock that meets the requirements can be used.
e. Because the delay (t_{DTR}) and the maximum transmitter speed (defined by T_{TR}) are related, a fast transmitter driven by a slow clock edge can result in t_{DTR} not exceeding t_{RC} which means t_{HTR} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{HTR} is greater than or equal to zero, provided the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{TR}$. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient set-up time.
f. The data set-up and hold time must not be less than the specified receiver set-up and hold time.

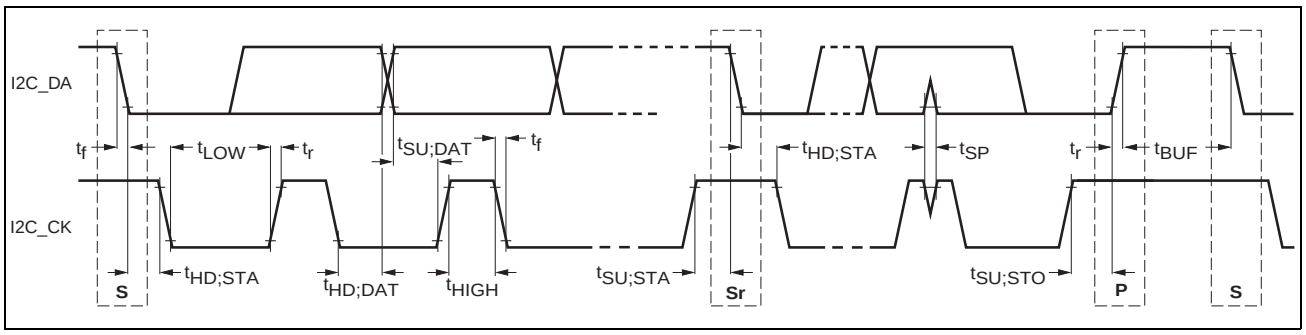
Table 40: Master Transmitter with Data Rate of 2.4 MHz (±10%)

	Minimum	*Typical*	*Maximum*	*Units*	*Condition*
Clock period T	375	417	459	ns	T_{tr} = 375
Clock high t_{HC}	160	–	–	ns	min > 0.35T = 146 (at typical data rate)
Clock low t_{LC}	160	–	–	ns	min > 0.35T = 146 (at typical data rate)
Delay t_{dtr}	–	–	300	ns	max < 0.80T = 334 (at typical data rate)
Hold time t_{htr}	100	–	–	ns	min > 0
Clock rise time t_{RC}	–	–	60	ns	min > 0.15T_{tr} = 56 (only relevant in slave mode)

Table 41: Slave Receiver with Data Rate of 2.4 MHz (±10%)

	Minimum	*Typical*	*Maximum*	*Units*	*Condition*
Clock period T	375	417	459	ns	T_{tr} = 375
Clock high t_{HC}	110	–	–	ns	min < 0.35T = 131
Clock Low t_{LC}	110	–	–	ns	min < 0.35T = 131
Setup time t_{sr}	60	–	–	ns	min < 0.20T = 75
Hold time t_{htr}	0	–	–	ns	min < 0

FM I²C-Compatible Interface Timing



Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*
I2C_CK clock frequency	f_{I2C_CK}	0	400	kHz
Bus-free times between a stop and start condition	t_{BUF}	1.3	–	µs
Hold time (repeated) start condition. After this period, the first clock pulse is generated.	$t_{HD,STA}$	0.6	–	µs
Low period of the I2C_CK clock	t_{LOW}	1.3	–	µs
High period of the I2C_CK clock	t_{HIGH}	0.6	–	µs
Set-up time for a repeater start condition	$t_{SU,STA}$	0.6	–	µs
Data hold time	$t_{HD,DAT}$	0	0.9	µs
Data set-up time	$t_{SU,DAT}$	–	–	µs
Rise time of both I2C_DA and I2C_CK signals	t_r	$20 + 0.1C_b$[a]	300	ns
Fall time of both I2C_DA and I2C_CK signals	t_r	$20 + 0.1C_b$[a]	300	ns
Set-up time for stop condition	$t_{SU,STO}$	0.6	–	µs

a. C_b = Total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

JTAG Timing

Table 42: JTAG Timing Characteristics

Signal Name	*Period*	*Output Maximum*	*Output Minimum*	*Setup*	*Hold*
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

Sequencing of Reset and Regulator Control Signals

The BCM4329 has four signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 30, Figure 31 on page 133, and Figure 32 and Figure 33 on page 134). The timing values indicated are minimum required values; longer delays are also acceptable.

Note: The WL_REG_ON and BT_REG_ON are ORed in the BCM4329. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the BCM4329 regulators.

Also note that the reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.

Note: The BCM4329 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the 0.6V threshold. Wait at least 110 ms after VDDC and VDDIO are available before initiating SDIO accesses. The external reset signals are logically ORed with this POR. So if either the internal POR or one of the external resets are asserted, the device will be in reset.

Description of Control Signals

- **WL_REG_ON**: Used by the PMU (along with BT_REG_ON) to decide whether to power down the internal BCM4329 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be disabled.
- **BT_REG_ON**: Used by the PMU (along with WL_REG_ON) to decide whether to power down the internal BCM4329 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be

disabled.

- **WL_RST_N**: Low Asserting Reset for WLAN Core. This pin must be driven high or low (not left floating). *If WL_RST_N is low (regardless of BT_RST_N state), the WLAN core will be shut down*.
- **BT_RST_N**: Low asserting reset for Bluetooth core. This pin must be driven high or low (not left floating).

Control Signal Timing Diagrams

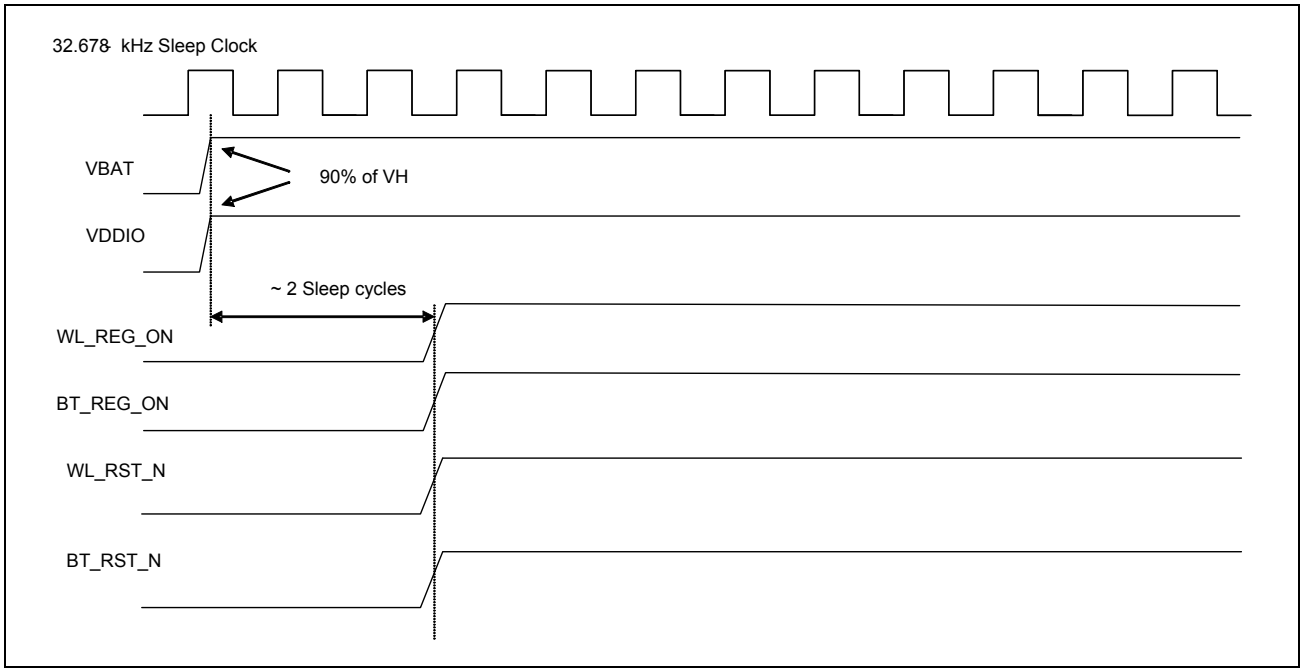


Figure 30: WLAN = ON, Bluetooth = ON

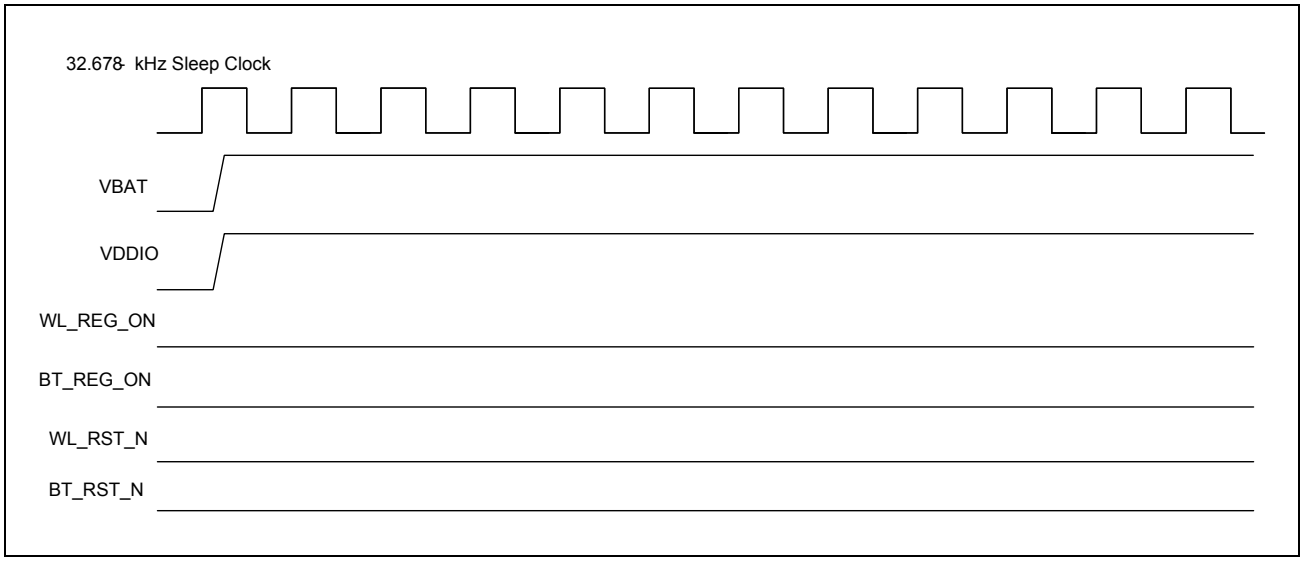


Figure 31: WLAN = OFF, Bluetooth = OFF

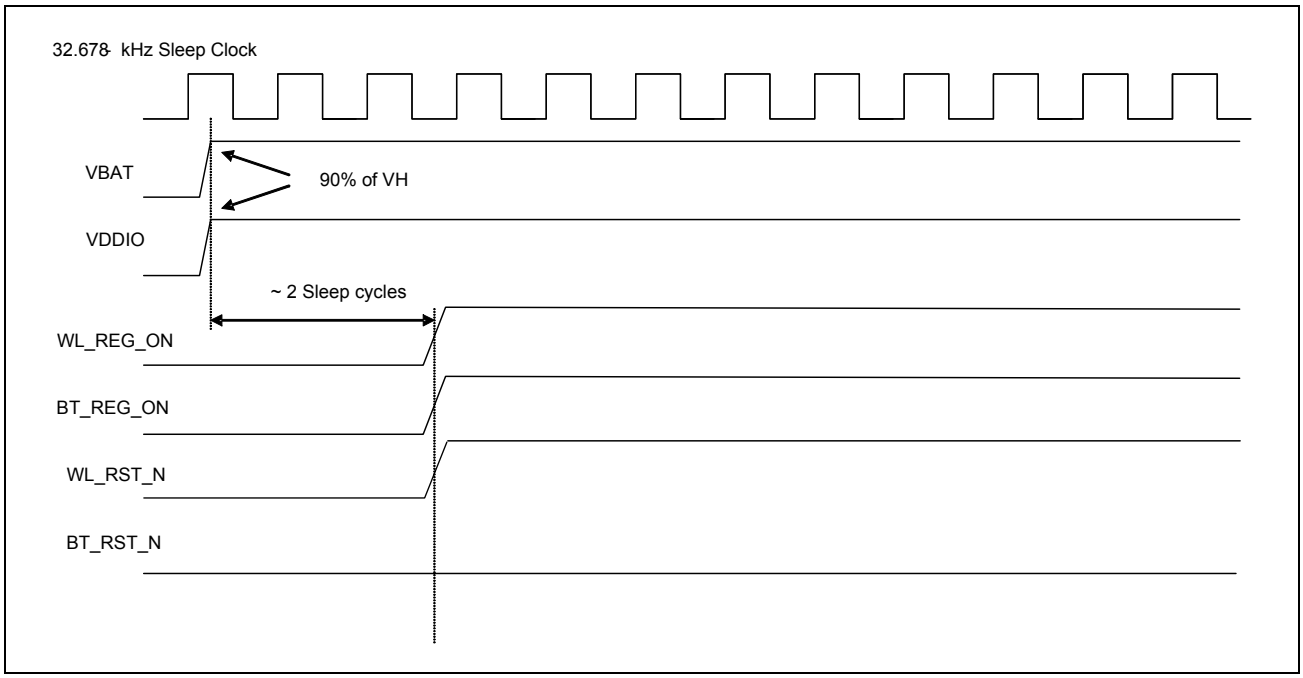


Figure 32: WLAN = ON, Bluetooth = OFF

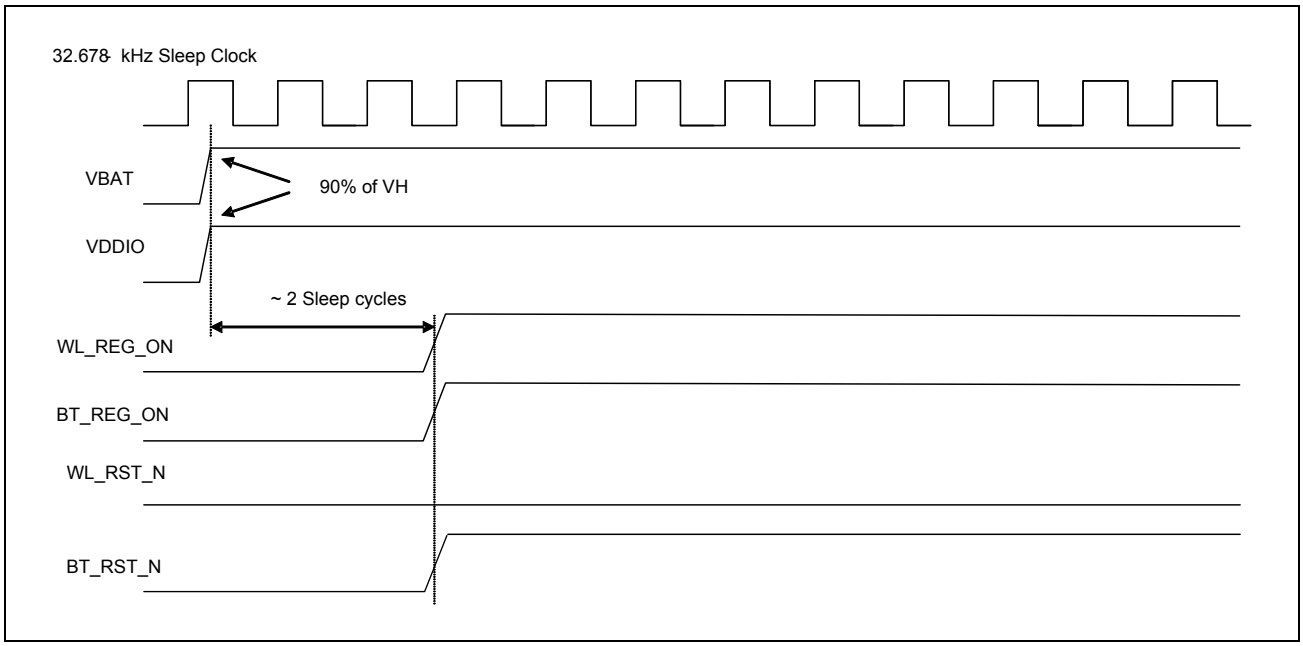


Figure 33: WLAN = OFF, Bluetooth = ON

Section 24: Package Information

Package Thermal Characteristics

Table 43: Package Thermal Characteristics Per JEDEC 51 Standards

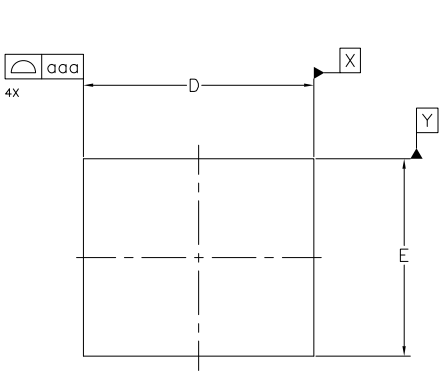
Characteristic	*Value in Still Air*
θ_{JA} (°C/W)	34.85
θ_{JB} (°C/W)	3.52
θ_{JC} (°C/W)	1.83
Ψ_{JT} (°C/W)	5.28
Ψ_{JB} (°C/W)	27.19
Maximum Junction Temperature T_j (°C)	125
Maximum Power Dissipation (W)	1.15

Environmental Ratings

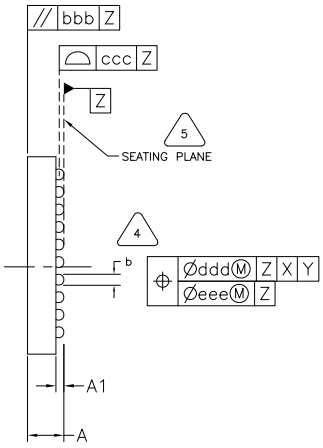
Table 44: Environmental Characteristics

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient Temperature (T_A)	–30 to +85°C	°C	Operation
Storage Temperature	–40 to +105°C	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

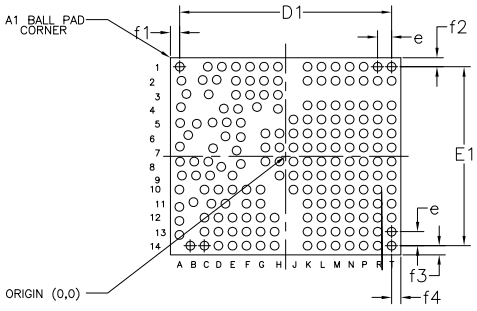
Section 25: Mechanical Information



TOP VIEW



SIDE VIEW



BOTTOM VIEW
(182 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	6.52	6.57	6.62
D1		6.04 REF.	
E	5.57	5.62	5.67
E1		5.10 REF.	
b	0.200	0.250	0.300
e		0.40 BSC	
f1		0.26 BSC	
f2		0.26 BSC	
f3		0.26 BSC	
f4		0.26 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-033-1211-001

6. ARRAY CENTER H7–H8–J8–J7 IS PKG ORIGIN PLUS(+25,+50).

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.03
ANGULAR: ±1°
DO NOT SCALE DRAWING
PROJECTION

Figure 34: 182-Ball WLBGA Mechanical Information (5.62 mm x 6.57 mm, 0.4 mm Pitch)

Section 26: Ordering Information

Part Number	*Package*[a]
BCM4329GKUBG	Single Band 2.4 GHz WLAN, Bluetooth 2.1 + EDR
BCM4329EKUBG	Single Band 2.4 GHz WLAN + Bluetooth 2.1 + EDR + FM (Tx + Rx)
BCM4329HKUBG	Dual Band 2.4 GHz and 5.0 GHz WLAN + Bluetooth 2.1 + EDR + FM (Tx + Rx)

a. All packages are 182-ball flip-chip WLBGA.

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