CY7C188

32 K × 9 Static RAM

Features

- High speed
  - 20 ns
- Automatic power-down when deselected
- Low active power
  - 935 mW
- Low standby power
  - 83 mW
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Available in non Pb-free 32-Lead (300-Mil) Molded SOJ

Functional Description

The CY7C188 is a high-performance CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is provided by an active-LOW chip enable ($\overline{CE}_1$), an active-HIGH chip enable (CE_2), an active-LOW output enable ($\overline{OE}$), and tri-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

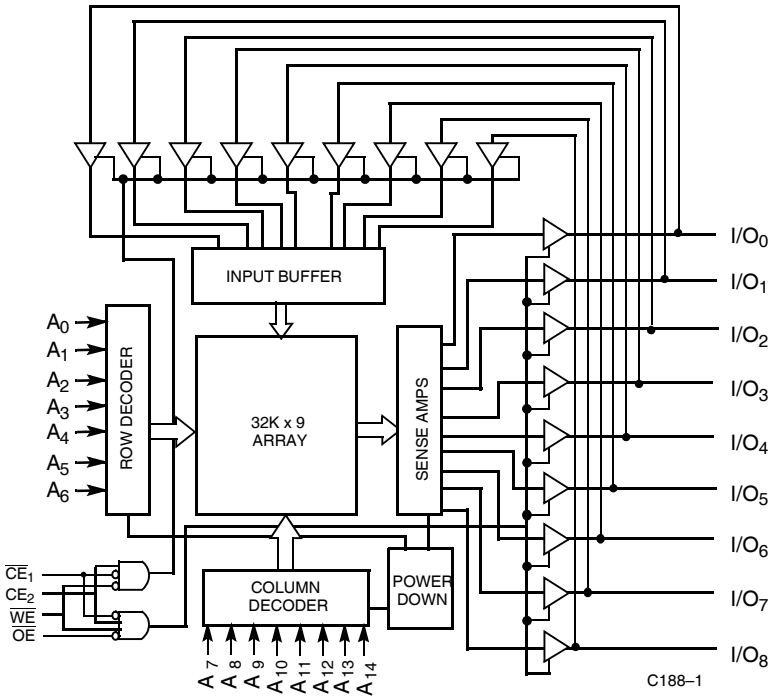
Writing to the device is accomplished by taking $\overline{CE}_1$ and write enable ($\overline{WE}$) inputs LOW and CE_2 input HIGH. Data on the nine I/O pins (I/O_0 – I/O_8) is then written into the location specified on the address pins (A_0 – A_{14}).

Reading from the device is accomplished by taking $\overline{CE}_1$ and $\overline{OE}$ LOW while forcing $\overline{WE}$ and CE_2 HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins (I/O_0 – I/O_8) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

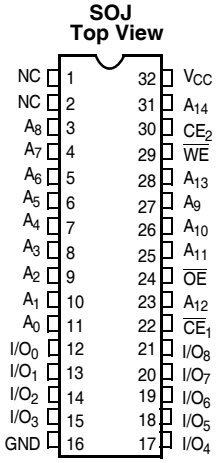
The CY7C188 is available in standard 300-mil-wide SOJ.

Logic Block Diagram



Contents

Pin Configuration



Selection Guide

Description	–20
Maximum Access Time (ns)	20
Maximum Operating Current (mA)	170
Maximum CMOS Standby Current (mA)	15

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND (Pin 32 to Pin 16)..... –0.5 V to +7.0 V

DC Voltage Applied to Outputs in high Z State[1] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage[1] ..... –0.5 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range[2]

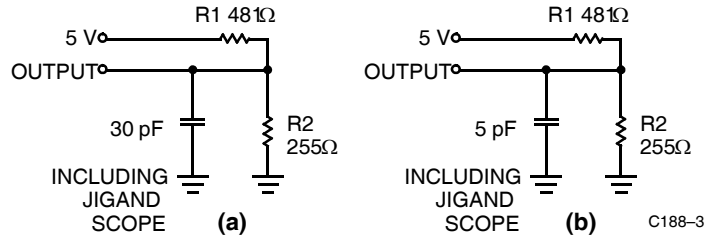
Parameter	Description	Test Conditions	–20		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	170	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max V_{CC}, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	–	35	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE}_1 \geq V_{CC}$ –0.3 V or $CE_2 \leq 0.3$ V, $V_{IN} \geq V_{CC}$ – 0.3 V or $V_{IN} \leq 0.3$ V, f = 0	–	15	mA

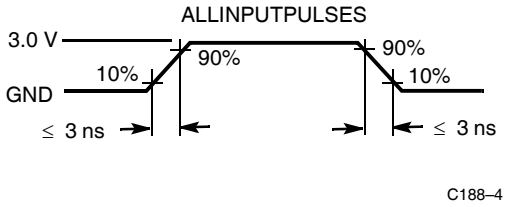
Capacitance[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	6	pF
C_{IN}: Controls	Input Capacitance		8	pF
C_{OUT}	Output Capacitance		8	pF

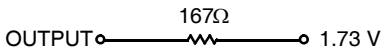
Notes
1. Minimum voltage is equal to –2.0 V for pulse durations less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4, 5]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics

Over the Operating Range[4, 6]

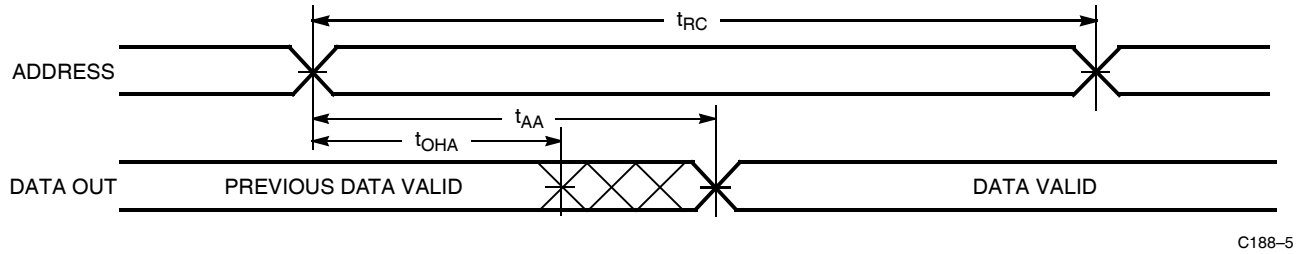
Parameter	Description	–20		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	20	–	ns
t_{AA}	Address to Data Valid	–	20	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Data Valid	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 7]	–	9	ns
t_{LZCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to low Z[7]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to high Z[5, 7]	–	9	ns
t_{PU}	$\overline{CE}_1$ LOW or CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to power-down	–	20	ns
WRITE CYCLE[8, 9]				
t_{WC}	Write Cycle Time	20	–	ns
t_{SCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Write End	15	–	ns
t_{AW}	Address set-up to Write End	15	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address set-up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	15	–	ns
t_{SD}	Data Set-Up to Write End	10	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[5]	0	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[5, 7]	3	–	ns

Notes

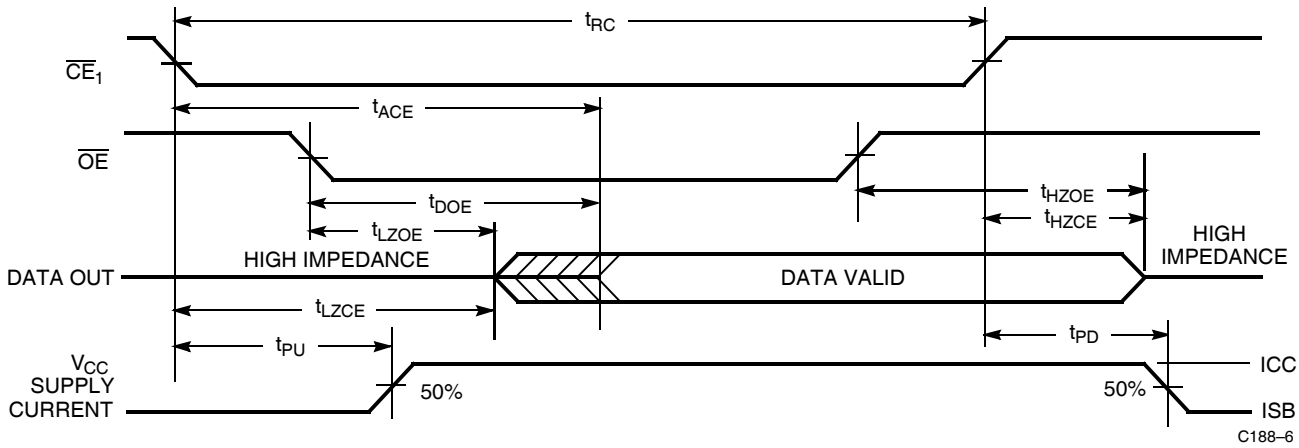
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. See the last page of this specification for Group A subgroup testing information.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$, LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

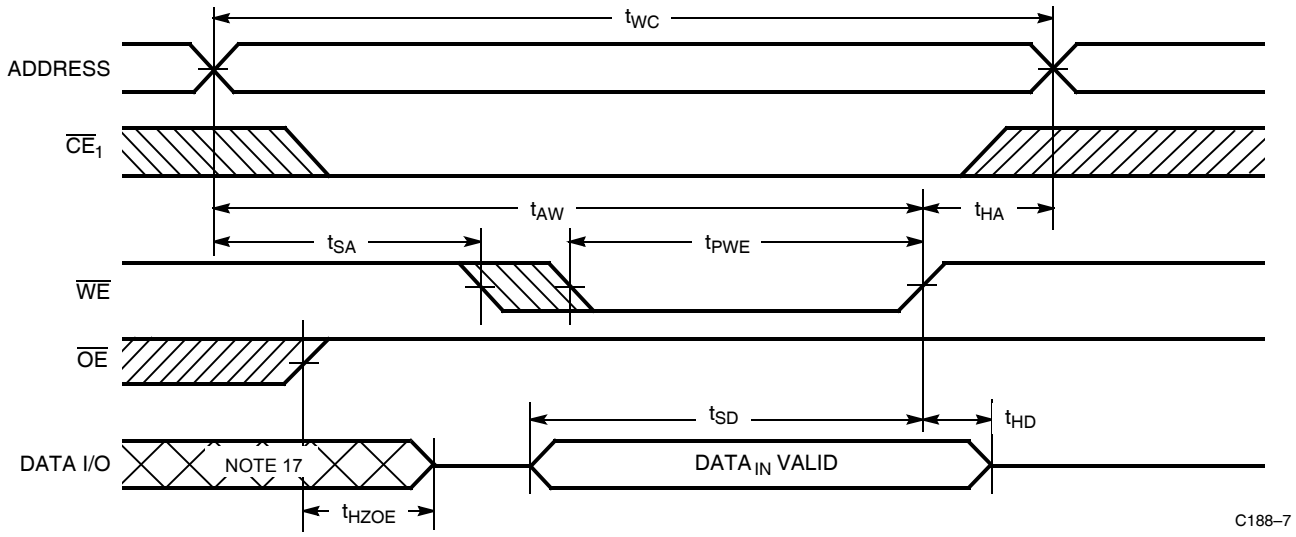
Read Cycle No. 1[10, 11]



Read Cycle No. 2 (Chip-Enable Controlled)[11, 12, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[13, 14, 15, 16]

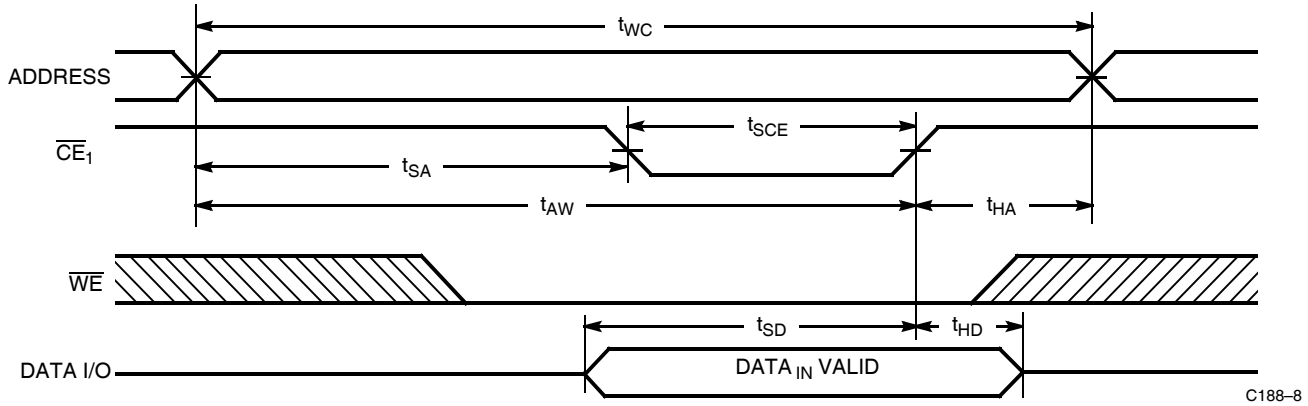


Notes

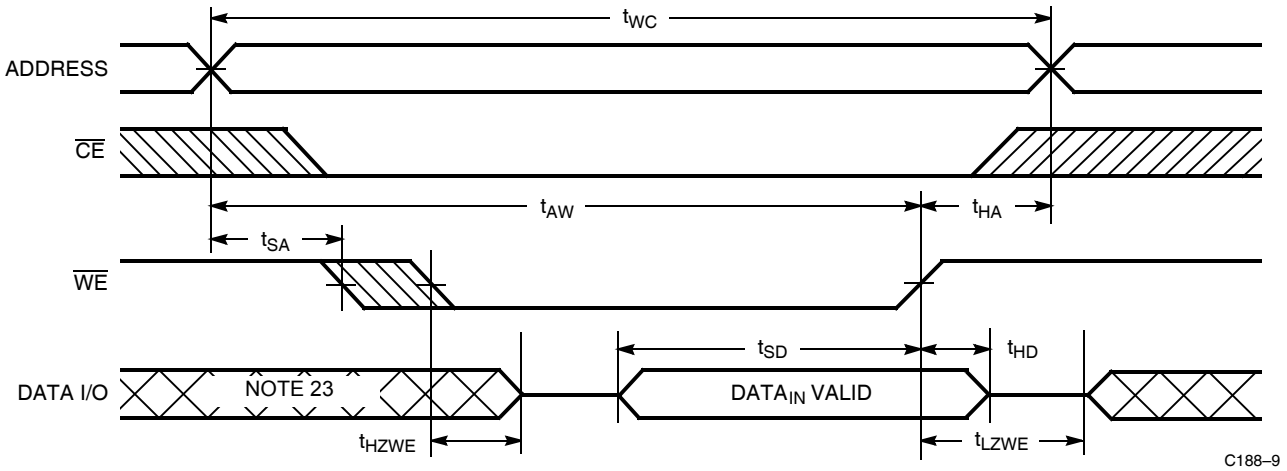
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Timing parameters are the same for all chip enable signals ($\overline{CE_1}$ and CE_2), so only the timing for $\overline{CE_1}$ is shown.
14. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$, LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (Continued)

Write Cycle No.2 ($\overline{CE}$ Controlled)[18, 20, 21, 22]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[19, 20, 22]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Notes

18. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$, LOW, CE_2 HIGH, and $\overline{WE}$ LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
19. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
20. Timing parameters are the same for all chip enable signals ($\overline{CE}_1$ and CE_2), so only the timing for $\overline{CE}_1$ is shown.
21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
23. During this period, the I/Os are in the output state and input signals should not be applied.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C188–20VC	51-85041	32-pin (300-Mil) Molded SOJ	Commercial

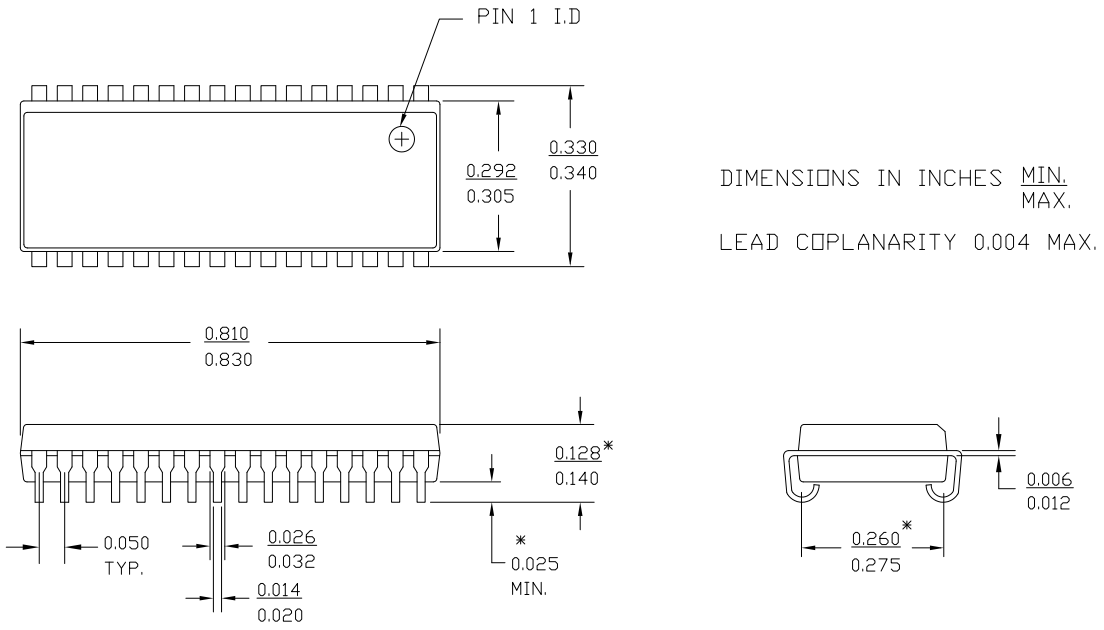
Ordering Code Definitions

CY 7C 188 - 20 V C

- C = Temperature range (Commercial)
- V = 32-pin (300-Mil) Molded SOJ
- 20 = Speed grade
- Part Identifier
- Family: 7C = Fast asynchronous SRAM
- Company ID: CY = Cypress

Package Diagram

Figure 1. 32-Lead (300-Mil) Molded SOJ, 51-85041



51-85041 *B

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
DIP	dual inline package
I/O	input/output
OE	output enable
SRAM	static random access memory
SOJ	small outline J-lead
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent
MHz	Mega Hertz

Document History Page

Document Title: CY7C188 32 K × 9 Static RAM Document Number: 38-05053				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107155	09/10/01	SZV	Change from Spec number: 38-00220 to 38-05053
*A	506367	See ECN	NXR	Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information table
*B	2894123	03/17/2010	VKN	Added Table of Contents Removed 15ns speed bin Updated Ordering Information table Updated Package Diagram (Figure 1) Added Sales, Solutions, and Legal Information
*C	3096933	11/30/2010	PRAS	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits.

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