CY7C168A

4 K × 4 RAM

Features

- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- High speed
  - t_{AA} = 20 ns
- Low active power
  - 495 mW
- Low standby power
  - 110 mW
- TTL-compatible inputs and outputs
- V_{IH} of 2.2 V
- Capable of withstanding greater than 2001 V electrostatic discharge

Functional Description

The CY7C168A is a high-performance CMOS static RAM organized as 4096 by 4-bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

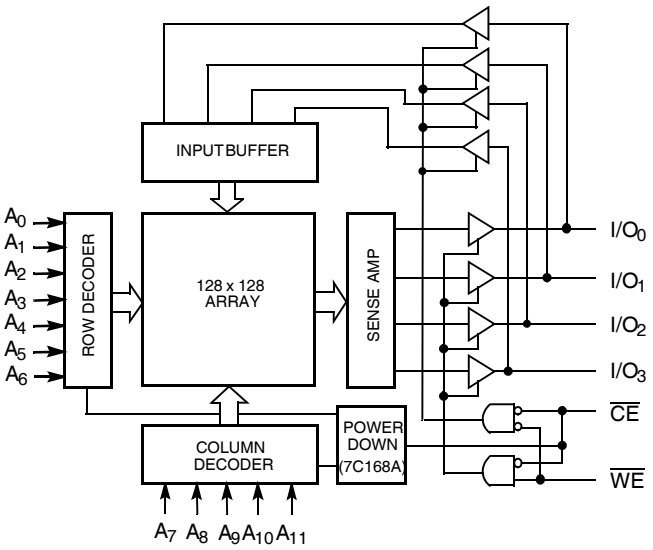
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram

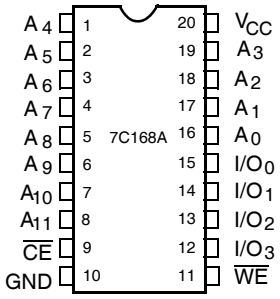


C168A-1

Contents

Pin Configuration

Figure 1. DIP Top View



C168A-2

Selection Guide

		7C168A-20
Maximum access time (ns)		20
Maximum operating current (mA)	Commercial	90
	Military	100

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied..... –55 °C to +125 °C

Supply voltage to ground potential (pin 20 to pin 10)..... –0.5 V to +7.0 V

DC voltage applied to outputs in high Z state..... –0.5 V to +7.0 V

DC input voltage ..... –3.0 V to +7.0 V

Output current into outputs (low) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

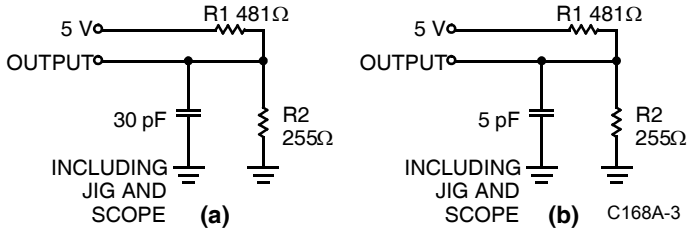
Parameter	Description	Test Conditions	7C168A-20		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.2	V_{CC}	V
V_{IL}	Input LOW voltage[1]		–0.5	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled	–10	+10	µA
I_{OS}	Output short circuit current[2]	V_{CC} = Max, V_{OUT} = GND	–	–350	mA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA	–	90	mA
I_{SB1}	Automatic $\overline{CE}$ power-down current	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}	–	40	mA
I_{SB2}	Automatic $\overline{CE}$ power-down current	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V	–	20	mA

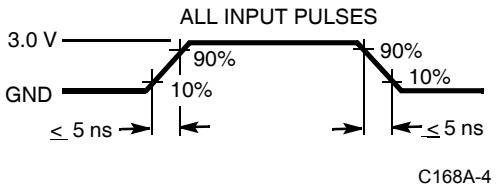
Notes
1. V_{IL} min = –3.0 V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance[3]

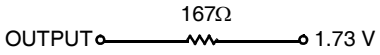
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Note
3. Tested initially and after any design or process changes that may affect these parameters.

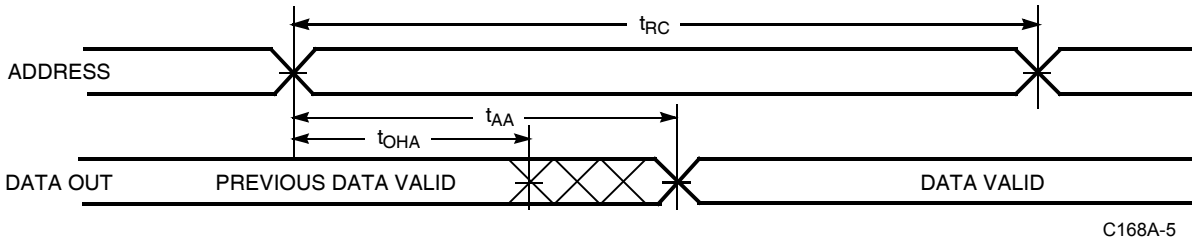
Switching Characteristics

Over the Operating Range[4]

Parameter	Description	7C168A-20		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read cycle time	20	–	ns
t_{AA}	Address to data valid	–	20	ns
t_{OHA}	Output hold from address change	5	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[5]	5	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[5, 6]	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	20	ns
t_{RCS}	Read command set-up	0	–	ns
t_{RCH}	Read command hold	0	–	ns
WRITE CYCLE[7]				
t_{WC}	Write cycle time	20	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	15	–	ns
t_{AW}	Address set-up to write end	15	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	15	–	ns
t_{SD}	Data set-up to write end	10	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[5]	7	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[5, 6]	5	–	ns

Switching Waveforms

Figure 2. Read Cycle No.1 [8, 9]



Notes

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
6. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE}$ = V_{IL}.

Switching Waveforms *(continued)*

Figure 3. Read Cycle[10, 11]

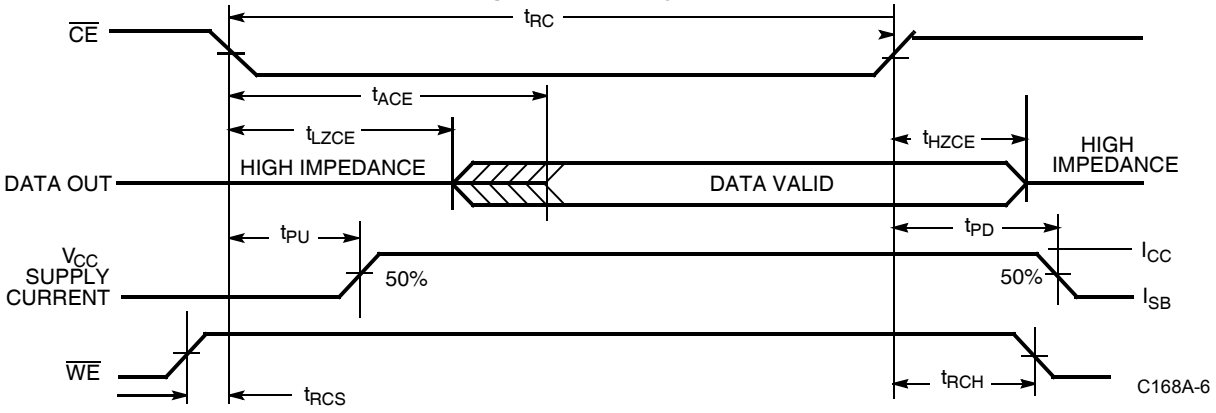


Figure 4. Write Cycle No.1 ($\overline{WE}$ Controlled)[12]

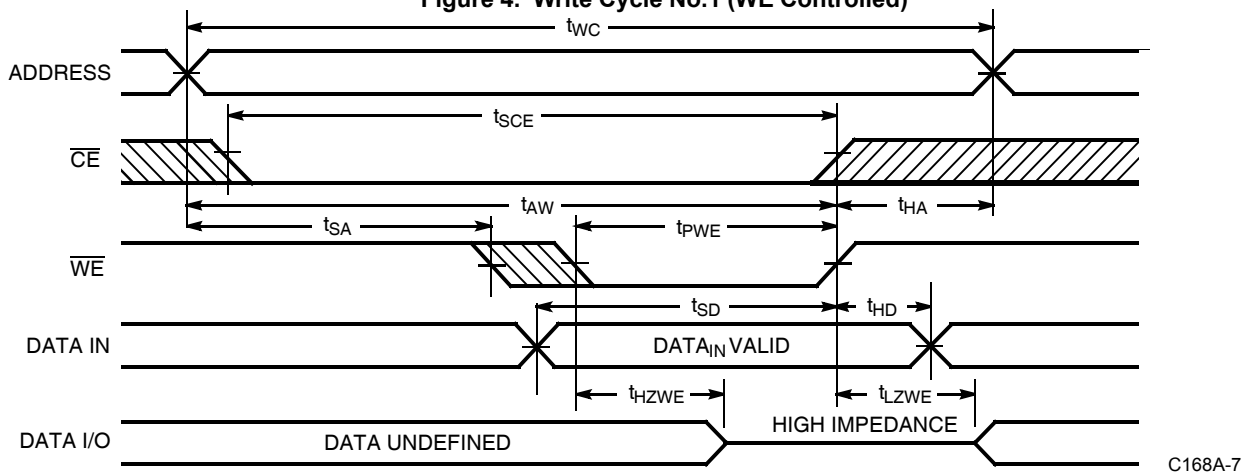
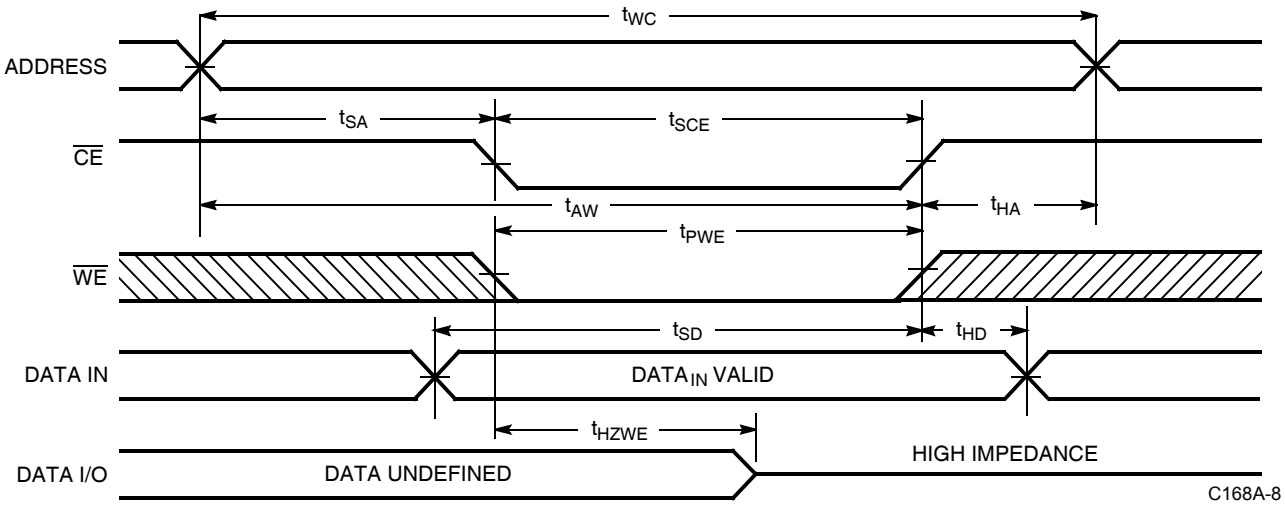


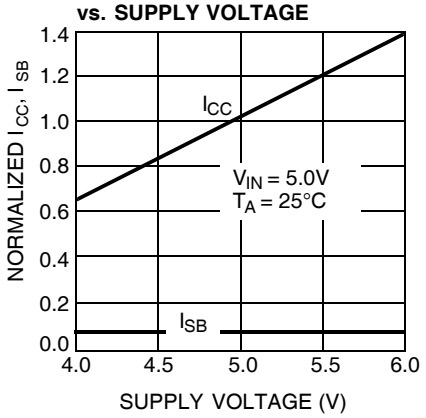
Figure 5. Write Cycle No. 2 ($\overline{CS}$ Controlled)[12, 13]



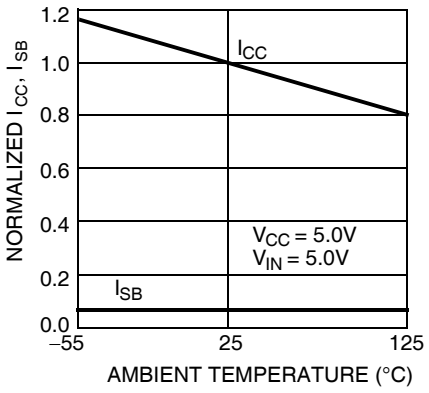
Notes
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

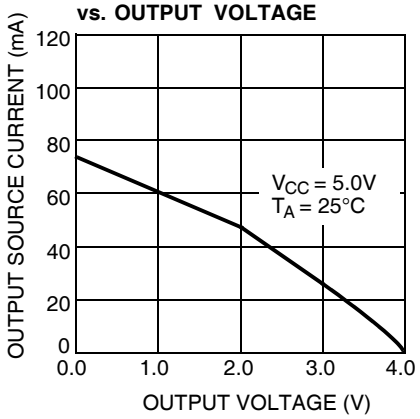
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



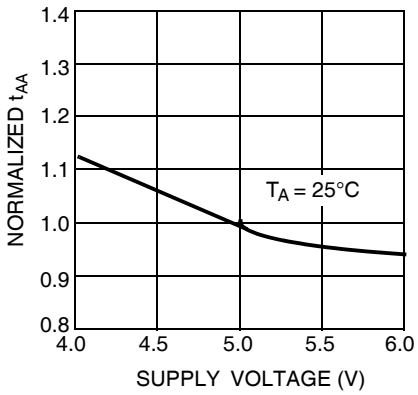
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



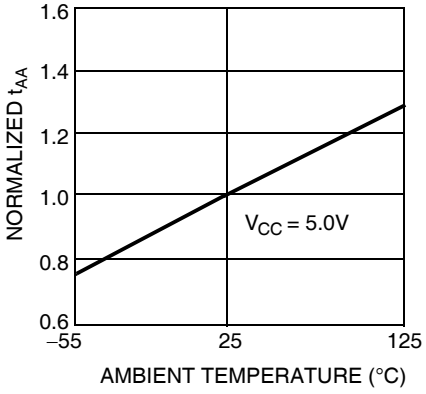
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



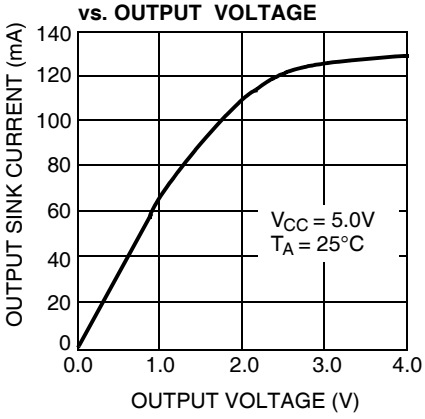
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



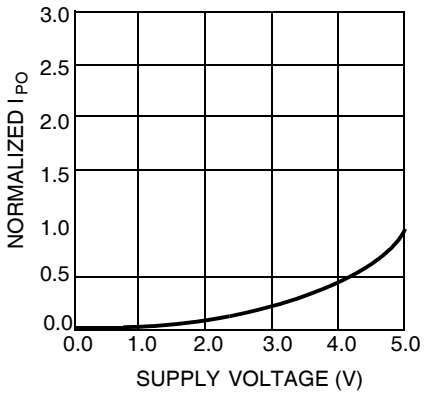
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



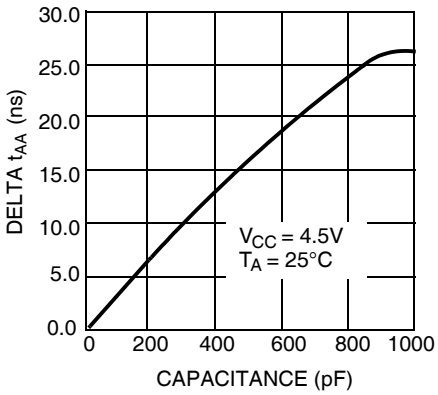
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



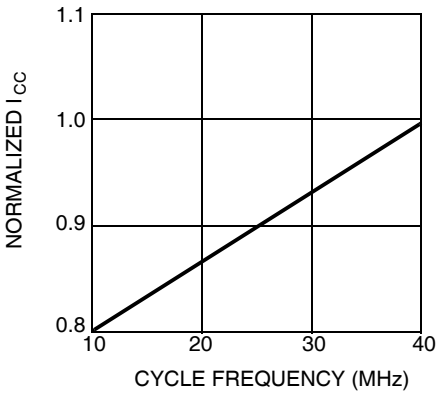
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs.CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C168A-20PXC	P5	20-Lead Molded DIP	Commercial

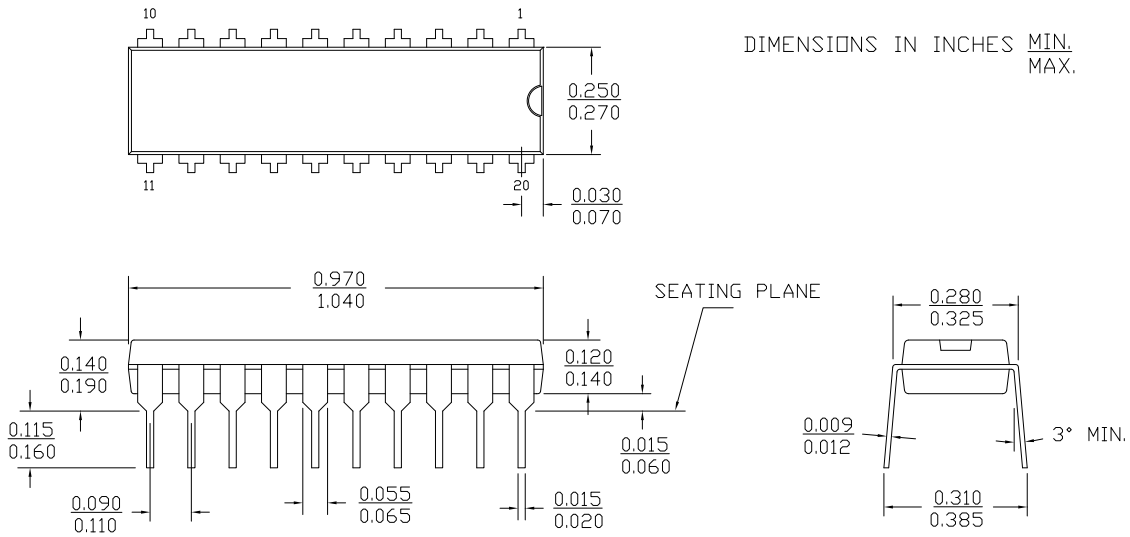
Ordering Code Definitions

CY 7C 168A - 20 PX C

- C = Temperature range (Commercial)
- PX = 20-lead molded DIP (Pb-free)
- 20 = Speed grade
- 168A = 4 K × 4 architecture
- Family: 7C = Fast asynchronous SRAM
- Company ID: CY = Cypress

Package Diagram

Figure 6. 20-Lead (300-Mil) Molded DIP P5



51-85011 *B

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
DIP	dual inline package
I/O	input/output
SRAM	static random access memory
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History Page

Document Title: CY7C168A 4 K × 4 RAM Document Number: 38-05029				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106815	09/10/01	SZV	Change from Spec number: 38-00095 to 38-05029
*A	3008799	08/19/2010	AJU	Updated t_{AA} to 20 ns under High Speed, 495 mW under Low active power in Features section Updated Figure caption to DIP Top View in Pin Configuration section Updated Selection Guide section with only 7C168A-20 values Updated Operating Range section with only Commercial temperature range Updated Electrical Characteristics section with only 7C168A-20 values Updated Switching Characteristics section with only 7C168A-20 values Updated Ordering Information section with only CY7C168A-20PXC Ordering Code Updated Package Diagram with only the latest revision of “20-Lead (300-Mil) Molded DIP P5” (Figure 6 in page 8) Minor edits and updated in new template
*B	3090588	11/19/2010	AJU	Post to external web.
*C	3097955	11/30/2010	PRAS	No technical updates. Sunset review.

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