CY7C1546V18
CY7C1557V18
CY7C1548V18
CY7C1550V18

72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)

Features

- 72-Mbit density (8M x 8, 8M x 9, 4M x 18, 2M x 36)
- 300 MHz to 375 MHz clock for high bandwidth
- 2-Word burst for reducing address bus frequency
- Double Data Rate (DDR) interfaces (data transferred at 750 MHz) at 375 MHz
- Read latency of 2.0 clock cycles
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- Core V_{DD} = 1.8V ± 0.1V; IO V_{DDQ} = 1.4V to V_{DD}[1]
- HSTL inputs and Variable drive HSTL output buffers
- Available in 165-Ball FBGA package (15 x 17 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- Delay Lock Loop (DLL) for accurate data placement

Configurations

With Read Cycle Latency of 2.0 cycles:

CY7C1546V18 – 8M x 8

CY7C1557V18 – 8M x 9

CY7C1548V18 – 4M x 18

CY7C1550V18 – 2M x 36

Functional Description

The CY7C1546V18, CY7C1557V18, CY7C1548V18, and CY7C1550V18 are 1.8V Synchronous Pipelined SRAM equipped with DDR-II+ architecture. The DDR-II+ consists of an SRAM core with advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of both K and $\overline{K}$. Each address location is associated with two 8-bit words (CY7C1546V18), 9-bit words (CY7C1557V18), 18-bit words (CY7C1548V18), or 36-bit words (CY7C1550V18) that burst sequentially into or out of the device.

Asynchronous inputs include output impedance matching input (ZQ). Synchronous data outputs (Q, that share the same physical pins with the data inputs, D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need to capture data separately from individual DDR SRAMs in the system design.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

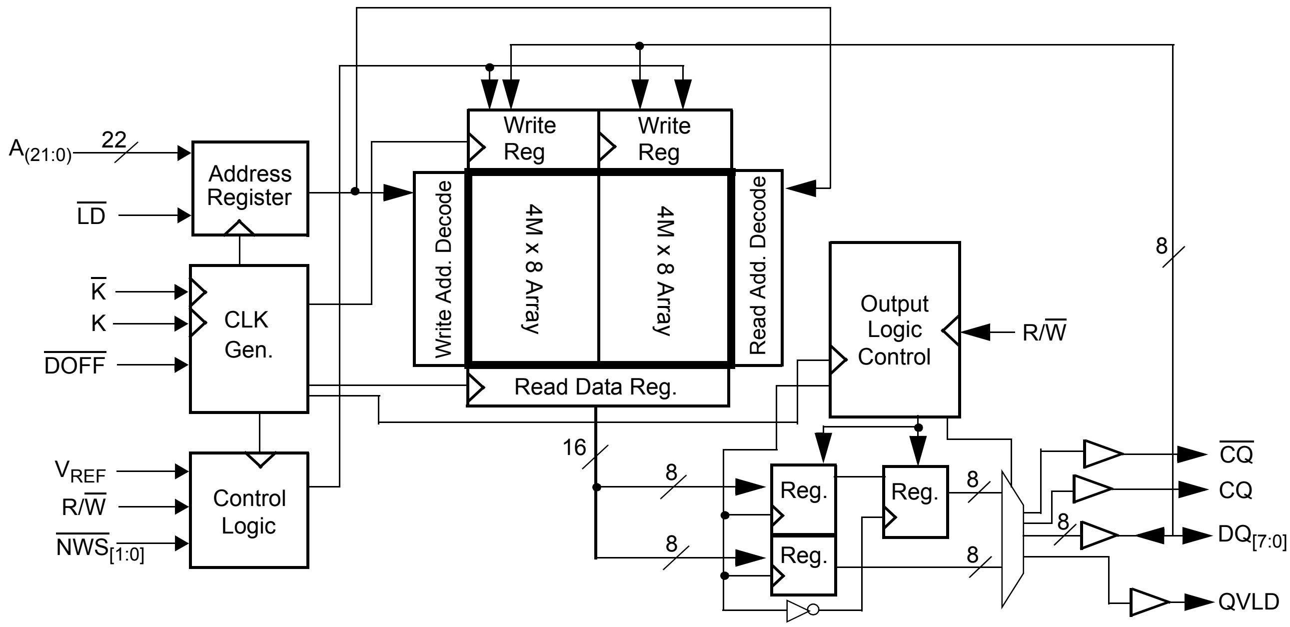
Selection Guide

		375 MHz	333 MHz	300 MHz	Unit
Maximum Operating Frequency		375	333	300	MHz
Maximum Operating Current	x8	1300	1200	1100	mA
	x9	1300	1200	1100	
	x18	1300	1200	1100	
	x36	1300	1200	1100	

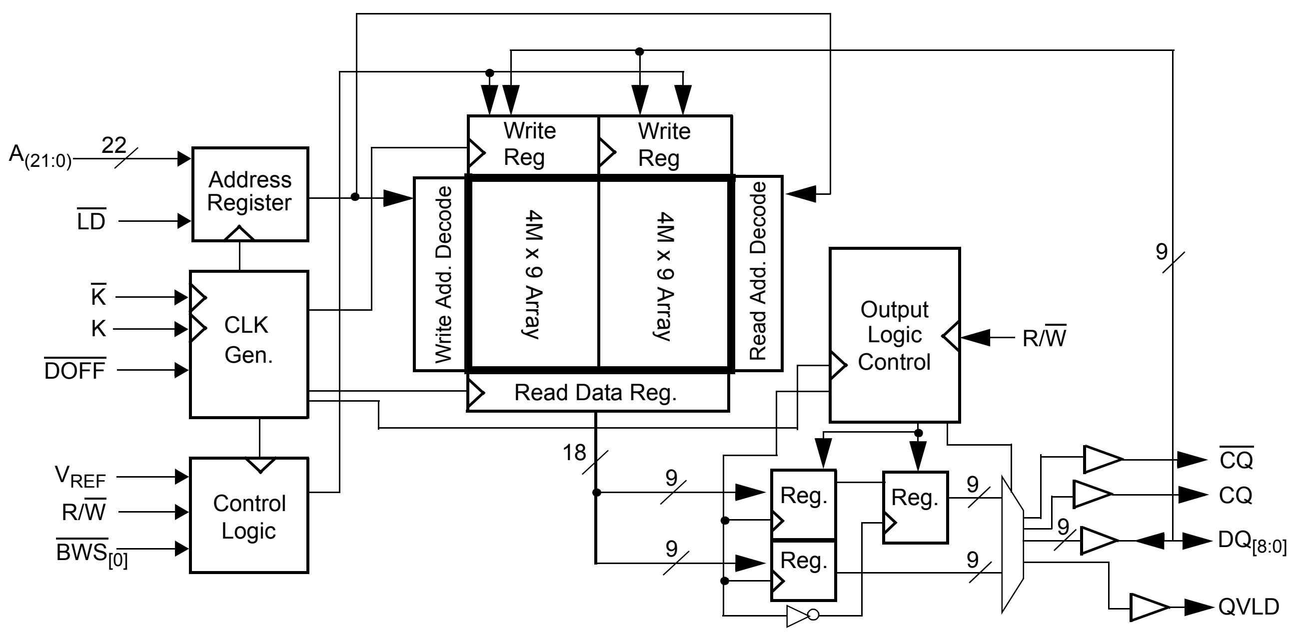
Note

1. The QDR consortium specification for V_{DDQ} is 1.5V ± 0.1V. The Cypress QDR devices exceed the QDR consortium specification and are capable of supporting V_{DDQ} = 1.4V to V_{DD}.

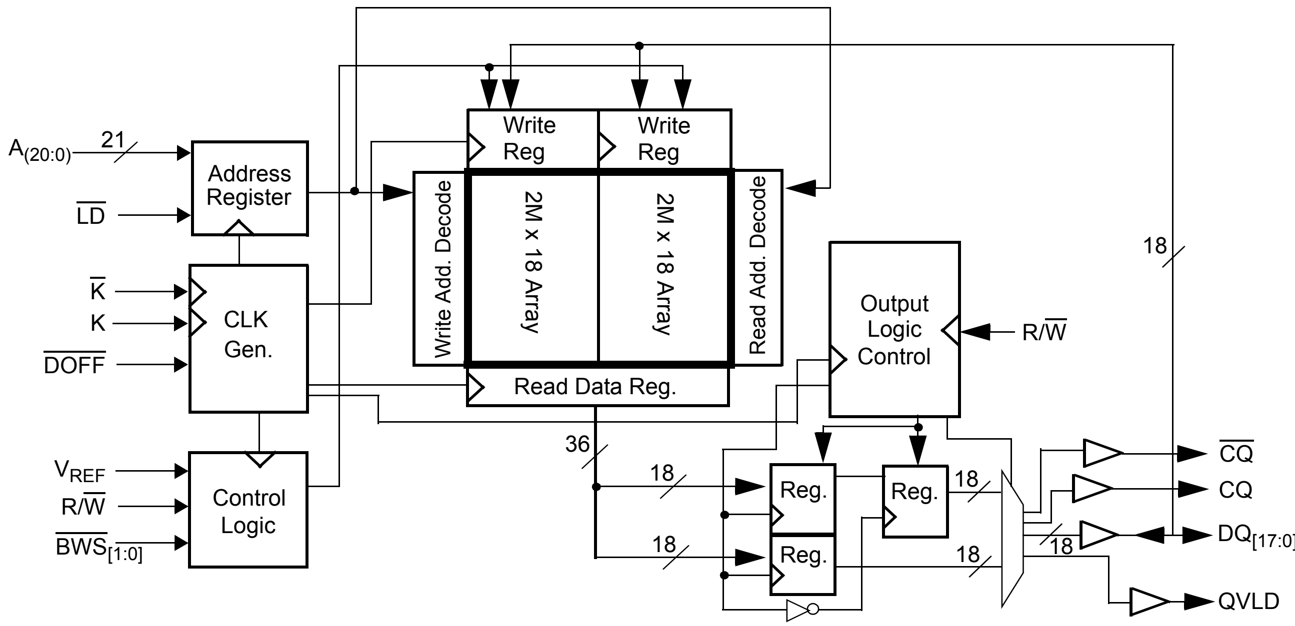
Logic Block Diagram (CY7C1546V18)



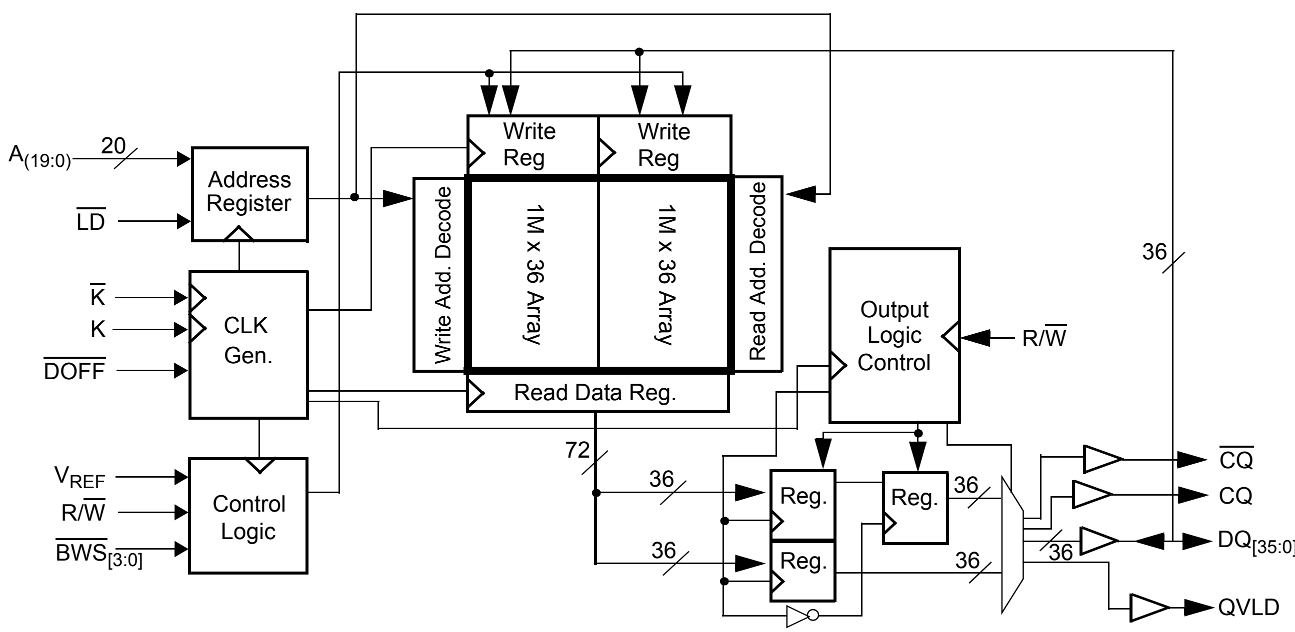
Logic Block Diagram (CY7C1557V18)



Logic Block Diagram (CY7C1548V18)



Logic Block Diagram (CY7C1550V18)



Pin Configuration

The Pin Configuration for CY7C1546V18, CY7C1557V18, CY7C1548V18, and CY7C1550V18 follows.[2]

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1546V18 (8M x 8)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	$R/\overline{W}$	$\overline{NWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	C	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

CY7C1557V18 (8M x 9)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	$R/\overline{W}$	NC	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	A	A	QVLD	A	A	NC	NC	DQ8
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Note
2. NC/144M and NC/288M are not connected to the die and can be tied to any voltage level.

Pin Configuration

The Pin Configuration for CY7C1546V18, CY7C1557V18, CY7C1548V18, and CY7C1550V18 follows.[2] (continued)

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1548V18 (4M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	A	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C1550V18 (2M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	R/$\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	A	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	NC	A	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	QVLD	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Pin Definitions

Pin Name	IO	Pin Description
$DQ_{[x:0]}$	Input and Output Synchronous	**Data Input or Output Signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the K and $\overline{K}$ clocks during read operations. When read access is deselected, $Q_{[x:0]}$ are automatically tri-stated. CY7C1546V18 − $DQ_{[7:0]}$ CY7C1557V18 − $DQ_{[8:0]}$ CY7C1548V18 − $DQ_{[17:0]}$ CY7C1550V18 − $DQ_{[35:0]}$
$\overline{LD}$	Input Synchronous	**Synchronous Load**. Sampled on the rising edge of the K clock. This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read or write direction. All transactions operate on a burst of 2 data. $\overline{LD}$ must meet the setup and hold times around edge of K.
$\overline{NWS_0}$, $\overline{NWS_1}$	Input Synchronous	**Nibble Write Select 0, 1, Active LOW (CY7C1546V18 only)**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select the nibble that is written into the device during the current portion of the write operations. Nibbles not written remain unaltered. $\overline{NWS_0}$ controls $D_{[3:0]}$ and $\overline{NWS_1}$ controls $D_{[7:4]}$. All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select ignores the corresponding nibble of data and does not write into the device.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input Synchronous	**Byte Write Select 0, 1, 2, and 3, Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select the byte written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1557V18 − $\overline{BWS_0}$ controls $D_{[8:0]}$ CY7C1548V18 − $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$ CY7C1550V18 − $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and does not write into the device.
A	Input Synchronous	**Address Inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 8M x 8 (2 arrays each of 4M x 8) for CY7C1546V18, 8M x 9 (2 arrays each of 4M x 9) for CY7C1557V18, 4M x 18 (2 arrays each of 2M x 18) for CY7C1548V18, and 2M x 36 (2 arrays each of 1M x 36) for CY7C1550V18.
R/$\overline{W}$	Input Synchronous	**Synchronous Read or Write Input**. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for loaded address. R/$\overline{W}$ must meet the setup and hold times around edge of K.
QVLD	Valid output indicator	**Valid Output Indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous data presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Clock Output	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the DDR-II+. The timing for the echo clocks is shown in “Switching Characteristics” on page 22.
$\overline{CQ}$	Clock Output	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the DDR-II+. The timing for the echo clocks is shown in “Switching Characteristics” on page 22.

Pin Definitions (continued)

Pin Name	IO	Pin Description
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin is connected directly to V_{DDQ} and enables the minimum impedance mode. This pin is not connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off, Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timing in the DLL turned off operation is different from that listed in this datasheet. For normal operation, this pin is connected to a pull up through a 10 Kohm or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, the device is operated at a frequency of up to 167 MHz with DDR-I timing.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK Pin for JTAG**.
TDI	Input	**TDI Pin for JTAG**.
TMS	Input	**TMS Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Is tied to any voltage level.
NC/72M	N/A	**Not Connected to the Die**. Is tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Is tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Is tied to any voltage level.
V_{REF}	Input Reference	**Reference Voltage Input**. Static input is used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

Functional Overview

The CY7C1546V18, CY7C1557V18, CY7C1548V18, and CY7C1550V18 are synchronous pipelined Burst SRAMs equipped with a DDR interface.

Accesses for both ports are initiated on the Positive Input Clock (K). All synchronous input and output timing refer to the rising edge of the input clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{NWS}_{[0:X]}$, $\overline{BWS}_{[0:X]}$) inputs pass through input registers controlled by the rising edge of the input clock (K\$\overline{K}$).

CY7C1548V18 is described in the following sections. The same basic descriptions apply to CY7C1546V18, CY7C1557V18, and CY7C1550V18.

Read Operations

The CY7C1548V18 is organized internally as two arrays of 4M x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). Following the next two K clock rising edges, drive the corresponding 18-bit word of data from this address location onto the $Q_{[17:0]}$ using K as the output timing reference. On the subsequent rising edge of $\overline{K}$, drive the next 18-bit data word onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K and $\overline{K}$). To maintain the internal logic, each read access is allowed to complete. Read accesses are initiated on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C1548V18 completes the pending read transactions. Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the positive input clock (K). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the Write Address register. On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit Write Data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the Negative Input Clock ($\overline{K}$), the information presented to $D_{[17:0]}$ is also stored into the Write Data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data is then written into the memory array at the specified location. Write accesses are initiated on every rising edge of the positive input clock (K). This pipelines the data flow such that 18 bits of data is transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When write access is deselected, the device ignores all inputs after the pending write operations are completed.

Byte Write Operations

Byte write operations are supported by the CY7C1548V18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, that are sampled with each set of 18-bit data words. The data presented is latched and written into the device by asserting the appropriate Byte Write Select input during the data portion of a write. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature is used to simplify read, modify, and write operations to a byte write operation.

Double Date Rate Operation

The CY7C1548V18 enables high performance operation through high clock frequencies (achieved through pipelining) and DDR mode of operation. The CY7C1548V18 requires two No Operation (NOP) cycles when transitioning from a read to a write cycle. At higher frequencies, some applications require a third NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information is stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a Posted Write.

If a read is performed on the same address where a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals are common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, is connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ is 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR-II+ to simplify data capture on high speed systems. Two echo clocks are generated by the DDR-II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free running clocks and are synchronized to the input clock of the DDR-II+. The timing for the echo clocks is shown in "Switching Characteristics" on page 22.

Valid Data Indicator (QVLD)

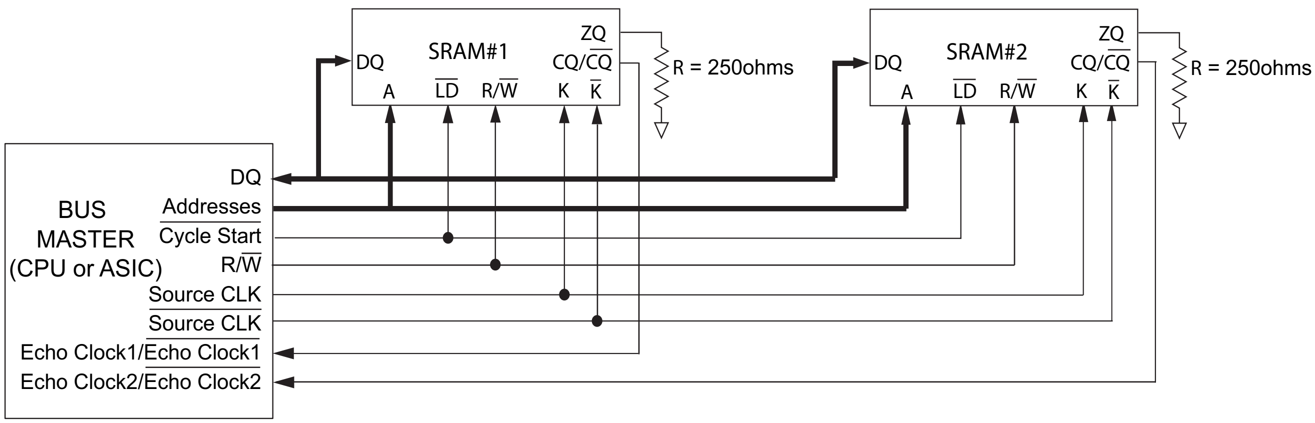
QVLD is provided on the DDR-II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR-II+ device along with data output. This signal is also edge aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

DLL

These chips use a DLL that is designed to function between 120 MHz and the specified maximum clock frequency. The DLL is disabled by applying ground to the $\overline{DOFF}$ pin. When the DLL is turned off, the device behaves in DDR-I mode (with 1.0 cycle latency and a longer access time). For more information, refer to the application note, *DLL Considerations in QDRII/DDRII/QDRII+/DDRII+*. The DLL is reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the DLL to lock at the desired frequency. During power up, when the $\overline{DOFF}$ is tied HIGH, the DLL gets locked after 2048 cycles of stable clock.

Application Example

Figure 1. Application Example



Truth Table

The truth table for CY7C1546V18, CY7C1557V18, CY7C1548V18, and CY7C1550V18 follows.[3, 4, 5, 6, 7, 8]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L-H	L	L	D(A) at K(t + 1) ↑	D(A+1) at $\overline{K}$(t + 1) ↑
Read Cycle: (2.0 cycle Latency) Load address; wait two cycle; read data on consecutive K and $\overline{K}$ rising edges.	L-H	L	H	Q(A) at K(t + 2) ↑	Q(A+1) at $\overline{K}$(t + 2) ↑
NOP: No Operation	L-H	H	X	High Z	High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

Notes
3. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
4. Device powers up deselected with the outputs in a tri-state condition.
5. "A" represents address location latched by the devices when transaction was initiated. A + 1 represents the address sequence in the burst.
6. "t" represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the "t" clock cycle.
7. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges.
8. Cypress recommends that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.

Write Cycle Descriptions

The write cycle description table for CY7C1546V18 and CY7C1548V18 follows. [3, 9]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence : CY7C1546V18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1548V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the data portion of a write sequence : CY7C1546V18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1548V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence : CY7C1546V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1548V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence : CY7C1546V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1548V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence : CY7C1546V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1548V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence : CY7C1546V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1548V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Write Cycle Descriptions

The write cycle description table for CY7C1557V18 follows. [3, 9]

$\overline{BWS_0}$	K	$\overline{K}$	
L	L–H	–	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L–H	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L–H	–	No data is written into the device during this portion of a write operation.
H	–	L–H	No data is written into the device during this portion of a write operation.

Note

9. Assumes a write cycle is initiated as per the Write Cycle Descriptions table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ is altered on different portions of a write cycle, as long as the setup and hold requirements are met.

Write Cycle Descriptions

The write cycle description table for CY7C1550V18 follows. [3, 9]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remain unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remain unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remain unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remain unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard 1149.1-2001. The TAP operates using JEDEC standard 1.8V IO logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW (V_{SS}) to prevent device clocking. TDI and TMS are internally pulled up and are unconnected. They are alternately connected to V_{DD} through a pull up resistor. TDO is left unconnected. Upon power up, the device comes up in a reset state that does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. Leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data In (TDI)

The TDI pin is used to serially input information into the registers and is connected to the input of any of the registers. The register between TDI and TDO is selected by the instruction that is loaded into the TAP instruction register. For information about loading the Instruction register, see "TAP Controller State Diagram" on page 14. TDI is internally pulled up and is unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSb) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The active state of the output depends on the current state of the TAP state machine (see "Instruction Codes" on page 17). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSb) of any register.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and is performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO pins enabling data scanning into and out of the SRAM test circuitry. Only one register is selected at a time through the Instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions is serially loaded into the Instruction register. This register placed between the TDI and TDO pins is loaded as shown in "TAP Controller Block Diagram" on page 15. Upon power up, the Instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the Performing a TAP Reset.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary '01' pattern to enable fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The Bypass register is a single-bit register that is placed between TDI and TDO pins. This enables data shifting through the SRAM with minimal delay. The Bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The Boundary Scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the Scan register to reserve pins for higher density devices.

The Boundary Scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state. It is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions are used to capture the contents of the input and output ring.

"Boundary Scan Order" on page 18 shows the order of the bits that are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSb of the register is connected to TDI and the LSb is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific 32-bit code during the Capture-DR state when the IDCODE command is loaded in the Instruction register. The IDCODE is hardwired into the SRAM and is shifted out, when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in "Identification Register Definitions" on page 17.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in "Instruction Codes" on page 17. Three of these instructions are listed as RESERVED and are not used. The other five instructions are described in this section.

Instructions are loaded into the TAP controller during the Shift-IR state when the Instruction register is placed between TDI and TDO. During this state, instructions are shifted through the Instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller is moved into the Update-IR state.

IDCODE

A vendor specific 32-bit code is loaded into the Instruction register by the IDCODE instruction. It also places the Instruction register between the TDI and TDO pins and enables shifting the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the Instruction register upon power up or whenever the TAP controller is in a Test-Logic-Reset state.

SAMPLE Z

The Boundary Scan register is connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state by the SAMPLE Z instruction. The SAMPLE Z command puts the output bus into a High Z state until the next command is issued during the Update-IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the Instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the Boundary Scan register.

The TAP controller clock only operates at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state an input or output may undergo a transition. The TAP then tries to capture a signal while in transition (metastable state). This does not harm the device but there is no guarantee as to the value that is captured. Repeatable results are not possible.

To guarantee that the Boundary Scan register captures the correct value of a signal, the SRAM signal is stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input is not captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the Boundary Scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the Boundary Scan register between the TDI and TDO pins.

An initial data pattern is placed at the latched parallel outputs of the Boundary Scan register cells before the selection of another boundary scan test operation by PRELOAD.

The shifting of data for the SAMPLE and PRELOAD phases occur concurrently when required — that is, while data captured is shifted out, the preloaded data is shifted in.

BYPASS

When the BYPASS instruction is loaded in the Instruction register and the TAP is placed in a Shift-DR state, the Bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The preloaded data is driven out through the system output pins by the EXTEST instruction. This instruction also selects the Boundary Scan register connected for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST Output Bus Tri-State

IEEE Standard 1149.1 mandates that the TAP controller puts the output bus into a tri-state mode.

The Boundary Scan register has a special bit located at bit 108 called the “extest output bus tri-state”. When this scan cell is latched into the Preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

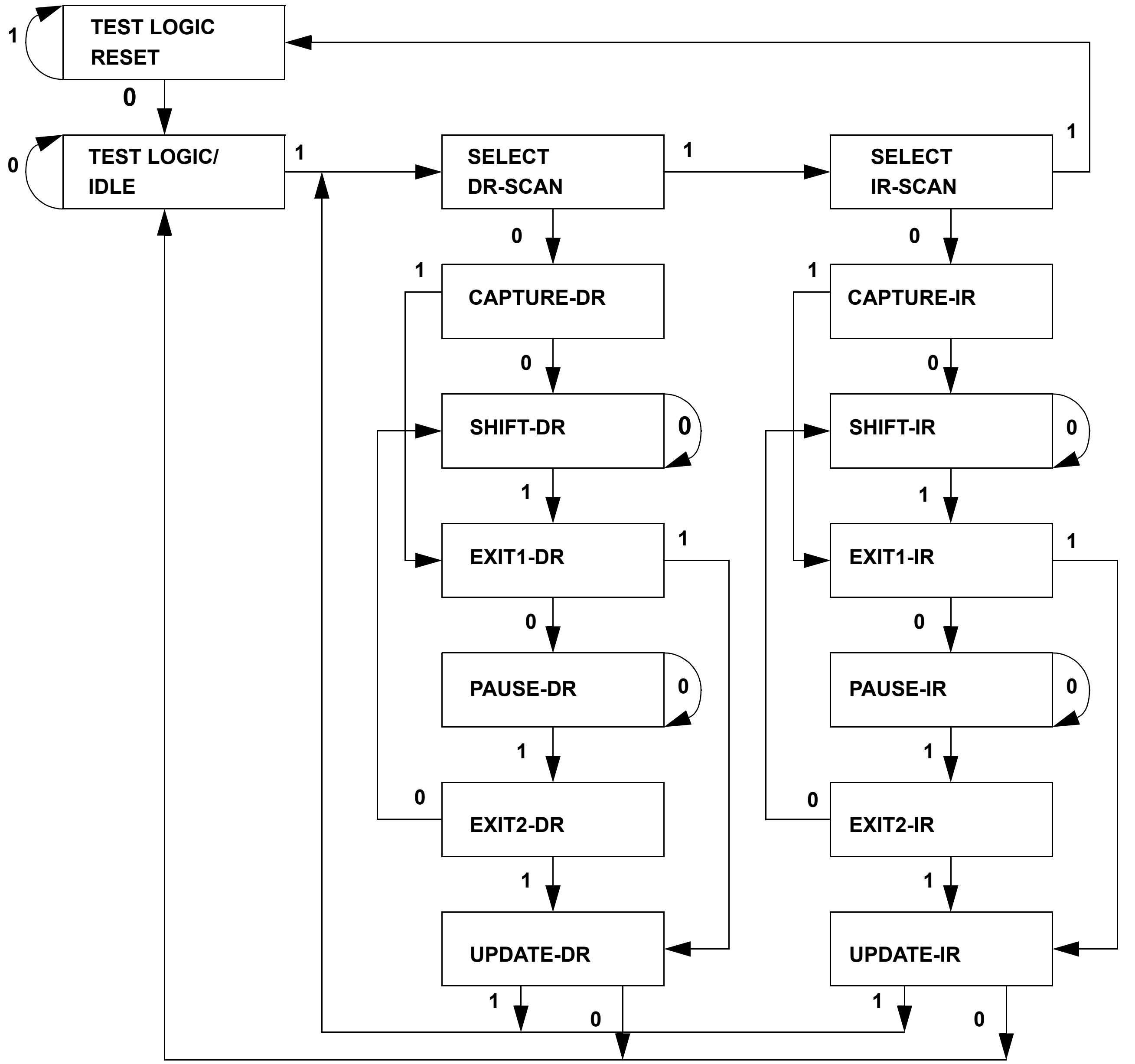
This bit is set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell during the Shift-DR state. During Update-DR, the value loaded into that shift register cell latches into the Preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions

TAP Controller State Diagram

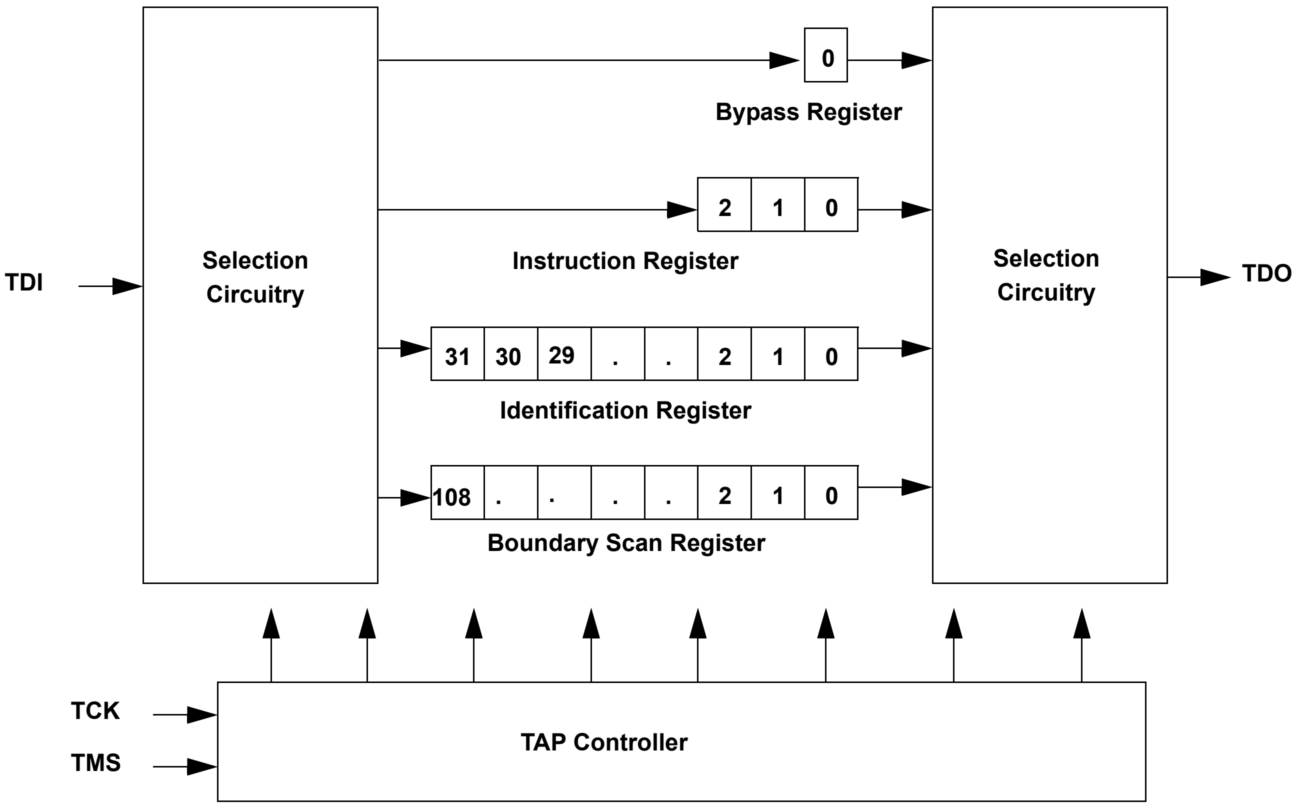
The state diagram for the TAP controller follows.[10]



Note

10. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range [11, 12, 13]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	$I_{OH} = -2.0$ mA	1.4		V
V_{OH2}	Output HIGH Voltage	$I_{OH} = -100\ \mu A$	1.6		V
V_{OL1}	Output LOW Voltage	$I_{OL} = 2.0$ mA		0.4	V
V_{OL2}	Output LOW Voltage	$I_{OL} = 100\ \mu A$		0.2	V
V_{IH}	Input HIGH Voltage		$0.65V_{DD}$	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage		–0.3	$0.35V_{DD}$	V
I_X	Input and Output Load Current	$GND \le V_I \le V_{DD}$	–5	5	µA

Notes

11. These characteristics apply to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in “Electrical Characteristics” on page 20.
12. Overshoot: $V_{IH}(AC) \le V_{DDQ} + 0.3V$ (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL}(AC) \ge -0.3V$ (pulse width less than $t_{CYC}/2$).
13. All voltage refers to ground.

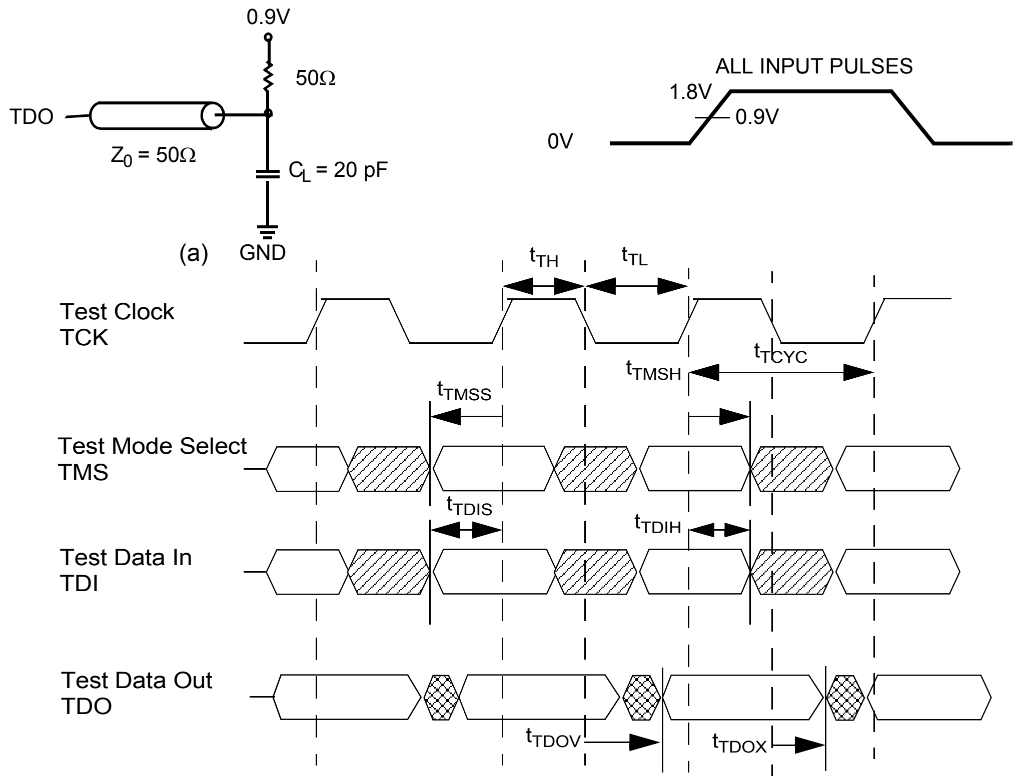
TAP AC Switching Characteristics

Over the Operating Range [14, 15]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold After TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold After Clock Rise	5		ns
t_{CH}	Capture Hold After Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions

Figure 2. TAP Timing and Test Conditions [15]



Notes

14. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
15. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value				Description
	CY7C1546V18	CY7C1557V18	CY7C1548V18	CY7C1550V18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010111100000100	11010111100001100	11010111100010100	11010111100100100	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Enables unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the Boundary Scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the Boundary Scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the Bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit Number	Bump ID	Bit Number	Bump ID	Bit Number	Bump ID	Bit Number	Bump ID
0	6R	28	10G	56	6A	84	1J
1	6P	29	9G	57	5B	85	2J
2	6N	30	11F	58	5A	86	3K
3	7P	31	11G	59	4A	87	3J
4	7N	32	9F	60	5C	88	2K
5	7R	33	10F	61	4B	89	1K
6	8R	34	11E	62	3A	90	2L
7	8P	35	10E	63	2A	91	3L
8	9R	36	10D	64	1A	92	1M
9	11P	37	9E	65	2B	93	1L
10	10P	38	10C	66	3B	94	3N
11	10N	39	11D	67	1C	95	3M
12	9P	40	9C	68	1B	96	1N
13	10M	41	9D	69	3D	97	2M
14	11N	42	11B	70	3C	98	3P
15	9M	43	11C	71	1D	99	2N
16	9N	44	9B	72	2C	100	2P
17	11L	45	10B	73	3E	101	1P
18	11M	46	11A	74	2D	102	3R
19	9L	47	10A	75	2E	103	4R
20	10L	48	9A	76	1E	104	4P
21	11K	49	8B	77	2F	105	5P
22	10K	50	7C	78	3F	106	5N
23	9J	51	6C	79	1G	107	5R
24	9K	52	8A	80	1F	108	Internal
25	10J	53	7A	81	3G		
26	11J	54	7B	82	2G		
27	11H	55	6B	83	1H		

Power Up Sequence in DDR-II+ SRAM

DDR-II+ SRAMs is powered up and initialized in a pre-defined manner to prevent undefined operations. During power up, when the $\overline{DOFF}$ is tied HIGH, the DLL is locked after 2048 cycles of stable clock.

Power Up Sequence

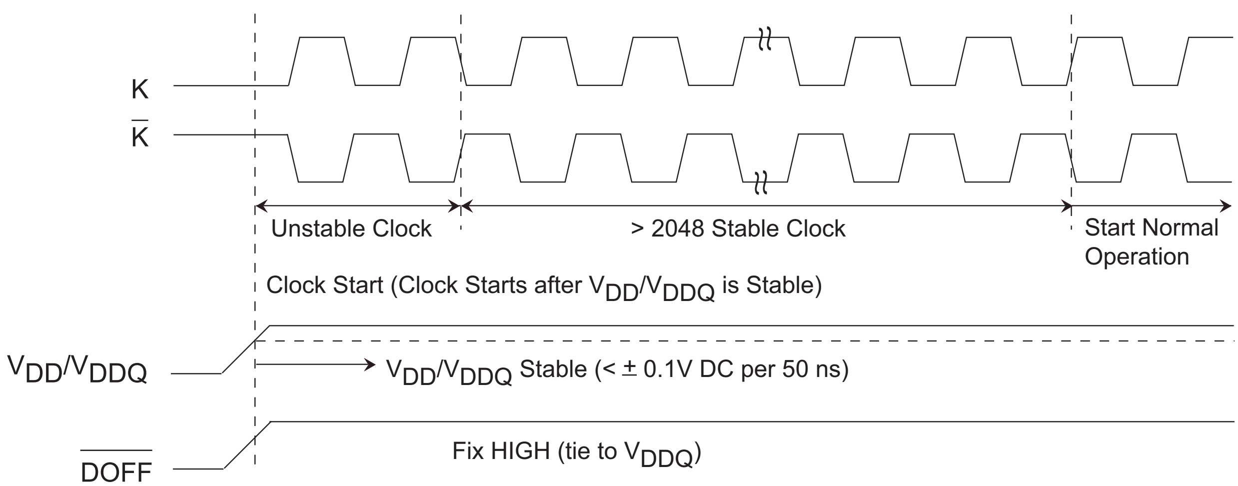
- Apply power with $\overline{DOFF}$ tied HIGH (All other inputs are HIGH or LOW)
  - Apply V_{DD} before V_{DDQ}
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
- Provide stable power and clock (K, $\overline{K}$) for 2048 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input has low phase jitter that is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL locks onto an incorrect frequency. This causes unstable SRAM behavior. To avoid this, provide 2048 cycles stable clock to relock to the desired clock frequency.

Power Up Waveforms

Figure 3. Power Up Waveforms



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND ....–0.5V to +2.9V

Supply Voltage on V_{DDQ} Relative to GND.......–0.5V to +V_{DD}

DC Applied to Outputs in High Z ....–0.5V to V_{DDQ} + 0.3V

DC Input Voltage[12]............................. –0.5V to V_{DD} + 0.3V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, M. 3015)... >2001V

Latch up Current.. >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}[16]	V_{DDQ}[16]
Commercial	0°C to +70°C	1.8 ± 0.1V	1.4V to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics

Over the Operating Range[13]

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage			1.7	1.8	1.9	V
V_{DDQ}	IO Supply Voltage			1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 17		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 18		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	I_{OH} = –0.1 mA, Nominal Impedance		V_{DDQ} – 0.2		V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	I_{OL} = 0.1 mA, Nominal Impedance		V_{SS}		0.2	V
V_{IH}	Input HIGH Voltage			V_{REF} + 0.1		V_{DDQ} + 0.15	V
V_{IL}	Input LOW Voltage			–0.15		V_{REF} – 0.1	V
I_X	Input Leakage Current	GND ≤ V_I ≤ V_{DDQ}		–2		2	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–2		2	µA
V_{REF}	Input Reference Voltage[19]	Typical Value = 0.75V		0.68	0.75	0.95	V
I_{DD} (x8)	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	300 MHz			1100	mA
			333 MHz			1200	
			375 MHz			1300	
I_{DD} (x9)	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	300 MHz			1100	mA
			333 MHz			1200	
			375 MHz			1300	
I_{DD} (x18)	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	300 MHz			1100	mA
			333 MHz			1200	
			375 MHz			1300	
I_{DD} (x36)	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	300 MHz			1100	mA
			333 MHz			1200	
			375 MHz			1300	
I_{SB1}	Automatic Power Down Current	Max V_{DD}, Both Ports Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = $1/t_{CYC}$, Inputs Static	300 MHz			450	mA
			333 MHz			500	
			375 MHz			525	

Notes

16. Power up: assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
17. Outputs are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
18. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175Ω ≤ RQ ≤ 350Ω.
19. V_{REF} (min) = 0.68V or $0.46V_{DDQ}$, whichever is larger. V_{REF} (max) = 0.95V or $0.54V_{DDQ}$, whichever is smaller.

AC Electrical Characteristics

Over the Operating Range[12]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		V_{REF} + 0.2	–	V_{DDQ} + 0.24	V
V_{IL}	Input LOW Voltage		–0.24	–	V_{REF} – 0.2	V

Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V	5.5	pF
C_{CLK}	Clock Input Capacitance		8.5	pF
C_O	Output Capacitance		8	pF

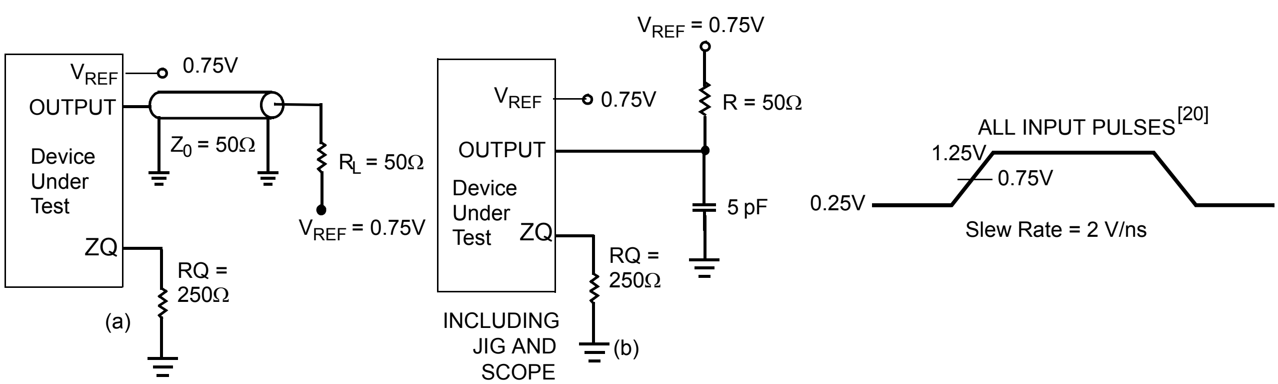
Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	11.82	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.33	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Note

20. Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, output loading of the specified $I_{OL}/I_{OH,}$ and load capacitance shown in (a) of AC Test Loads and Waveforms.

Switching Characteristics

Over the Operating Range [20, 21]

Cypress Parameter	Consortium Parameter	Description	375 MHz		333 MHz		300 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the First Access[22]	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K Clock Cycle Time	2.66	8.40	3.0	8.40	3.3	8.40	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$) HIGH	0.4	–	0.4	–	0.4	–	t_{CYC}
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$) LOW	0.4	–	0.4	–	0.4	–	t_{CYC}
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	1.13	–	1.28	–	1.40	–	ns
Setup Times									
t_{SA}	t_{AVKH}	Address Setup to K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t_{SC}	t_{IVKH}	Control Setup to K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.4	–	ns
t_{SCDDR}	t_{IVKH}	Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.28	–	0.28	–	0.28	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	ns
Hold Times									
t_{HA}	t_{KHAX}	Address Hold After K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t_{HC}	t_{KHIX}	Control Hold After K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.4	–	0.4	–	0.4	–	ns
t_{HCDDR}	t_{KHIX}	Double Data Rate Control Hold After Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.28	–	0.28	–	0.28	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold After Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	ns
Output Times									
t_{CO}	t_{CHQV}	K/$\overline{K}$ Clock Rise to Data Valid	–	0.45	–	0.45	–	0.45	ns
t_{DOH}	t_{CHQX}	Data Output Hold After K/$\overline{K}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold After K/$\overline{K}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid	–	0.2	–	0.2	–	0.2	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.2	–	–0.2	–	–0.2	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH [23]	0.88	–	1.03	–	1.15	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise [23] (rising edge to rising edge)	0.88	–	1.03	–	1.15	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) Rise to High Z (Active to High Z) [24, 25]	–	0.45	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) Rise to Low Z[24, 25]	–0.45	–	–0.45	–	–0.45	–	ns
t_{QVLD}	t_{QVLD}	Echo Clock High to QVLD Valid [26]	–0.20	0.20	–0.20	0.20	–0.20	0.20	ns
DLL Timing									
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL Lock Time (K)	2048	–	2048	–	2048	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to DLL Reset [27]	30	–	30	–	30	–	ns

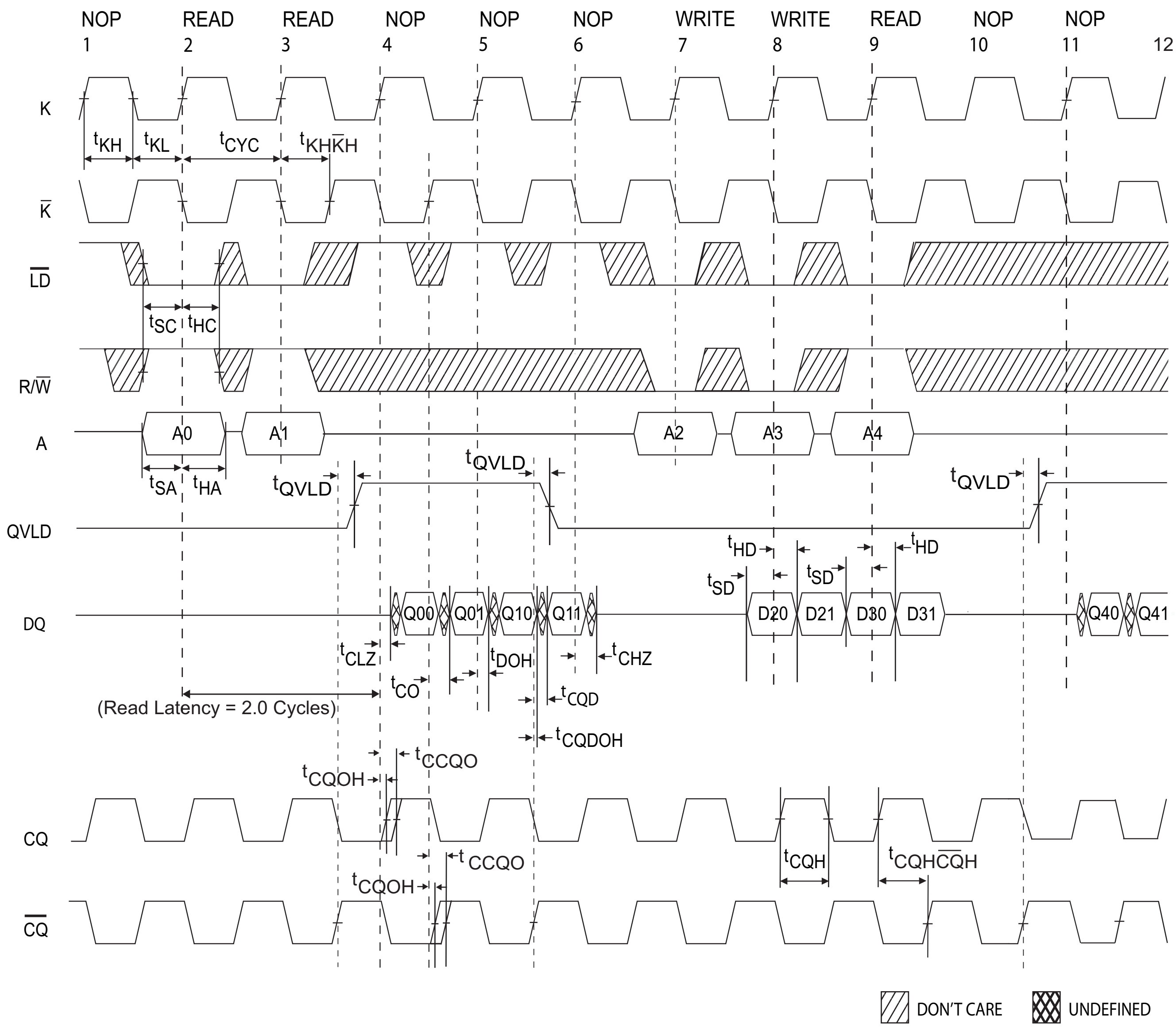
Notes

21. When a part with a maximum frequency above 300 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is operated and outputs data with the output timings of that frequency range.
22. This part has a voltage regulator internally; t_{POWER} is the time that the power is supplied above V_{DD} minimum initially before a read or write operation is initiated.
23. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production
24. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±100 mV from steady-state voltage.
25. At any given voltage and temperature, t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
26. t_{QVLD} specification is applicable for both rising and falling edges of QVLD signal.
27. Hold to >V_{IH} or <V_{IL}.

Switching Waveforms

Read/Write/Deselect Sequence [28, 29, 30]

Figure 5. Waveform for 2.0 Cycle Read Latency



Notes

28. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
29. Outputs are disabled (High-Z) one clock cycle after a NOP.
30. The third NOP cycle between read to write transition is not necessary for correct device operation when Read Latency = 2.0 cycles; however at high frequency operation, it is required to avoid bus contention.

Ordering Information

Not all of the speed, package, and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
375	CY7C1546V18-375BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1557V18-375BZC			
	CY7C1548V18-375BZC			
	CY7C1550V18-375BZC			
	CY7C1546V18-375BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-375BZXC			
	CY7C1548V18-375BZXC			
	CY7C1550V18-375BZXC			
	CY7C1546V18-375BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1557V18-375BZI			
	CY7C1548V18-375BZI			
	CY7C1550V18-375BZI			
	CY7C1546V18-375BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-375BZXI			
	CY7C1548V18-375BZXI			
	CY7C1550V18-375BZXI			
333	CY7C1546V18-333BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1557V18-333BZC			
	CY7C1548V18-333BZC			
	CY7C1550V18-333BZC			
	CY7C1546V18-333BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-333BZXC			
	CY7C1548V18-333BZXC			
	CY7C1550V18-333BZXC			
	CY7C1546V18-333BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1557V18-333BZI			
	CY7C1548V18-333BZI			
	CY7C1550V18-333BZI			
	CY7C1546V18-333BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-333BZXI			
	CY7C1548V18-333BZXI			
	CY7C1550V18-333BZXI			

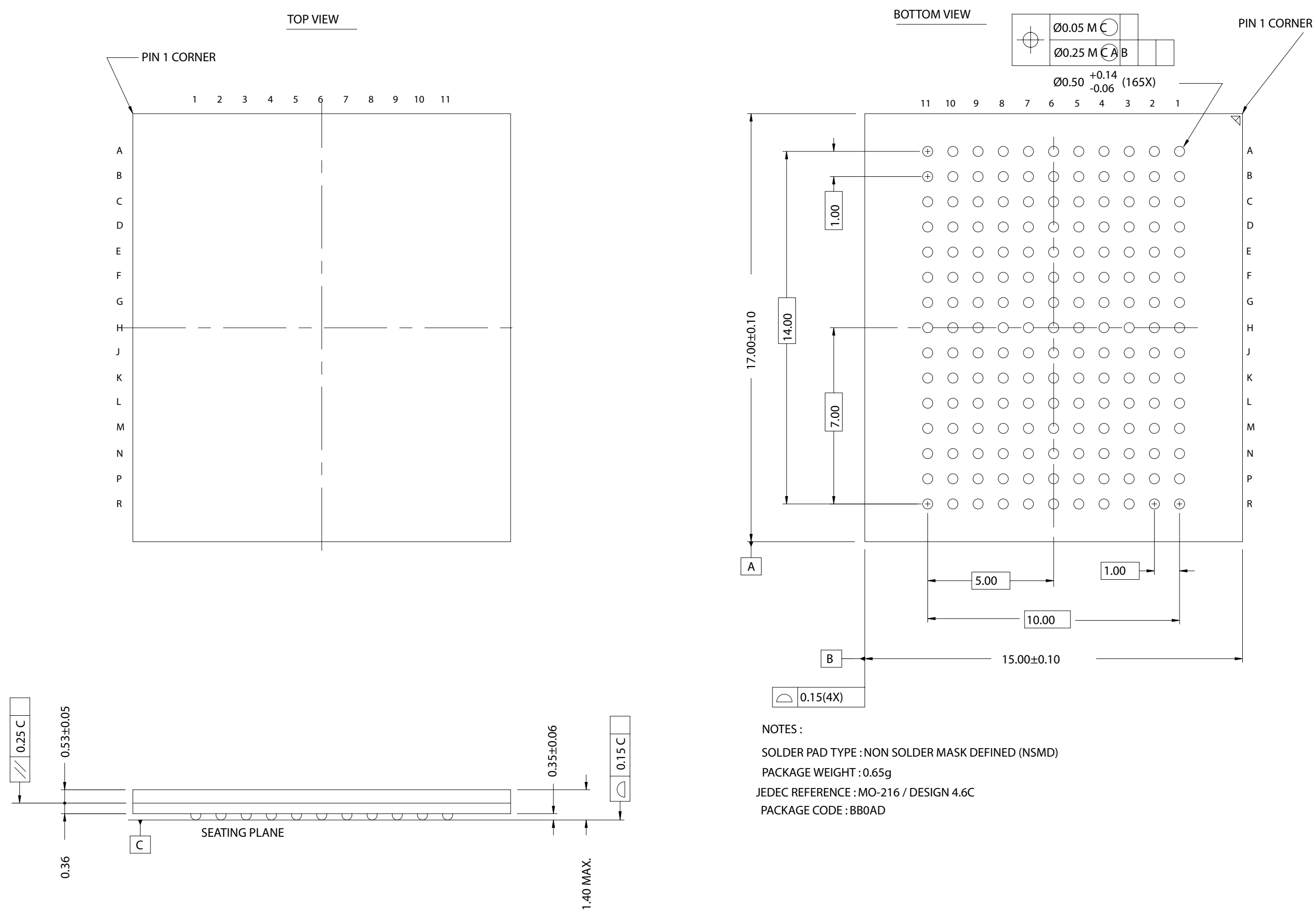
Ordering Information (continued)

Not all of the speed, package, and temperature ranges are available. Contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
300	CY7C1546V18-300BZC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1557V18-300BZC			
	CY7C1548V18-300BZC			
	CY7C1550V18-300BZC			
	CY7C1546V18-300BZXC	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-300BZXC			
	CY7C1548V18-300BZXC			
	CY7C1550V18-300BZXC			
	CY7C1546V18-300BZI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1557V18-300BZI			
	CY7C1548V18-300BZI			
	CY7C1550V18-300BZI			
	CY7C1546V18-300BZXI	51-85195	165-Ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1557V18-300BZXI			
	CY7C1548V18-300BZXI			
	CY7C1550V18-300BZXI			

Package Diagram

Figure 6. 165-Ball FBGA (15 x 17 x 1.40 mm)



51-85195-*A

Document History Page

Document Title: CY7C1546V18/CY7C1557V18/CY7C1548V18/CY7C1550V18, 72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) Document Number: 001-06550				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	432718	See ECN	NXR	New datasheet
*A	437000	See ECN	IGS	ECN for show on web
*B	461934	See ECN	NXR	Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power up waveform
*C	497567	See ECN	NXR	Changed the V_{DDQ} operating voltage to 1.4V to V_{DD} in the Features section, Operating Range table, and the DC Electrical Characteristics table Added foot note in page 1 Changed the Maximum rating of ambient temperature with power applied from –10°C to +85°C to –55°C to +125°C Changed V_{REF} (Max) specification from 0.85V to 0.95V in the DC Electrical Characteristics table and in the note below the table Updated footnote 18 to specify overshoot and undershoot specifications Updated I_{DD} and I_{SB} values Updated Θ_{JA} and Θ_{JC} values Removed x9 part and its related information Updated footnote 25
*D	1351504	See ECN	VKN/AESA	Converted from preliminary to final Added x8 and x9 parts Updated logic block diagram for x18 and x36 parts Changed t_{CYC} max spec to 8.4 ns for all speed bins Updated footnote# 21 Updated Ordering Information table