CY7C1324H

2-Mbit (128 K × 18) Flow-Through Sync SRAM

Features

- 128 K × 18 common I/O
- 3.3 V core power supply
- 3.3- / 2.5-V I/O supply
- Fast clock-to-output times
  - 6.5 ns (133 MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Offered in JEDEC-standard Pb-free 100-pin thin quad flat pack (TQFP) package
- "ZZ" sleep mode option

Functional Description

The CY7C1324H[1] is a 128 K × 18 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE_1}$), depth-expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_{[A:B]}}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin. The CY7C1324H allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the Address Advancement ($\overline{ADV}$) input. Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

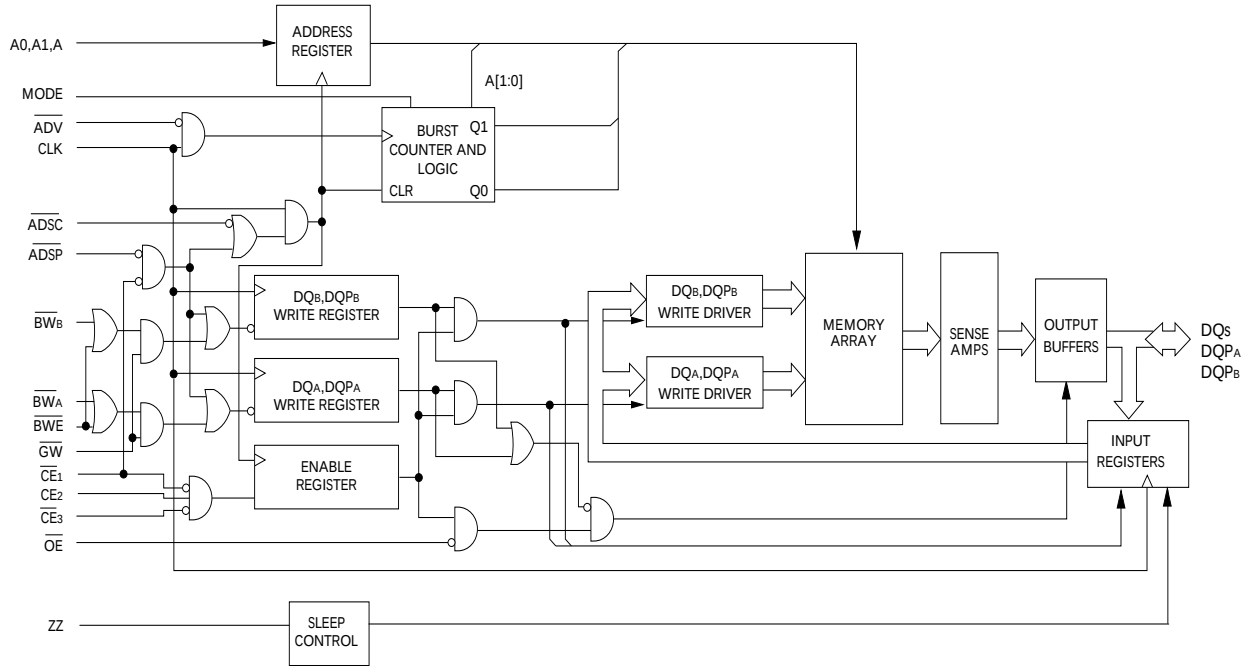
The CY7C1324H operates from a +3.3 V core power supply while all outputs may operate with either a +3.3 V or +2.5 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Selection Guide

	133 MHz	Unit
Maximum access time	6.5	ns
Maximum operating current	225	mA
Maximum standby current	40	mA

Note
1. Refer to the application note, SRAM System Design Guidelines for more information on best-practices recommendations.

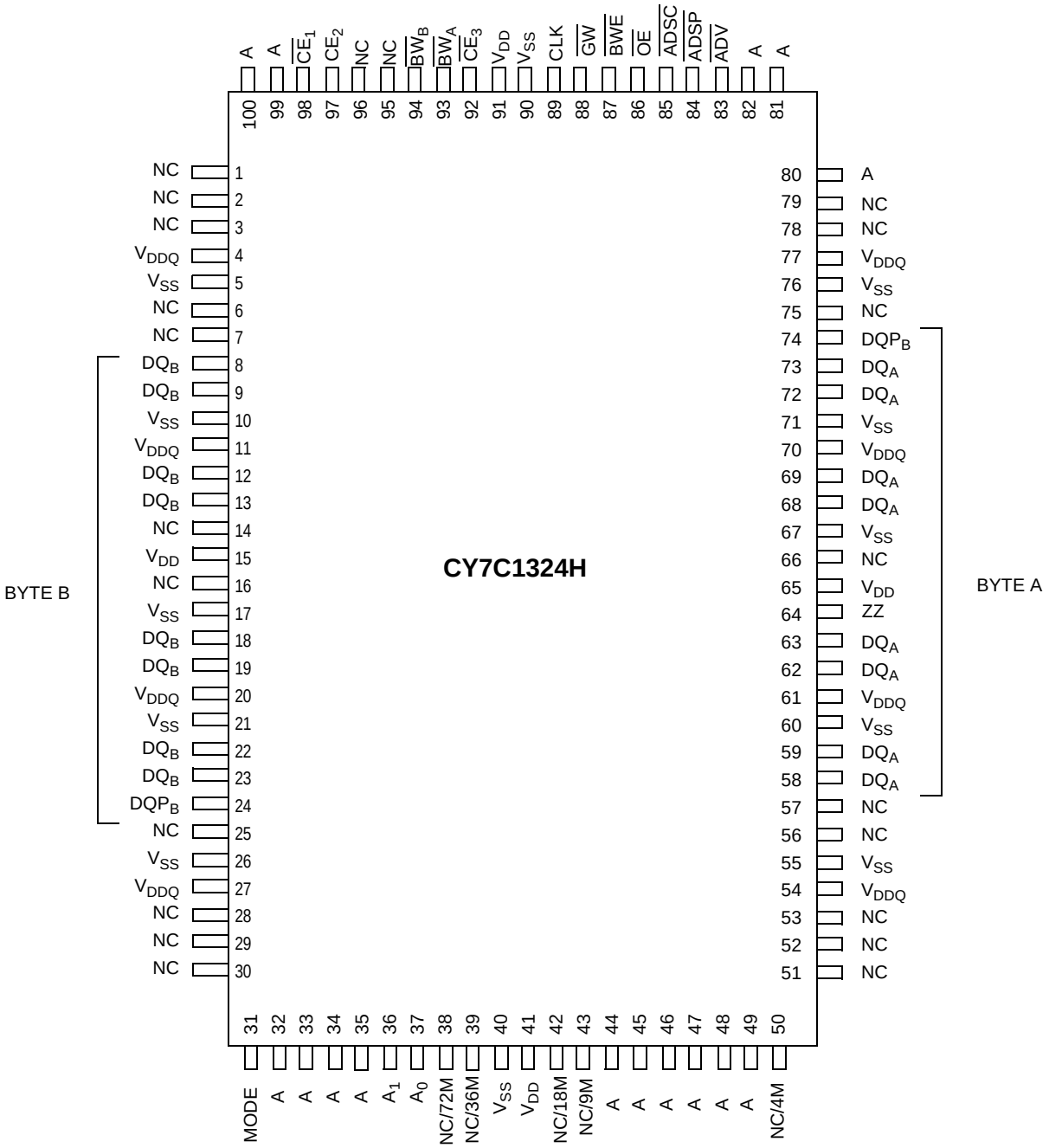
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 100-Pin TQFP Pinout[2]



Note
2. Refer to the application note, AN4025 for more information on SRAM address and I/O pin order.

Pin Definitions

Name	I/O	Description
A0, A1, A	Input-Synchronous	**Address Inputs used to select one of the 128 K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:B]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a Read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs DQP_A, DQP_B	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the Read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and $DQP_{[A:B]}$ are placed in a tristate condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the device**.

Pin Definitions (continued)

Name	I/O	Description
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
MODE	Input-static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC		**No Connects**. **Not internally connected to the die**. 4M, 9M, 18M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1324H supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ($BW_{[A:B]}$) inputs. A Global Write Enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tristate control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data is available at the data outputs a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and $BW_{[A:B]}$) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a Write) on the next clock rise, the appropriate data is latched and written into the device. Byte Writes are allowed. During Byte Writes, BWA controls DQA and BWB controls DQB. All I/Os are tristated during a Byte Write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals (GW, BWE, and BW[A:B]) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to DQ[A:D] is written into the specified address location. Byte Writes are allowed. During Byte Writes, BWA controls DQA and BWB controls DQB. All I/Os are tristated when a Write is detected, even a Byte Write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1324H provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to an interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CEs, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Linear Burst Address Table (MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V		40	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

Cycle Description[3, 4, 5, 6]	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselected cycle, power-down	None	X	X	X	L	H	L	X	X	X	L-H	Tristate
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D

Truth Table

Cycle Description[3, 4, 5, 6]	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	CLK	DQ
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Truth Table for Read/Write

Function[3, 4]	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X
Read	H	L	H	H
Write byte (A, DQP_A)	H	L	H	L
Write byte (B, DQP_B)	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes

3. X = “Do not care.” H = Logic HIGH, L =Logic LOW.
4. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$) and $\overline{BWE}$ = L or $\overline{GW}$= L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$), $\overline{BWE}$, $\overline{GW}$ = H.The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:B]}}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND.....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND..... –0.5 V to +V_{DD}

DC voltage applied to outputs in tristate–0.5 V to V_{DDQ} + 0.5 V

DC input voltage ..... –0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V –5%/+10%	2.5 V –5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the operating range [7, 8]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	For 3.3 V I/O		3.135	V_{DD}	V
		For 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	For 3.3 V I/O, I_{OH} = –4.0 mA		2.4		V
		For 2.5 V I/O, I_{OH} = –1.0 mA		2.0		
V_{OL}	Output LOW voltage	For 3.3 V I/O, I_{OL} = 8.0 mA			0.4	V
		For 2.5 V I/O, I_{OL} = 1.0 mA			0.4	
V_{IH}	Input HIGH voltage	For 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		For 2.5 V I/O		1.7	V_{DD} + 0.3 V	
V_{IL}	Input LOW voltage[7]	For 3.3 V I/O		–0.3	0.8	V
		For 2.5 V I/O		–0.3	0.7	
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX}= 1/t_{CYC}	7.5 ns cycle, 133 MHz		225	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	Maximum V_{DD}, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		90	mA
I_{SB2}	Automatic CE power-down Current—CMOS inputs	Maximum V_{DD}, device deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, inputs static	7.5 ns cycle, 133 MHz		40	mA

Notes

7. Overshoot: V_{IH}(AC) < V_{DD} +1.5 V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2 V (Pulse width less than t_{CYC}/2).
8. $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to V_{DD}(min) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics

Over the operating range (continued)[7, 8]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE power-down current—CMOS inputs	Maximum V_{DD}, device deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		75	mA
I_{SB4}	Automatic CE power-down current—TTL inputs	Maximum V_{DD}, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz		45	mA

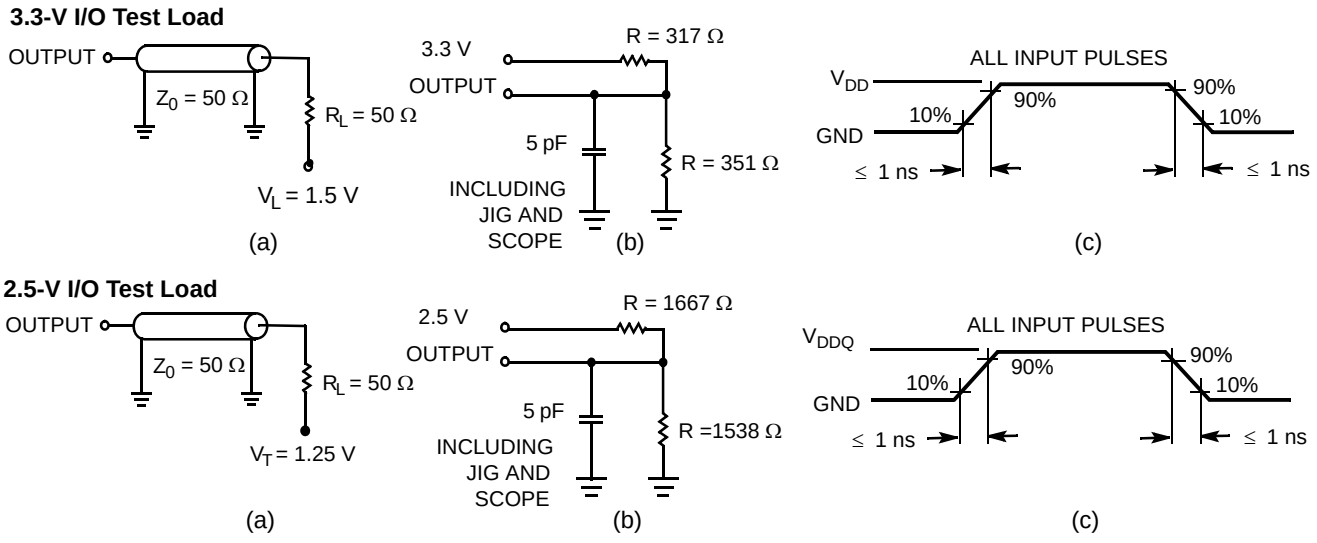
Capacitance

Parameter[9]	Description	Test Conditions	100 TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	I/O capacitance		5	pF

Thermal Resistance

Parameter[9]	Description	Test Conditions	100 TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	30.32	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	°C/W

Figure 2. AC Test Loads and Waveforms



Note
9. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the operating range[10, 11]

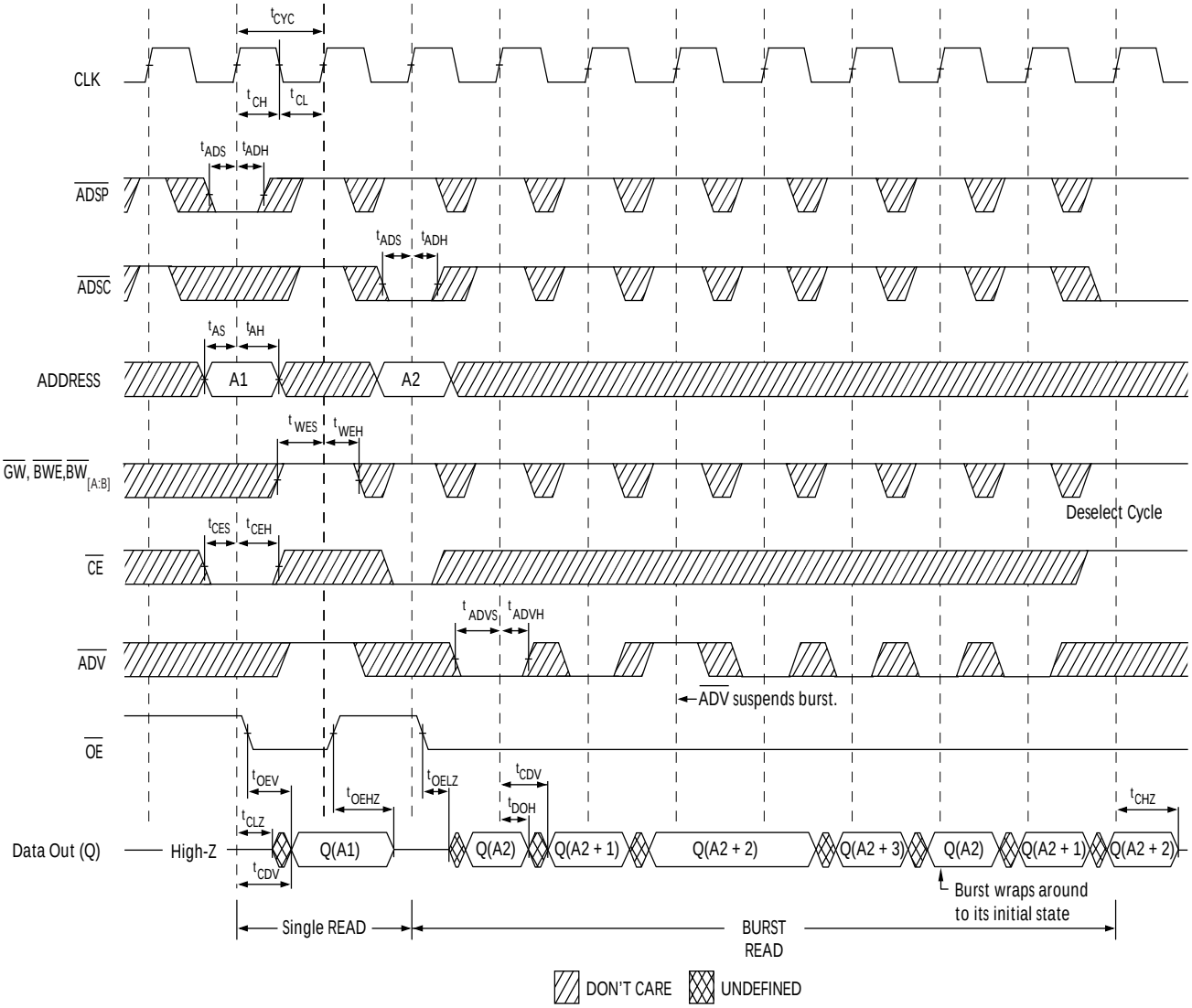
Parameter	Description	–133		Units
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access[12]	1		ms
Clock				
t_{CYC}	Clock cycle time	7.5		ns
t_{CH}	Clock HIGH	2.5		ns
t_{CL}	Clock LOW	2.5		ns
Output Times				
t_{CDV}	Data output valid after CLK Rise		6.5	ns
t_{DOH}	Data output hold after CLK Rise	2.0		ns
t_{CLZ}	Clock to low Z[13, 14, 15]	0		ns
t_{CHZ}	Clock to high Z[13, 14, 15]		3.5	ns
t_{OEV}	$\overline{OE}$ LOW to output valid		3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z[13, 14, 15]	0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z[13, 14, 15]		3.5	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ setup before CLK rise	1.5		ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:B]}$ setup before CLK Rise	1.5		ns
t_{DS}	Data input setup before CLK rise	1.5		ns
t_{CES}	Chip enable setup	1.5		ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:B]}$ hold after CLK rise	0.5		ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5		ns
t_{DH}	Data input hold after CLK rise	0.5		ns
t_{CEH}	Chip enable hold after CLK rise	0.5		ns

Notes

10. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and 1.25 V when V_{DDQ} = 2.5 V
11. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
12. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied higher than V_{DD}(minimum) initially before a read or write operation can be initiated.
13. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
15. This parameter is sampled and not 100% tested.

Timing Diagrams

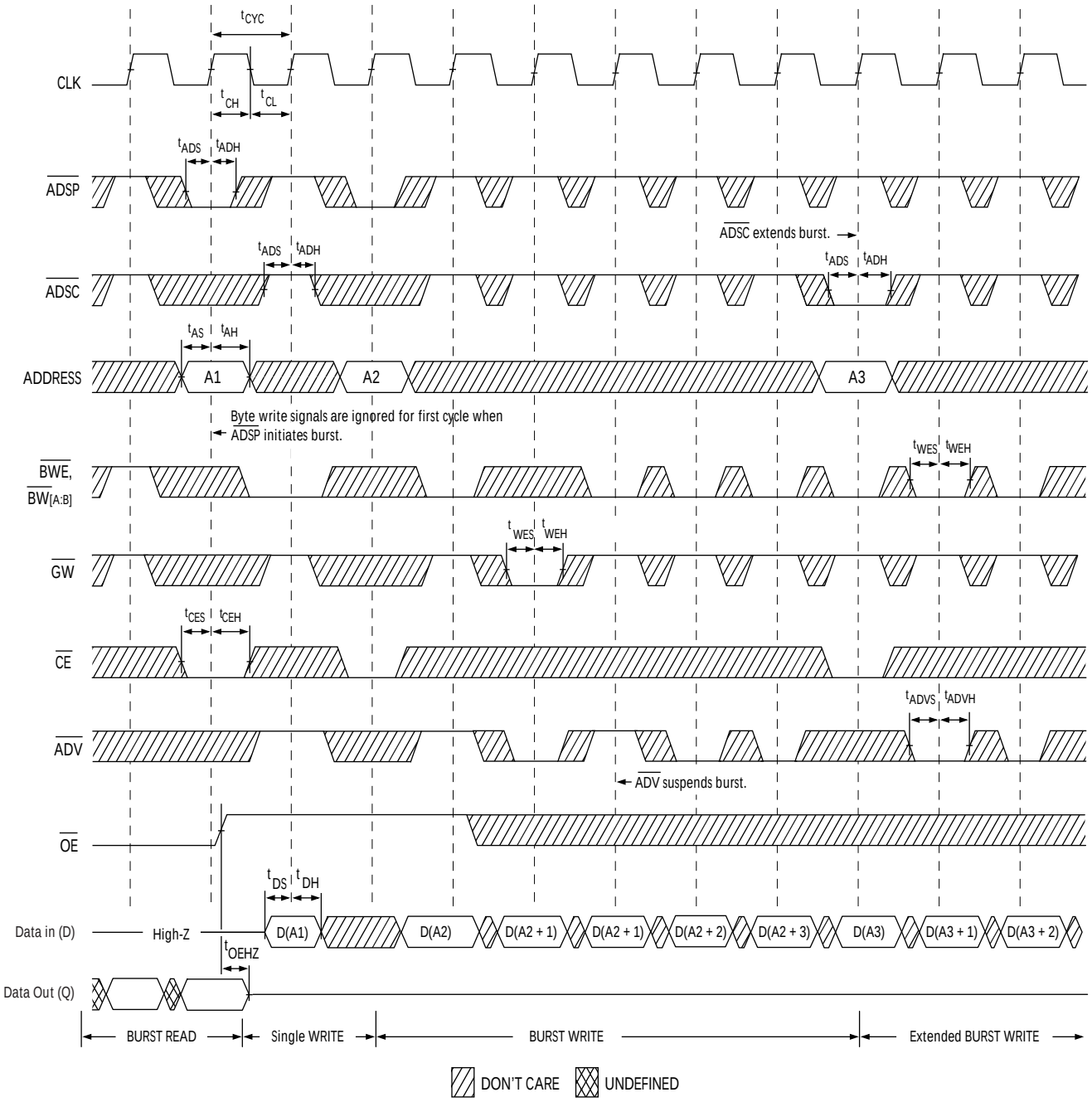
Figure 3. Read Cycle Timing[16]



Note
16. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

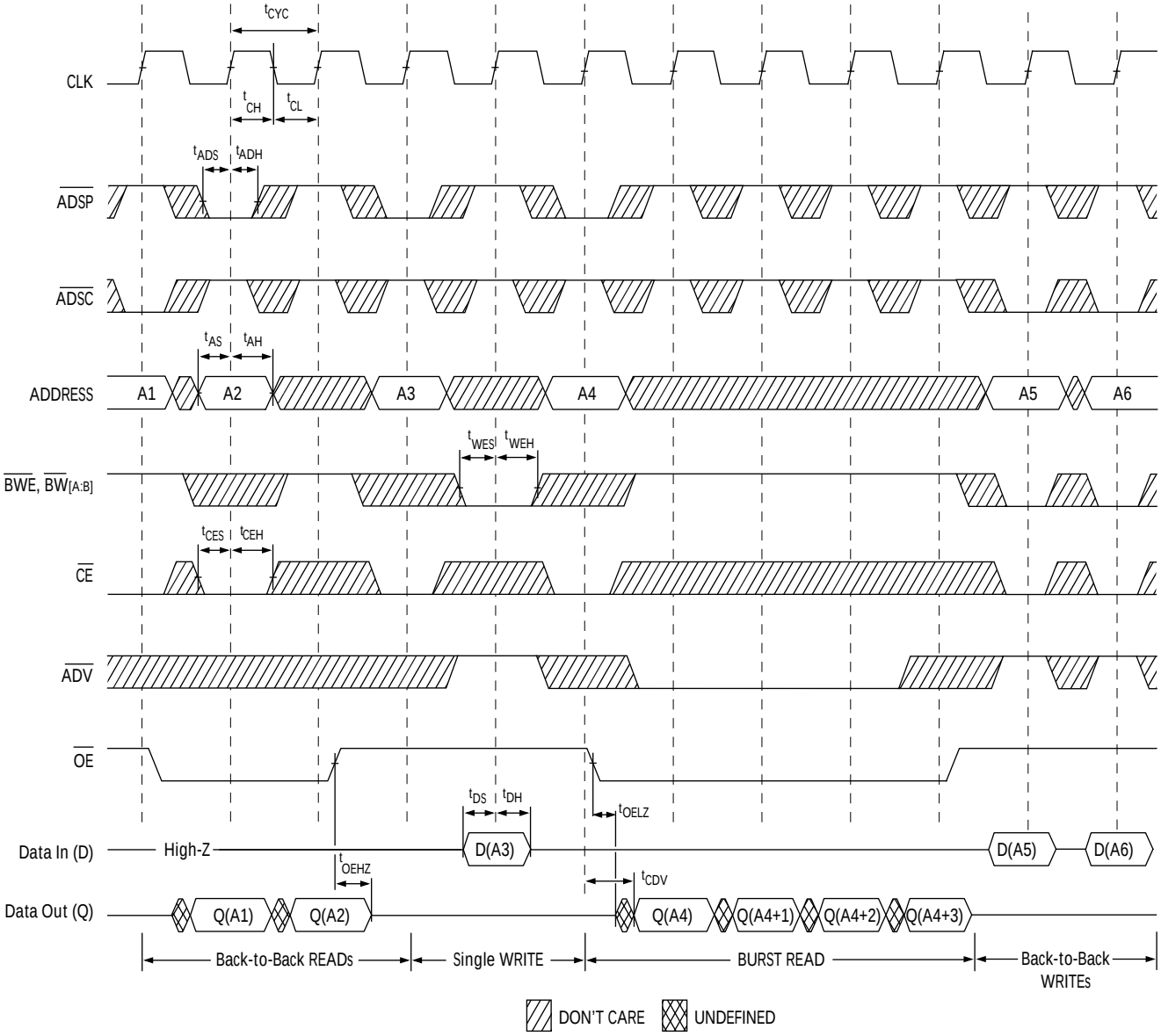
Figure 4. Write Cycle Timing[16, 17]



Note
17. Full width Write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:B]}$ LOW

Timing Diagrams (continued)

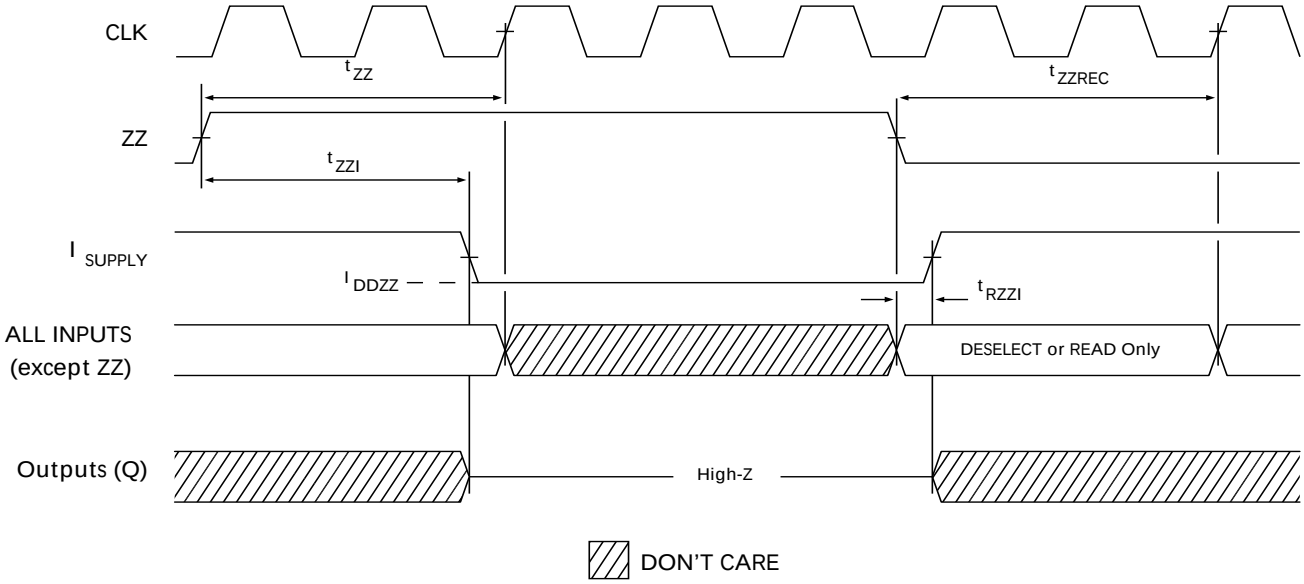
Figure 5. Read/Write Timing[16, 18, 19]



Notes
18. The data bus (Q) remains in high Z following a write cycle unless an ADSP, ADSC, or ADV cycle is performed.
19. GW is HIGH.

Timing Diagrams (continued)

Figure 6. ZZ Mode Timing[20, 21]



Notes
20. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
21. DQs are in High Z when exiting ZZ sleep mode.

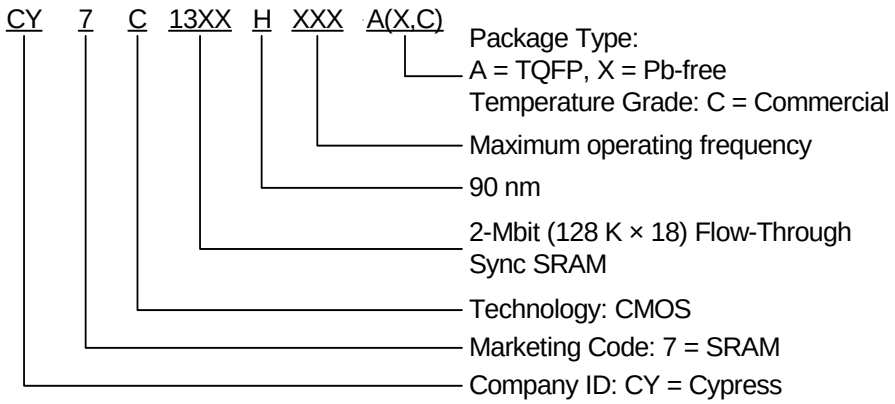
Ordering Information

Table 1 lists the CY7C1324H key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

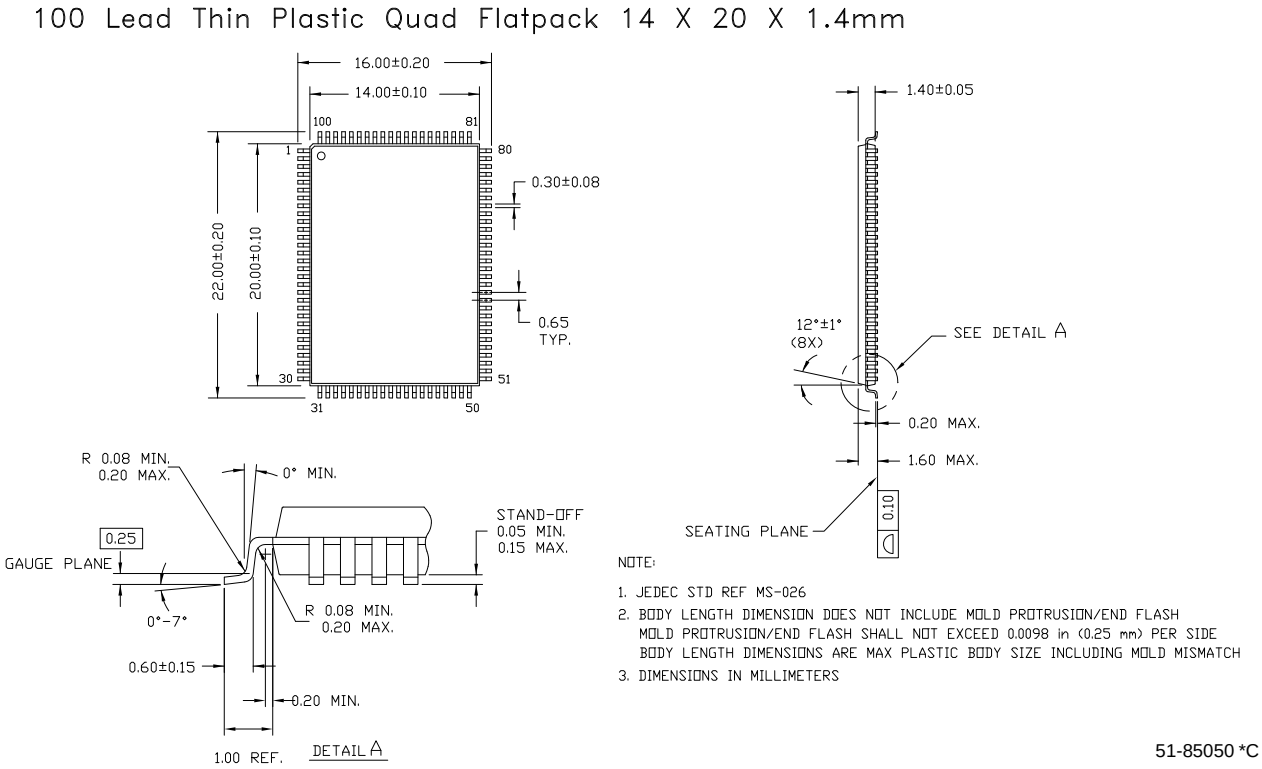
Table 1. Key Features and Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1324H-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions



Package Diagram



Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
I/O	input/output
JEDEC	joint electron device engineering council
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	micro amperes
mA	milliamperes
mm	millimeters
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	volts
W	watts

Document History Page

Document Title: CY7C1324H 2-Mbit (128 K × 18) Flow-Through Sync SRAM Document Number: 001-00208				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	347377	PCI	See ECN	New datasheet
*A	428408	NXR	See ECN	Converted from Preliminary to Final. Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Removed 100 MHz Speed-bin Changed Three-State to tristate. Modified “Input Load” to “Input Leakage Current except ZZ and MODE” in the Electrical Characteristics Table. Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ Replaced Package Name column with Package Diagram in the Ordering Information table. Updated the Ordering Information Table. Replaced Package Diagram of 51-85050 from *A to *B
*B	459347	NXR	See ECN	Included 2.5 V I/O option Updated the Ordering Information table.
*C	2897120	NJY	03/22/10	Removed inactive parts from Ordering Information table; Updated package diagram.
*D	3025128	RAJA/NJY	09/08/10	Template update. Added ordering code definitions, acronyms, units of measure, reference documents, and table of contents.

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