

16-Mbit (1M x 16) Static RAM

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - 990 mW (max)
- Operating voltages of $3.3 \pm 0.3\text{V}$
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- Available in Pb-free and non Pb-free 54-pin TSOP II package and non Pb-free 60-ball fine pitch ball grid array (FBGA) package

Functional Description

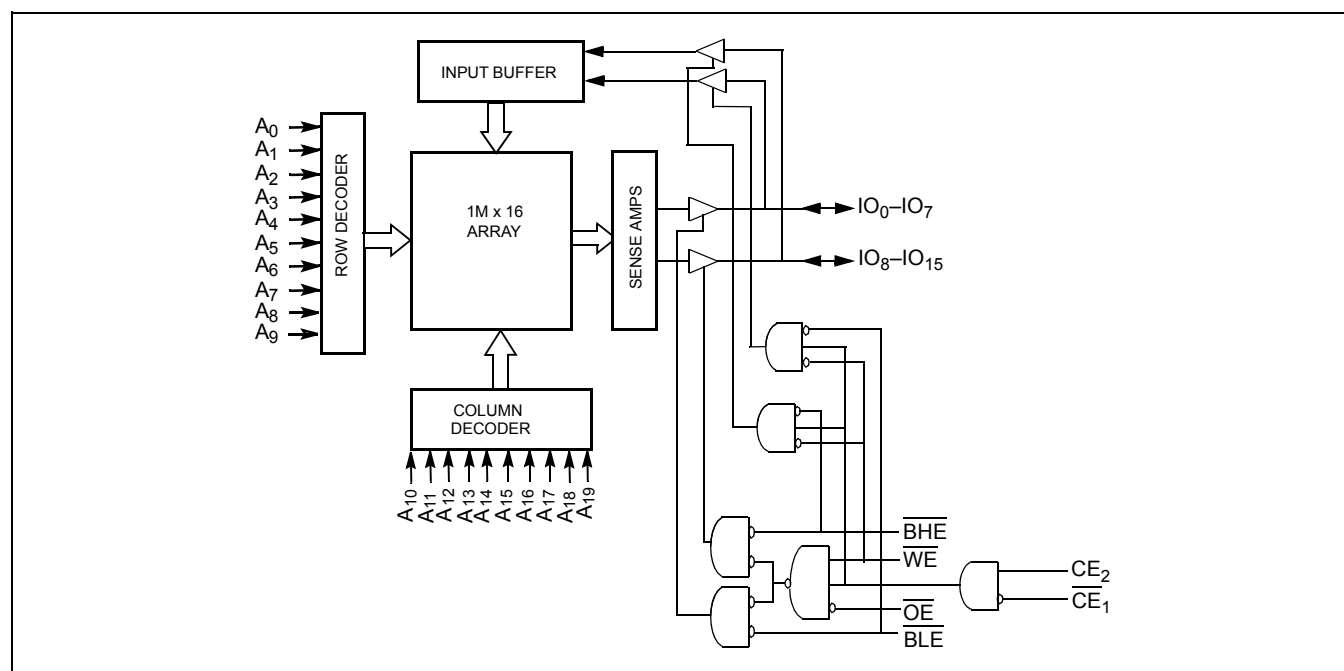
The CY7C1061AV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, enable the chip (\overline{CE}_1 LOW and CE_2 HIGH) while forcing the Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable (\overline{BHE}) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, enable the chip by taking \overline{CE}_1 LOW and CE_2 HIGH while forcing the Output Enable (\overline{OE}) LOW and the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on IO_0 to IO_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on IO_8 to IO_{15} . See "Truth Table" on page 7 for a complete description of Read and Write modes.

The input/output pins (IO_0 through IO_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH/ CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or a Write operation is in progress (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

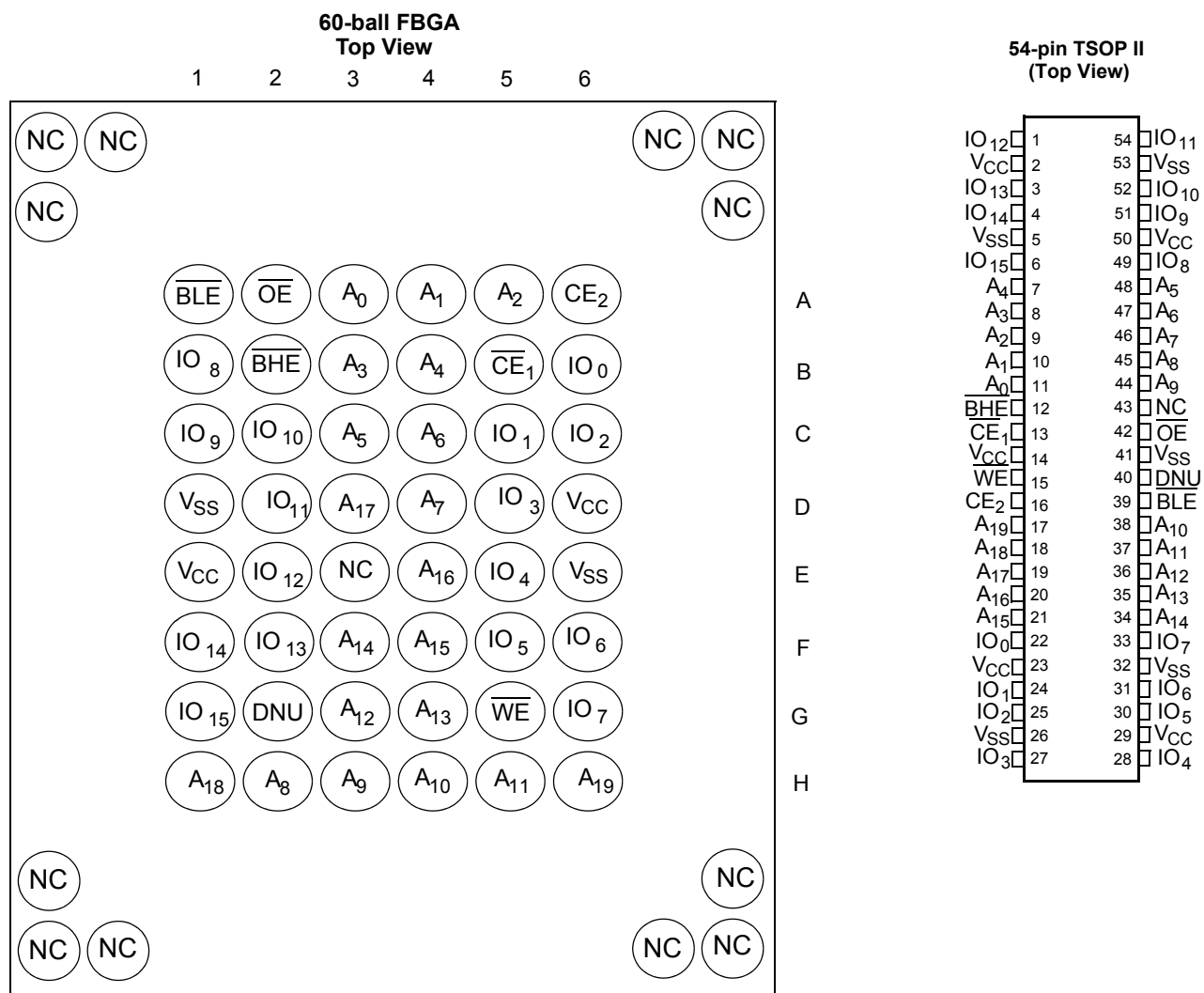
Logic Block Diagram



Selection Guide

| | | -10 | -12 | Unit |
|------------------------------|-----------------------|-----|-----|------|
| Maximum Access Time | | 10 | 12 | ns |
| Maximum Operating Current | Commercial | 275 | 260 | mA |
| | Industrial | 275 | 260 | |
| Maximum CMOS Standby Current | Commercial/Industrial | 50 | 50 | mA |

Pin Configurations ^[1, 2]



Notes

1. NC pins are not connected on the die.
2. DNU (Do Not Use) pins have to be left floating or tied to VSS to ensure proper operation.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND ^[3] ... -0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State ^[3] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage ^[3] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|-------------|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | |

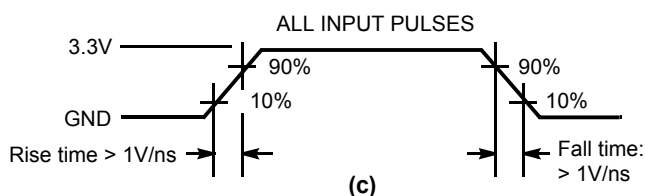
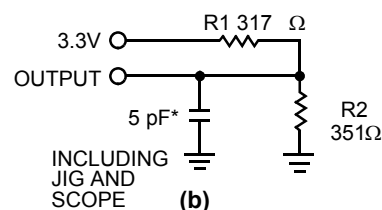
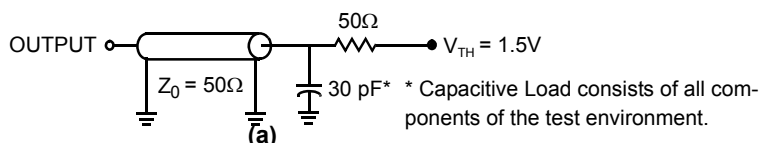
DC Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | -10 | | -12 | | Unit |
|-----------|---|---|---------------------------|----------------|------|----------------|------|
| | | | Min | Max | Min | Max | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | $V_{CC} + 0.3$ | 2.0 | $V_{CC} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ^[3] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IX} | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{max}$, $f = f_{\text{max}} = 1/t_{RC}$ | | 275 | | 260 | mA |
| | | | | 275 | | 260 | |
| I_{SB1} | Automatic CE Power-down Current — TTL Inputs | $CE_2 \leq V_{IL}$, max V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{\text{max}}$ | | 70 | | 70 | mA |
| I_{SB2} | Automatic CE Power-down Current — CMOS Inputs | $CE_2 \leq 0.3V$ max V_{CC} , $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$ | Commercial/ Industrial | 50 | | 50 | mA |

Capacitance ^[4]

| Parameter | Description | Test Conditions | TSOP II | FBGA | Unit |
|-----------|-------------------|--|---------|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3V$ | 6 | 8 | pF |
| C_{OUT} | IO Capacitance | | 8 | 10 | pF |

AC Test Loads and Waveforms ^[5]



Notes

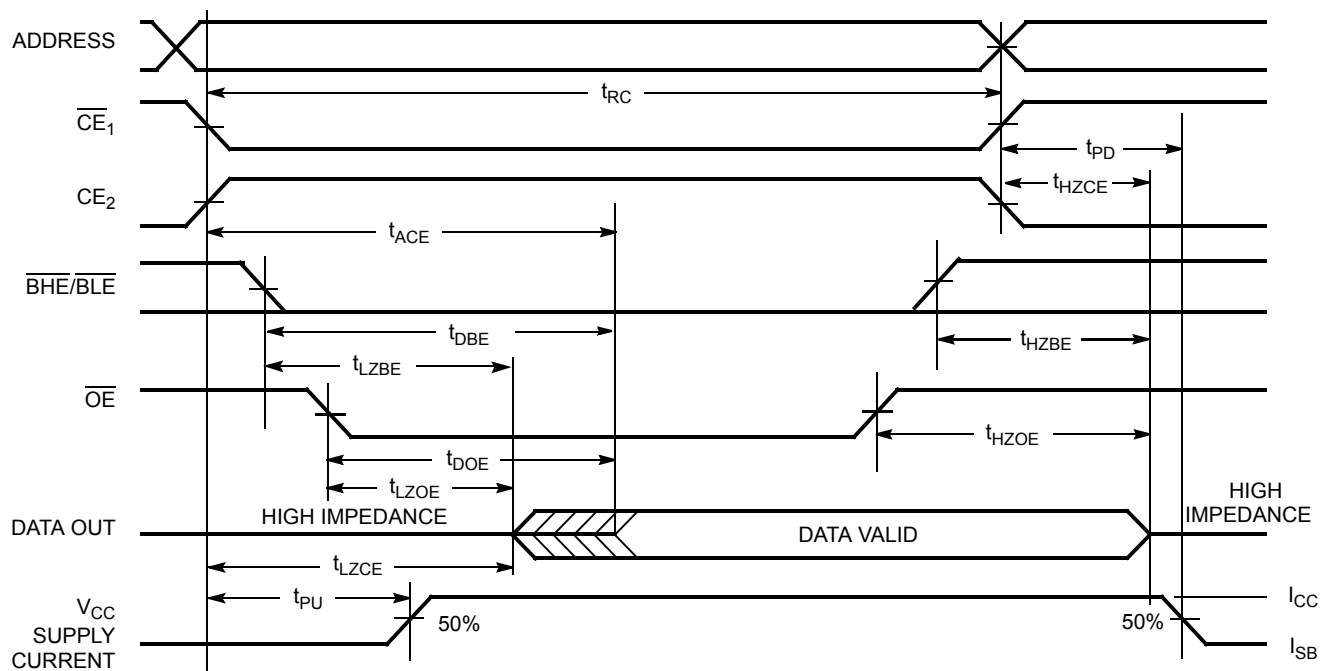
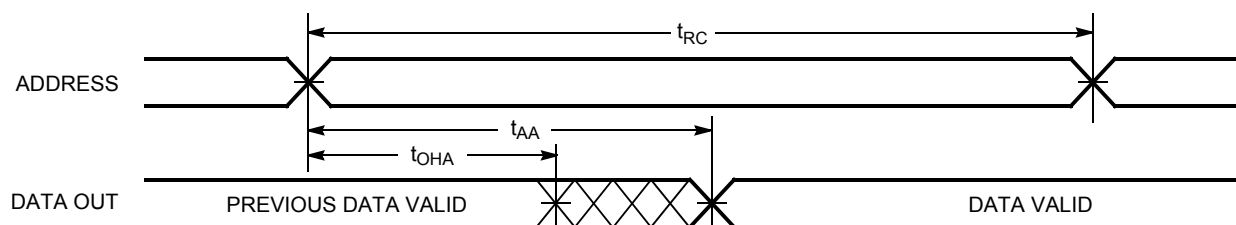
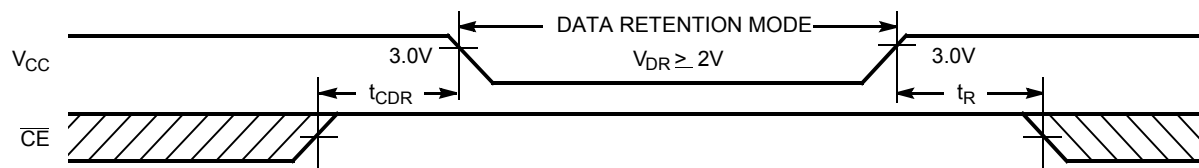
- V_{IL} (min) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1 ms (T_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR} , 2.0V) voltage.

AC Switching Characteristics (Over the Operating Range) ^[6]

| Parameter | Description | −10 | | −12 | | Unit |
|---------------------------------|---|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t _{power} | V _{CC} (typical) to the first access ^[7] | 1 | | 1 | | ms |
| t _{RC} | Read Cycle Time | 10 | | 12 | | ns |
| t _{AA} | Address to Data Valid | | 10 | | 12 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE}_1 LOW/CE ₂ HIGH to Data Valid | | 10 | | 12 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 5 | | 6 | ns |
| t _{LZOE} | \overline{OE} LOW to Low-Z | 1 | | 1 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High-Z ^[8] | | 5 | | 6 | ns |
| t _{LZCE} | \overline{CE}_1 LOW/CE ₂ HIGH to Low-Z ^[8] | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE}_1 HIGH/CE ₂ LOW to High-Z ^[8] | | 5 | | 6 | ns |
| t _{PU} | \overline{CE}_1 LOW/CE ₂ HIGH to Power Up ^[9] | 0 | | 0 | | ns |
| t _{PD} | \overline{CE}_1 HIGH/CE ₂ LOW to Power Down ^[9] | | 10 | | 12 | ns |
| t _{DBE} | Byte Enable to Data Valid | | 5 | | 6 | ns |
| t _{LZBE} | Byte Enable to Low-Z | 1 | | 1 | | ns |
| t _{HZBE} | Byte Disable to High-Z | | 5 | | 6 | ns |
| Write Cycle ^[10, 11] | | | | | | |
| t _{WC} | Write Cycle Time | 10 | | 12 | | ns |
| t _{SCE} | \overline{CE}_1 LOW/CE ₂ HIGH to Write End | 7 | | 8 | | ns |
| t _{AW} | Address Setup to Write End | 7 | | 8 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t _{SA} | Address Setup to Write Start | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 7 | | 8 | | ns |
| t _{SD} | Data Setup to Write End | 5.5 | | 6 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low-Z ^[8] | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High-Z ^[8] | | 5 | | 6 | ns |
| t _{BW} | Byte Enable to End of Write | 7 | | 8 | | ns |

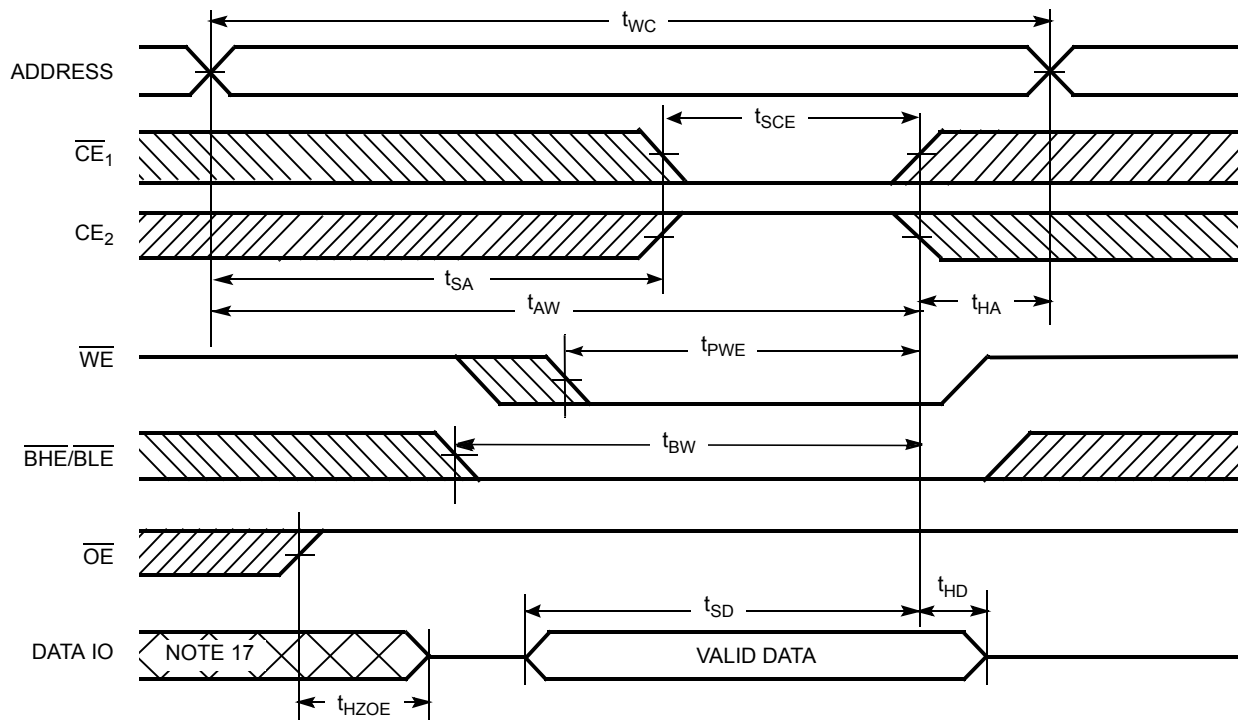
Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in (a) of the "AC Test Loads and Waveforms ^[5]" on page 3, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3V to 2V internally. t_{power} time must be provided initially before a Read/Write operation is started.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} and t_{LZOE} , t_{LZCE} , t_{LZWE} , t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of "AC Test Loads and Waveforms ^[5]" on page 3. Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of \overline{CE}_1 LOW (CE_2 HIGH) and \overline{WE} LOW. Chip enables must be active and \overline{WE} and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 2 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

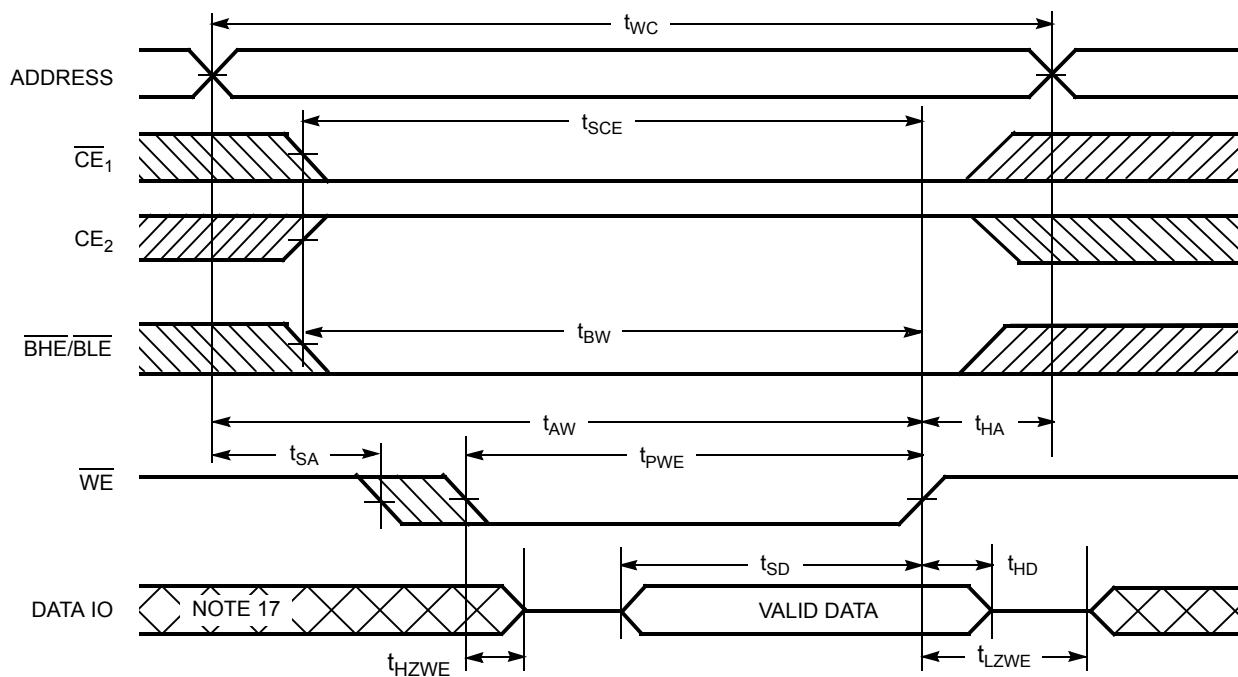


Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled) [15, 16]



Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) [15, 16]

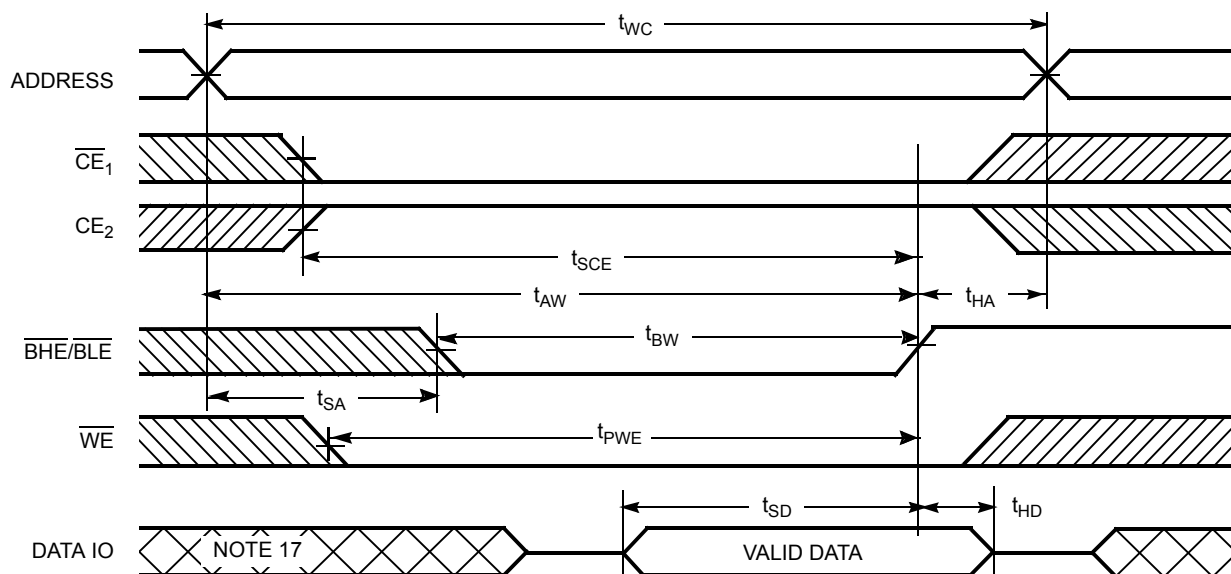


Notes

15. Data IO is high impedance if \overline{OE} , or \overline{BHE} or \overline{BLE} or both = V_{IH} .
16. If CE_1 goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
17. During this period, the IOs are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled)



Truth Table

| $\overline{\text{CE}}_1$ | $\overline{\text{CE}}_2$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{BLE}}$ | $\overline{\text{BHE}}$ | $\text{IO}_0\text{--}\text{IO}_7$ | $\text{IO}_8\text{--}\text{IO}_{15}$ | Mode | Power |
|--------------------------|--------------------------|------------------------|------------------------|-------------------------|-------------------------|-----------------------------------|--------------------------------------|----------------------------|-----------------------------|
| H | X | X | X | X | X | High-Z | High-Z | Power Down | Standby (I_{SB}) |
| X | L | X | X | X | X | High-Z | High-Z | Power Down | Standby (I_{SB}) |
| L | H | L | H | L | L | Data Out | Data Out | Read All Bits | Active (I_{CC}) |
| L | H | L | H | L | H | Data Out | High-Z | Read Lower Bits Only | Active (I_{CC}) |
| L | H | L | H | H | L | High-Z | Data Out | Read Upper Bits Only | Active (I_{CC}) |
| L | H | X | L | L | L | Data In | Data In | Write All Bits | Active (I_{CC}) |
| L | H | X | L | L | H | Data In | High-Z | Write Lower Bits Only | Active (I_{CC}) |
| L | H | X | L | H | L | High-Z | Data In | Write Upper Bits Only | Active (I_{CC}) |
| L | H | H | H | X | X | High-Z | High-Z | Selected, Outputs Disabled | Active (I_{CC}) |

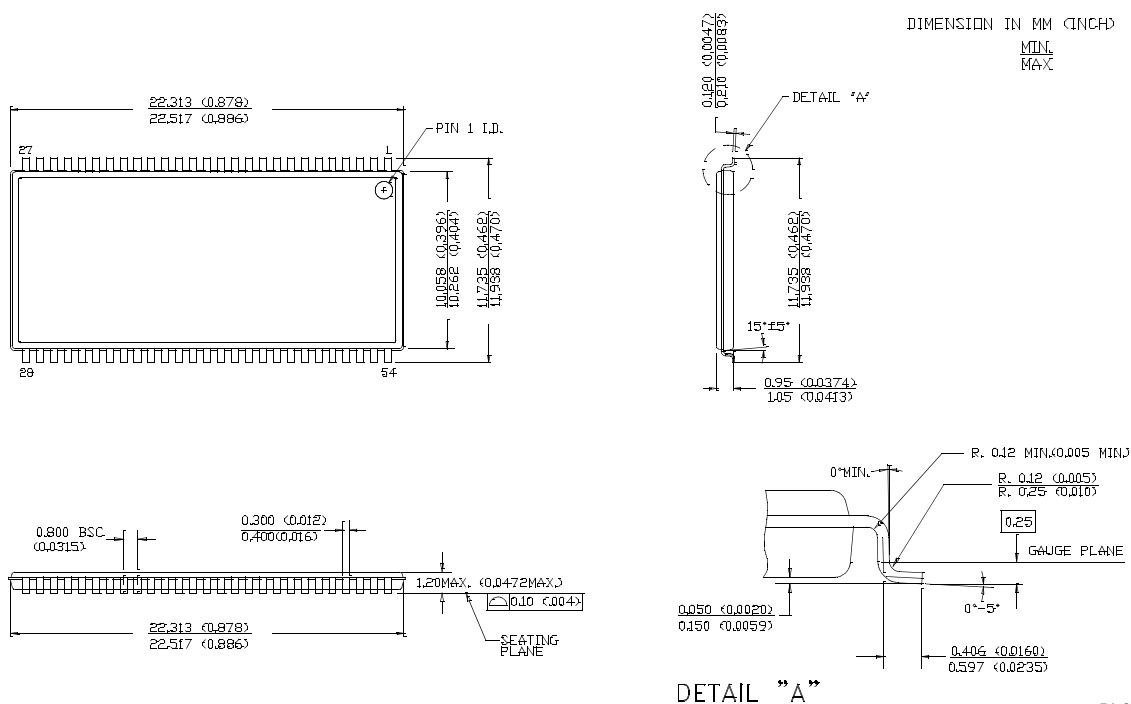
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|-----------------|--------------------------|-----------------|
| 10 | CY7C1061AV33-10ZXC | 51-85160 | 54-pin TSOP II (Pb-free) | Commercial |
| | CY7C1061AV33-10BAC | 51-85162 | 60-ball FBGA | |
| | CY7C1061AV33-10ZI | 51-85160 | 54-pin TSOP II | Industrial |
| | CY7C1061AV33-10ZXI | | 54-pin TSOP II (Pb-free) | |
| | CY7C1061AV33-10BAXI | 51-85162 | 60-ball FBGA (Pb-free) | |
| 12 | CY7C1061AV33-12ZC | 51-85160 | 54-pin TSOP II | Commercial |
| | CY7C1061AV33-12ZXC | | 54-pin TSOP II (Pb-free) | |
| | CY7C1061AV33-12BAC | 51-85162 | 60-ball FBGA | Industrial |
| | CY7C1061AV33-12ZXI | 51-85160 | 54-pin TSOP II (Pb-free) | |

Contact local Cypress representative for availability of the these parts.

Package Diagrams

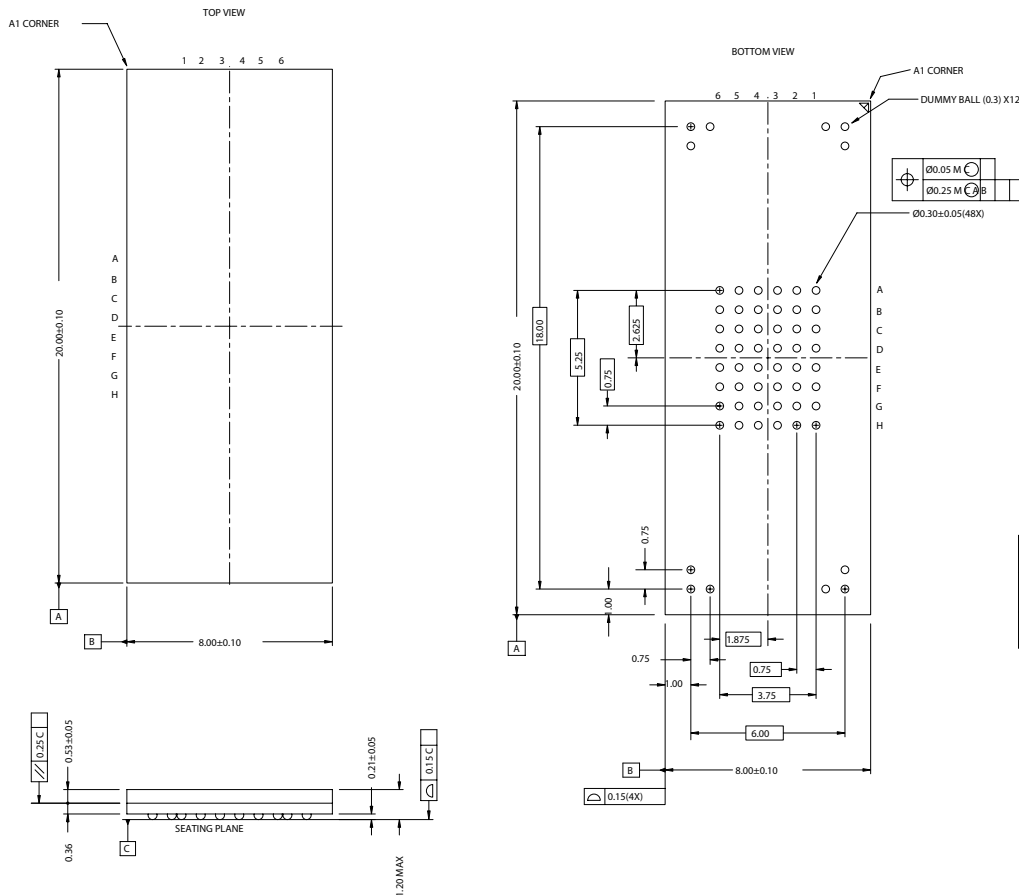
Figure 1. 54-pin TSOP II, 51-85160



51-85160-**

Package Diagrams (continued)

Figure 2. 60-ball FBGA (8 x 20 x 1.2 mm), 51-85162



51-85162-*D

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Document History Page

| Document Title: CY7C1061AV33 16-Mbit (1M x 16) Static RAM Document Number: 38-05256 | | | | |
|--|---------|------------|-----------------|--|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 113725 | 03/28/02 | NSL | New Data Sheet |
| *A | 117058 | 07/31/02 | DFP | Removed 15-ns bin |
| *B | 117989 | 08/30/02 | DFP | Added 8-ns bin Changed Icc for 8, 10, 12 bins t _{power} changed from 1 μ s to 1 ms. Load Cap Comment changed (for Tx line load) t _{SD} changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin numbers (t _{HZ} , t _{DOE} , t _{DBE}) Removed hz<lz comments from data sheet |
| *C | 120383 | 11/06/02 | DFP | Final data sheet Added note 3 to "AC Test Loads and Waveforms" and note 7 to t _{pu} and t _{pd} Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF |
| *D | 124439 | 2/25/03 | MEG | Changed ISB1 from 100 mA to 70 mA Shaded fBGA production ordering information |
| *E | 492137 | See ECN | NXR | Corrected Block Diagram on page #1 Removed 8 ns speed bin Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Included Note #1 and 2 on page #2 Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table |
| *F | 508117 | See ECN | NXR | Updated FBGA Pin Configuration Updated Ordering Information table |
| *G | 877322 | See ECN | VKN | Updated Ordering Information table |