

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 110 \text{ mA}$  at 10 ns
- Low CMOS standby power
  - $I_{SB2} = 20 \text{ mA}$
- 2.0V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 44-pin TSOP II package
- Offered in standard and high reliability (Q) grades

## Functional Description

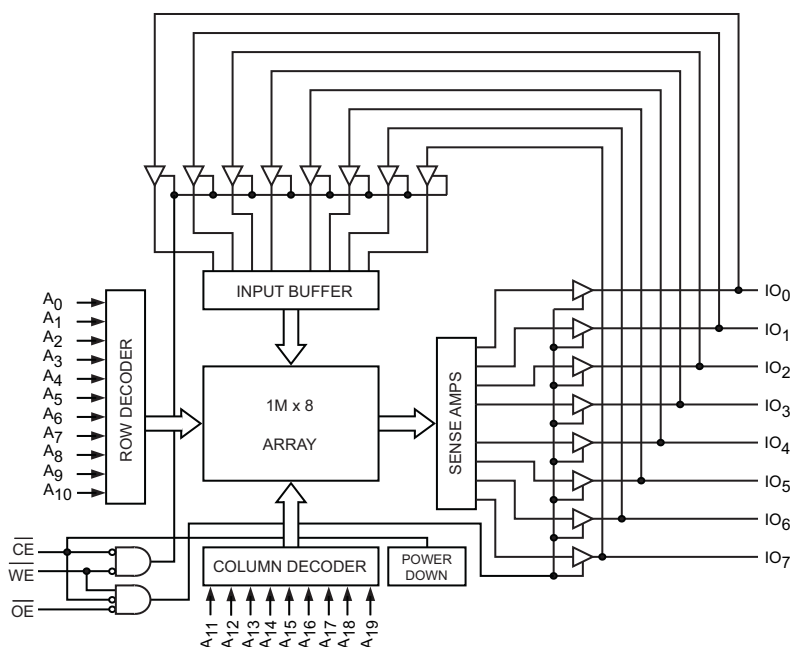
The CY7C1059DV33<sup>[1]</sup> is a high performance CMOS Static RAM organized as 1M words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight IO pins ( $IO_0$  through  $IO_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

The eight input or output pins ( $IO_0$  through  $IO_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY7C1059DV33 is available in 36-ball FBGA and 44-pin TSOP II packages with center power and ground (revolutionary) pinout.

## Logic Block Diagram

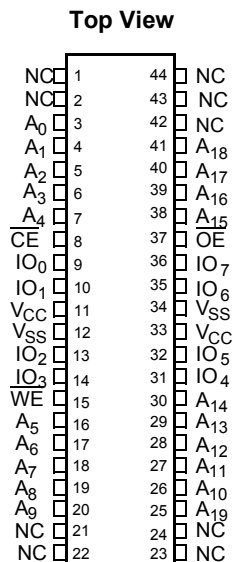


### Note

1. For guidelines about SRAM system design, refer to the Cypress application note [AN1064, SRAM System Guidelines](#) available at [www.cypress.com](http://www.cypress.com).

## Pin Configuration

Figure 1. 44-Pin TSOP II



## Selection Guide

Description	-10	-12	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	110	100	mA
Maximum CMOS Standby Current	20	20	mA

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> ..... -0.5V to + 4.6V

DC Voltage Applied to Outputs  
in High-Z State<sup>[2]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

DC Input Voltage<sup>[2]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V  
(MIL-STD-883, Method 3015)

Latch up Current..... >200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40°C to +85°C	3.3V ± 0.3V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		Unit
			Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$		110		100	mA
$I_{SB1}$	Automatic CE Power Down Current — TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		40		35	mA
$I_{SB2}$	Automatic CE Power Down Current — CMOS Inputs	Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V, f = 0$		20		20	mA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.]

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 3.3V$	12	pF
$C_{OUT}$	IO Capacitance		12	pF

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.43	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		15.8	°C/W

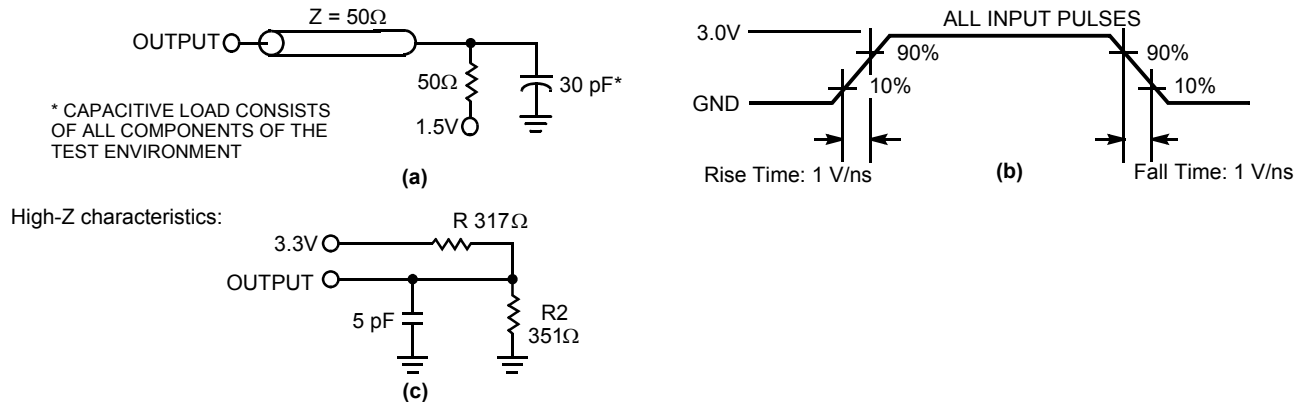
### Notes

- $V_{IL(\text{min})} = -2.0V$  and  $V_{IH(\text{max})} = V_{CC} + 2V$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

**Figure 2. AC Test Loads and Waveforms**

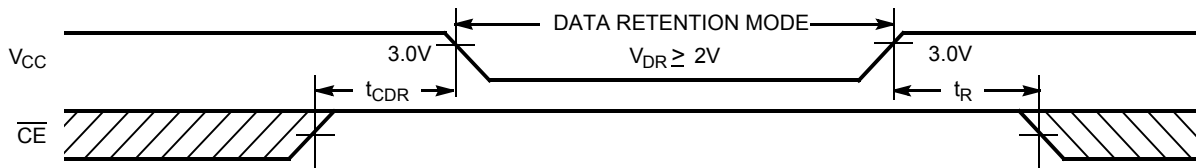


## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[4]</sup>	Min	Max	Unit
$V_{\text{DR}}$	$V_{\text{CC}}$ for Data Retention		2.0		V
$I_{\text{CCDR}}$	Data Retention Current	$V_{\text{CC}} = V_{\text{DR}} = 2.0\text{V}$ , $\overline{\text{CE}} \geq V_{\text{CC}} - 0.3\text{V}$ , $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$ or $V_{\text{IN}} \leq 0.3\text{V}$		20	mA
$t_{\text{CDR}}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_{\text{R}}^{[5]}$	Operation Recovery Time		$t_{\text{RC}}$		ns

**Figure 3. Data Retention Waveform**



### Notes

- No inputs may exceed  $V_{\text{CC}} + 0.3\text{V}$ .
- Full device operation requires linear  $V_{\text{CC}}$  ramp from  $V_{\text{DR}}$  to  $V_{\text{CC}(\text{min})} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{\text{CC}(\text{min})} \geq 50\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range<sup>[6]</sup>

Parameter	Description	−10		−12		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>power</sub> <sup>[7]</sup>	V <sub>CC</sub> (typical) to the First Access	100		100		μs
t <sub>RC</sub>	Read Cycle Time	10		12		ns
t <sub>AA</sub>	Address to Data Valid		10		12	ns
t <sub>OHA</sub>	Data Hold from Address Change	2.5		2.5		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		10		12	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		5		6	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low-Z	0		0		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High-Z <sup>[8, 9]</sup>		5		6	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low-Z <sup>[9]</sup>	3		3		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High-Z <sup>[8, 9]</sup>		5		6	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power up	0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power down		10		12	ns
Write Cycle <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	10		12		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	7		8		ns
t <sub>AW</sub>	Address Setup to Write End	7		8		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	7		8		ns
t <sub>SD</sub>	Data Setup to Write End	5		6		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[9]</sup>	3		3		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High-Z <sup>[8, 9]</sup>		5		6	ns

### Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.

7.  $t_{\text{POWER}}$  is the minimum amount of time that the power supply must be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.

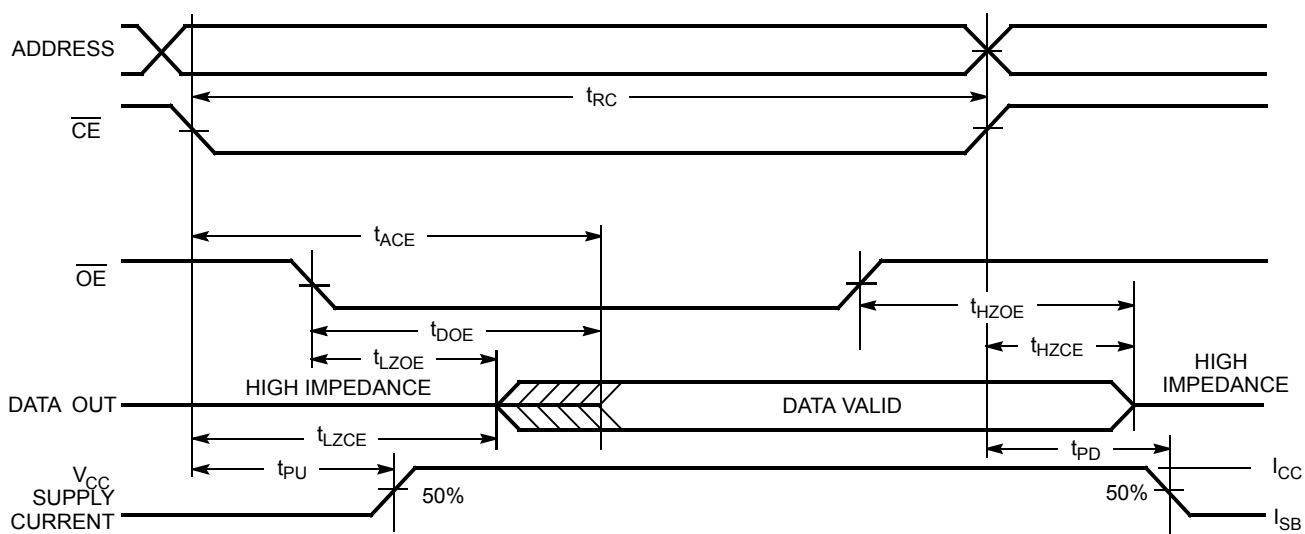
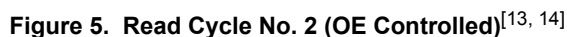
8.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 4. Transition is measured when the outputs enter a high impedance state.

9. At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.

10. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the Write.

11. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

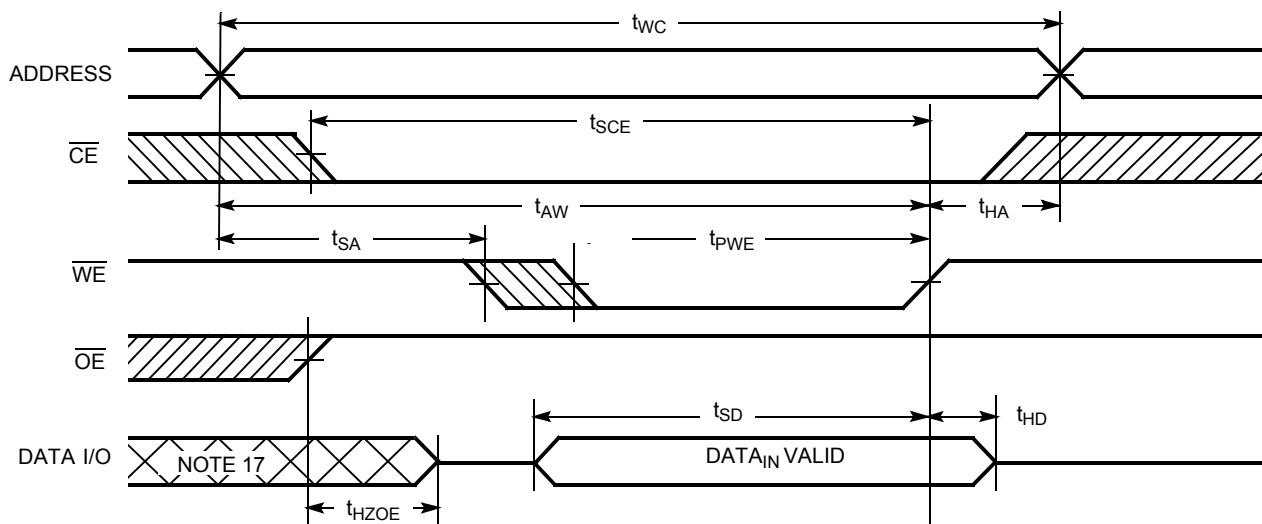
**Figure 4. Read Cycle No. 1 (Address Transition Controlled)<sup>[12, 13]</sup>**



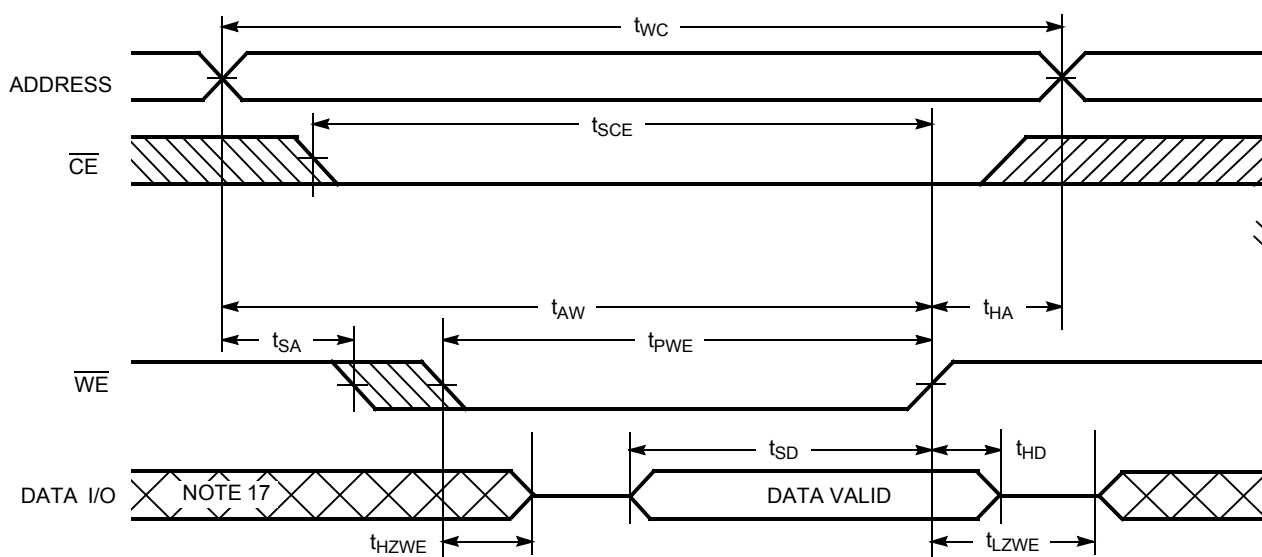
12.  $\overline{\text{OE}}$  is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$ .  
13.  $\overline{\text{WE}}$  is HIGH for Read cycle.  
14. Address valid before or coincident with  $\overline{\text{CE}}$  transition LOW.

## Switching Waveforms(continued)

**Figure 6. Write Cycle No. 1 (WE Controlled, OE High During Write)<sup>[15, 16]</sup>**



**Figure 7. Write Cycle No. 2 (WE Controlled, OE Low)<sup>[16]</sup>**



### Notes

15. Data IO is high-impedance if  $\overline{OE} = V_{IH}$ .

16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

17. During this period the IOs are in the output state and input signals must not be applied.

## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$IO_0$ - $IO_7$	Mode	Power
H	X	X	High-Z	Power Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

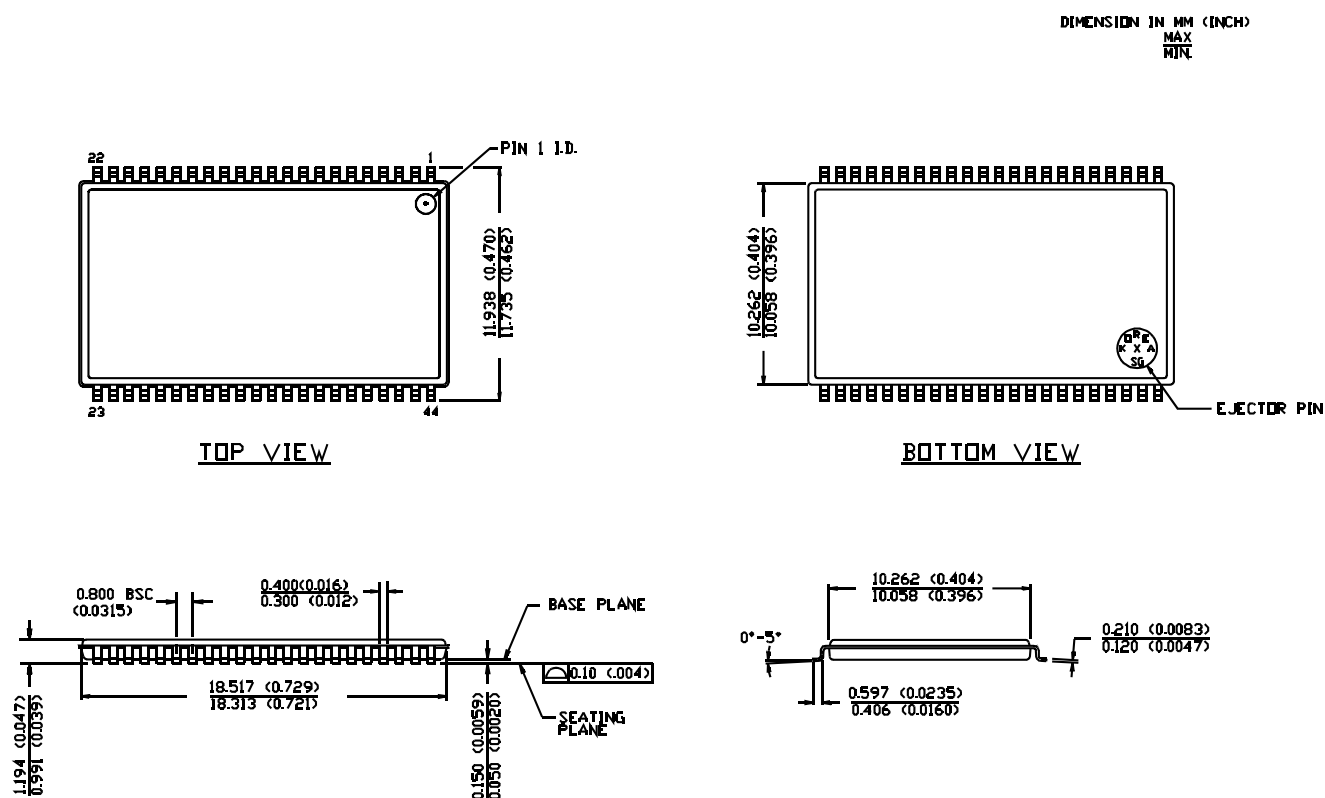
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range	Grade
10	CY7C1059DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial	Standard
12	CY7C1059DV33-12ZSXQ	51-85087	44-pin TSOP II (Pb-Free)	Industrial	High reliability (< 100 ppm)
	CY7C1059DV33-12ZSXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial	Standard

Contact your local Cypress sales representative for availability of these parts.

## Package Diagrams

Figure 8. 44-Pin TSOP II (51-85087)





## Document History Page

Document Title: CY7C1059DV33, 8-Mbit (1M x 8) Static RAM Document Number: 001-00061				
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	342195	PCI	See ECN	New Data Sheet
*A	380574	SYT	See ECN	Redefined $I_{CC}$ values for Com'I and Ind'I temperature ranges $I_{CC}$ (Com'I): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively $I_{CC}$ (Ind'I): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively Changed the Capacitance values from 8 pF to 10 pF on Page # 3
*B	485796	NXR	See ECN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -8 and -12 Speed bins from product offering, Removed Commercial Operating Range option, Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$ Updated footnote #7 on High-Z parameter measurement Added footnote #11 Changed the Description of $I_{IX}$ from Input Load Current to Input Leakage Current. Updated the Ordering Information table and Replaced Package Name column with Package Diagram.
*C	1513285	VKN/AESA	See ECN	Converted from preliminary to final Added 12 ns speed bin Changed $C_{IN}$ and $C_{OUT}$ specs from 16 pF to 12 pF Changed $t_{OHA}$ spec from 3 ns to 2.5 ns Updated Ordering information table
*D	2594352	NXR/PYRS	10/21/08	Added Q-Grade part
*E	2764423	AJU	09/16/2009	Corrected typo in the ordering information table

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