CY7C0837AV, CY7C0830AV
CY7C0831AV, CY7C0832AV
CY7C0832BV, CY7C0833AV

FLEx18™ 3.3V 64K/128K x 36 and 128K/256K x 18 Synchronous Dual-Port RAM

Features

- True Dual-Ported Memory Cells that Allow Simultaneous Access of the Same Memory Location
- Synchronous Pipelined Operation
- Family of 512 Kbit, 1 Mbit, 2 Mbit, 4 Mbit, and 9 Mbit Devices
- Pipelined Output Mode Allows Fast Operation
- 0.18 micron CMOS for Optimum Speed and Power
- High Speed Clock to Data Access
- 3.3V Low Power
  - Active as Low as 225 mA (typ)
  - Standby as Low as 55 mA (typ)
- Mailbox Function for Message Passing
- Global Master Reset
- Separate Byte Enables on Both Ports
- Commercial and Industrial Temperature Ranges
- IEEE 1149.1 Compatible JTAG Boundary Scan
- 144-Ball FBGA (13 mm × 13 mm) (1.0 mm pitch)
- 120 TQFP (14 mm x 14 mm x 1.4 mm)
- Pb-Free Packages Available
- Counter Wrap Around Control
  - Internal Mask Register Controls Counter Wrap Around
  - Counter-Interrupt Flags to Indicate Wrap Around
  - Memory Block Retransmit Operation
- Counter Readback on Address Lines
- Mask Register Readback on Address Lines
- Dual Chip Enables on Both Ports for Easy Depth Expansion

Functional Description

The FLEx18™ family includes 512 Kbit, 1 Mbit, 2 Mbit, 4 Mbit, and 9 Mbit pipelined, synchronous, true dual port static RAMs that are high speed, low power 3.3V CMOS. Two ports are provided, permitting independent, simultaneous access to any location in memory. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal setup and hold time.

During a Read operation, data is registered for decreased cycle time. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address, the counter increments the address internally (more details to follow). The internal Write pulse width is independent of the duration of the R/$\overline{W}$ input signal. The internal Write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle powers down the internal circuitry to reduce the static power consumption. One cycle with chip enables asserted is required to reactivate the outputs.

Additional features include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap around, counter interrupt ($\overline{CNTINT}$) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, $\overline{JTAG}$ for boundary scan, and asynchronous Master Reset ($\overline{MRST}$).

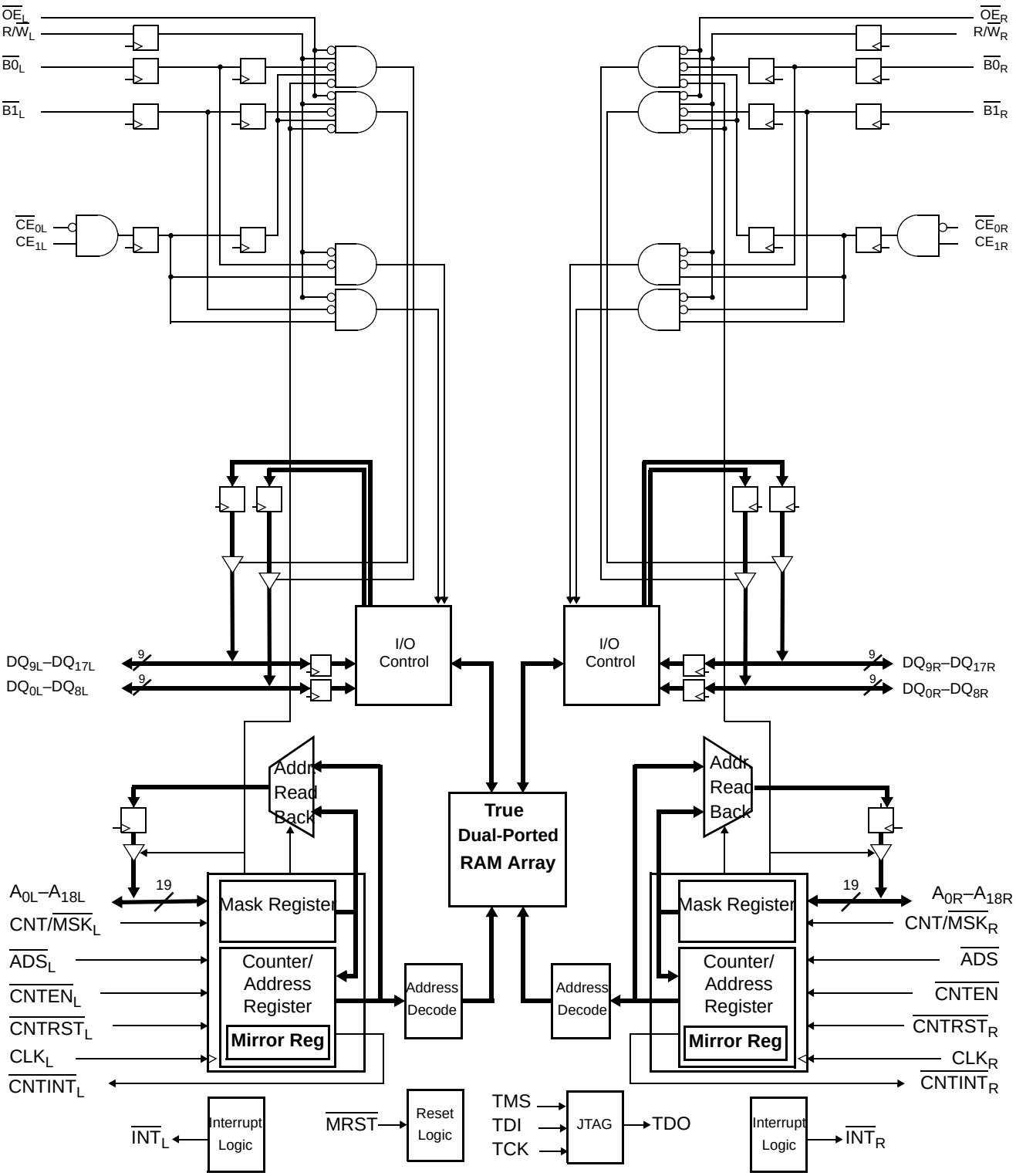
The CY7C0833AV device in this family has limited features. See Address Counter and Mask Register Operations [16] on page 6 for details.

Table 1. Product Selection Guide

Density	512 Kbit (32K x 18)	1 Mbit (64K x 18)	2 Mbit (128K x 18)	4 Mbit (256K x 18)		9 Mbit (512K x 18)
Part Number	CY7C0837AV	CY7C0830AV	CY7C0831AV	CY7C0832AV	CY7C0832BV [1]	CY7C0833AV
Maximum Speed (MHz)	167	167	167	167	133	133
Maximum Access Time - Clock to Data (ns)	4.0	4.0	4.0	4.0	4.4	4.7
Typical Operating Current (mA)	225	225	225	225	225	270
Package	144 FBGA	120 TQFP 144 FBGA	120 TQFP 144 FBGA	120 TQFP 144 FBGA	120 TQFP	144 FBGA

Note
1. CY7C0832AV and CY7C0832BV are functionally identical.

Logic Block Diagram [2]



Note
2. CY7C0837AV has 15 address bits, CY7C0830AV has 16 address bits, CY7C0831AV has 17 address bits, CY7C0832AV/CY7C0832BV has 18 address bits and CY7C0833AV has 19 address bits.

Pin Configurations

Figure 1. 144-Ball BGA (Top View)

CY7C0837AV / CY7C0830AV / CY7C0831AV / CY7C0832AV / CY7C0833AV

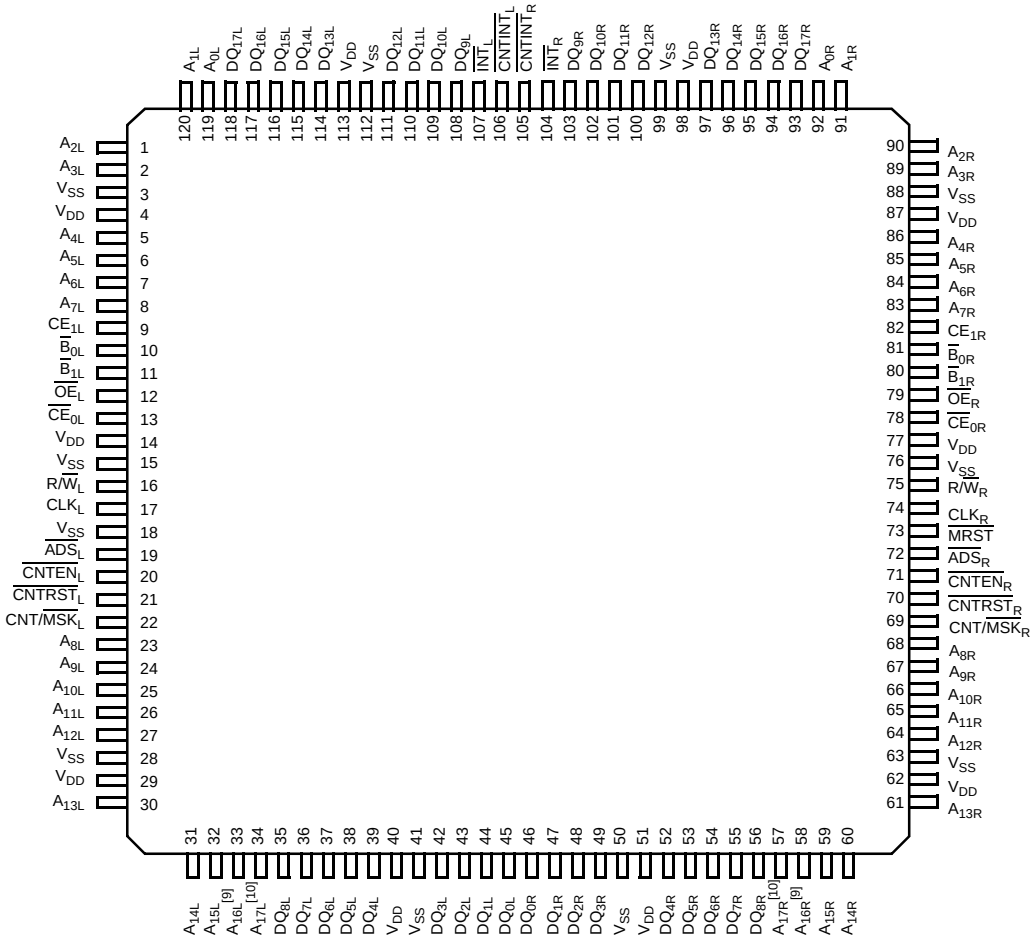
	1	2	3	4	5	6	7	8	9	10	11	12
A	$DQ17_L$	$DQ16_L$	$DQ14_L$	$DQ12_L$	$DQ10_L$	$DQ9_L$	$DQ9_R$	$DQ10_R$	$DQ12_R$	$DQ14_R$	$DQ16_R$	$DQ17_R$
B	$A0_L$	$A1_L$	$DQ15_L$	$DQ13_L$	$DQ11_L$	$\overline{MRST}$	NC	$DQ11_R$	$DQ13_R$	$DQ15_R$	$A1_R$	$A0_R$
C	$A2_L$	$A3_L$	$CE1_L$ [7]	$\overline{INT}_L$	$\overline{CNTINT}_L$ [9]	$\overline{ADS}_L$ [8]	$\overline{ADS}_R$ [8]	$\overline{CNTINT}_R$ [9]	$\overline{INT}_R$	$CE1_R$ [7]	$A3_R$	$A2_R$
D	$A4_L$	$A5_L$	$\overline{CE0}_L$ [8]	NC	VDD	VDD	VDD	VDD	NC	$\overline{CE0}_R$ [8]	$A5_R$	$A4_R$
E	$A6_L$	$A7_L$	$\overline{B1}_L$	NC	VDD	VSS	VSS	VDD	NC	$\overline{B1}_R$	$A7_R$	$A6_R$
F	$A8_L$	$A9_L$	C_L	NC	VSS	VSS	VSS	VSS	NC	C_R	$A9_R$	$A8_R$
G	$A10_L$	$A11_L$	$\overline{B0}_L$	NC	VSS	VSS	VSS	VSS	NC	$\overline{B0}_R$	$A11_R$	$A10_R$
H	$A12_L$	$A13_L$	$\overline{OE}_L$	NC	VDD	VSS	VSS	VDD	NC	$\overline{OE}_R$	$A13_R$	$A12_R$
J	$A14_L$	$A15_L$ [3]	$R\overline{W}_L$	NC	VDD	VDD	VDD	VDD	NC	$R\overline{W}_R$	$A15_R$ [3]	$A14_R$
K	$A16_L$ [4]	$A17_L$ [5]	$CNT/\overline{MSK}_L$ [7]	TDO	$\overline{CNTRST}_L$ [7]	TCK	TMS	$\overline{CNTRST}_R$ [7]	TDI	$CNT/\overline{MSK}_R$ [7]	$A17_R$ [5]	$A16_R$ [4]
L	$A18_L$ [6]	NC	$DQ6_L$	$DQ4_L$	$DQ2_L$	$\overline{CNTEN}_L$ [8]	$\overline{CNTEN}_R$ [8]	$DQ2_R$	$DQ4_R$	$DQ6_R$	NC	$A18_R$ [6]
M	$DQ8_L$	$DQ7_L$	$DQ5_L$	$DQ3_L$	$DQ1_L$	$DQ0_L$	$DQ0_R$	$DQ1_R$	$DQ3_R$	$DQ5_R$	$DQ7_R$	$DQ8_R$

Notes
3. Leave this ball unconnected for CY7C0837AV.
4. Leave this ball unconnected for CY7C0837AV and CY7C0830AV.
5. Leave this ball unconnected for CY7C0837AV, CY7C0830AV and CY7C0831AV.
6. Leave this ball unconnected for CY7C0837AV, CY7C0830AV, CY7C0831AV, and CY7C0832AV.
7. These balls are not applicable for CY7C0833AV device. They must be tied to VDD.
8. These balls are not applicable for CY7C0833AV device. They must be tied to VSS.
9. These balls are not applicable for CY7C0833AV device. They must not be connected.

Pin Configurations

Figure 2. 120-Pin Thin Quad Flat Pack (TQFP) (Top View)

CY7C0830AV / CY7C0831AV / CY7C0832AV / CY7C0832BV



Notes
10. Leave this pin unconnected for CY7C0830AV.
11. Leave this pin unconnected for CY7C0830AV and CY7C0831AV.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{18L}[2]	A_{0R}–A_{18R}[2]	**Address Inputs**.
ADS_L[8]	ADS_R[8]	**Address Strobe Input**. Used as an address qualifier. This signal should be asserted LOW for the part using the externally supplied address on the address pins and for loading this address into the burst address counter.
$\overline{CE0_L}$[8]	$\overline{CE0_R}$[8]	**Active LOW Chip Enable Input**.
$CE1_L$[7]	$CE1_R$[7]	**Active HIGH Chip Enable Input**.
CLK_L	CLK_R	**Clock Signal**. Maximum clock input rate is f_{MAX}.
$CNTEN_L$[8]	$CNTEN_R$[8]	**Counter Enable Input**. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. The increment is disabled if ADS or CNTRST are asserted LOW.
$CNTRST_L$[7]	$CNTRST_R$[7]	**Counter Reset Input**. Asserting this signal LOW resets to zero the unmasked portion of the burst address counter of its respective port. CNTRST is not disabled by asserting ADS or CNTEN.
CNT/$\overline{MSK_L}$[7]	CNT/$\overline{MSK_R}$[7]	**Address Counter Mask Register Enable Input**. Asserting this signal LOW enables access to the mask register. When tied HIGH, the mask register is not accessible and the address counter operations are enabled based on the status of the counter control signals.
DQ_{0L}–DQ_{17L}	DQ_{0R}–DQ_{17R}	**Data Bus Input/Output**.
$\overline{OE_L}$	$\overline{OE_R}$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INTL}$	$\overline{INTR}$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations are used for message passing. $\overline{INT_L}$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$CNTINT_L$[9]	$\overline{CNTINT_R}$[9]	**Counter Interrupt Output**. This pin is asserted LOW when the unmasked portion of the counter is incremented to all '1s.'
R/$\overline{W_L}$	R/$\overline{W_R}$	**Read/Write Enable Input**. Assert this pin LOW to write to, or HIGH to Read from the dual port memory array.
$\overline{B_{0L}}$–$\overline{B_{1L}}$	$\overline{B_{0R}}$–$\overline{B_{1R}}$	**Byte Select Inputs**. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting MRST LOW performs all of the reset functions as described in the text. A MRST operation is required at power up.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TDI		**JTAG Test Data Input**. Data on the TDI input is shifted serially into selected registers.
TCK		**JTAG Test Clock Input**.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP.
V_{SS}		**Ground Inputs**.
V_{DD}		**Power Inputs**.

Byte Select Operation

Control Pin	Effect
$\overline{B_0}$	$DQ_{0–8}$ Byte Control
$\overline{B_1}$	$DQ_{9–17}$ Byte Control

Master Reset

The FLEx18 family devices undergo a complete reset by taking its MRST input LOW. The MRST input can switch asynchronously to the clocks. An MRST initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). MRST also forces the Mailbox Interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH. MRST must be performed on the FLEx18 family devices after power up.

Mailbox Interrupts

The upper two memory locations may be used for message passing and permit communications between ports. Table 2 shows the interrupt operation for both ports of CY7C0833AV. The highest memory location, 7FFFF is the mailbox for the right port and 7FFFE is the mailbox for the left port. Table 2 shows that to set the INT_R flag, a Write operation by the left port to address 7FFFF asserts INT_R LOW. At least one byte has to be active for a Write to generate an interrupt. A valid Read of the 7FFFF location by the right port resets INT_R HIGH. At least one byte must be active for a Read to reset the interrupt. When one port Writes to the other port's mailbox, the INT of the port that the mailbox belongs to is asserted LOW. The INT is reset when the owner (port) of the mailbox Reads the contents of the mailbox. The interrupt flag is set in a flow-through mode (that is, it follows the clock edge of the writing port). Also, the flag is reset in a flow-through mode (that is, it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. And each port can write to its own mailbox without setting the interrupt. If an application does not require message passing, INT pins should be left open.

Address Counter and Mask Register Operations [16]

This section describes the features only apply to 512 Kbit,1 Mbit, 2 Mbit, and 4 Mbit devices. It does not apply to 9 Mbit device. Each port of these devices has a programmable burst address counter. The burst counter contains three registers: a counter register, a mask register, and a mirror register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Counter Load, Increment, Counter Reset, and by master reset (MRST) operations.

The **mask register** value affects the Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is changed only by the Mask Load and Mask Reset operations and by the MRST. The mask register defines the counting range of the counter register. It divides the counter register into two regions: zero or more '0s' in the most significant bits define the masked region, one or more '1s' in the least significant bits define the unmasked region. Bit 0 may also be '0,' masking the least significant counter bit and causing the counter to increment by two instead of one.

The mirror register is used to reload the counter register on increment operations (see Retransmit on page 8). It always contains the value last loaded into the counter register, and is changed only by the Counter Load, and by the MRST instructions. Table 3 on page 7 summarizes the operation of these registers and the required input control signals. The MRST control signal is asynchronous. All the other control signals in Table 3 on page 7 (CNT/MSK, CNTRST, ADS, CNTEN) are synchronized to the port's CLK. All these counter and mask operations are independent of the port's chip enable inputs (CE0 and CE1).

Counter enable ($\overline{CNTEN}$) inputs are provided to stall the operation of the address input and use the internal address generated by the internal counter for fast, interleaved memory applications. A port's burst counter is loaded when the port's address strobe (ADS) and CNTEN signals are LOW. When the port's CNTEN is asserted and the ADS is deasserted, the address counter increments on each LOW to HIGH transition of that port's clock signal. This reads and writes one word from and to each successive address location until CNTEN s deasserted. The counter can address the entire memory array, and loops back to the start. Counter reset ($\overline{CNTRST}$) is used to reset the unmasked portion of the burst counter to I/0s. A counter-mask register is used to control the counter wrap.

Table 2. Interrupt Operation Example [2, 12, 13, 14, 15, 17]

FUNCTION	LEFT PORT				RIGHT PORT			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L}–A_{18L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R}–A_{18R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	3FFFF	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	3FFFF	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	3FFFE	X
Reset Left $\overline{INT}_L$ Flag	H	L	3FFFE	H	X	X	X	X
Set Right $\overline{INT}_R$ Flag	L	L	3FFFF	X	X	X	X	L

Notes
12. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data is out after the following CLK edge and is three-stated after the next CLK edge.
13. $\overline{OE}$ is "Don't Care" for mailbox operation.
14. At least one of $\overline{BE0}$, $\overline{BE1}$ must be LOW.
15. A18x is a NC for CY7C0832AV/CY7C0832BV, therefore the Interrupt Addresses are 3FFFF and 3FFFE. A18x and A17x are NC for CY7C0831AV, therefore the Interrupt addresses are 1FFFF and 1FFFE; A18x, A17x and A16x are NC for CY7C0830AV, therefore the Interrupt Addresses are FFFF and FFFE;A18x, A17x, A16x and A15x are NC for CY7C0837AV, therefore the Interrupt Addresses are 7FFF and 7FFE.
16. This section describes the CY7C0832AV/CY7C0832BV, CY7C0831AV, CY7C0830AV and CY7C0837AV having 18, 17, 16 and 15 address bits.
17. "X" = "Don't Care," "H" = HIGH, "L" = LOW.

Counter Reset Operation

All unmasked bits of the counter are reset to ‘0.’ All masked bits remain unchanged. The mirror register is loaded with the value of the burst counter. A Mask Reset followed by a Counter Reset resets the counter and mirror registers to 00000, as does master reset (MRST).

Counter Load Operation

The address counter and mirror registers are both loaded with the address value presented at the address lines.

Counter Increment Operation

When the address counter register is initially loaded with an external address, the counter can internally increment the address value, potentially addressing the entire memory array. Only the unmasked bits of the counter register are incremented. The corresponding bit in the mask register must be a ‘1’ for a counter bit to change. The counter register is incremented by 1 if the least significant bit is unmasked, and by 2 if it is masked. If all unmasked bits are ‘1,’ the next increment wraps the counter back to the initially loaded value. If an Increment results in all the unmasked bits of the counter being ‘1s,’ a counter interrupt flag ($\overline{\text{CNTINT}}$) is asserted. The next Increment returns the counter register to its initial value, which was stored in the mirror register. The counter address can instead be forced to loop to 00000 by externally connecting $\overline{\text{CNTINT}}$ to $\overline{\text{CNTRST}}$.[19] An increment that results in one or more of the unmasked bits of the counter being ‘0’ deasserts the counter interrupt flag. The example in Figure 4 on page 10 shows the counter mask register loaded with a mask value of 0003Fh unmasking the first 6 bits with bit ‘0’ as the LSB and bit ‘16’ as the MSB. The maximum value the mask register can be loaded with is 3FFFFh. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 8h. The base address bits (in this case, the 6th address through the 16th address) are loaded with an address value but do not increment after the counter is configured for increment operation. The counter address starts at address 8h. The counter increments its internal address value until it reaches the mask register value of 3Fh. The counter wraps around the memory block to location 8h at the next count. $\overline{\text{CNTINT}}$ is issued when the counter reaches its maximum value

Counter Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Counter Interrupt

The counter interrupt ($\overline{\text{CNTINT}}$) is asserted LOW when an increment operation results in the unmasked portion of the counter register being all ‘1s.’ It is deasserted HIGH when an Increment operation results in any other value. It is also de-asserted by Counter Reset, Counter Load, Mask Reset and Mask Load operations, and by $\overline{\text{MRST}}$.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. Readback is pipelined; the address is valid t_{CA2} after the next rising edge of the port’s clock. If address readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) are three-stated. Figure 3 on page 9 shows a block diagram of the operation.

Table 3. Address Counter and Counter-Mask Register Control Operation (Any Port) [17, 18]

CLK	$\overline{\text{MRST}}$	CNT/$\overline{\text{MSK}}$	$\overline{\text{CNTRST}}$	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	Operation	Description
X	L	X	X	X	X	Master Reset	Reset address counter to all 0s and mask register to all 1s.
⎍	H	H	L	X	X	Counter Reset	Reset counter unmasked portion to all 0s.
⎍	H	H	H	L	L	Counter Load	Load counter with external address value presented on address lines.
⎍	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	H	H	L	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	L	L	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	L	H	L	L	Mask Load	Load mask register with value presented on the address lines.
⎍	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	L	H	H	X	Reserved	Operation undefined

Notes
18. Counter operation and mask register operation is independent of chip enables.
19. $\overline{\text{CNTINT}}$ and $\overline{\text{CNTRST}}$ specs are guaranteed by design to operate properly at speed grade operating frequency when tied together.

Retransmit

Retransmit is a feature that allows the Read of a block of memory more than once without the need to reload the initial address. This eliminates the need for external logic to store and route data. It also reduces the complexity of the system design and saves board space. An internal mirror register is used to store the initially loaded address counter value. When the counter unmasked portion reaches its maximum value set by the mask register, it wraps back to the initial value stored in this mirror register. If the counter is continuously configured in increment mode, it increments again to its maximum value and wraps back to the value initially stored into the mirror register. Thus, the repeated access of the same data is allowed without the need for any external logic.

Mask Reset Operation

The mask register is reset to all ‘1s,’ which unmasks every bit of the counter. Master reset (MRST) also resets the mask register to all ‘1s’.

Mask Load Operation

The mask register is loaded with the address value presented at the address lines. Not all values permit correct increment operations. Permitted values are of the form $2^n – 1$ or $2^n – 2$. From the most significant bit to the least significant bit, permitted values have zero or more ‘0s,’ one or more ‘1s,’ or one ‘0.’ Thus 3FFFF, 003FE, and 00001 are permitted values, but 3F0FF, 003FC, and 00000 are not.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. Readback is pipelined; the address is valid t_{CM2} after the next rising edge of the port’s clock. If mask readback occurs while the port is enabled ($\overline{CE0}$ LOW and CE1 HIGH), the data lines (DQs) is three-stated. Figure 3 on page 9 shows a block diagram of the operation.

Counting by Two

When the least significant bit of the mask register is ‘0,’ the counter increments by two. This may be used to connect the x18 devices as a 36-bit single port SRAM in which the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 36-bit data in even memory locations, and the other half in odd memory locations.

Figure 3. Counter, Mask, and Mirror Logic Block Diagram [1]

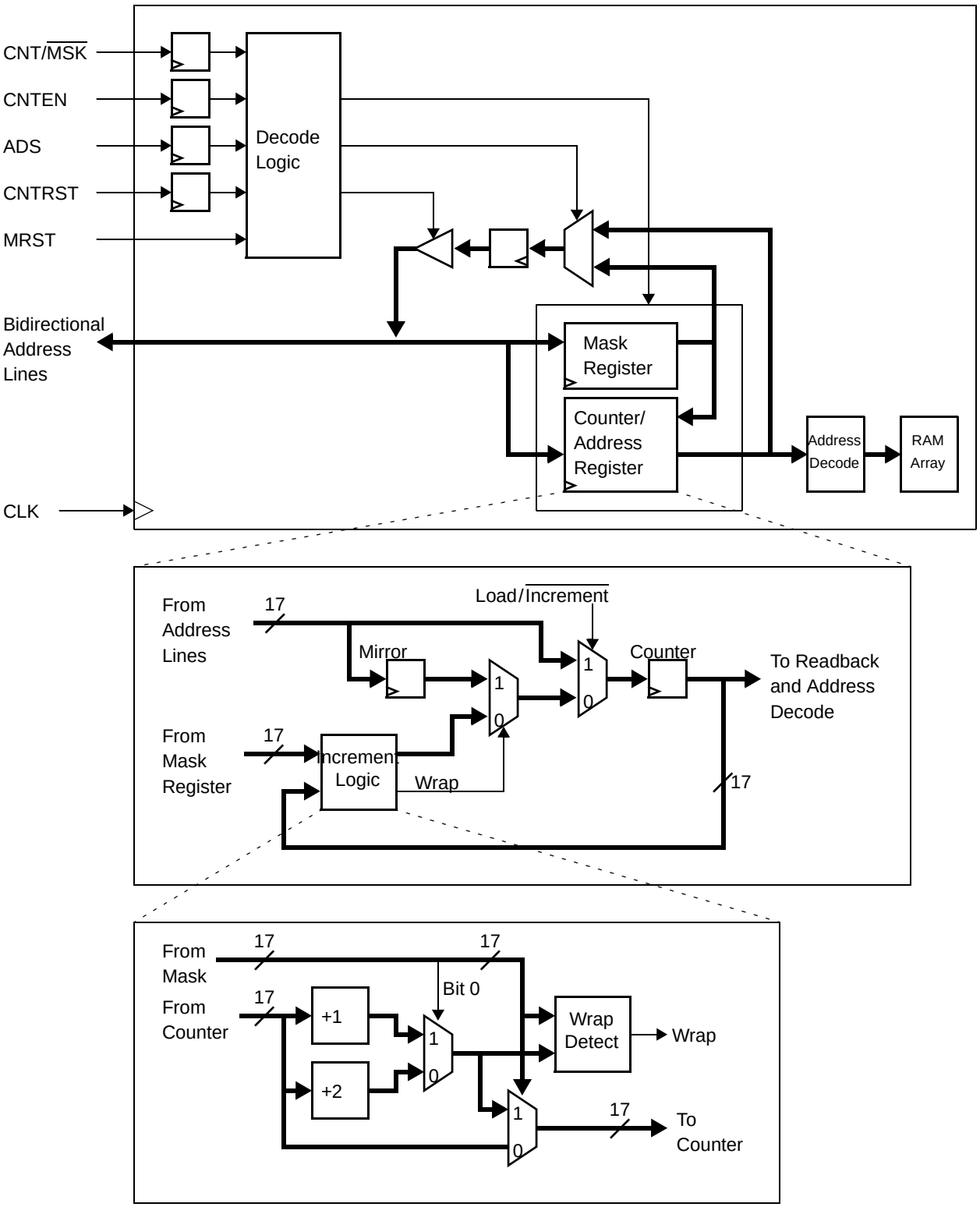
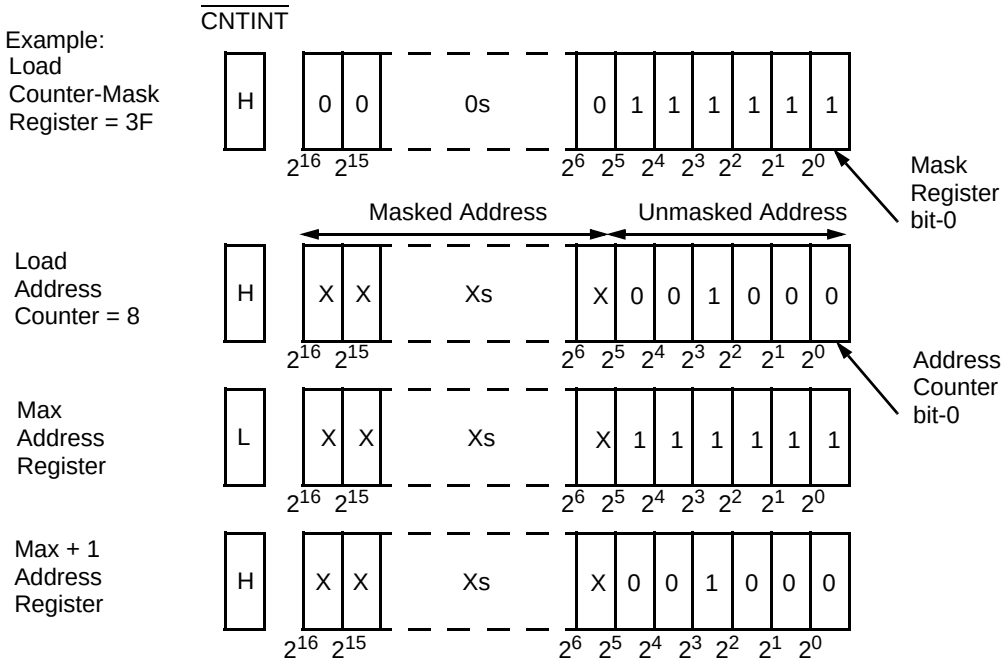


Figure 4. Programmable Counter-Mask Register Operation [2, 20]



IEEE 1149.1 Serial Boundary Scan (JTAG) [21]

The FLEx18 family devices incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 compliant TAPs. The TAP operates using JEDEC-standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the devices, and may be performed while the device is operating. An MRST must be performed on the devices after power up.

Performing a Pause/Restart

When a SHIFT-DR PAUSE-DR SHIFT-DR is performed the scan chain outputs the next bit in the chain twice. For example, if the value expected from the chain is 1010101, the device outputs a 11010101. This extra bit causes some testers to report an erroneous failure for the devices in a scan test. Therefore the tester should be configured to never enter the PAUSE-DR state.

Boundary Scan Hierarchy for 9-Mbit Device

Internally, the CY7C0833AV have two DIEs. Each DIE contain all the circuitry required to support boundary scan testing. The circuitry includes the TAP, TAP controller, instruction register, and data registers. The circuity and operation of the DIE boundary scan are described in detail below. The scan chain of each DIE are connected serially to form the scan chain of the CY7C0833AV as shown in Figure 5 on page 11. TMS and TCK are connected in parallel to each DIE to drive all TAP controllers in unison. In many cases, each DIE is supplied with the same instruction. In other cases, it might be useful to supply different instructions to each DIE. One example would be testing the device ID of one DIE while bypassing the others.

Each pin of FLEx18 family is typically connected to multiple DIEs. For connectivity testing with the EXTEST instruction, it is desirable to check the internal connections between DIEs and the external connections to the package. This is accomplished by merging the netlist of the devices with the netlist of the user's circuit board. To facilitate boundary scan testing of the devices, Cypress provides the BSDL file for each DIE, the internal netlist of the device, and a description of the device scan chain. The user can use these materials to easily integrate the devices into the board's boundary scan environment. Further information is found in the Cypress application note *Using JTAG Boundary Scan For System in a Package (SIP) Dual-Port SRAMs*.

Notes
20. The "X" in this diagram represents the counter upper bits
21. Boundary scan is IEEE 1149.1-compatible. See Performing a Pause/Restart on page 10 for deviation from strict 1149.1 compliance

Figure 5. Scan Chain for 9 Mb Device

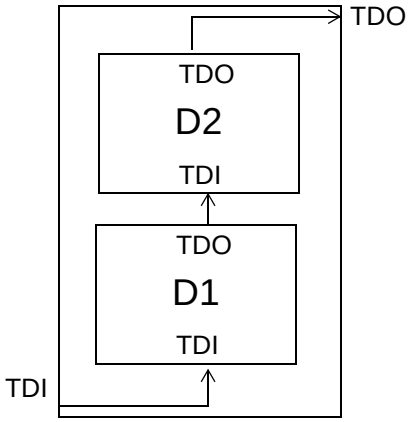


Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0h	Reserved for version number.
Cypress Device ID (27:12)	C090h	Defines Cypress part number for CY7C0832AV/CY7C0832BV
	C091h	Defines Cypress part number for CY7C0831AV
	C093h	Defines Cypress part number for CY7C0830AV
	C094h	Defines Cypress part number for CY7C0837AV.
Cypress JEDEC ID (11:1)	034h	Allows unique identification of the DP family device vendor.
ID Register Presence (0)	1	Indicates the presence of an ID register.

Table 5. Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[22]

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
NBSRST	1100	Resets the non-boundary scan logic. Places BYR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Note
22. See details in the device BSDL file.

Maximum Ratings

Exceeding maximum ratings[23] may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{DD} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V[24]

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2000V (JEDEC JESD22-A114-2000B)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V±165 mV
Industrial	–40°C to +85°C	3.3V±165 mV

Electrical Characteristics

Over the Operating Range

Parameter	Description		-167			-133			-100			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (V_{DD} = Min., I_{OH}= –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{DD} = Min., I_{OL}= +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, $\overline{MRST}$		–10		10	–10		10	–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, $\overline{MRST}$		–0.1		1.0	–0.1		1.0	–0.1		1.0	mA
I_{CC}	Operating Current for (V_{DD} = Max., I_{OUT} = 0 mA), Outputs Disabled	CY7C0837AV CY7C0830AV CY7C0831AV CY7C0832AV CY7C0832BV		225	300		225	300				mA
		CY7C0833AV					270	400		200	310	mA
I_{SB1}[25]	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}			90	115		90	115		90	115	mA
I_{SB2}[25]	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}			160	210		160	210		160	210	mA
I_{SB3}[25]	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD}$ – 0.2V, f = 0			55	75		55	75		55	75	mA
I_{SB4}[25]	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}			160	210		160	210		160	210	mA
I_{SB5}	Operating Current (V_{DD} = Max, I_{OUT} = 0 mA, f = 0) Outputs Disabled	CY7C0833AV					70	100		70	100	mA

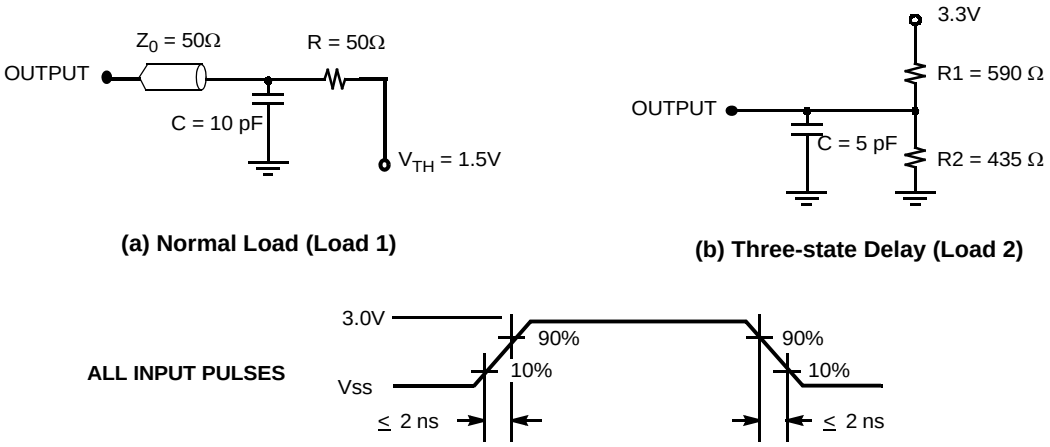
Capacitance

Part Number [26]	Parameter	Description	Test Conditions	Max	Unit
CY7C0837AV/CY7C0830AV/CY7C0831AV CY7C0832AV/CY7C0832BV	C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	13	pF
	C_{OUT}	Output Capacitance		10	pF
CY7C0833AV	C_{IN}	Input Capacitance		22	pF
	C_{OUT}	Output Capacitance		20	pF

Notes

23. The voltage on any input or I/O pin can not exceed the power pin during power up.
24. Pulse width < 20 ns.
25. I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} are not applicable for CY7C0833AV because it can not be powered down by using chip enable pins.
26. C_{OUT} also references $C_{I/O}$.

Figure 6. AC Test Load and Waveforms



(a) Normal Load (Load 1)

(b) Three-state Delay (Load 2)

Switching Characteristics

Over the Operating Range

Parameter	Description	-167		-133				-100		Unit
		CY7C0837AV CY7C0830AV CY7C0831AV CY7C0832AV		CY7C0837AV CY7C0830AV CY7C0831AV CY7C0832AV CY7C0832BV		CY7C0833AV		CY7C0833AV		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX2}	Maximum Operating Frequency		167		133		133		100	MHz
t_{CYC2}	Clock Cycle Time	6.0		7.5		7.5		10		ns
t_{CH2}	Clock HIGH Time	2.7		3.0		3.0		4.0		ns
t_{CL2}	Clock LOW Time	2.7		3.0		3.0		4.0		ns
t_R[27]	Clock Rise Time		2.0		2.0		2.0		3.0	ns
t_F[27]	Clock Fall Time		2.0		2.0		2.0		3.0	ns
t_{SA}	Address Setup Time	2.3		2.5		2.5		3.0		ns
t_{HA}	Address Hold Time	0.6		0.6		0.6		0.6		ns
t_{SB}	Byte Select Setup Time	2.3		2.5		2.5		3.0		ns
t_{HB}	Byte Select Hold Time	0.6		0.6		0.6		0.6		ns
t_{SC}	Chip Enable Setup Time	2.3		2.5		NA		NA		ns
t_{HC}	Chip Enable Hold Time	0.6		0.6		NA		NA		ns
t_{SW}	R/W Setup Time	2.3		2.5		2.5		3.0		ns
t_{HW}	R/$\overline{W}$ Hold Time	0.6		0.6		0.6		0.6		ns
t_{SD}	Input Data Setup Time	2.3		2.5		2.5		3.0		ns
t_{HD}	Input Data Hold Time	0.6		0.6		0.6		0.6		ns
t_{SAD}	$\overline{ADS}$ Setup Time	2.3		2.5		NA		NA		ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	2.3		2.5		NA		NA		ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	2.3		2.5		NA		NA		ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCM}	CNT/$\overline{MSK}$ Setup Time	2.3		2.5		NA		NA		ns

Note

27. Except JTAG signals (t_r and t_f < 10 ns [max.]).

Switching Characteristics (continued)

Over the Operating Range

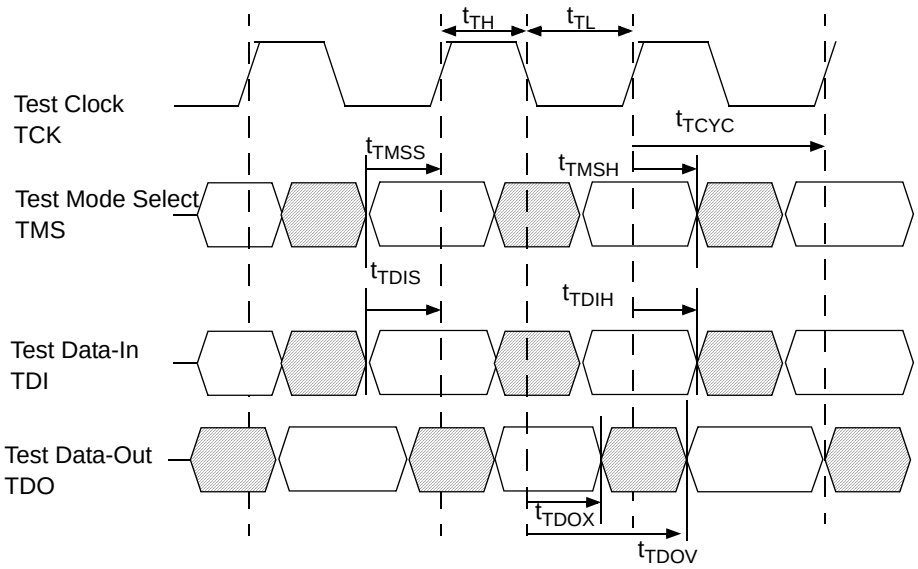
Parameter	Description	-167		-133				-100		Unit
		CY7C0837AV CY7C0830AV CY7C0831AV CY7C0832AV		CY7C0837AV CY7C0830AV CY7C0831AV CY7C0832AV CY7C0832BV		CY7C0833AV		CY7C0833AV		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HCM}	CNT/$\overline{MSK}$ Hold Time	0.6		0.6		NA		NA		ns
t_{OE}	Output Enable to Data Valid		4.0		4.4		4.7		5.0	ns
t_{OLZ}[28,29]	$\overline{OE}$ to Low Z	0		0						ns
t_{OHZ}[28,29]	$\overline{OE}$ to High Z	0	4.0	0	4.4		4.7		5.0	ns
t_{CD2}	Clock to Data Valid		4.0		4.4		4.7		5.0	ns
t_{CA2}	Clock to Counter Address Valid		4.0		4.4		NA		NA	ns
t_{CM2}	Clock to Mask Register Readback Valid		4.0		4.4		NA		NA	ns
t_{DC}	Data Output Hold After Clock HIGH	1.0		1.0		1.0		1.0		ns
t_{CKHZ}[28,29]	Clock HIGH to Output High Z	0	4.0	0	4.4		4.7		5.0	ns
t_{CKLZ}[28, 29]	Clock HIGH to Output Low Z	1.0	4.0	1.0	4.4	1.0	4.7	1.0	5.0	ns
t_{SINT}	Clock to $\overline{INT}$ Set Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
Port to Port Delays										
t_{CCS}	Clock to Clock Skew	5.2		6.0		6.0		8.0		ns
Master Reset Timing										
t_{RS}	Master Reset Pulse Width	7.0		7.5		7.5		10		ns
t_{RS}	Master Reset Setup Time	6.0		6.0		6.0		8.5		ns
t_{RSR}	Master Reset Recovery Time	6.0		7.5		7.5		10		ns
t_{RSF}	Master Reset to Outputs Inactive		10.0		10.0		10.0		10.0	ns
$t_{RSCNTINT}$	Master Reset to Counter Interrupt Flag Reset Time		10.0		10.0		NA		NA	ns

Notes
28. This parameter is guaranteed by design, but is not production tested.
29. Test conditions used are Load 2.

JTAG Timing and Switching Waveforms

Parameter	Description	CY7C0837AV/CY7C0830AV CY7C0831AV/CY7C0832AV CY7C0832BV/CY7C0833AV		Unit
		Min	Max	
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TH}	TCK Clock HIGH Time	40		ns
t_{TL}	TCK Clock LOW Time	40		ns
t_{TMSS}	TMS Setup to TCK Clock Rise	10		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	10		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold After TCK Clock Rise	10		ns
t_{TDOV}	TCK Clock LOW to TDO Valid		30	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Figure 7. JTAG Switching Waveform



Switching Waveforms

Figure 8. Master Reset

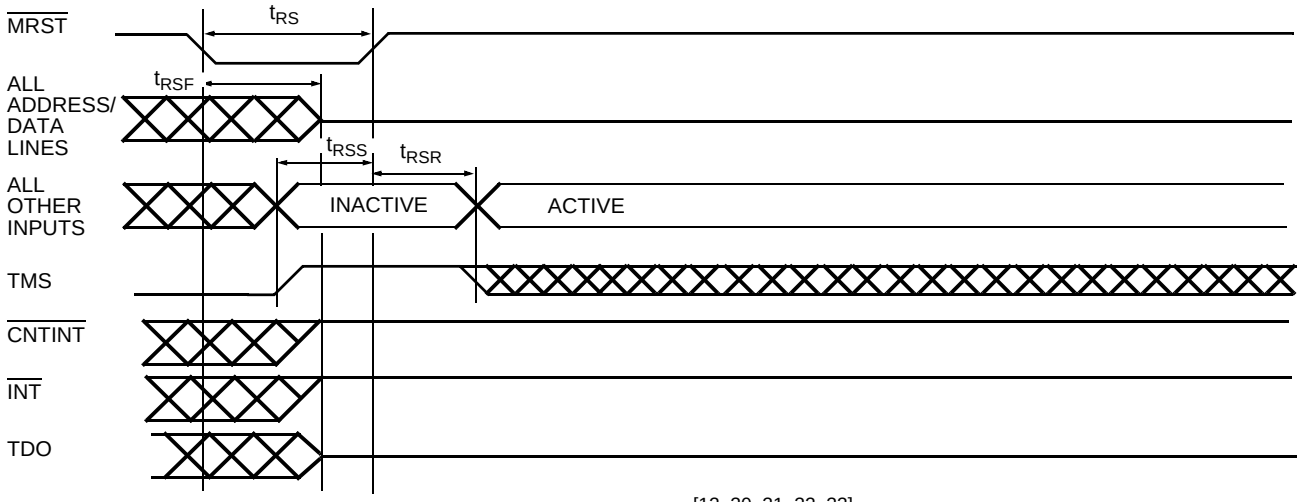
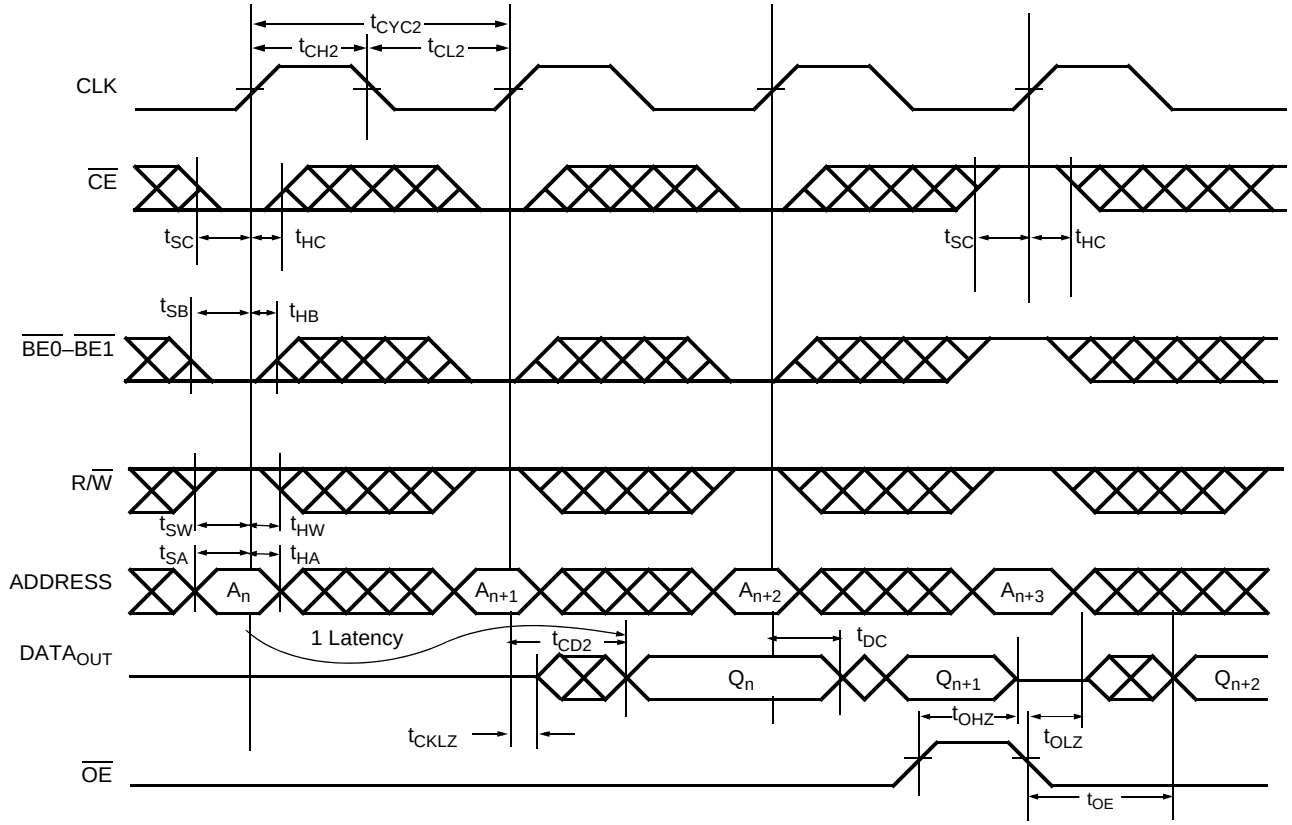


Figure 9. Read Cycle[12, 30, 31, 32, 33]



Notes
30. OE is asynchronously controlled; all other inputs (excluding MRST and JTAG) are synchronous to the rising clock edge.
31. ADS = CNTEN = LOW, and MRST = CNTRST = CNT/MSK = HIGH.
32. The output is disabled (high-impedance state) by CE = V_{IH} following the next rising edge of the clock.
33. Addresses need not be accessed sequentially because ADS = CNTEN = V_{IL} with CNT/MSK = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 10. Bank Select Read[34, 35]

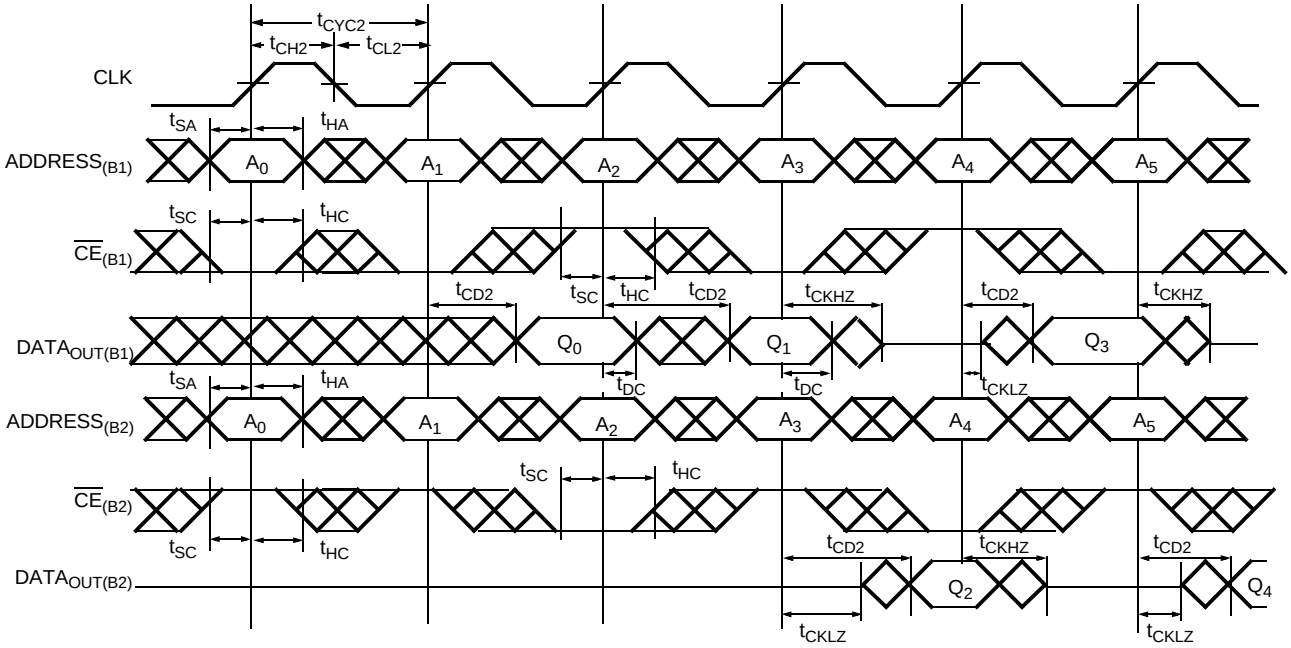
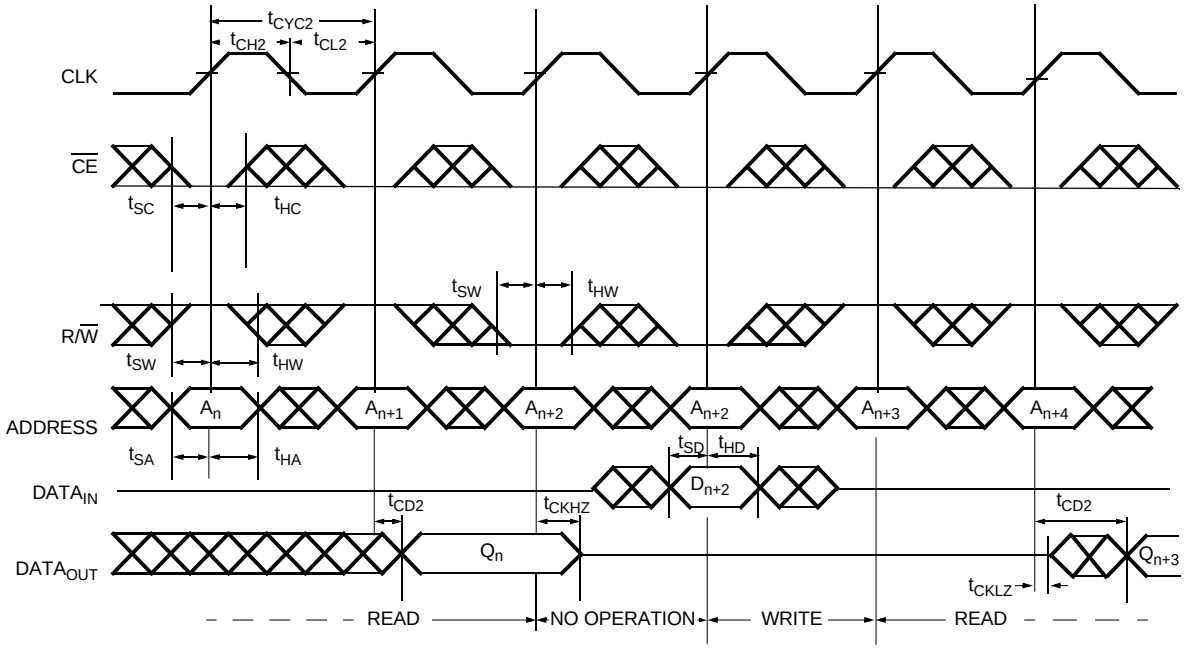


Figure 11. Read-to-Write-to-Read ($\overline{OE}$ = LOW)[33, 36, 37, 38, 39]



Notes

34. In this depth-expansion example, B1 represents Bank #1 and B2 is Bank #2; each bank consists of one Cypress FLEx18 device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
35. $\overline{ADS}$ = CNTEN= $\overline{BE0}$ – $\overline{BE1}$ = $\overline{OE}$ = LOW; $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
36. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
37. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
38. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE1}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
39. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE1}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, because OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Figure 12. Read-to-Write-to-Read ($\overline{OE}$ Controlled)[33, 36, 38, 39]

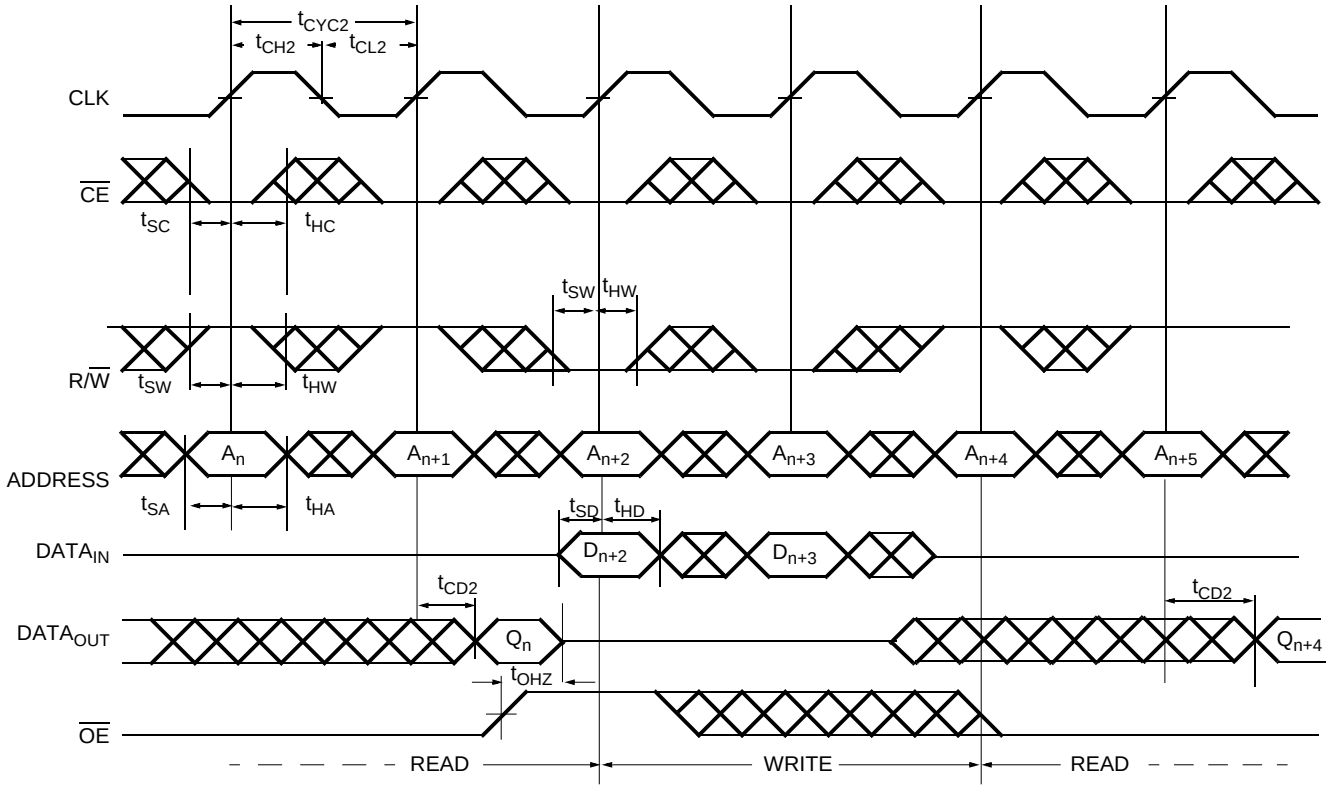
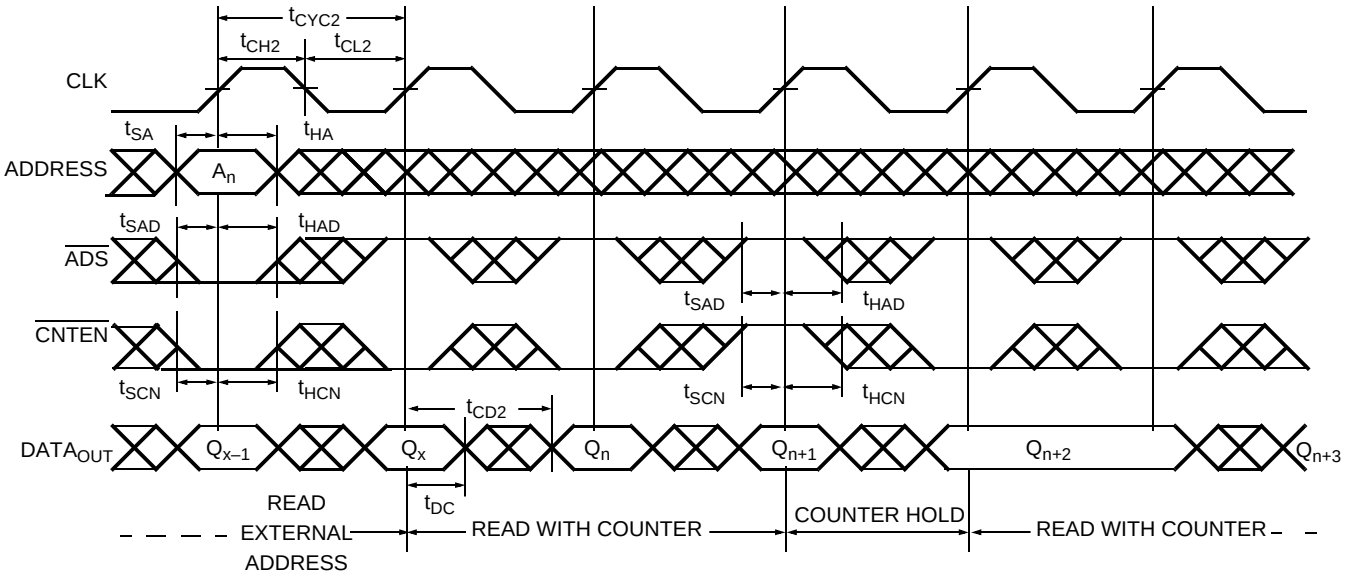


Figure 13. Read with Address Counter Advance[38]



Switching Waveforms (continued)

Figure 14. Write with Address Counter Advance[39]

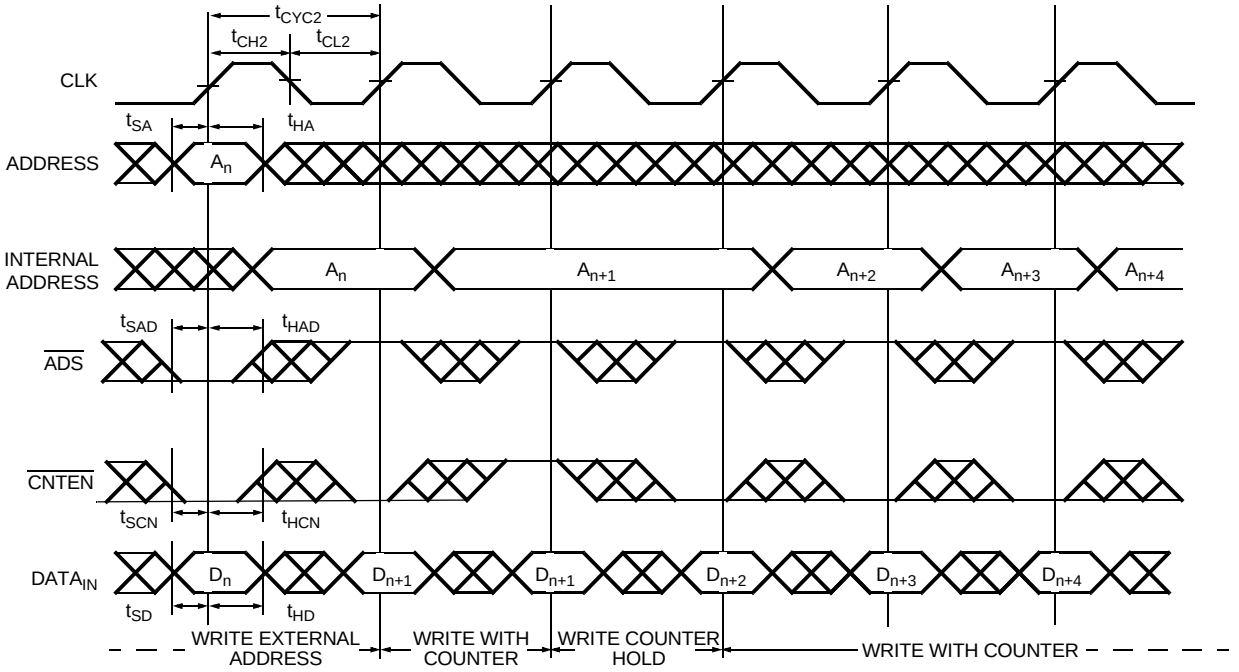
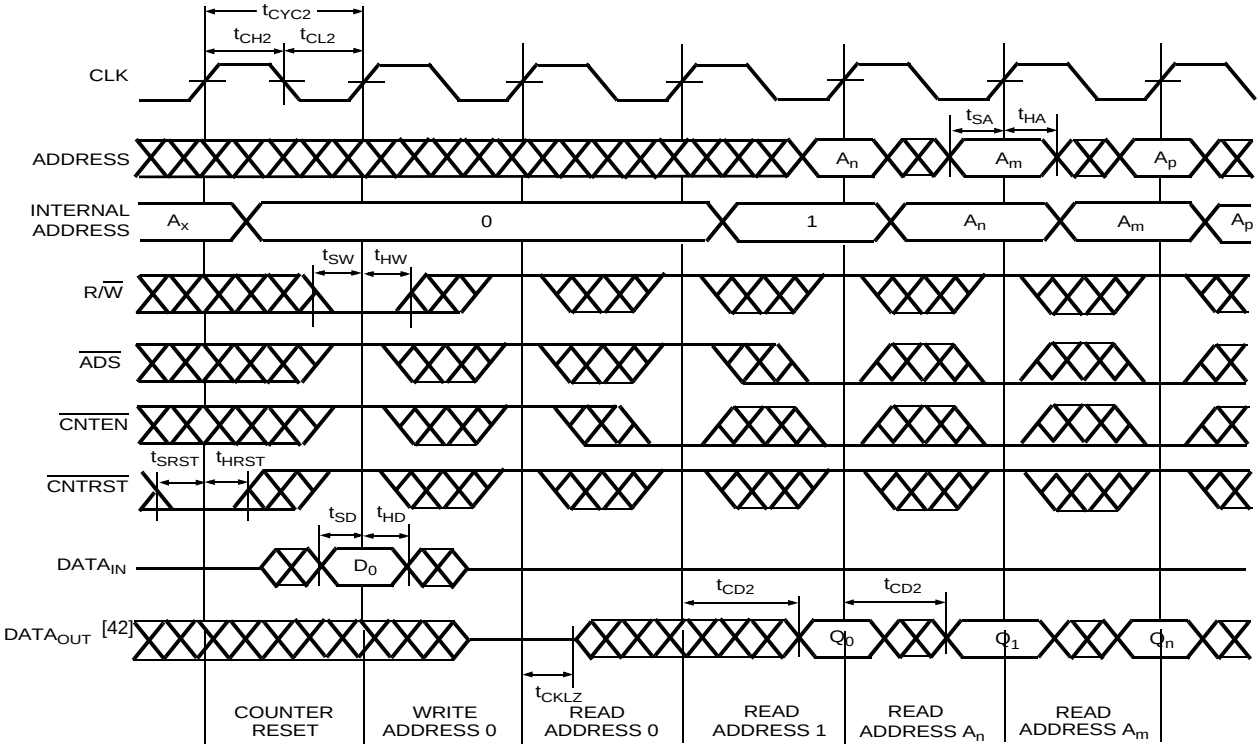


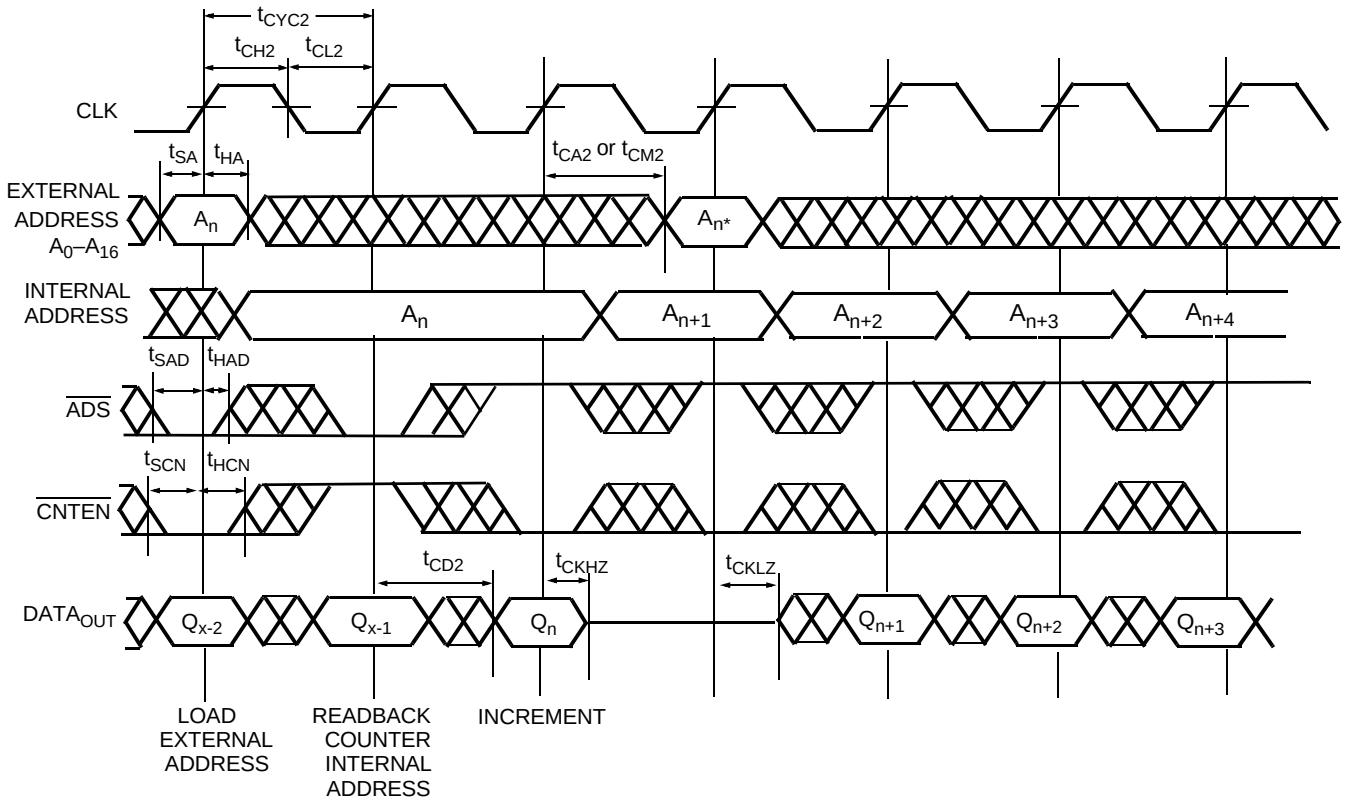
Figure 15. Counter Reset[40, 41]



Notes
40. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE1}$ = LOW; CE_1 = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
41. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.
42. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value.

Switching Waveforms (continued)

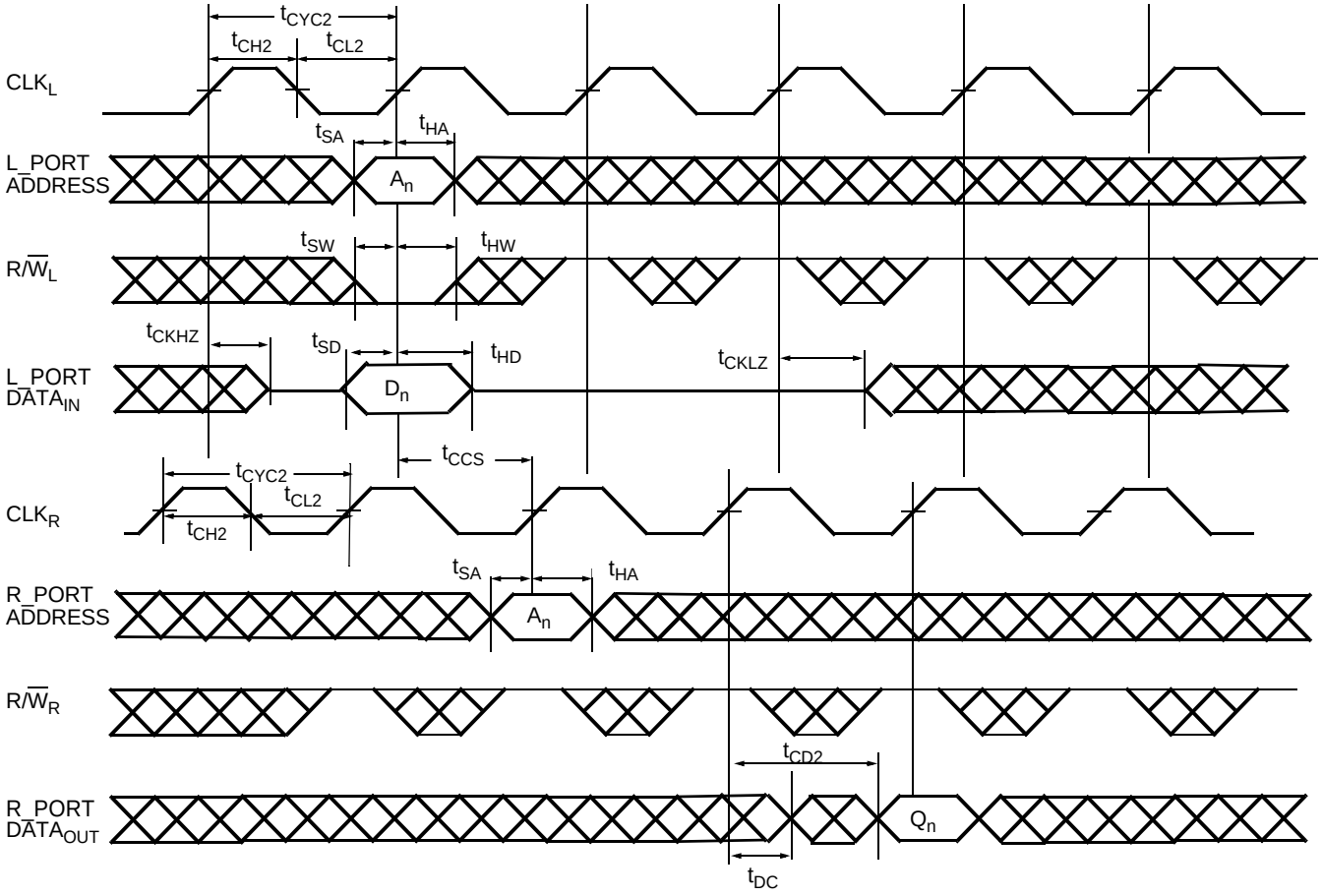
Figure 16. Readback State of Address Counter or Mask Register[43, 44, 45, 46]



Notes
43. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE1}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
44. Address in output mode. Host must not be driving address bus after t_{CKLZ} in next clock cycle.
45. Address in input mode. Host can drive address bus after t_{CKHZ}.
46. An * is the internal value of the address counter (or the mask register depending on the CNT/$\overline{MSK}$ level) being Read out on the address lines.

Switching Waveforms (continued)

Figure 17. Left_Port (L_Port) Write to Right_Port (R_Port) Read[47, 48, 49]

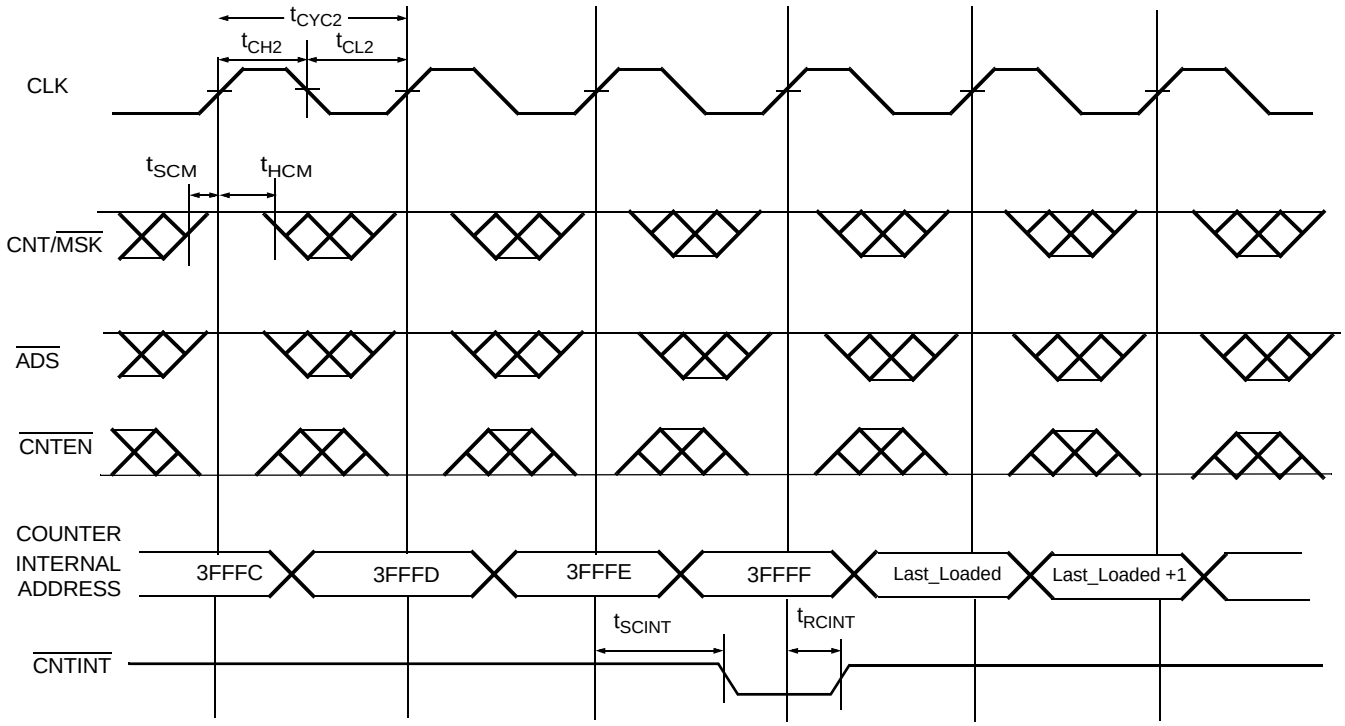


Notes

47. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = $\overline{BE0}$ – $\overline{BE1}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
48. This timing is valid when one port is writing, and other port is reading the same location at the same time. If t_{CCS} is violated, indeterminate data is Read out.
49. If t_{CCS} < minimum specified value, then R_Port is Read the most recent data (written by L_Port) only (2 * t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock. If t_{CCS} ≥ minimum specified value, then R_Port is Read the most recent data (written by L_Port) (t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock.

Switching Waveforms (continued)

Figure 18. Counter Interrupt and Retransmit [15, 42, 50, 51, 52, 53]



Notes
50. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE1}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
51. $\overline{CNTINT}$ is always driven.
52. $\overline{CNTINT}$ goes LOW when the unmasked portion of the address counter is incremented to the maximum value.
53. The mask register assumed to have the value of 3FFFFh.

Switching Waveforms (continued)

Figure 19. MailBox Interrupt Timing [54, 55, 56, 57, 58]

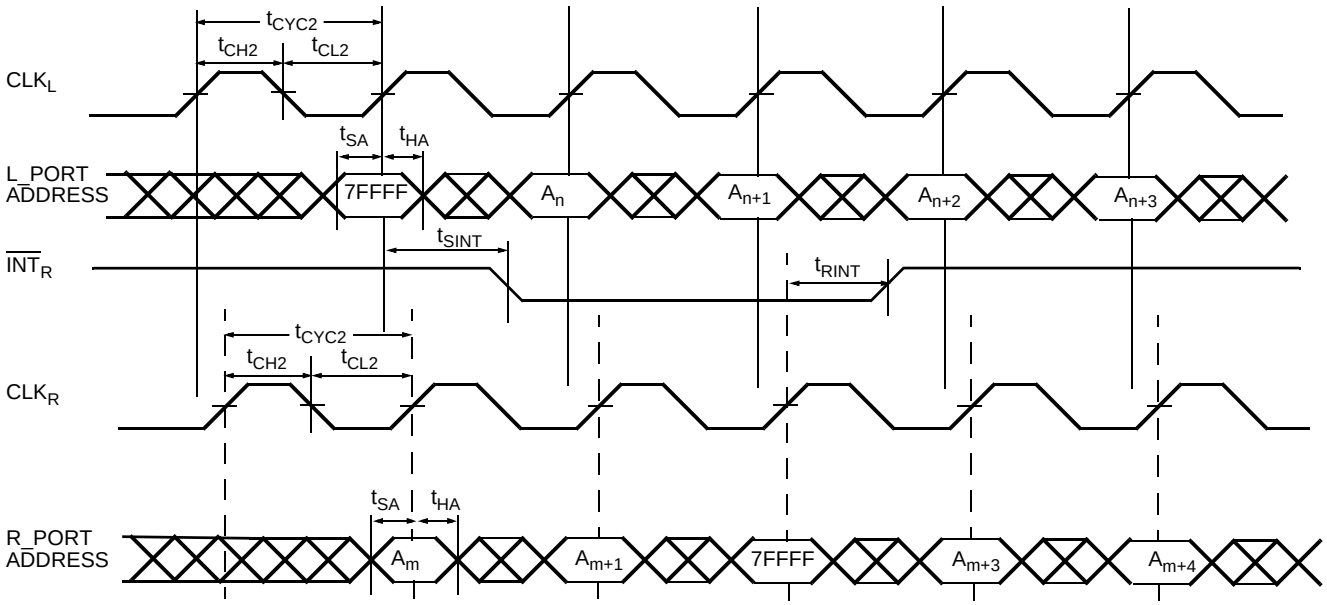


Table 7. Read/Write and Enable Operation (Any Port) [2, 17, 59, 60, 61]

Inputs					Outputs	Operation
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	$DQ_0 - DQ_{17}$	
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Notes
54. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
55. Address “7FFFF” is the mailbox location for R_Port of the 9Mb device.
56. L_Port is configured for Write operation, and R_Port is configured for Read operation.
57. At least one byte enable ($\overline{BE0}$ – $\overline{BE1}$) is required to be active during interrupt operations.
58. Interrupt flag is set with respect to the rising edge of the Write clock, and is reset with respect to the rising edge of the Read clock.
59. $\overline{OE}$ is an asynchronous input signal.
60. When $\overline{CE}$ changes state, deselection and Read happen after one cycle of latency.
61. $\overline{CE_0}$ = $\overline{OE}$ = LOW; CE_1 = R/$\overline{W}$ = HIGH.

Ordering Information

512K × 18 (9M) 3.3V Synchronous CY7C0833AV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C0833AV-133BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0833AV-133BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial
100	CY7C0833AV-100BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0833AV-100BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial

256K × 18 (4M) 3.3V Synchronous CY7C0832AV/CY7C0832BV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0832AV-167BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0832AV-167AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0832AV-167AXC		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	
133	CY7C0832AV-133BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0832AV-133AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0832AV-133AXC		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	
	CY7C0832AV-133BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial
	CY7C0832BV-133AI	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0832AV-133AXI		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	

128K × 18 (2M) 3.3V Synchronous CY7C0831AV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0831AV-167BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0831AV-167AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0831AV-167AXC		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	
133	CY7C0831AV-133BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0831AV-133BBXC		144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch (Pb-Free)	
	CY7C0831AV-133AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0831AV-133AXC		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	
	CY7C0831AV-133BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial
	CY7C0831AV-133BBXI		144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch (Pb-Free)	
	CY7C0831AV-133AI	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0831AV-133AXI		120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm) (Pb-Free)	

64K × 18 (1M) 3.3V Synchronous CY7C0830AV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0830AV-167BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0830AV-167AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
133	CY7C0830AV-133BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0830AV-133AC	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	
	CY7C0830AV-133BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial
	CY7C0830AV-133AI	51-85100	120-Pin Thin Quad Flat Pack (14 x 14 x 1.4 mm)	

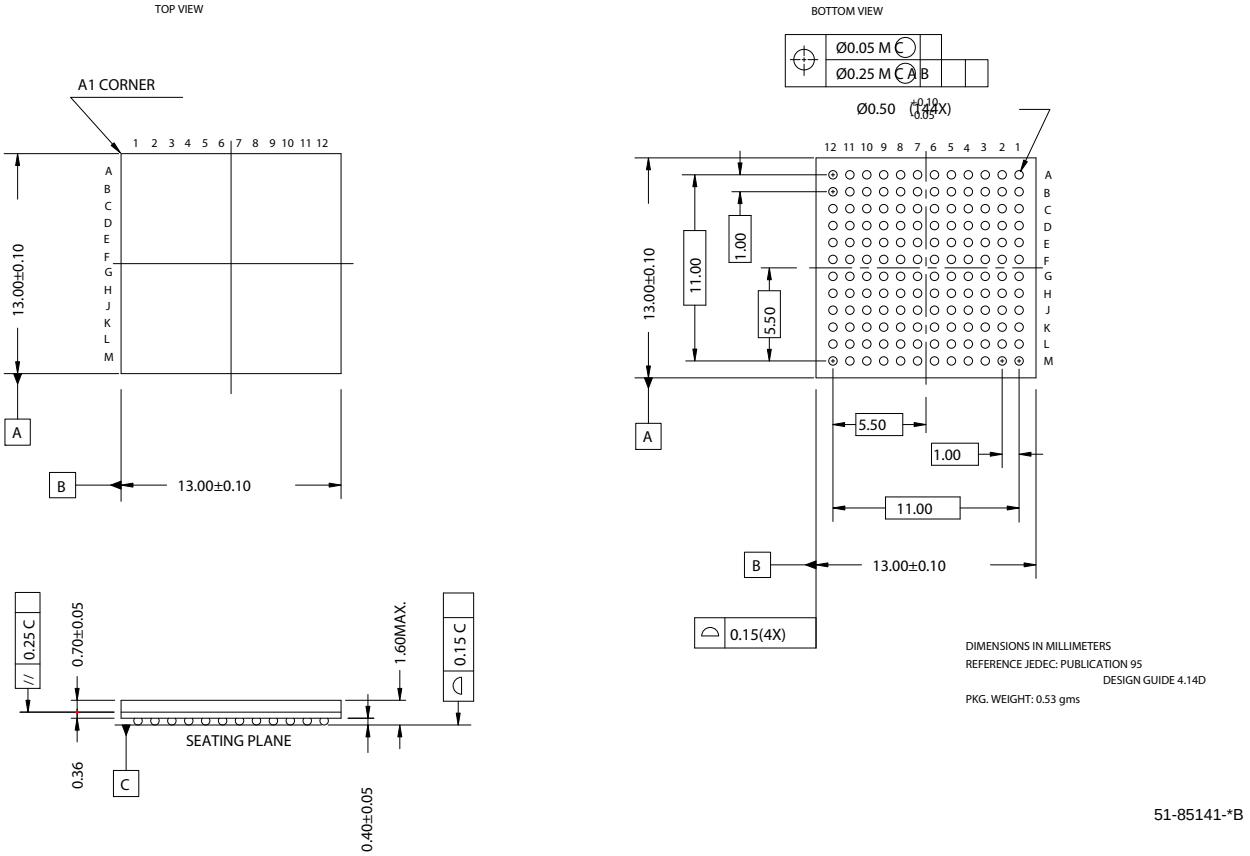
Ordering Information

32K × 18 (512K) 3.3V Synchronous CY7C0837AV Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
167	CY7C0837AV-167BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
133	CY7C0837AV-133BBC	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Commercial
	CY7C0837AV-133BBI	51-85141	144-Ball Grid Array (13 x 13 x 1.6 mm) with 1 mm pitch	Industrial

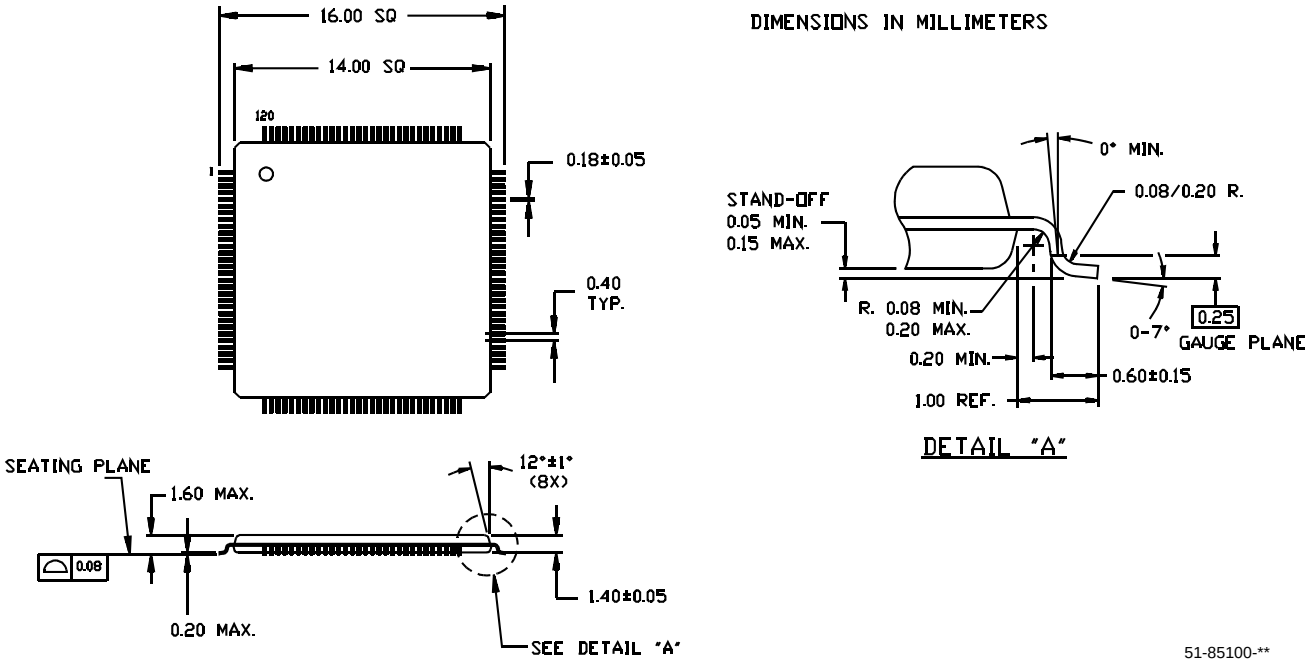
Package Diagrams

Figure 20. 144-Ball FBGA (13 x 13 x 1.6 mm) (51-85141)



Package Diagrams

Figure 21. 120-Pin Thin Quad Flatpack (14 x 14 x 1.4 mm) (51-85100)



Document History Page

Document Title: CY7C0837AV/CY7C0830AV/CY7C0831AV/CY7C0832AV/CY7C0832BV/CY7C0833AV, FLEx18™ 3.3V 64K/128K x 36 and 128K/256K x 18 Synchronous Dual-Port RAM Document Number: 38-06059				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	111473	DSG	11/27/01	Change from Spec number: 38-01056 to 38-06059
*A	111942	JFU	12/21/01	Updated capacitance values Updated switching parameters and I_{SB3} Updated “Read-to-Write-to-Read (OE Controlled)” waveform Revised static discharge voltage Revised footnote regarding I_{SB3}
*B	113741	KRE	04/02/02	Updated I_{sb} values Updated ESD voltage Corrected 0853 pins L3 and L12
*C	114704	KRE	04/24/02	Added discussion of Pause/Restart for JTAG boundary scan
*D	115336	KRE	07/01/02	Revised speed offerings for all densities
*E	122307	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*F	123636	KRE	1/27/03	Revise t_{cd2}, t_{OE}, t_{OHZ}, t_{CKHZ}, t_{CKLZ} for the CY7C0853V to 4.7 ns
*G	126053	SPN	08/11/03	Separated out 4M and 9M data sheets Updated I_{sb} and I_{CC} values
*H	129443	RAZ	11/03/03	Updated I_{sb} and I_{CC} values
*I	231993	YDT	See ECN	Removed “A particular port can write to a certain location while another port is reading that location.” from Functional Description.
*J	231813	WWZ	See ECN	Removed x36 devices (CY7C0852/CY7C0851) from this datasheet. Added 0.5M, 1M and 9M x18 devices to it. Changed title to FLEx18 3.3V 32K/64K/128K/256K/512K x18 Synchronous Dual-Port RAM. Changed datasheet to accommodate the removals and additions. Removed general JTAG description. Updated JTAG ID codes for all devices. Added 144FBGA package for all devices. Updated selection guide table and moved to the front page. Updated block diagram to reflect x18 configuration. Added preliminary status back due to the addition of the new devices.
*K	311054	RYQ	See ECN	Minor Change: Correct the revision indicated on the footer.
*L	329111	SPN	See ECN	Updated Marketing part numbers Updated tRSF
*M	330561	RUY	See ECN	Added Byte Select Operation Table
*N	375198	YDT	See ECN	Removed Preliminary status Added I_{SB5} Changed $t_{RSCNTINT}$ to 10ns
*O	391525	SPN	See ECN	Updated Counter reset section to reflect what is loaded into the mirror register
*P	414109	LIJ	See ECN	Corrected Ordering Codes for 0831 devices in the 133 Mhz speed bin. Added CY7C0833AV-133BBI.
*Q	461113	YDT	SEE ECN	Changed VDDIO to VDD (typo) Added lead(Pb)-free parts Corrected typo in DC table
*R	2544945	VKN/AESA	07/29/08	Updated Template. Updated ordering information
*S	2668478	VKN/PYRS	02/04/09	Added CY7C0832BV part Added footnote #1 Updated Ordering information table

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