

16-Mbit (1M x 16) Static RAM

Features

- TSOP I Configurable as 1M x 16 or as 2M x 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 2.2V – 3.6V
- Ultra-low active power
 - Typical active current: 2 mA @ f = 1 MHz
 - Typical active current: 18.5 mA @ f = f_{Max} (45 ns speed)
- Ultra-low standby power
- Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Available in Pb-free and non Pb-free 48-ball VFBGA and 48-pin TSOP I package

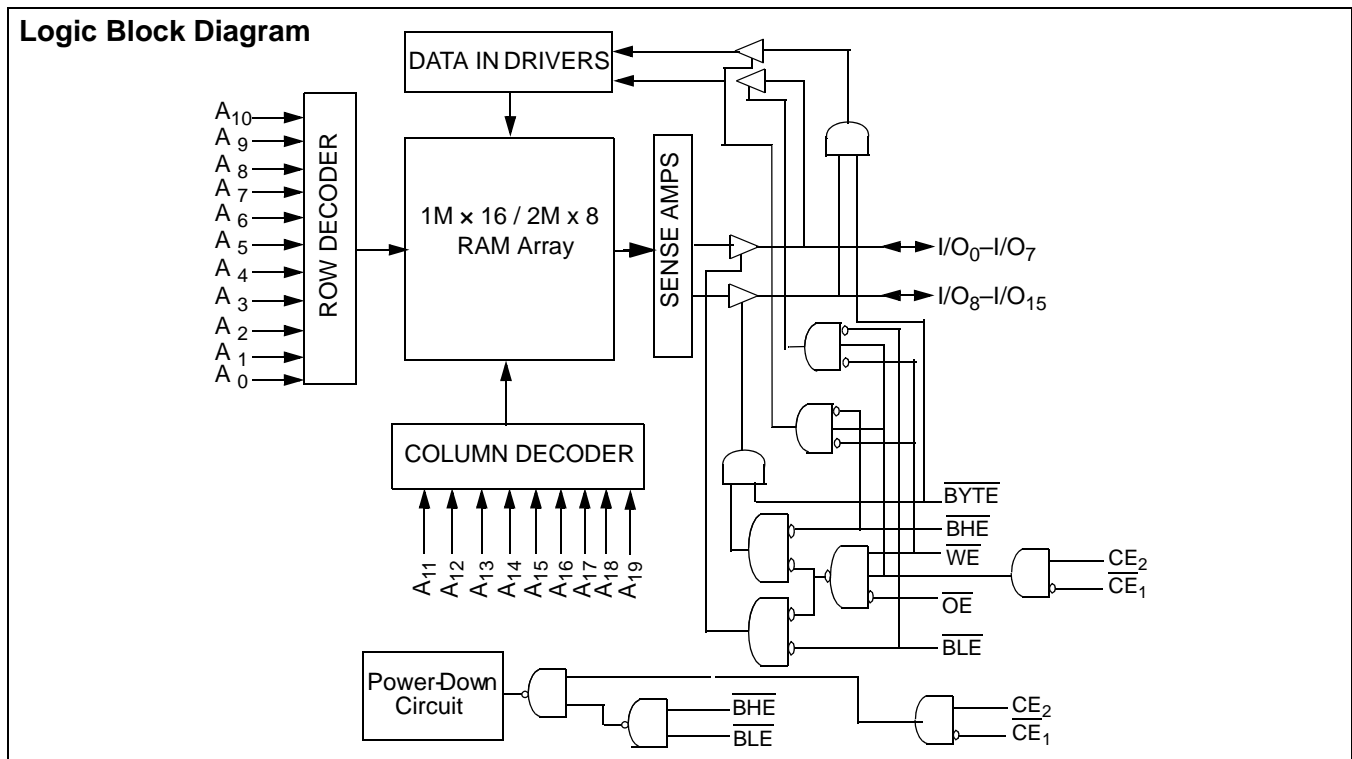
Functional Description^[1]

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW or both BHE and BLE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a Write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables (\overline{CE}_1 LOW and \overline{CE}_2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by taking Chip Enables (\overline{CE}_1 LOW and \overline{CE}_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of Read and Write modes.



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.2V to $V_{CC} + 0.3V$

DC Voltage Applied to Outputs in High-Z State^[7, 8] -0.2V to $V_{CC} + 0.3V$

DC Input Voltage^[7, 8] -0.2V to $V_{CC} + 0.3V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[9]
CY62167DV30LL	Industrial	-40°C to +85°C	2.20V to 3.60V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62167DV30-45			CY62167DV30-55			CY62167DV30-70			Unit
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$, $V_{CC} = 2.20V$	2.0			2.0			2.0			V
		$I_{OH} = -1.0 \text{ mA}$, $V_{CC} = 2.70V$	2.4			2.4			2.4			
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$, $V_{CC} = 2.20V$			0.4			0.4			0.4	V
		$I_{OL} = 2.1 \text{ mA}$, $V_{CC} = 2.70V$										
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$	1.8		$V_{CC} + 0.3V$	1.8		$V_{CC} + 0.3V$	1.8		$V_{CC} + 0.3V$	V
		$V_{CC} = 2.7V \text{ to } 3.6V$	2.2			2.2			2.2			
V_{IL}	Input LOW Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$	-0.3		0.6	-0.3		0.6	-0.3		0.6	V
		$V_{CC} = 2.7V \text{ to } 3.6V$			0.8			0.8			0.8	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	-1		+1	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = V_{CC(max)}$ $I_{OUT} = 0 \text{ mA}$ CMOS levels $f = f_{Max} = 1/t_{RC}$ $f = 1 \text{ MHz}$	18.5	37		15	30		12	25	mA	
			2	4		2	4		2	4		
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{Max}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, BLE), $V_{CC} = 3.60V$		2.5	22		2.5	22		2.5	22	μA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.60V$		2.5	22		2.5	22		2.5	22	μA

Notes:

7. $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns.

8. $V_{IH(max.)} = V_{CC} + 0.75V$ for pulse durations less than 20 ns.

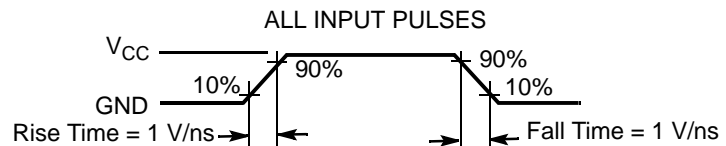
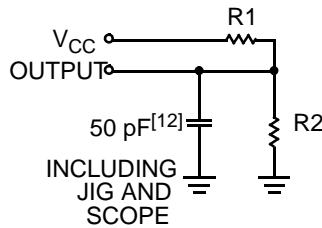
9. Full Device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min.)}$ and V_{CC} must be stable at $V_{CC(min.)}$ for 500 μs .

Capacitance^[10, 11]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	8	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance^[10]

Parameter	Description	Test Conditions	VFBGA	TSOP I	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	55	60	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		16	4.3	°C/W

AC Test Loads and Waveforms^[12]


Equivalent to: THEVENIN EQUIVALENT



Parameters	2.5V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ₁ ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V			10	μA
t _{CDR} ^[10]	Chip Deselect to Data Retention Time		0			ns
t _R ^[13]	Operation Recovery Time		t _{RC}			ns

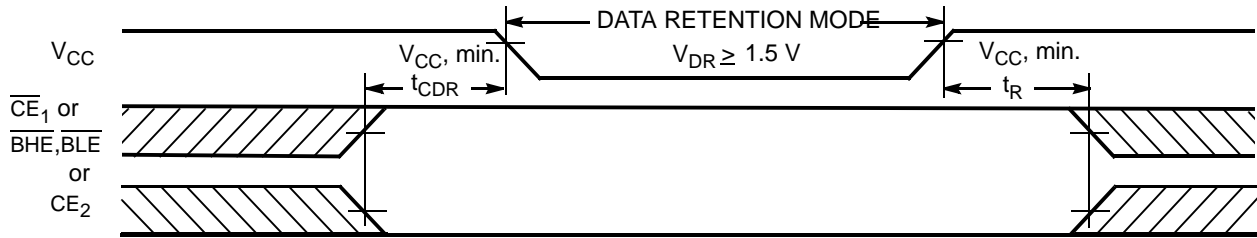
Notes:

10. Tested initially and after any design or process changes that may affect these parameters.

11. This applies for all packages.

12. Test condition for the 45 ns part is with a load capacitance of 30 pF.

13. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.

Data Retention Waveform^[14]

Switching Characteristics Over the Operating Range^[15]

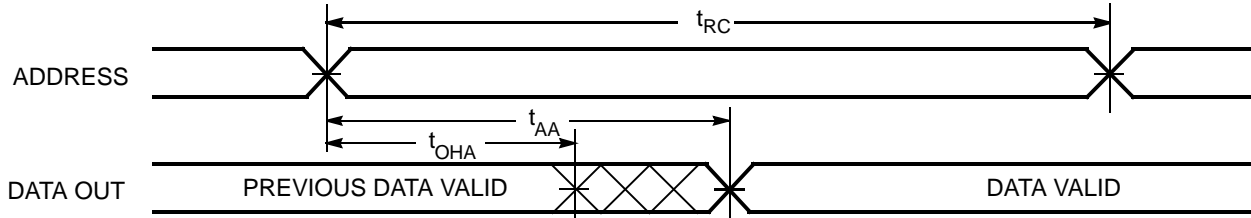
Parameter	Description	45 ns ^[12]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to Data Valid		45		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[16]	5		5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[16, 17]		15		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[16]	10		10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to High Z ^[16, 17]		20		20		25	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-up	0		0		0		ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to Power-down		45		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[16]	10		10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z ^[16, 17]		15		20		25	ns
Write Cycle^[18]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	40		40		60		ns
t_{AW}	Address Set-Up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	35		40		45		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t_{SD}	Data Set-Up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[16, 17]		15		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[16]	10		10		10		ns

Notes:

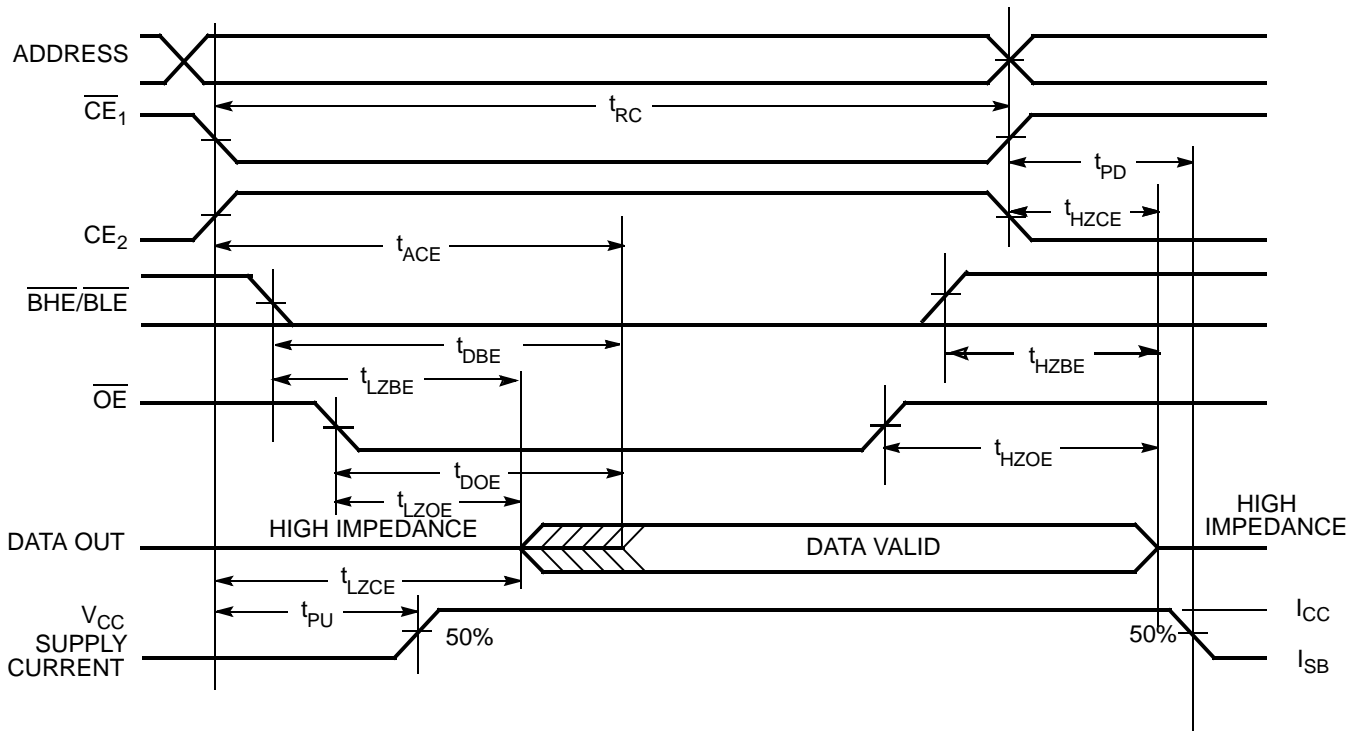
- $\overline{BHE}, \overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .
- Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[19, 20]



Read Cycle 2 (\overline{OE} Controlled)^[20, 21]

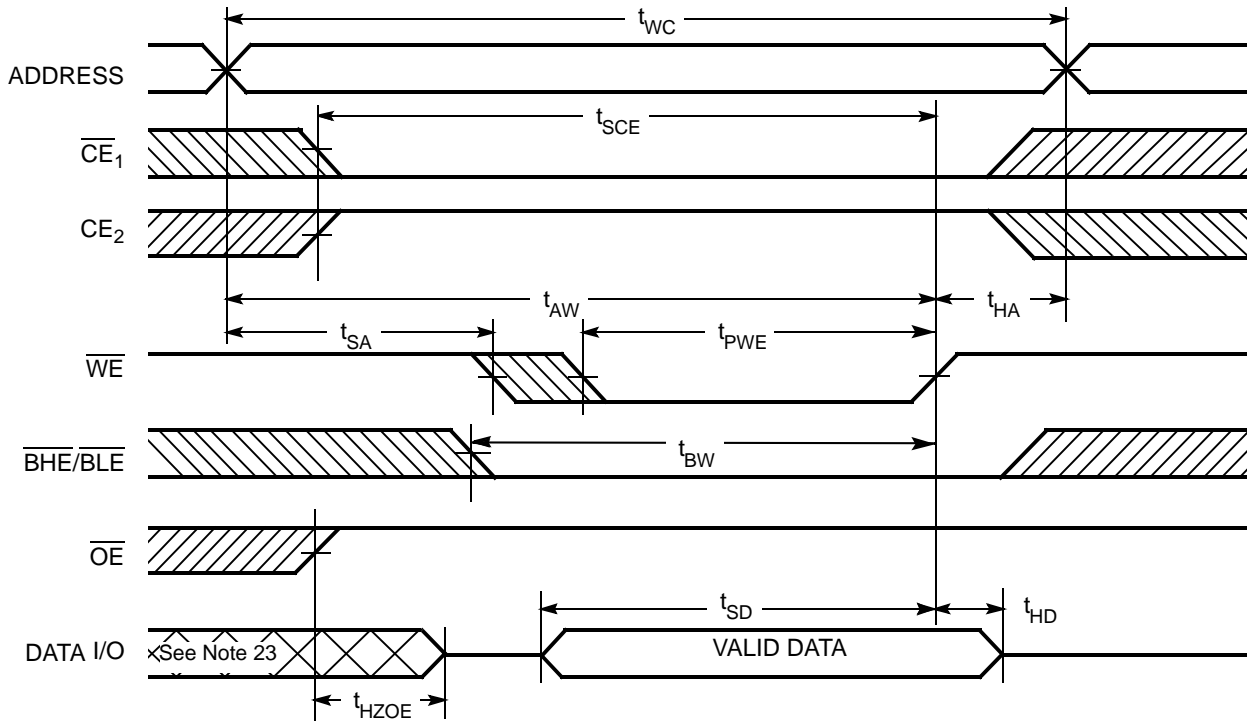


Notes:

- 19. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
- 20. \overline{WE} is HIGH for read cycle.
- 21. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 (WE Controlled)^[18, 22, 23, 24]

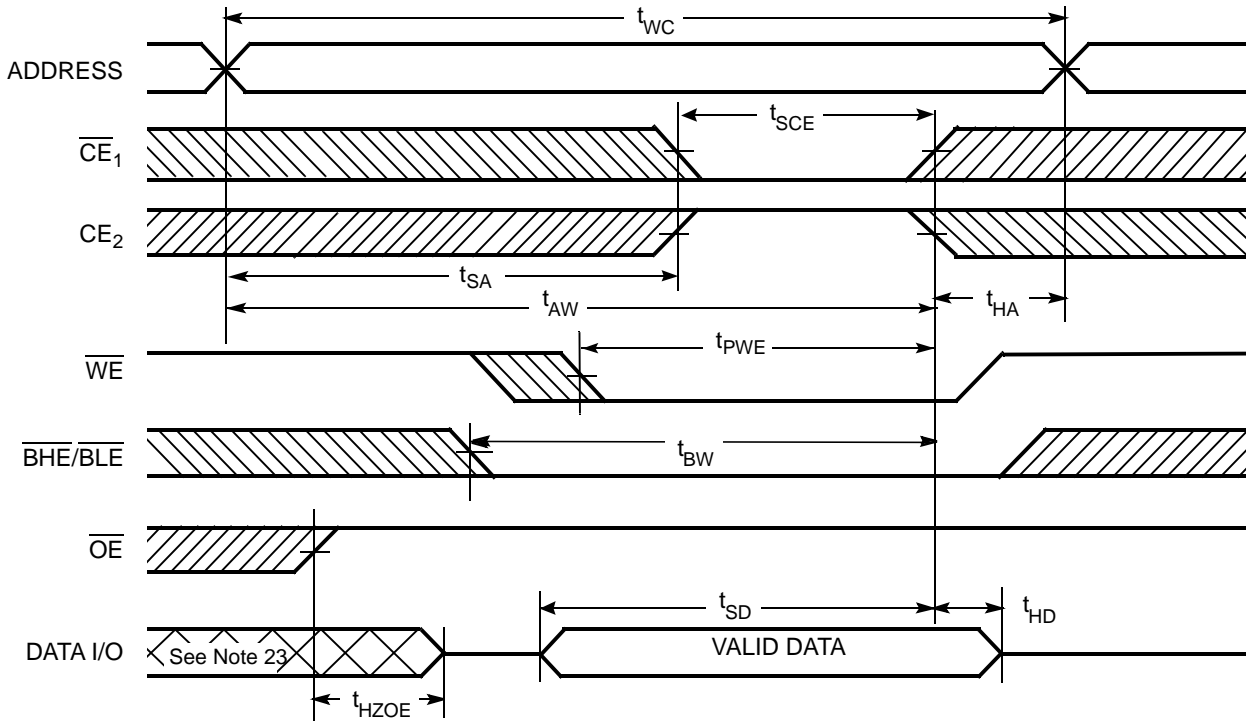


Notes:

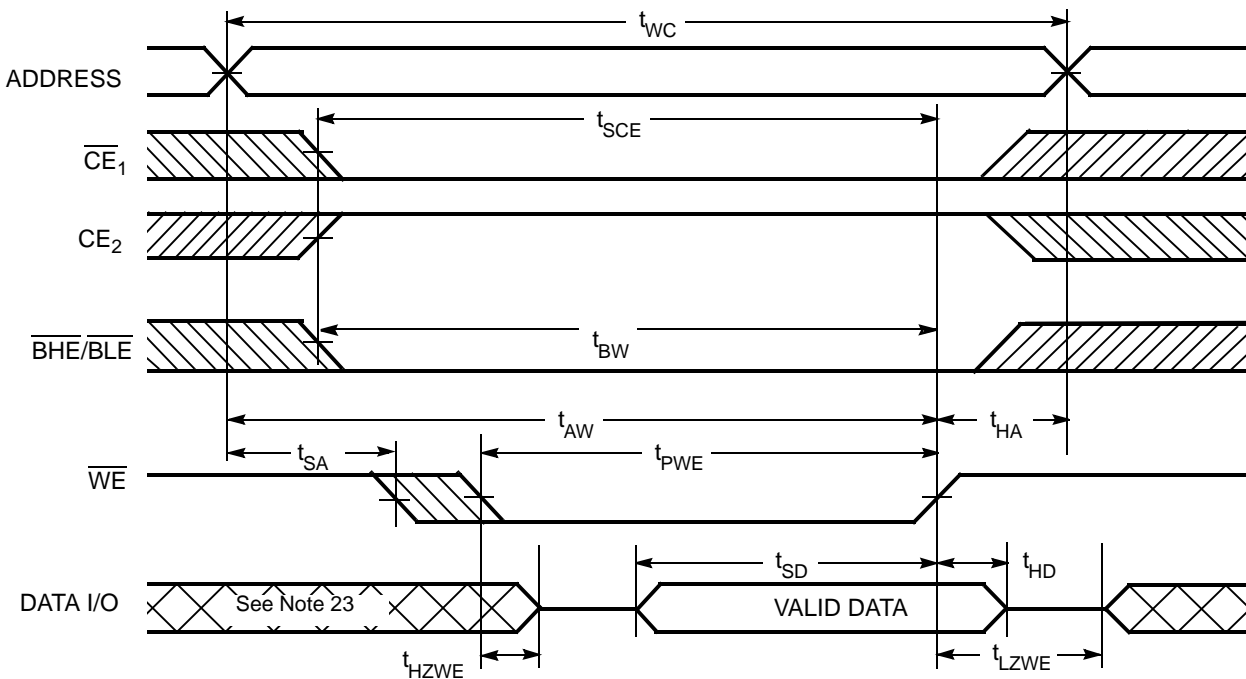
- 22. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
- 23. If CE₁ goes HIGH and CE₂ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
- 24. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 2 (\overline{CE}_1 or \overline{CE}_2 Controlled)^[18, 22, 23, 24]

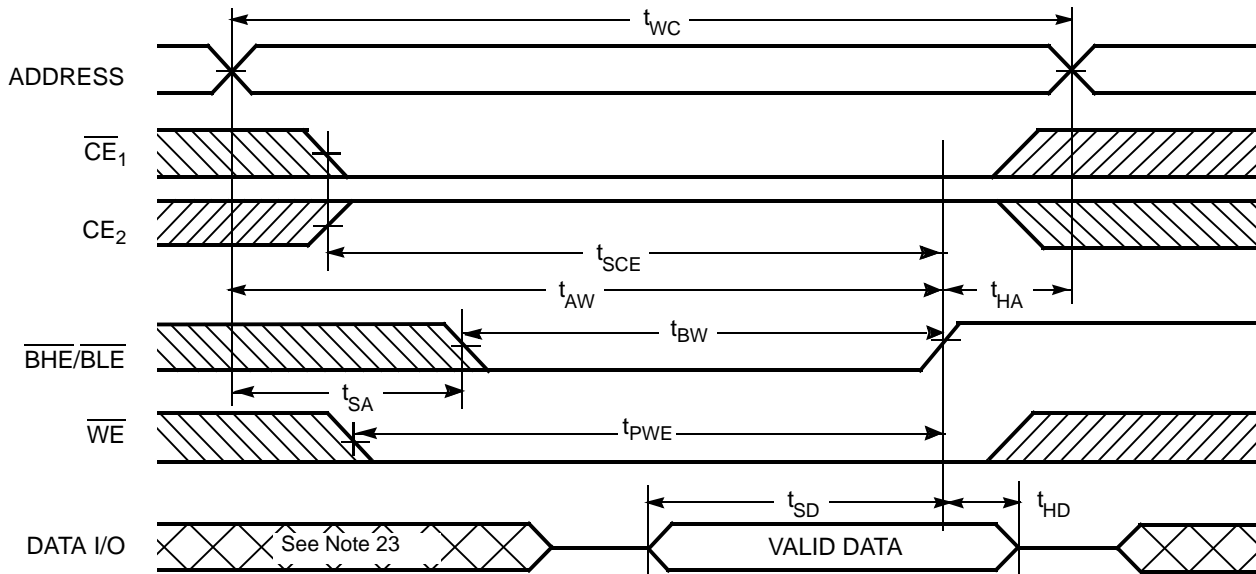


Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)^[23, 24]



Switching Waveforms (continued)

Write Cycle 4 (BHE/BLE Controlled, OE LOW)^[23, 24]



Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (I/O_8 – I/O_{15}); Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (I/O_8 – I/O_{15}); Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

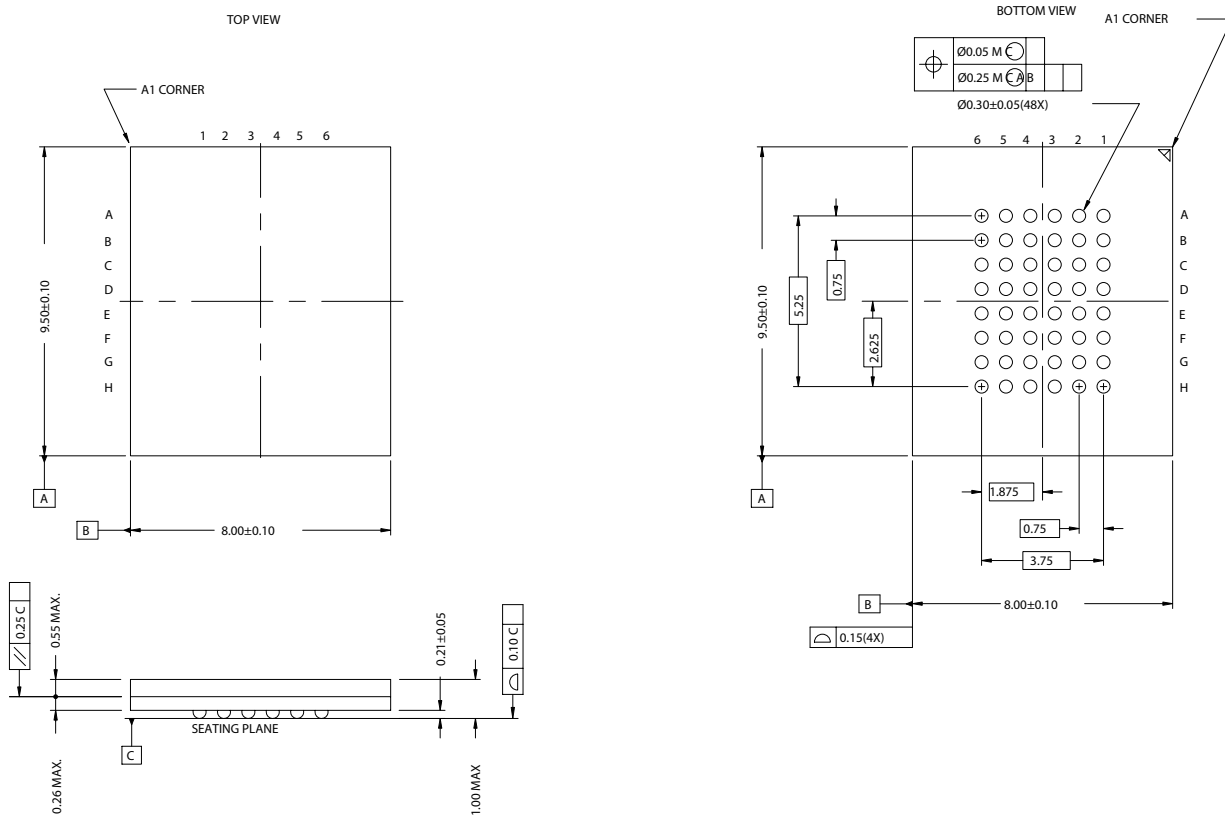
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167DV30LL-45ZXI	51-85183	48-pin TSOP I (12 x 18.4 x 1 mm) (Pb-free)	Industrial
55	CY62167DV30LL-55BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	
	CY62167DV30LL-55BVXI		48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) (Pb-free)	
	CY62167DV30LL-55ZI	51-85183	48-pin TSOP I (12 x 18.4 x 1 mm)	
	CY62167DV30LL-55ZXI		48-pin TSOP I (12 x 18.4 x 1 mm) (Pb-free)	
70	CY62167DV30LL-70BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

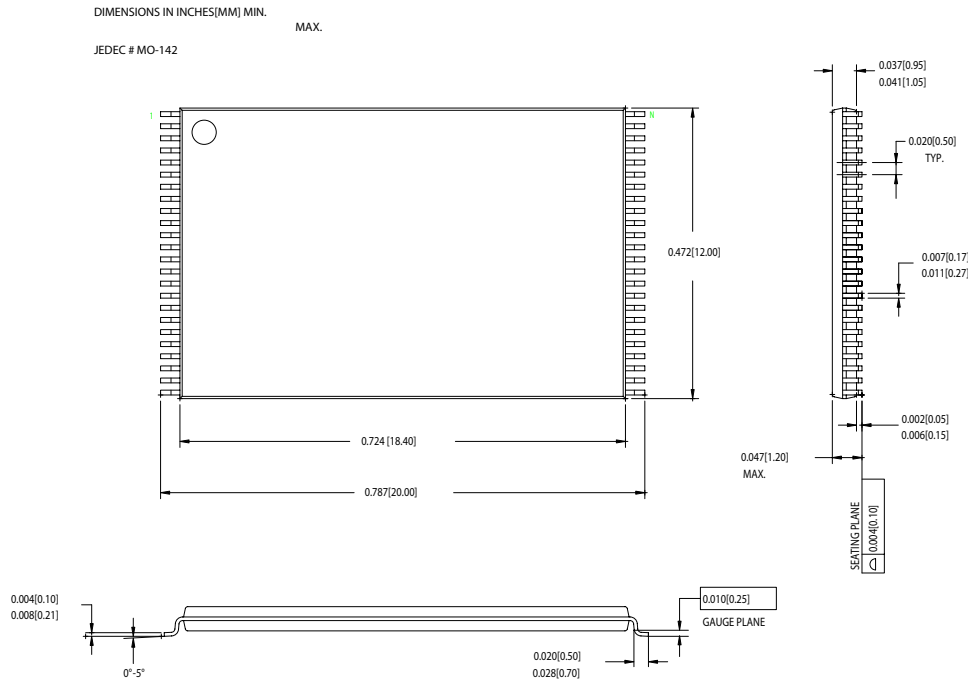
48-ball VFBGA (8 x 9.5 x 1 mm) (51-85178)



51-85178-**

Package Diagrams (continued)

48-pin TSOP I (12 x 18.4 x 1mm) (51-85183)



51-85183-A

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Document History Page

Document Title: CY62167DV30 MoBL®, 16-Mbit (1M x 16) Static RAM Document Number: 38-05328				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	118408	09/30/02	GUG	New Data Sheet
*A	123692	02/11/03	DPM	Changed Advanced to Preliminary Added package diagram
*B	126555	04/25/03	DPM	Minor change: Changed Sunset Owner from DPM to HRT
*C	127841	09/10/03	XRJ	Added 48 TSOP I package
*D	205701		AJU	Changed BYTE pin usage description for 48 TSOPI package
*E	238050	See ECN	KKV/AJU	Replaced 48-ball VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B
*F	304054	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #12 on page #4 Added Pb-free packages on page # 10
*G	492895	See ECN	VKN	Modified datasheet to explain x8 configurability Removed L power bin from the product offering Updated Ordering Information Table