512K x 16 Static RAM

Features

- **Temperature Ranges**
  - **Automotive-A: –40°C to 85°C**
  - **Automotive-E: –40°C to 125°C**
- **Voltage range:**
  - **CY62157CV30: 2.7V–3.3V**
  - **CY62157CV33: 3.0V–3.6V**
- **Ultra-low active power**
  - **Typical active current: 1.5 mA @ f = 1 MHz**
  - **Typical active current: 5.5 mA @ f = f_{max}**
- **Low standby power**
- **Easy memory expansion with $\overline{CE_1}$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball FBGA package**

Functional Description[1]

The CY62157CV30/33 are high-performance CMOS static RAMs organized as 512K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected (CE_1 HIGH or CE_2 LOW or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable 2 (CE_2) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

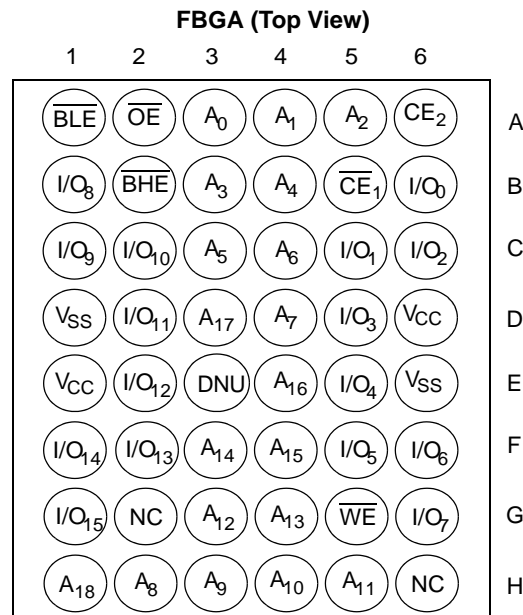The CY62157CV30/33 are available in a 48-ball FBGA package.

Logic Block Diagram
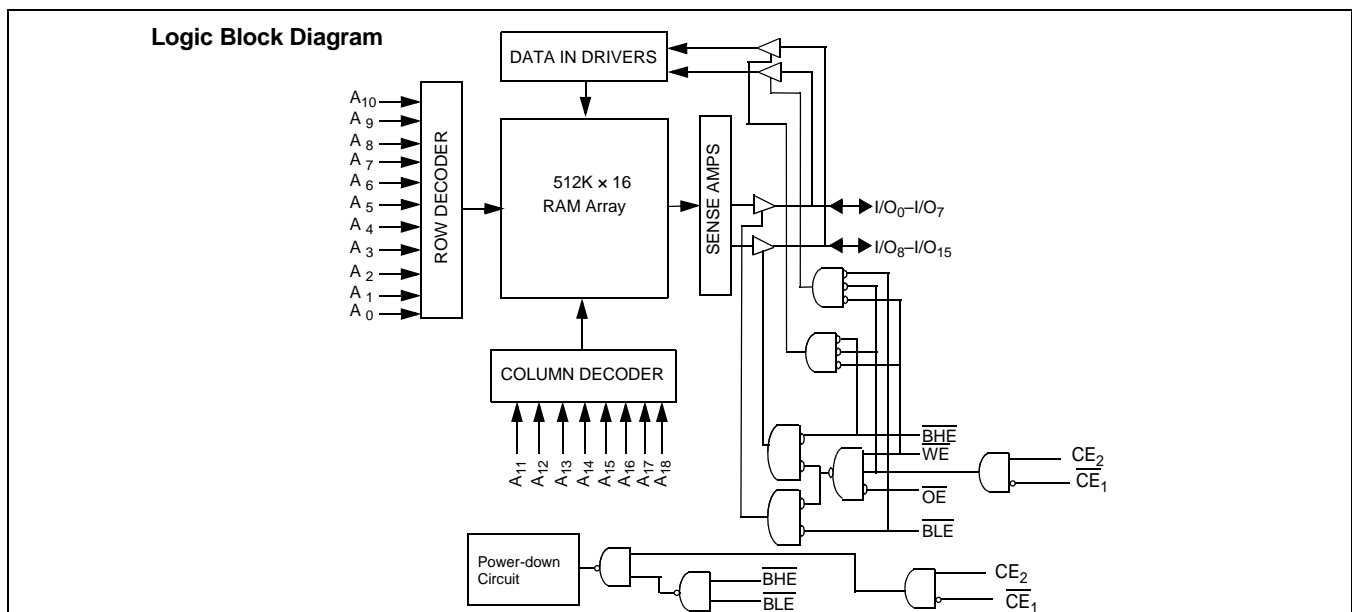
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

[+] Feedback

Product Portfolio

Product	Range	V_{CC} Range			Power Dissipation					
					Operating (I_{CC}) mA				Standby (I_{SB2}) μA	
					f = 1 MHz		f = f_{max}			
		Min.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
CY62157CV30	Automotive-E	2.7V	3.0V	3.3V	1.5	3	7	15	8	70
CY62157CV33	Automotive-A	3.0V	3.3V	3.6V	1.5	3	5.5	12	10	30
	Automotive-E				1.5	3	7	15	10	80

Pin Configurations[2, 3, 4]

FBGA (Top View)

Pin Definitions

Name	Definition
Input	A_0-A_{18}. Address Inputs
Input/Output	I/O_0-I/O_{15}. Data lines. Used as input or output lines depending on operation
Input/Control	$\overline{WE}$. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	$\overline{CE_1}$. Chip Enable 1, Active LOW.
Input/Control	CE_2. Chip Enable 2, Active HIGH.
Input/Control	$\overline{OE}$. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins
Ground	**Vss**. Ground for the device
Power Supply	**Vcc**. Power supply for the device

Notes:
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25°C.
3. NC pins are not connected on the die.
4. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential ...–0.5V to V_{ccmax} + 0.5V

DC Voltage Applied to Outputs
in High-Z State[5] ....–0.5V to V_{CC} + 0.3V

DC Input Voltage[5]................................–0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW) ....20 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current .... > 200 mA

Operating Range

Device	Range	Ambient Temperature [T_A][6]	V_{CC}
CY62157CV30	Automotive-E	–40°C to +125°C	2.7V – 3.3V
CY62157CV33	Automotive-A	–40°C to +85°C	3.0V – 3.6V
	Automotive-E	–40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62157CV30-70 Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage			–0.3		0.8	V
I_{IX}	Input Leakage Current	GND $\le V_I \le V_{CC}$		–10		+10	μA
I_{OZ}	Output Leakage Current	GND $\le V_O \le V_{CC}$, Output Disabled		–10		+10	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = 3.3V I_{OUT} = 0 mA CMOS Levels		7	15	mA
		f = 1 MHz			1.5	3	
I_{SB1}	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \ge V_{CC}$ – 0.2V or $CE_2 \le$ 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = f_{max} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)			8	70	μA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \ge V_{CC}$ – 0.2V or $CE_2 \le$ 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0, V_{CC} = 3.3V			8	70	μA

Notes:
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
6. T_A is the "Instant-On" case temperature.

Electrical Characteristics Over the Operating Range

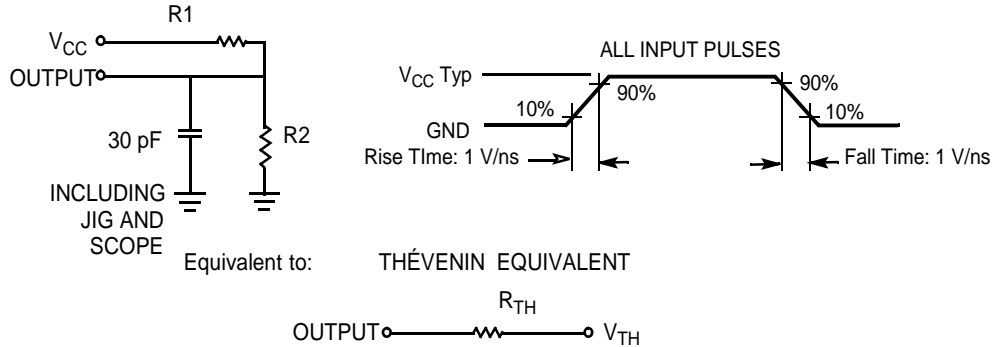| Parameter	Description	Test Conditions			CY62157CV33-70			Unit
					Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0$ mA $V_{CC} = 3.0V$			2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA $V_{CC} = 3.0V$					0.4	V
V_{IH}	Input HIGH Voltage				2.2		$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage				−0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		Auto-A	−1		+1	μA
				Auto-E	−10		+10	μA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		Auto-A	−1		+1	μA
				Auto-E	−10		+10	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V$ $I_{OUT} = 0$ mA CMOS Levels	Auto-A		5.5	12	mA
				Auto-E		7	15	
		$f = 1$ MHz		Auto-A/ Auto-E		1.5	3	
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $f = f_{max}$ (Address and Data Only), $f = 0$ ($\overline{OE}, \overline{WE}, \overline{BHE},$ and $\overline{BLE}$)		Auto-A		10	30	μA
				Auto-E		10	80	μA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \ge V_{CC} - 0.2V$ or $CE_2 \le 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $f = 0$, $V_{CC} = 3.6V$		Auto-A		10	30	μA
				Auto-E		10	80	μA

Thermal Resistance[7]

Parameter	Description	Test Conditions	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		16	°C/W

Note:
7. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms

Parameters	3.0V	3.3V	Unit
R1	1.105	1.216	KΩ
R2	1.550	1.374	KΩ
R_{TH}	0.645	0.645	KΩ
V_{TH}	1.75	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5V$, $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Auto-A		4	20	μA
			Auto-E		4	60	μA
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[8]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[9]
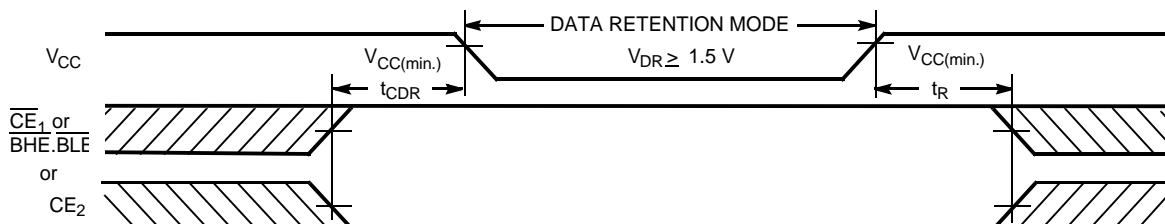
Notes:
8. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 100 μs or stable at $V_{CC(min.)}$ >100 μs.
9. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

[+] Feedback

Switching Characteristics Over the Operating Range [10]

| Parameter	Description	70 ns Min.	70 ns Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[11]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[11, 12]		25	ns
t_{LZCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Low-Z[11]	10		ns
t_{HZCE}	$\overline{CE_1}$ HIGH or CE_2 LOW to High-Z[11, 12]		25	ns
t_{PU}	$\overline{CE_1}$ LOW and CE_2 HIGH to Power-up	0		ns
t_{PD}	$\overline{CE_1}$ HIGH or CE_2 LOW to Power-down		70	ns
t_{DBE}	$\overline{BHE}/\overline{BLE}$ LOW to Data Valid		70	ns
t_{LZBE}[11]	$\overline{BHE}/\overline{BLE}$ LOW to Low-Z[13]	5		ns
t_{HZBE}	$\overline{BHE}/\overline{BLE}$ HIGH to High-Z[11, 12]		25	ns
Write Cycle[14]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{BW}	$\overline{BHE}/\overline{BLE}$ Pulse Width	60		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	5		ns

Notes:
10. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}$/2, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. When both byte enables are toggled together this value is 10 ns.
14. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, CE_2 = V_{IH}. All signals must be ACTIVE to initiate a Write and any of these signals can terminate a Write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[15, 16]
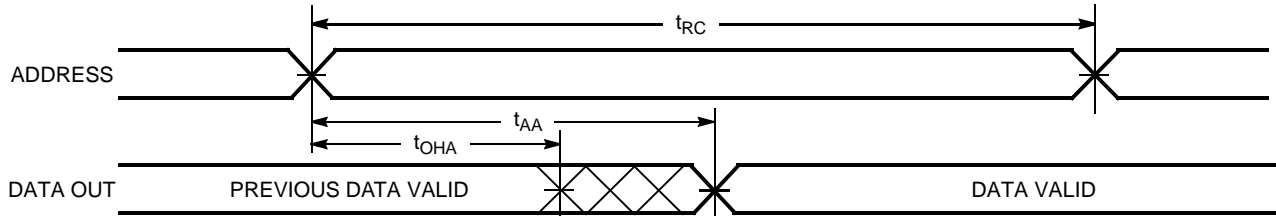
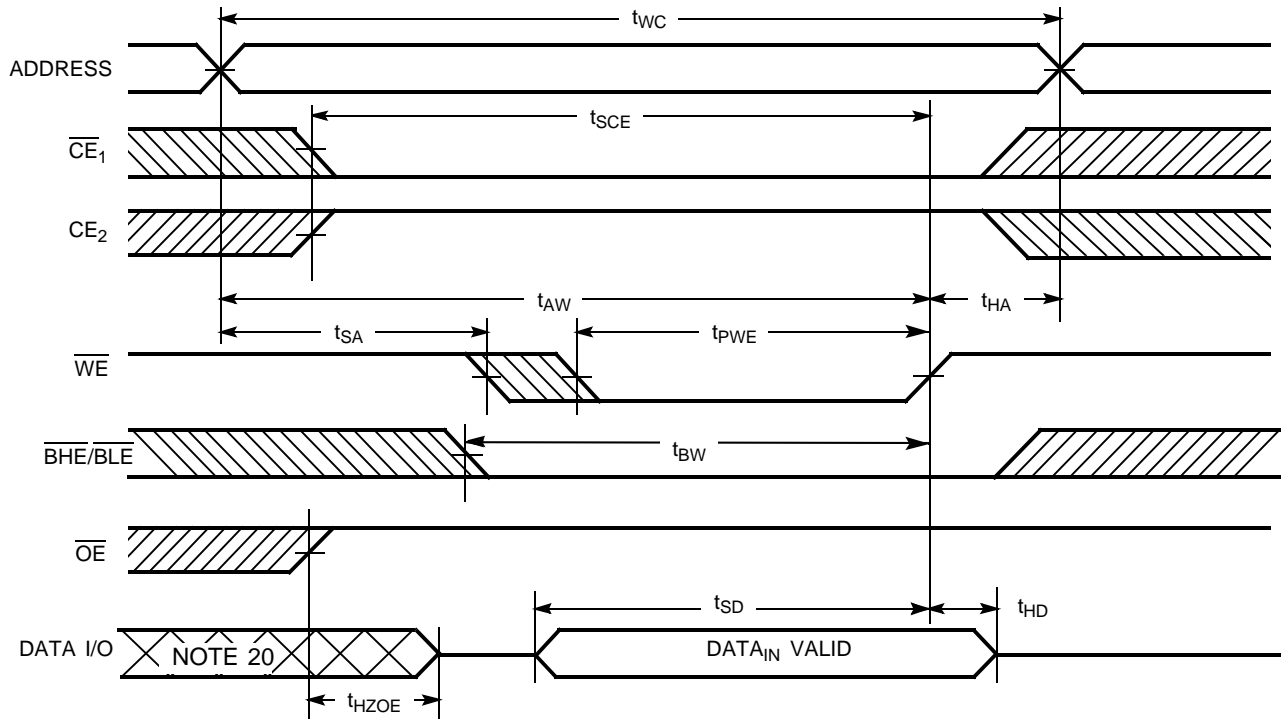### Read Cycle No. 2 ($\overline{OE}$ Controlled)[16, 17]
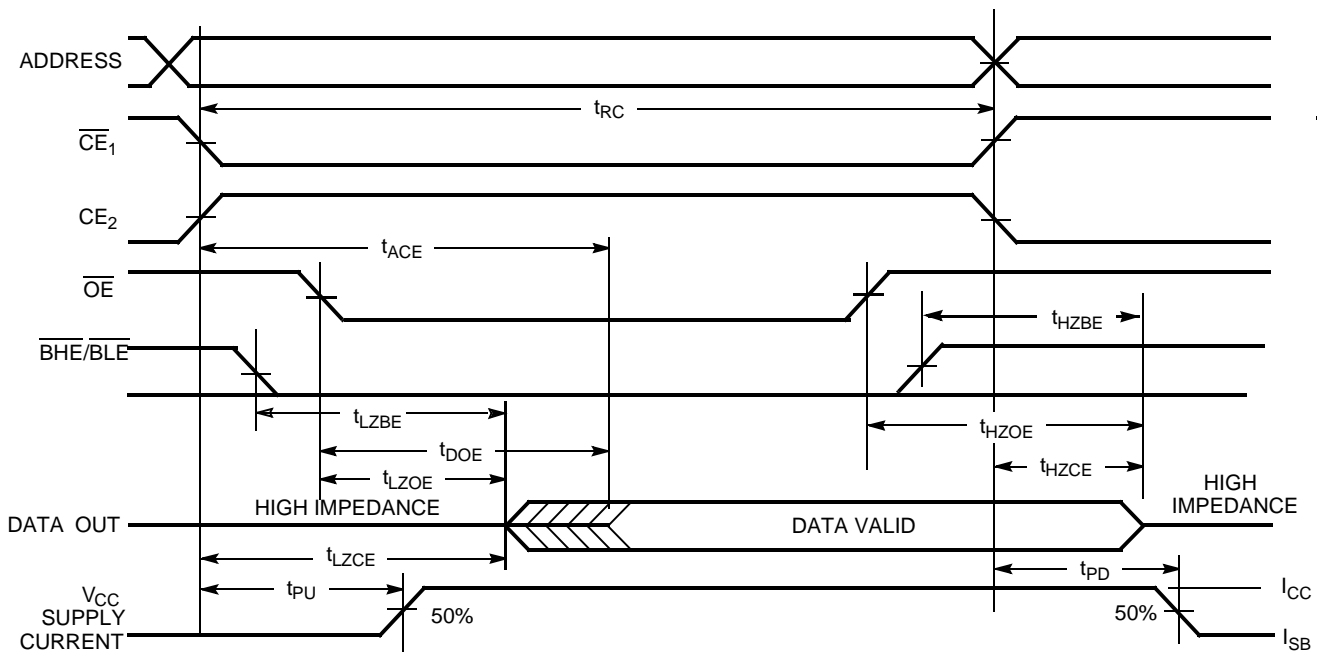
Notes:
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, $CE_2 = V_{IH}$.
16. $\overline{WE}$ is HIGH for Read cycle.
17. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[14, 18, 19]

Notes:
18. Data I/O is high-impedance if $\overline{\text{OE}}$ = V_{IH}.
19. If $\overline{\text{CE}}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}_1$ or CE$_2$ Controlled) [14, 18, 19]
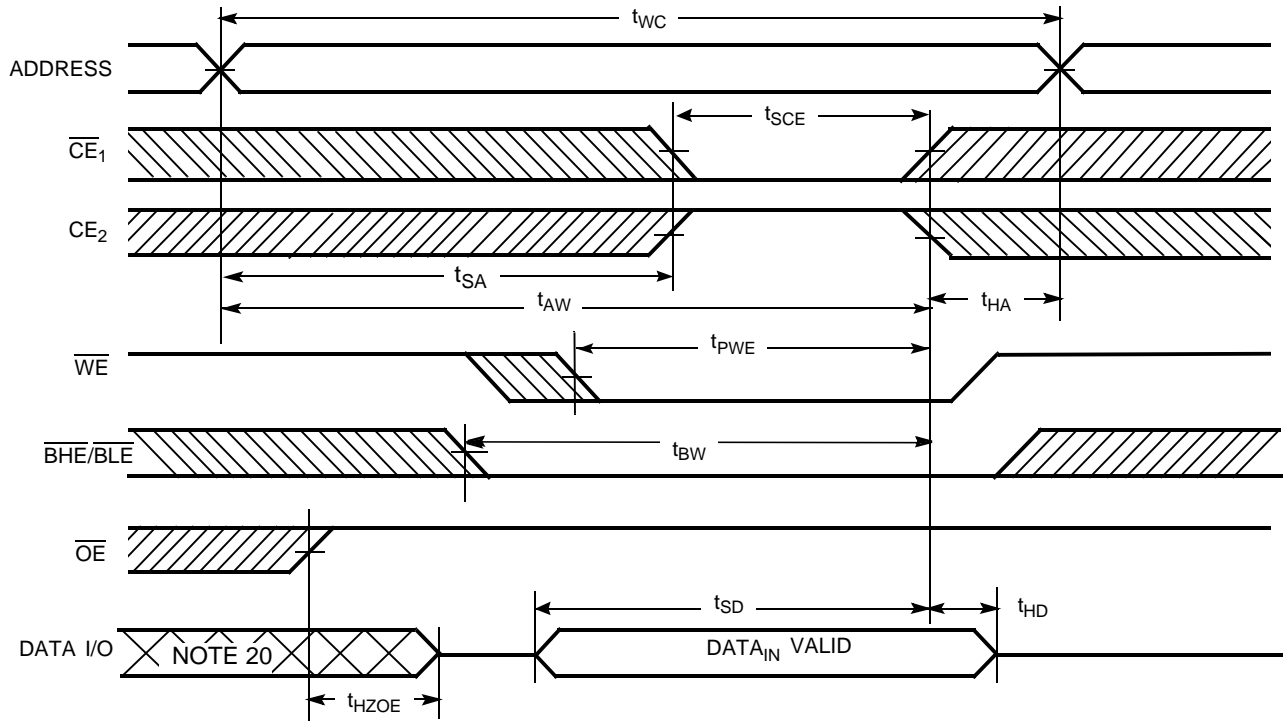
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[19]

[+] Feedback
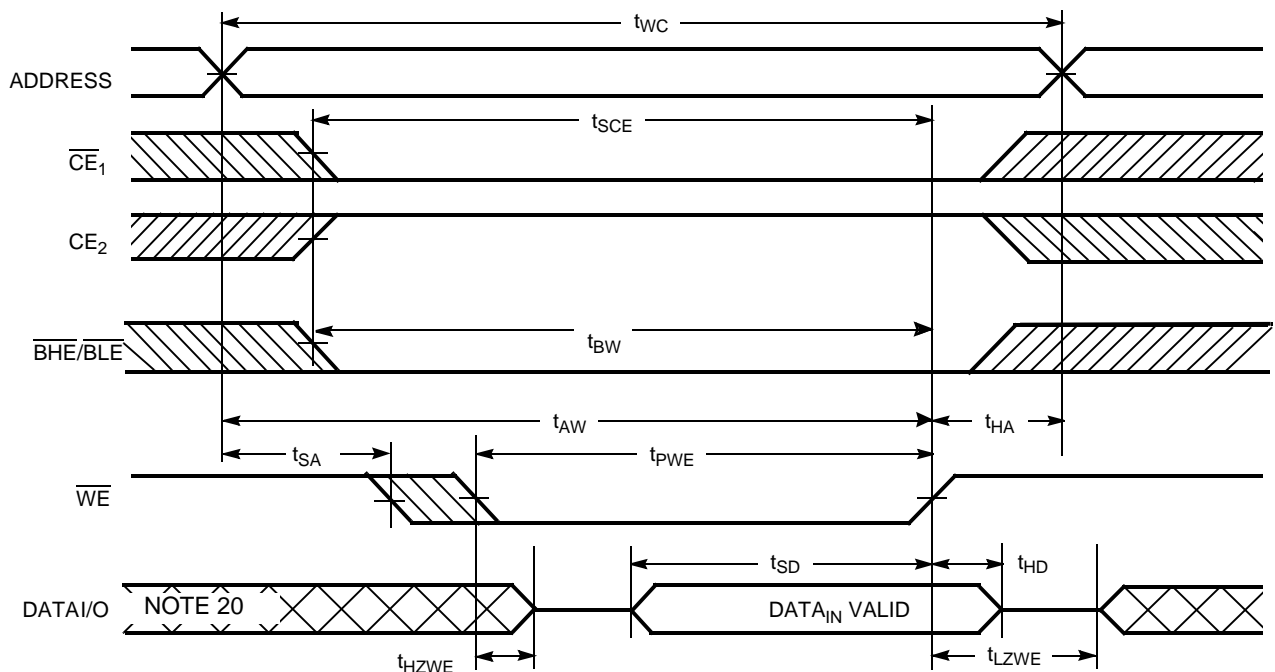
Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[19]
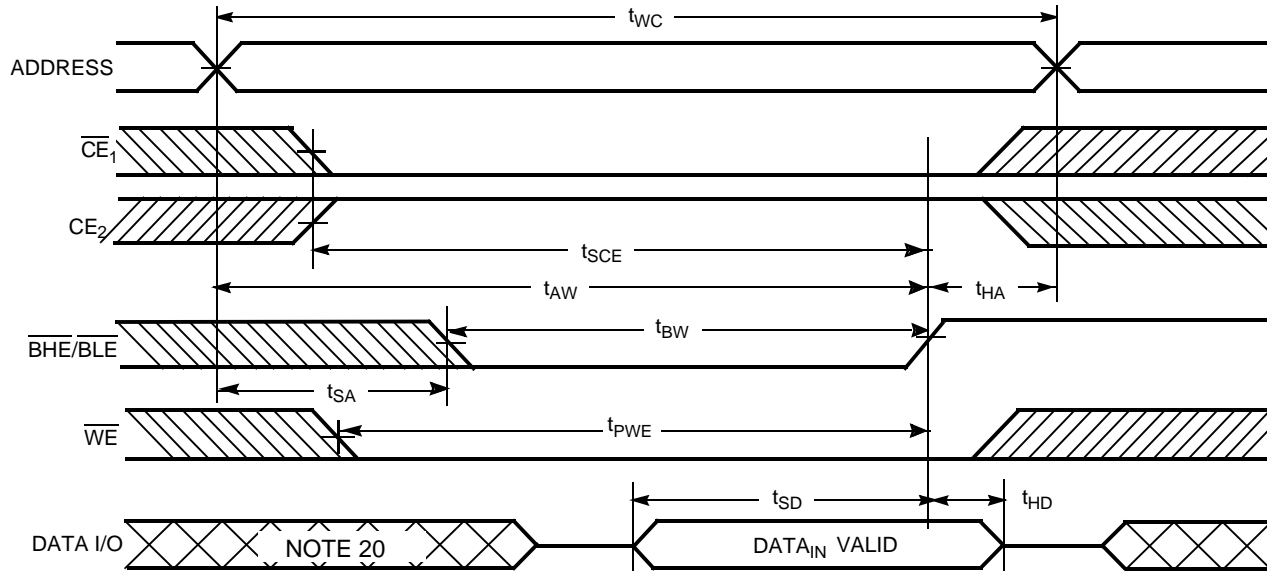

Truth Table

CE$_1$	CE$_2$	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I$_{SB}$)
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I$_{SB}$)
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I$_{SB}$)
L	H	H	L	L	L	Data Out (I/O$_O$–I/O$_{15}$)	Read	Active (I$_{CC}$)
L	H	H	L	H	L	Data Out (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z	Read	Active (I$_{CC}$)
L	H	H	L	L	H	Data Out (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High Z	Read	Active (I$_{CC}$)
L	H	H	H	L	L	High Z	Output Disabled	Active (I$_{CC}$)
L	H	H	H	H	L	High Z	Output Disabled	Active (I$_{CC}$)
L	H	H	H	L	H	High Z	Output Disabled	Active (I$_{CC}$)
L	H	L	X	L	L	Data In (I/O$_O$–I/O$_{15}$)	Write	Active (I$_{CC}$)
L	H	L	X	H	L	Data In (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z	Write	Active (I$_{CC}$)
L	H	L	X	L	H	Data In (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High Z	Write	Active (I$_{CC}$)

[+] Feedback
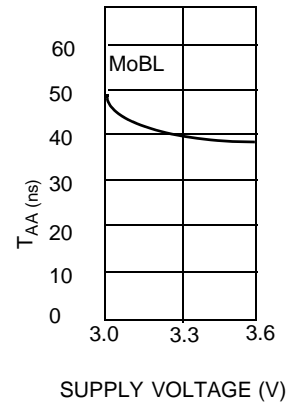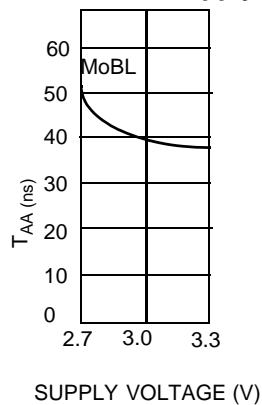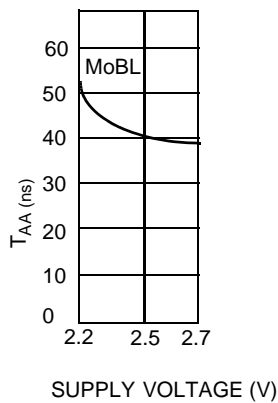
Typical DC and AC Characteristics [2]

Operating Current vs. Supply Voltage
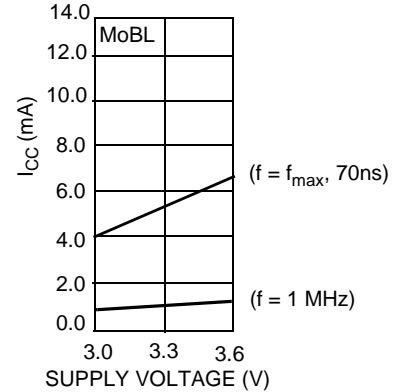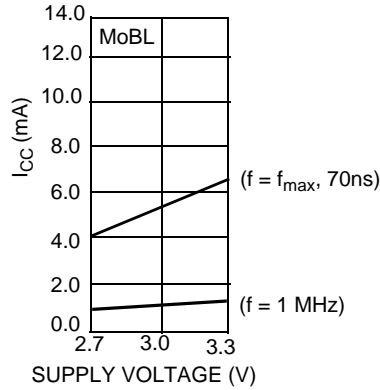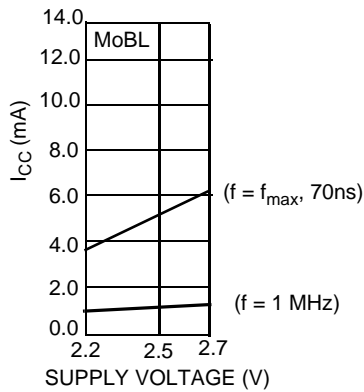
Standby Current vs. Supply Voltage
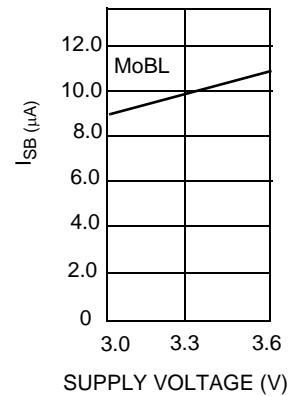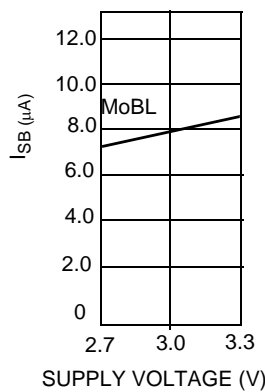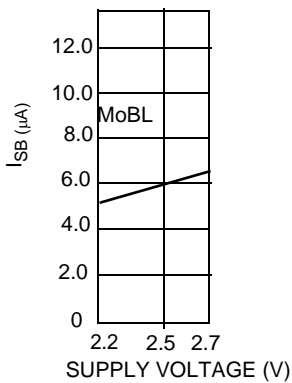
Access Time vs. Supply Voltage

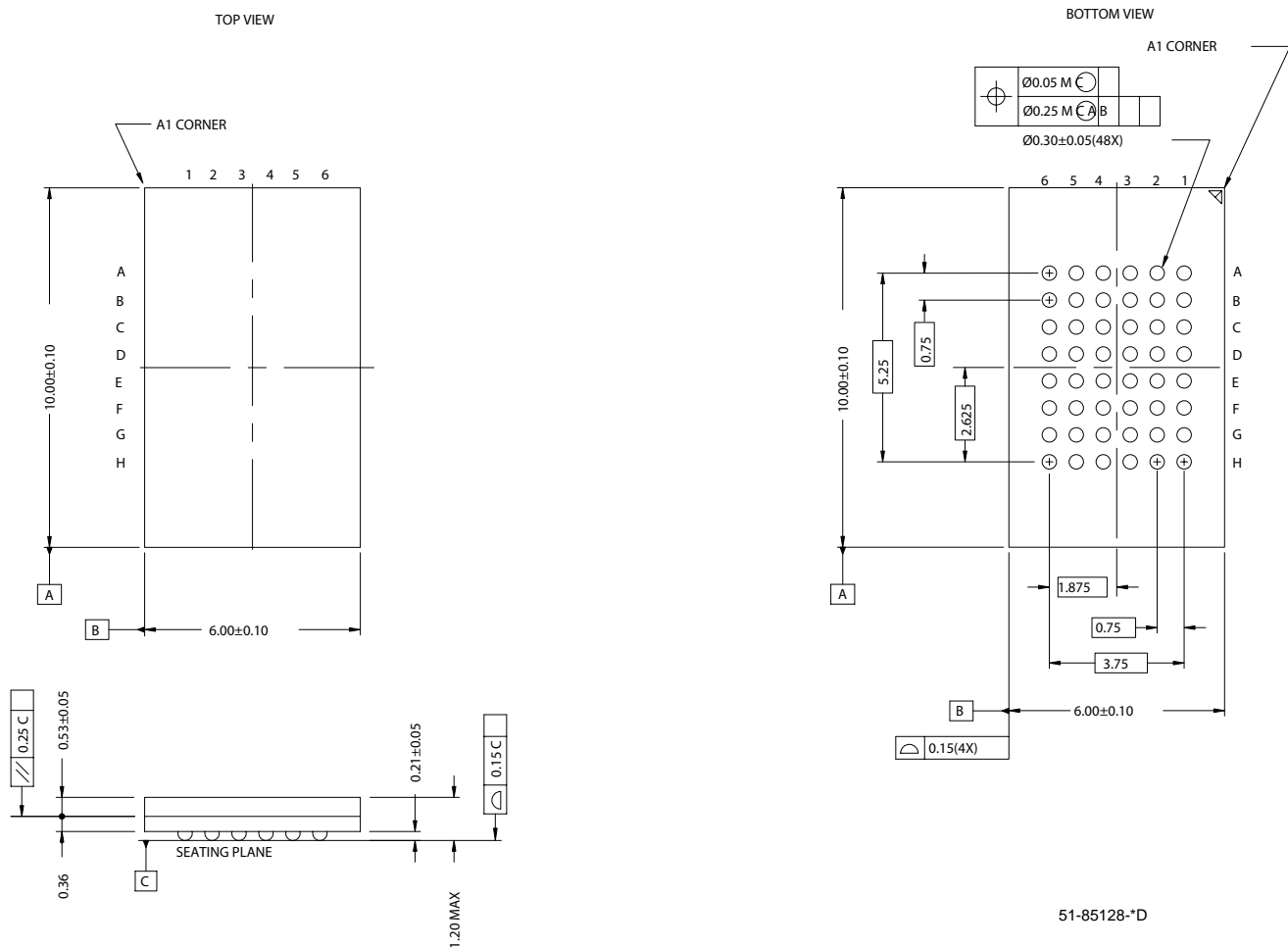## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62157CV30LL-70BAE	51-85128	48-Ball (6 mm x 10 mm x 1.2 mm) FBGA	Automotive-E
	CY62157CV33LL-70BAXA			Automotive-A
	CY62157CV33LL-70BAE			Automotive-E

Package Diagram

48-Ball (6 mm x 10 mm x 1.2 mm) FBGA (51-85128)

51-85128-*D

MoBL, MoBL2, and More Battery Life are trademarks of Cypress Semiconductor Corporation. All product and company names mentioned in this document may be the trademarks of their respective holders.

[+] Feedback

Document History Page

Document Title: CY62157CV30/33 512K x 16 Static RAM
Document Number: 38-05014

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106184	05/10/01	HRT/MGN	New data sheet – Advance Information
*A	107241	07/24/01	MGN	Made corrections to Advance Information Added 55 ns bin
*B	109621	03/11/02	MGN	Changed from Advance Information to Final
*C	114218	05/01/02	GUG/MGN	Improved Typical and Max I_{CC} values
*D	238448	See ECN	AJU	Added Automotive Product Information
*E	269729	See ECN	SYT	Added Automotive Product information for CY62157CV30 – 70 ns Added I_{IX} and I_{OZ} values for Automotive range of CY62157CV33 – 70 ns
*F	498575	See ECN	NXR	Removed Industrial Operating Range Removed 55 ns speed bin Removed CY62157CV25 part number from the Product Offering Added Automotive-A operating range Updated the Ordering Information Table

[+] Feedback