

## 4-Mbit (256K x 16) Static RAM

### Features

- **Very high speed: 45 ns**
- **Wide voltage range: 1.65V–2.25V**
- **Pin-compatible with CY62147DV18**
- **Ultra low standby power**
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- **Ultra-low active power**
  - Typical active current: 2 mA @ f = 1 MHz
- **Ultra low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$ , and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in a 48-ball Pb-free VFBGA package**

### Functional Description<sup>[1]</sup>

The CY62147EV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

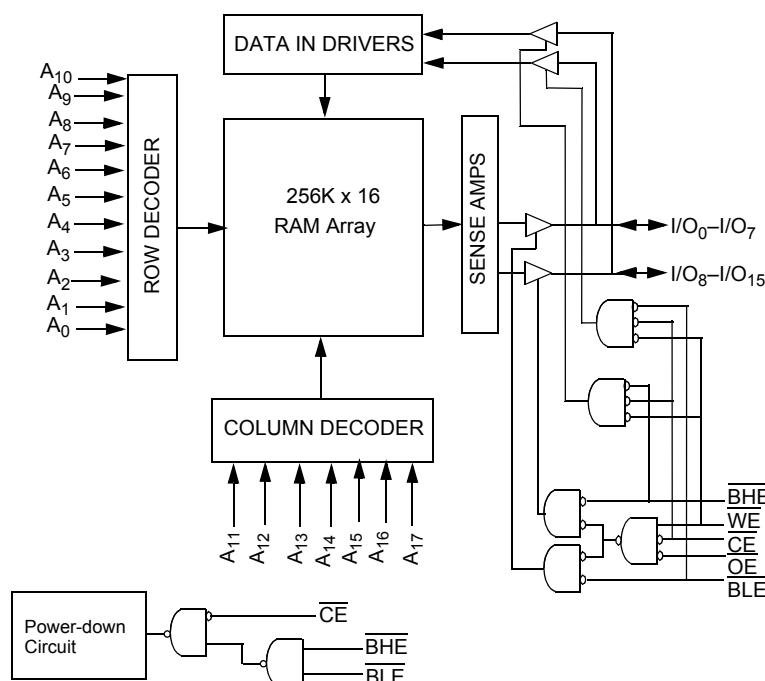
also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH or both  $\overline{\text{BLE}}$  and  $\overline{\text{BHE}}$  are HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both  $\overline{\text{Byte High Enable}}$  and  $\overline{\text{Byte Low Enable}}$  are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147EV18 is available in a 48-ball VFBGA package.

### Logic Block Diagram

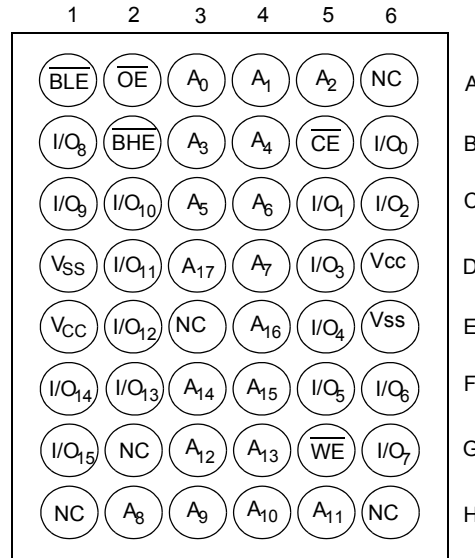


#### Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Pin Configuration<sup>[2, 3]</sup>

**48-ball VFBGA Pinout  
Top View**



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
	Min.	Typ. <sup>[4]</sup>	Max.		Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.
CY62147EV18-45LL	1.65	1.8	2.25	45	2	2.5	15	20	1	7

**Notes:**

- NC pins are not connected on the die.
- Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with

Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground

Potential ..... -0.2V to + 2.45V ( $V_{CCMAX} + 0.2V$ )

DC Voltage Applied to Outputs

in High-Z State<sup>[5,6]</sup> ..... -0.2V to 2.45V ( $V_{CCMAX} + 0.2V$ )

DC Input Voltage<sup>[5,6]</sup> ..... -0.2V to 2.45V ( $V_{CCMAX} + 0.2V$ )

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[7]</sup>
CY62147EV18	Industrial	-40°C to +85°C	1.65V to 2.25V

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$ $V_{CC} = 1.65V$	1.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$ $V_{CC} = 1.65V$			0.2	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 1.65V \text{ to } 2.25V$	1.4		$V_{CC} + 0.2V$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 1.65V \text{ to } 2.25V$	-0.2		0.4	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	$\mu A$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	$\mu A$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ $V_{CC(max)} = 2.25V$ $I_{OUT} = 0 \text{ mA}$ CMOS levels		15	20	mA
		$f = 1 \text{ MHz}$ $V_{CC(max)} = 2.25V$		2	2.5	mA
$I_{SB1}$	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE and BLE)		1	7	$\mu A$
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$		1	7	$\mu A$

## Capacitance (for all Packages) <sup>[8]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1 \text{ MHz}$ , $V_{CC} = V_{CC(typ)}$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

### Note:

5.  $V_{IL(min.)} = -2.0V$  for pulse durations less than 20 ns.

6.  $V_{IH(max)} = V_{CC} + 0.5V$  for pulse durations less than 20 ns.

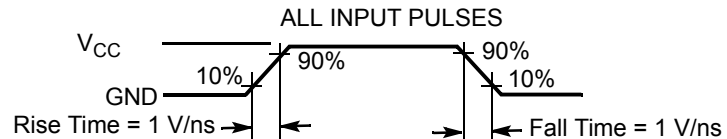
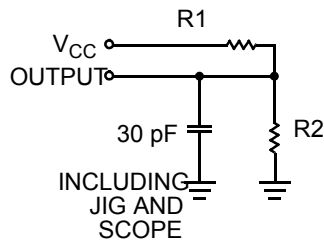
7. Full device AC operation assumes a minimum of 100  $\mu s$  ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu s$  wait time after  $V_{CC}$  stabilization.

8. Tested initially and after any design or process changes that may affect these parameters.

## Thermal Resistance

Parameter	Description	Test Conditions	VFBGA Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient) <sup>[8]</sup>	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case) <sup>[8]</sup>		10	°C/W

## AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

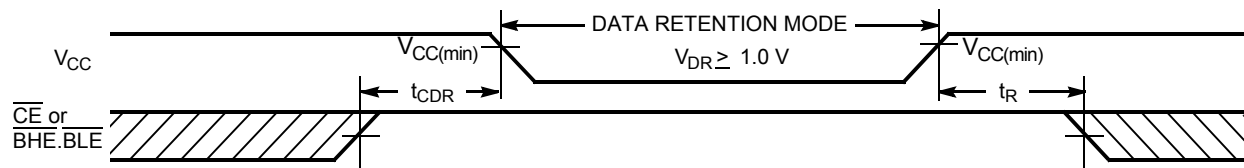


Parameters	1.80V	Unit
R1	13500	$\Omega$
R2	10800	$\Omega$
$R_{TH}$	6000	$\Omega$
$V_{TH}$	0.80	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V$ $\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.5	3	$\mu A$
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform<sup>[10]</sup>



### Notes:

9. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100 \mu s$  or stable at  $V_{CC(min.)} \geq 100 \mu s$ .

10. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

**Switching Characteristics** (Over the Operating Range) <sup>[11]</sup>

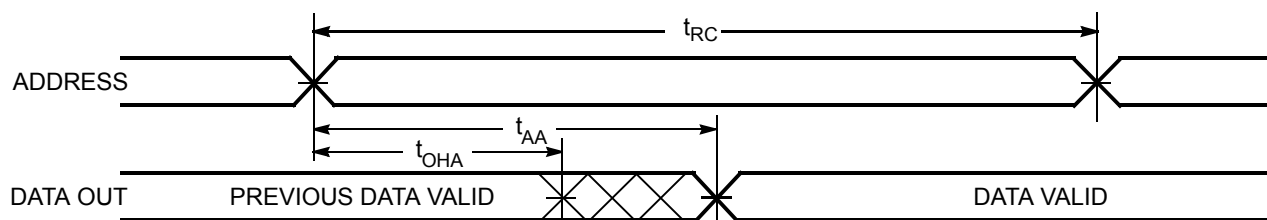
Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t <sub>RC</sub>	Read Cycle Time	45		ns
t <sub>AA</sub>	Address to Data Valid		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		45	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		22	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to LOW Z <sup>[12]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[12, 13]</sup>		18	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[12]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[12, 13]</sup>		18	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-up	0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-down		45	ns
t <sub>DBE</sub>	$\overline{\text{BLE/BHE}}$ LOW to Data Valid		45	ns
t <sub>LZBE</sub>	$\overline{\text{BLE/BHE}}$ LOW to Low Z <sup>[12]</sup>	10		ns
t <sub>HZBE</sub>	$\overline{\text{BLE/BHE}}$ HIGH to HIGH Z <sup>[12, 13]</sup>		18	ns
Write Cycle <sup>[14]</sup>				
t <sub>WC</sub>	Write Cycle Time	45		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	35		ns
t <sub>AW</sub>	Address Set-up to Write End	35		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	35		ns
t <sub>BW</sub>	$\overline{\text{BLE/BHE}}$ LOW to Write End	35		ns
t <sub>SD</sub>	Data Set-up to Write End	25		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High-Z <sup>[12, 13]</sup>		18	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[12]</sup>	10		ns

**Notes:**

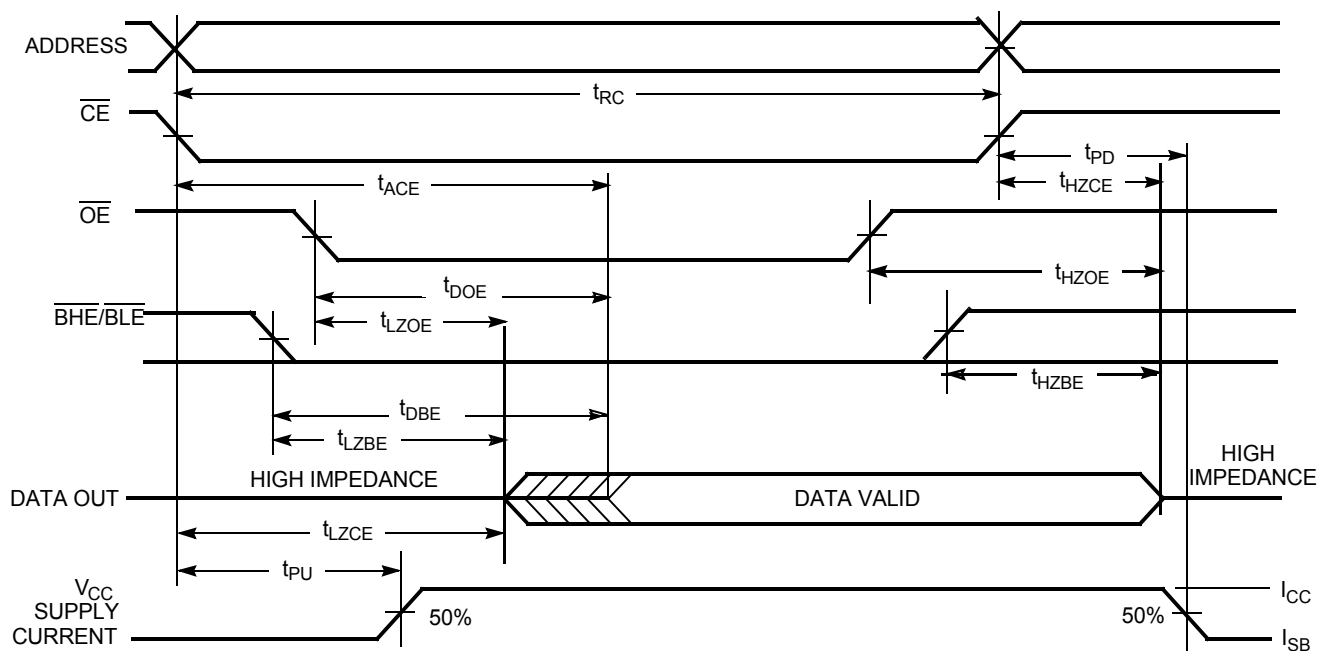
11. Test conditions for all parameters other than three-state parameters assume signal transition time of 1V/ns or less, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" section.
12. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
13. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
14. The internal Write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle 1 (Address Transition Controlled)<sup>[15, 16]</sup>



### Read Cycle No. 2 ( $\overline{\text{OE}}$ Controlled)<sup>[16, 17]</sup>



#### Notes:

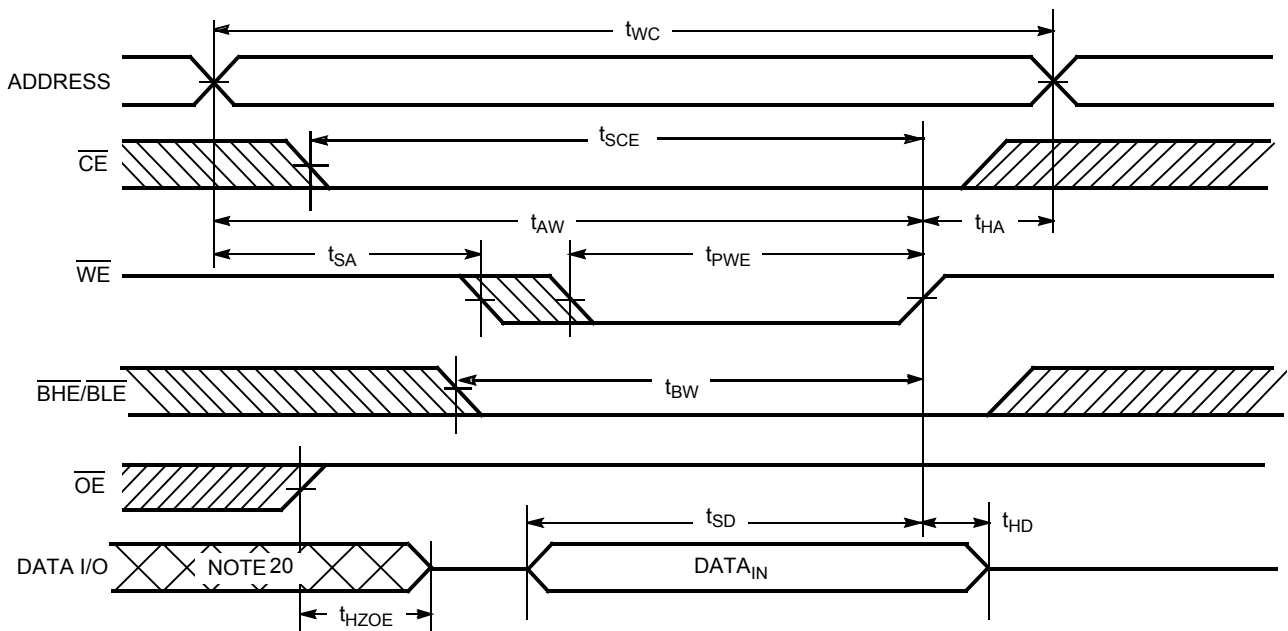
15. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}}$  =  $V_{\text{IL}}$ .

16.  $\overline{\text{WE}}$  is HIGH for read cycle.

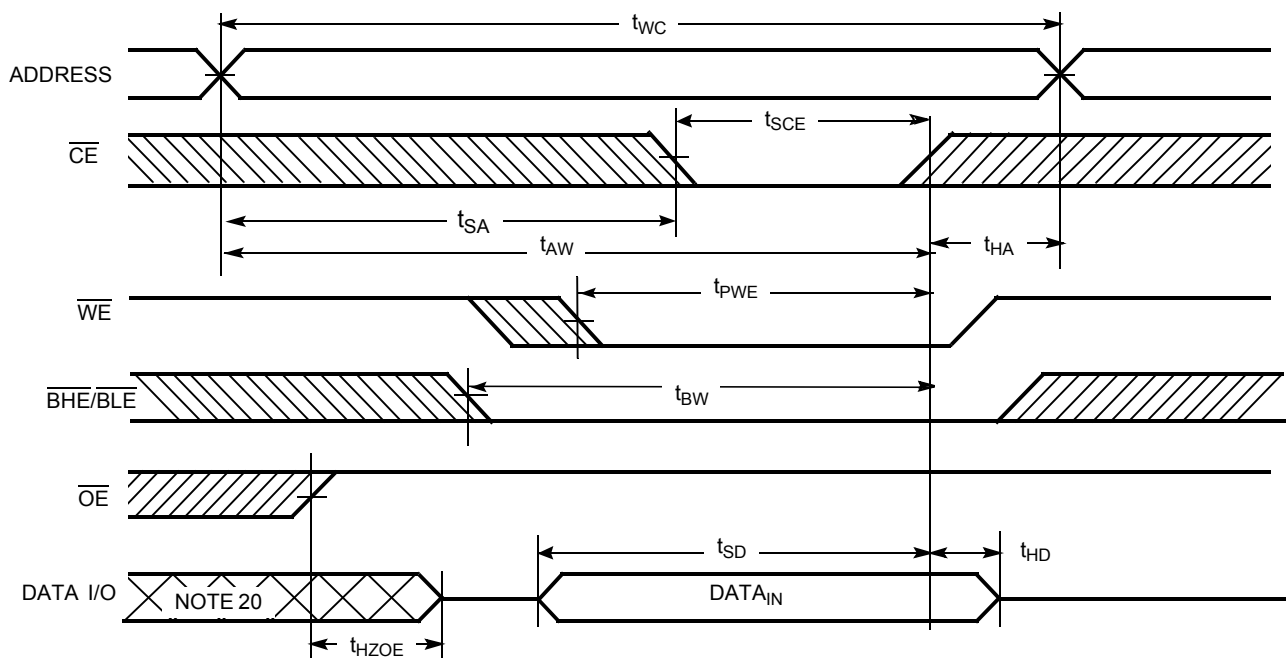
17. Address valid prior to or coincident with  $\overline{\text{CE}}$  and  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 ( $\overline{\text{WE}}$ Controlled)<sup>[14, 18, 19]</sup>



### Write Cycle No. 2 ( $\overline{\text{CE}}$ Controlled)<sup>[14, 18, 19]</sup>

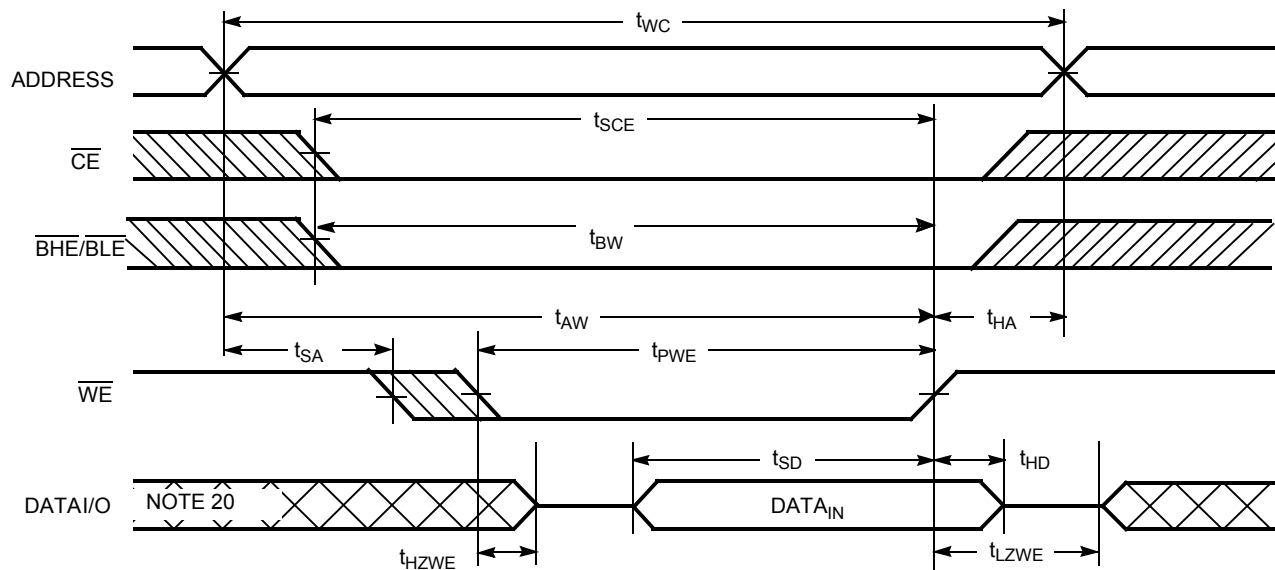


#### Notes:

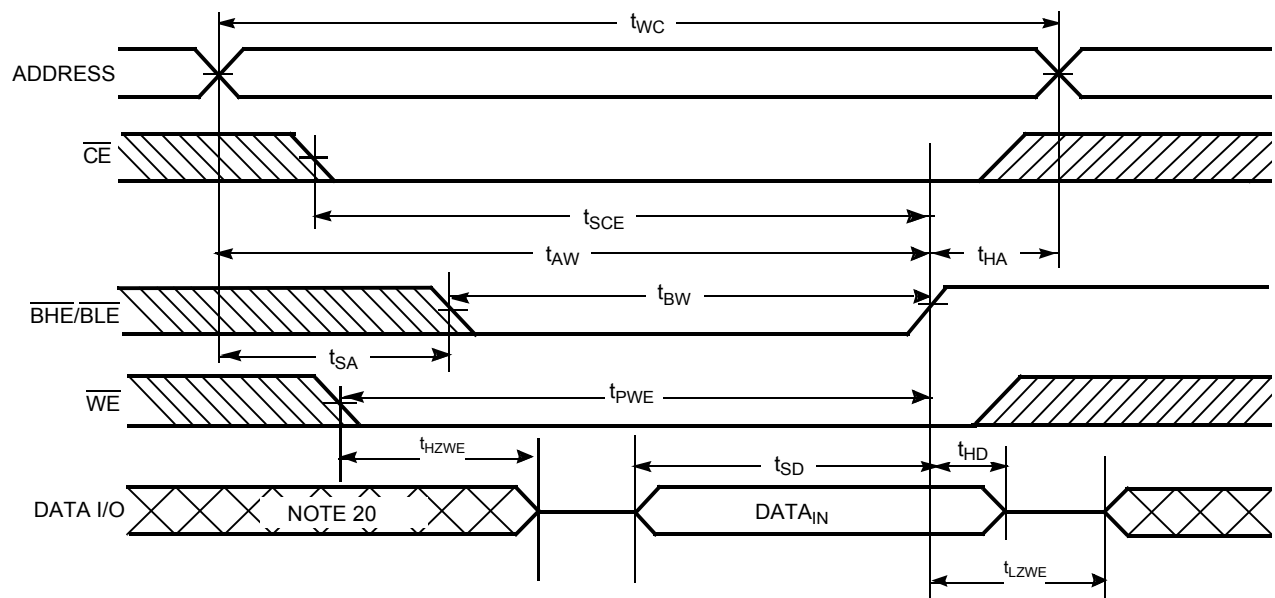
18. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
19. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{IH}$ , the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

### Write Cycle No. 3 ( $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)<sup>[19]</sup>



### Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)<sup>[19]</sup>





**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	X	X	H	H	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

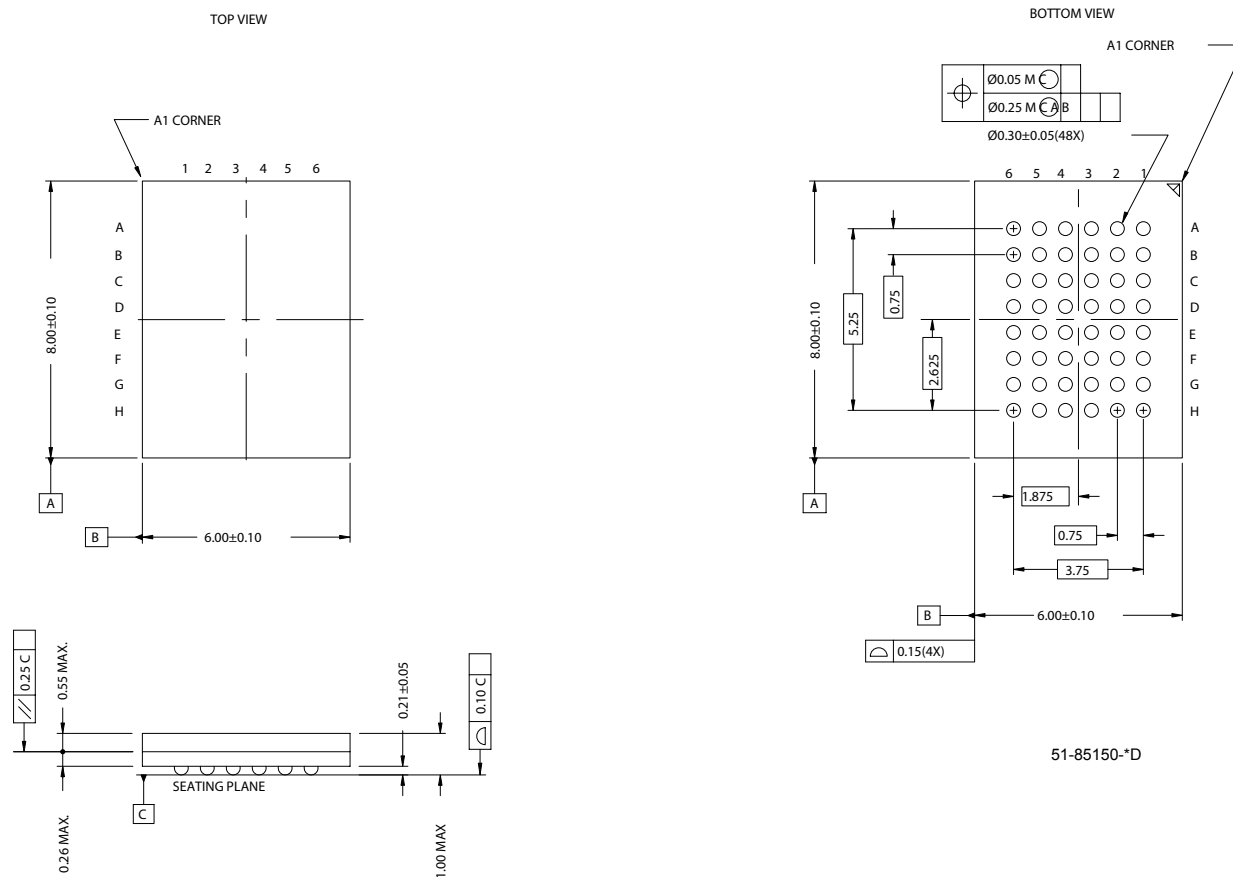
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV18LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array Pb-Free	Industrial

Please contact your local Cypress sales representative for availability of other parts

## Package Diagram

### 48-pin VFBGA (6 x 8 x 1 mm) (51-85150)



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**Document History Page**

Document Title: CY62147EV18 MoBL2™ 4-Mbit (256K x 16) Static RAM Document Number: 38-05441				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201580	01/08/04	AJU	New Data Sheet
*A	247009	See ECN	SYT	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Changed $V_{CCMax}$ from 2.20 to 2.25 V Changed $V_{CC}$ stabilization time in footnote #8 from 100 $\mu$ s to 200 $\mu$ s Removed Footnote #15 ( $t_{LZBE}$ ) from Previous Revision Changed $I_{CCDR}$ from 2.0 $\mu$ A to 2.5 $\mu$ A Changed typo in Data Retention Characteristics ( $t_R$ ) from 100 $\mu$ s to $t_{RC}$ ns Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed $t_{HZOE}$ , $t_{HZBE}$ , $t_{HZWE}$ from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed $t_{SCE}$ and $t_{BW}$ from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed $t_{HZCE}$ from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed $t_{SD}$ from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed $t_{DOE}$ from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414820	See ECN	ZSD	Changed from Preliminary to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court" Removed 35ns Speed Bin Removed "L" version of CY62147EV18 Changed ball E3 from DNU to NC Changed $I_{CC}$ (Typ) value from 1.5 mA to 2 mA at $f=1$ MHz Changed $I_{CC}$ (Max) value from 2 mA to 2.5 mA at $f=1$ MHz Changed $I_{CC}$ (Typ) value from 12 mA to 15 mA at $f=f_{max}$ Changed $I_{SB1}$ and $I_{SB2}$ Typ. values from 0.7 $\mu$ A to 1 $\mu$ A and Max. values from 2.5 $\mu$ A to 7 $\mu$ A. Extended undershoot limit to -2V in footnote #5 Changed $I_{CCDR}$ Max. from 2.5 $\mu$ A to 3 $\mu$ A. Added $I_{CCDR}$ typical value. Changed $t_{LZOE}$ from 3 ns to 5 ns Changed $t_{LZCE}$ , $t_{LZBE}$ and $t_{LZWE}$ from 6 ns to 10 ns Changed $t_{HZCE}$ from 22 ns to 18 ns Changed $t_{PWE}$ from 30 ns to 35 ns. Changed $t_{SD}$ from 22 ns to 25 ns. Updated the package diagram 48-pin VFBGA from *B to *D Updated the ordering information table and replaced Package Name column with Package Diagram