CY22180

Very Low Jitter Field and Factory Programmable Clock Generator

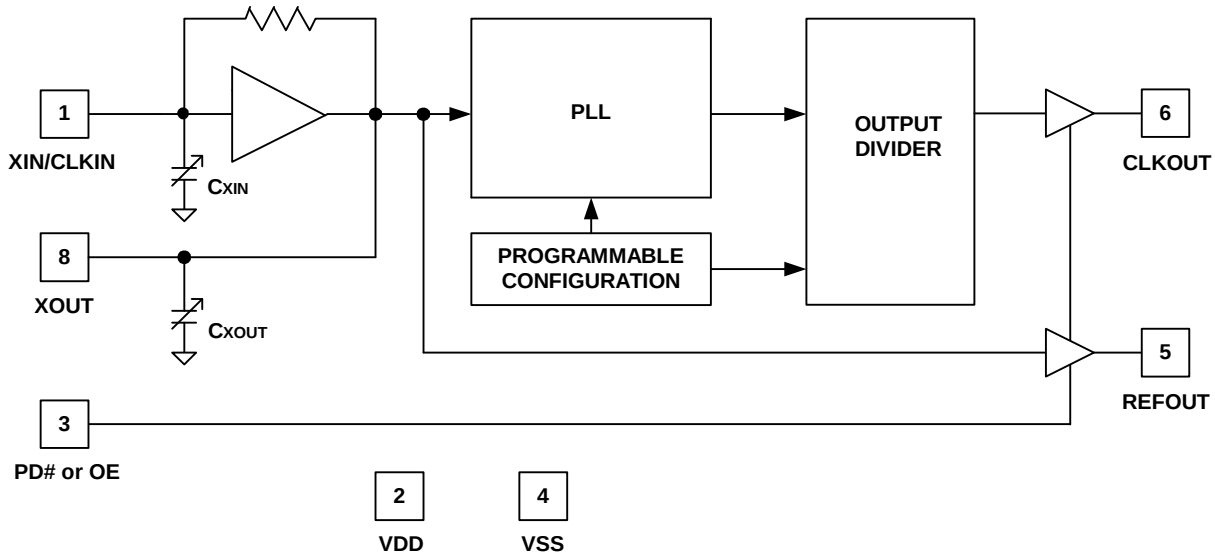
Features

- Low period and cycle-to-cycle jitter
  - Typical pk-pk period jitter: 60 ps
- Wide output frequency range
  - Commercial temperature: 20–200 MHz
  - Industrial temperature: 20–166 MHz
- Input frequency range
  - External crystal: 10–30 MHz fundamental crystal
  - External reference: 10–133 MHz clock
- Integrated phase-locked loop (PLL)
- Field programmable and factory programmed options
- Programmable crystal load capacitor tuning array
- 3.3V operation
- Commercial and industrial temperature ranges
- Power down or output enable function

Benefits

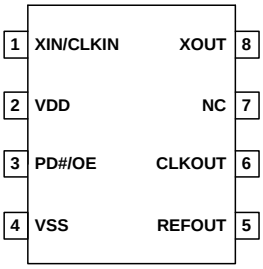
- Internal PLL generates up to 200 MHz output. Can generate custom frequencies from an external crystal or a driven source.
- In-house programming of samples and prototype quantities can be done using the CY3672-USB programmer and CY3619 socket adapter. Production quantities are available through Cypress's value added distribution partners or by using third party programmers from BP Microsystems, HiLo Systems, and others.
- Eliminates the need for expensive and difficult to use higher-order crystals.
- Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal. Eliminates the need for external C_{Load} capacitors.
- Application compatibility in standard and low-power systems
- Enables low-power state or output clocks to High-Z state

Logic Block Diagram



Pinouts

Figure 1. CY22180 - 8-Pin SOIC



Pin Definitions

Pin	Name	Description
1	XIN/CLKIN	Crystal input or reference clock input.
2	VDD	3.3V power supply.
3	PD#/OE	Power down pin, active LOW. If PD# = 0, the PLL and oscillator are powered down and outputs are weakly pulled low. Output enable pin, active HIGH. If OE = 1, CLKOUT and REFOUT are enabled. User has the option of choosing either PD# or OE function.
4	VSS	Power supply ground.
5	REFOUT	Buffered reference output.
6	CLKOUT	Low jitter clock output.
7	NC	No connect. Leave this pin floating.
8	XOUT	Crystal output. Leave this pin floating if external clock is used.

General Description

The CY22180 is a low jitter clock generator for use in networking, telecommunication, datacom, consumer electronics, and other general purpose applications. The CY22180 offers a single programmable output and an optional copy of the input frequency. The on-chip reference oscillator is designed to run off a 10–30 MHz crystal, or a 10–133 MHz external clock signal. The output frequency range is 20–200 MHz. The CY22180 comes in an 8-pin SOIC, and requires a 3.3V power supply.

Programming Description

Field Programmable (CY22180FSXC and CY22180FSXI)

The CY22180 is programmed at the package level, that is, in a programmer socket. The CY22180 is flash technology based, so the parts can be reprogrammed up to 100 times. This enables fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed on the CY3672 programmer with the CY3619 socket adapter.

CyberClocks™ Online Software

CyberClocks Online Software is a web-based software application that allows the user to custom-configure the CY22180. All the parameters in Table 1 on page 3 given as “Enter Data” can be programmed into the CY22180. CyberClocks Online outputs an industry-standard JEDEC file used for programming the CY22180. CyberClocks Online is available at www.cyberclocksonline.com through user registration. For more information on the registration process refer to the CY3672 data sheet.

CY3672-USB Programming Kit and CY3619 Socket Adapter

The Cypress CY3672 FTG programmer and CY3619 socket adapter are needed to program the CY22180. The socket adapter comes with small prototype quantities of CY22180. The CY3619 can be ordered separately, so existing users of the CY3672-USB programmer need order only the socket adapters to program the CY22180.

Factory Programmed CY22180

Factory programming is available for volume manufacturing by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you receive a new part number (dash number) and samples with the programmed values. This part number is used for additional sample requests and production orders.

Additional information on the CY22180 can be obtained from the Cypress website at www.cypress.com.

Table 1. Pin Function

Pin Function	Input Frequency	Total Xtal Load Capacitance	Output Frequency	Reference Output	Power down or Output Enable
Pin Name	XIN and XOUT	XIN and XOUT	CLKOUT	REFOUT	PD#/OE
Pin#	1 and 8	1 and 8	6	5	3
Unit	MHz	pF	MHz	On or Off	Select PD# or OE
Program Value	ENTER DATA	ENTER DATA	ENTER DATA	ENTER DATA	ENTER DATA

Product Functions

Input Frequency (XIN, pin 1 and XOUT, pin 8)

The input to the CY22180 can be a crystal or a clock. The input frequency range for crystals is 10 to 30 MHz, and for clock signals is 10 to 133 MHz.

C_{XIN} and C_{XOUT} (pin 1 and pin 8)

The internal load capacitors at pin 1 (C_{XIN}) and pin 8 (C_{XOUT}) can be programmed from 12 pF to 60 pF in 0.5 pF increments. Thus, these programmable capacitors support crystals with C_L values between 6 pF and 30 pF. The crystal C_L value, minus board parasitic capacitance, is the value entered into Cyber-Clocks Online Software.

If using a driven reference, CyberClocks Online Software sets C_{XIN} and C_{XOUT} to the minimum value 12 pF.

Output Clock (CLKOUT, pin 6)

The output clock can be programmed to any frequency in the range of 20–200 MHz.

Reference Output (REFOUT, pin 5)

The reference clock output has the same frequency as the input clock. This output can be programmed to be enabled (clock on) or disabled (High-Z, clock off) through CyberClocks Online software. If this output is not needed, Cypress recommends that users request the disabled (High-Z, Clock Off) option.

Power Down or Output Enable (PD# or OE, pin 3)

The CY22180 can be programmed to include either PD# or OE function. PD# function can be used to power down the oscillator and PLL. The OE function disables the outputs but does not turn off the PLL. PD# achieves lower power consumption, but PLL start up time means that turn-on time is slower than for OE.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... –0.5 to +7.0V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5
Storage Temperature (Non-condensing) .... –55°C to +125°C
Junction Temperature ..... –40°C to +125°C

Data Retention at Tj = 125°C ..... > 10 years
Package Power Dissipation ..... 350 mW
Static Discharge Voltage ..... ≥ 2000V (per MIL-STD-883, Method 3015) I

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ.	Max	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	10	–	30	MHz
C_{LNOM}	Nominal Load Capacitance		6	–	30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	–	25	Ω
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Supply Voltage	3.13	3.30	3.45	V
T_A	Ambient Commercial Temperature	0	–	70	°C
	Ambient Industrial Temperature	–40	–	85	°C
C_{LOAD}	Max. Load Capacitance at pin 5 and pin 6	–	–	10	pF
F_{XIN}	External Reference Crystal	10	–	30	MHz
F_{CLKIN}	External Reference Clock	10	–	133	MHz
F_{CLKOUT}	CLKOUT frequency, Commercial Temperature	20	–	200	MHz
	CLKOUT frequency, Industrial Temperature	20	–	166	MHz
F_{REFOUT}	REFOUT frequency	10	–	133	MHz
T_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5V$, V_{DD} = 3.3V (source)	10	12		mA
I_{OL}	Output Low Current	V_{OL} = 0.5V, V_{DD} = 3.3V (sink)	10	12		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–0.3	–	$0.3V_{DD}$	V
I_{IH}	Input High Current, PD#/OE	V_{IN}= V_{DD}	–	–	10	µA
I_{IL}	Input Low Current, PD#/OE	V_{IN} = V_{SS}, pull up disabled	–	–	10	µA
		V_{IN} = V_{SS}, pull up enabled	–	–	55	µA
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = 0	–10		10	µA
C_{XIN} or C_{XOUT}[1]	Programmable Capacitance at pin 1 and pin 8	Capacitance at minimum setting	–	12	–	pF
		Capacitance at maximum setting	–	60	–	pF
C_{IN}[1]	Input Capacitance at PD#/OE		–	5	7	pF
I_{DD}	Supply Current	f_{IN} = 10 MHz, f_{OUT} = 33 MHz, REFOUT off	–	11	15	mA
I_{DDS}	Standby current	Device powered down with PD# = 0V (driven reference pulled down)	–	10	40	µA

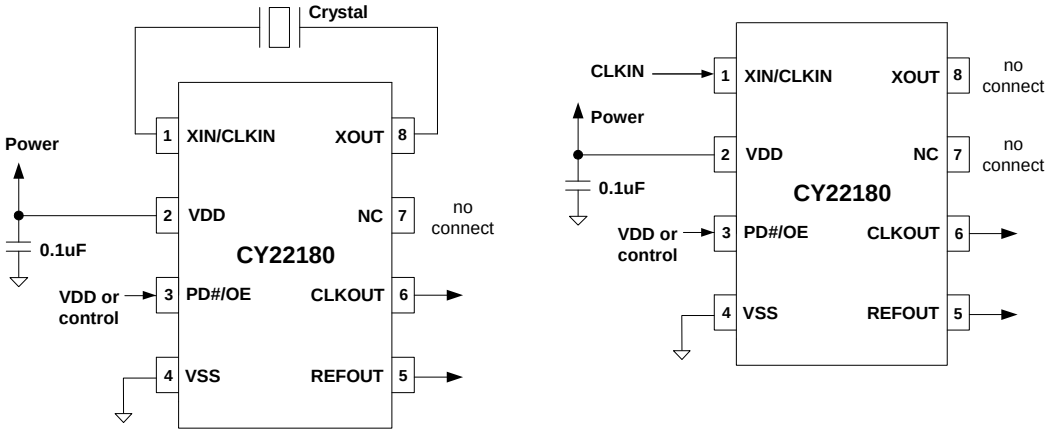
Note
1. Guaranteed by characterization, not 100% tested.

AC Electrical Characteristics[1]

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	CLKOUT ≤ 125 MHz, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	CLKOUT > 125 MHz, Measured at $V_{DD}/2$	40	50	60	%
	Output Duty Cycle	REFOUT, Measured at $V_{DD}/2$ Duty Cycle of CLKIN = 50%	45	50	55	%
SR1	Rising Edge Slew Rate	CLKOUT from 20 to 200 MHz; REFOUT from 10 to 133 MHz. 20%–80% of V_{DD}	2	3	–	V/ns
SR2	Falling Edge Slew Rate	CLKOUT from 20 to 200 MHz; REFOUT from 10 to 133 MHz. 80%–20% of V_{DD}	2	3	–	V/ns
T_{PJ1}[2, 3]	CLKOUT pk-pk Period Jitter, REFOUT off	CLKOUT = 20–200 MHz	–	–	75 (±38)	ps
T_{PJ2}[2, 3]	CLKOUT pk-pk Period Jitter, REFOUT off, specific frequencies	CLKIN = 10 MHz, CLKOUT = 20, 33, 66, 80, 106.25, 125, 133, or 200 MHz	–	–	60 (±30)	ps
		CLKIN = 25 MHz, CLKOUT = 125 MHz	–	–	56 (±28)	ps
		CLKIN = 30 MHz, CLKOUT = 33, 66, 80, 106.25, 125, or 133 MHz	–	–	62 (±31)	ps
		CLKIN = 66 MHz, CLKOUT = 33 or 66 MHz	–	–	47 (±24)	ps
		CLKIN = 66 MHz, CLKOUT = 80, 106.25, 125, 133, 166, or 200 MHz	–	–	68 (±34)	ps
		CLKIN = 133 MHz, CLKOUT = 33, 66, or 80 MHz	–	–	68 (±34)	ps
		CLKIN = 133 MHz, CLKOUT = 125, 133, or 166 MHz	–	–	52 (±26)	ps
T_{PJ3}[2, 3]	CLKOUT pk-pk Period Jitter, REFOUT on	CLKOUT = 20–200 MHz	–	150 (±75)	–	ps
T_{PJ4}[2, 3]	REFOUT pk-pk Period Jitter	REFOUT = 10-133 MHz	–	–	265 (±133)	ps
t_{STP}	Power Down Time (pin 3 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE1}	Output Disable Time (pin 3 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin 3 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
t_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3.5	5	ms
t_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous), reference clock at correct frequency	–	2	3	ms

Notes
2. Jitter is configuration dependent. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, temperature, and output load. For more information, refer to the application note, “Jitter in PLL Based Systems: Causes, Effects, and Solutions”.
3. Cycle-to-Cycle Jitter (peak) is always less than Period Jitter (peak-to-peak). Peak-to-Peak Period Jitter is the difference between the shortest and longest measured periods.

Figure 2. Application Circuits[4, 5]



Switching Waveforms

Figure 3. Duty Cycle Timing (DC = t_{1A}/t_{1B})

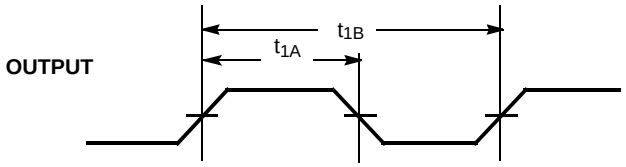
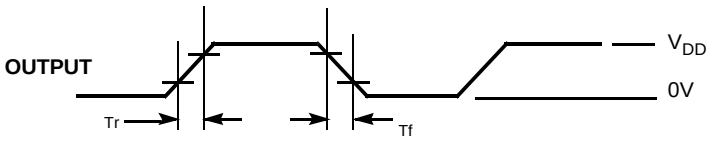


Figure 4. Output Rise/Fall Time (CLKOUT and REFOUT)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Notes
4. Since the load capacitors (C_{XIN} and C_{XOUT}) are provided by the CY22180, no external capacitors are needed on the XIN and XOUT pins to match the crystal load capacitor (C_L). Only a single 0.1-µF bypass capacitor is required on the V_{DD} pin.
5. If an external clock is used, apply the clock to XIN (pin 1) and leave XOUT (pin 8) floating (unconnected).

Switching Waveforms

Figure 5. Power Down Timing and Power Up Timing

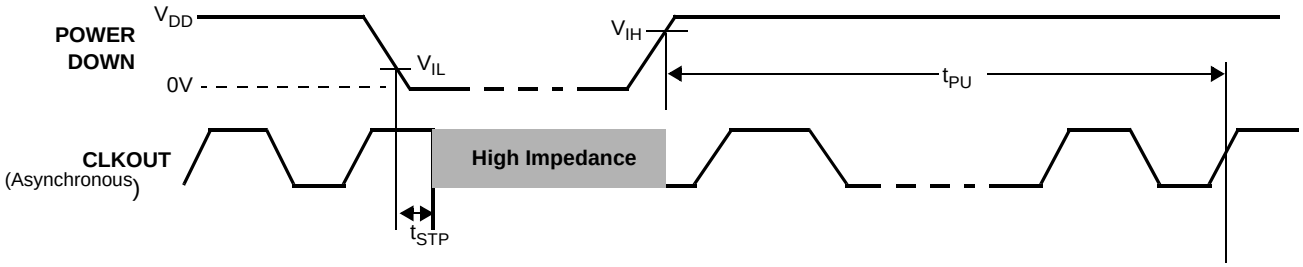
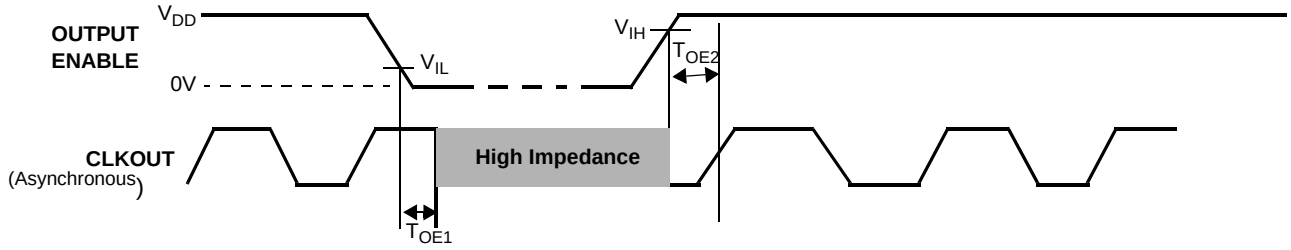


Figure 6. Output Enable/Disable Timing

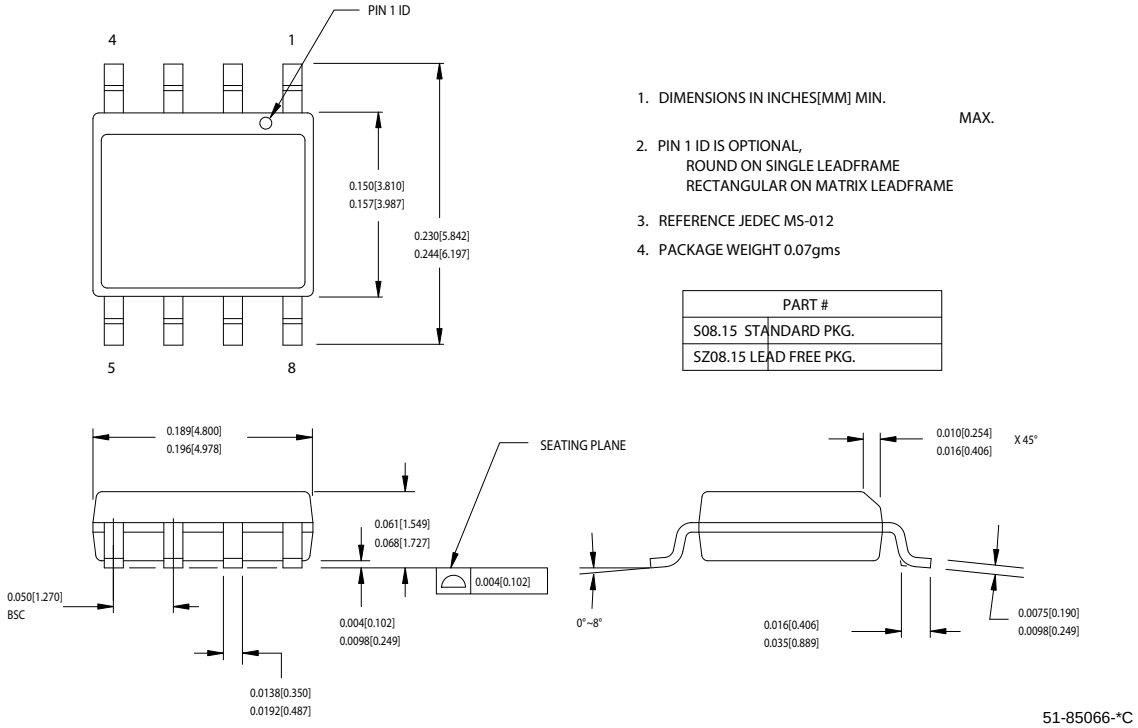


Ordering Information

Part Number[6]	Description	Product Flow
CY3672-USB	FTG programmer	n/a
CY3619	CY22180FS Socket Adapter for the CY3672-USB	n/a
Pb-Free		
CY22180FSXC	Field Programmable	Commercial, 0 to 70°C
CY22180FSXCT	Field Programmable - Tape and Reel	Commercial, 0 to 70°C
CY22180FSXI	Field Programmable	Industrial, –40 to 85°C
CY22180FSXIT	Field Programmable - Tape and Reel	Industrial, –40 to 85°C
CY22180SXC-xxx	Factory Programmed	Commercial, 0 to 70°C
CY22180SXC-xxxT	Factory Programmed - Tape and Reel	Commercial, 0 to 70°C
CY22180SXI-xxx	Factory Programmed	Industrial, –40 to 85°C
CY22180SXI-xxxT	Factory Programmed - Tape and Reel	Industrial, –40 to 85°C

Package Diagrams

Figure 7. 8-Pin (150-Mil) SOIC S8



Note
6. “xxx” denotes the assigned product dash number for devices that are factory-programmed.

Document History Page

Document Title: CY22180 Very Low Jitter Field and Factory Programmable Clock Generator Document Number: 001-15577				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1058460	KVM/ KKVTMP	05/11/07	New Data Sheet
*A	2632357	KVM/AESA	01/13/09	Change data sheet status from Preliminary to Final. Update template. Add part numbers CY22180FSXCT and CY22180FSXIT in Ordering Information table.

Sales, Solutions, and Legal Information

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