

# MediaClock™ MPEG Clock Generator with VCXO

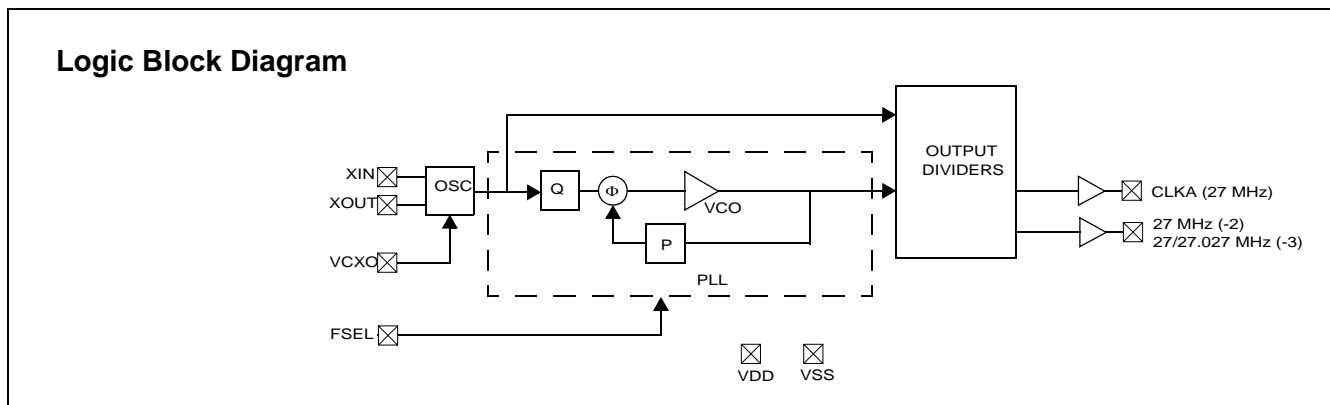
**Features**

- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation

**Benefits**

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large  $\pm 150$ -ppm range, better linearity
- Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24212-1	1	13.5 MHz/27 MHz (selectable)	27 MHz
CY24212-2	2	13.5 MHz/27 MHz (selectable)	Two copies of 27 MHz
CY24212-3	2	27 MHz	27 MHz/27.027 MHz (-1 ppm)
CY24212-5	2	27 MHz	27 MHz/27.027 MHz (0 ppm)



**Table 1. CY24212 (-1, -2) Frequency Select Option**

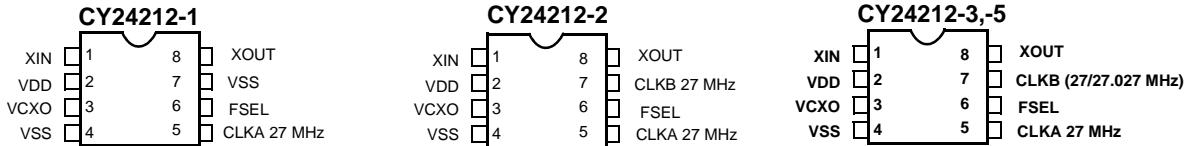
FSEL	Reference	CLKA/CLKB
0	13.5 MHz	27 MHz
1	27 MHz	27 MHz

**Table 2. CY24212 (-3, -5) Frequency Select Option**

FSEL	Reference	CLKA	CLKB
0	27 MHz	27 MHz	27 MHz
1	27 MHz	27 MHz	27.027 MHz

**Pin Configurations**

**Figure 1. CY24212, 8-pin SOIC**



**Table 3. Pin Definition**

Name	Pin Number	Description
XIN	1	Reference Input.
VDD	2	Voltage Supply.
VCXO	3	Input Analog Control for VCXO.
VSS	4	Ground.
CLKA	5	27-MHz Clock Output.
FSEL (-1,-2)	6	Input Frequency Select, Weak Internal Pull up. FSEL = 0, XIN = 13.5 MHz FSEL = 1, XIN = 27 MHz
FSEL (-3,-5)	6	Output Frequency Select, Weak Internal Pull up. FSEL = 0, CLKA = 27 MHz, CLKB = 27 MHz FSEL = 1, CLKA = 27 MHz, CLKB = 27.027 MHz
VSS (-1)	7	Ground.
CLKB (-2)	7	27 MHz.
CLKB (-3,-5)	7	27 MHz/27.027 MHz.
XOUT <sup>[1]</sup>	8	Reference Output.

**Pullable Crystal Specifications**

Parameter	Name	Min	Typ.	Max	Unit
CR <sub>load</sub>	Crystal Load Capacitance		14		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T <sub>o</sub>	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT <sub>s</sub>	Stability over Temperature and Aging			± 50	ppm

**Absolute Maximum Conditions**

Parameter	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[2]</sup>	-65	125	°C
T <sub>J</sub>	Junction Temperature		125	°C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electrostatic Discharge	2		kV

**Recommended Operating Conditions**

Parameter	Description	Min	Typ.	Max	Unit
V <sub>DD</sub>	Operating Voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max. Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency	13.5		27	MHz

**Notes**

1. Float XOUT if XIN is externally driven.
2. Rated for ten years.

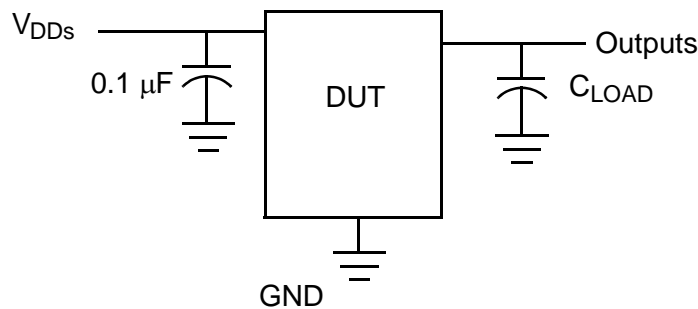
**DC Electrical Specifications**

Parameter	Name	Description	Min	Typ	Max	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V (source)	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V (sink)	12	24		mA
C <sub>IN</sub>	Input Capacitance				7	pF
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>	-	5	10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V	-	-	50	μA
f <sub>ΔXO</sub>	VCXO Pullability Range		±150			ppm
V <sub>VCXO</sub>	VCXO Input Range		0		V <sub>DD</sub>	V
I <sub>DD</sub>	Supply Current	Sum of Core and Output Current			35	mA
V <sub>IH</sub>	Input High Voltage	CMOS levels, 70% of V <sub>DD</sub>	0.7			V <sub>DD</sub>
V <sub>IL</sub>	Input Low Voltage	CMOS levels, 30% of V <sub>DD</sub>			0.3	V <sub>DD</sub>
R <sub>UP</sub>	Pull up resistor on inputs	V <sub>DD</sub> = 3.14 to 3.47V, measured V <sub>IN</sub> = 0V		100	150	kΩ

**AC Electrical Specifications (V<sub>DD</sub> = 3.3V)**

Parameter <sup>[3]</sup>	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 2</i> , 50% of V <sub>DD</sub>	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See <i>Figure 3</i> .	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See <i>Figure 3</i> .	0.8	1.4		V/ns
t <sub>9</sub>	Clock Jitter	Peak-to-peak period jitter		300		ps
t <sub>10</sub>	PLL Lock Time				3	ms

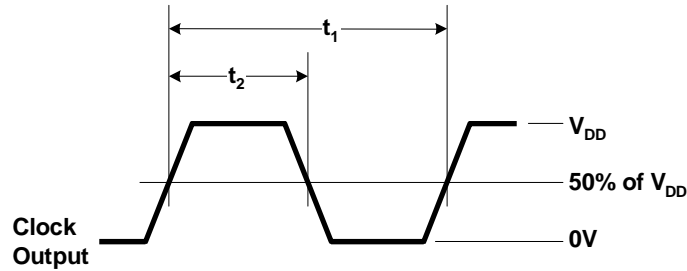
**Test and Measurement Setup**



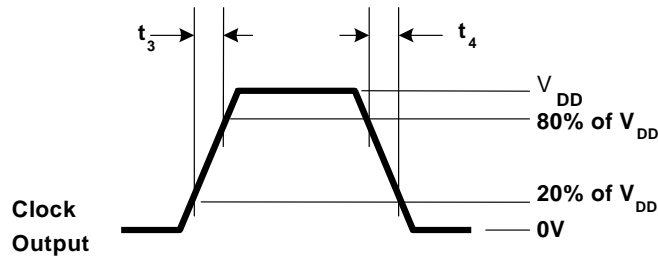
**Note**  
3. Not 100% tested.

**Voltage and Timing Definitions**

**Figure 2. Duty Cycle Definition**



**Figure 3.  $ER = (0.6 \times V_{DD}) / t_3$ ,  $EF = (0.6 \times V_{DD}) / t_4$**



**Ordering Information**

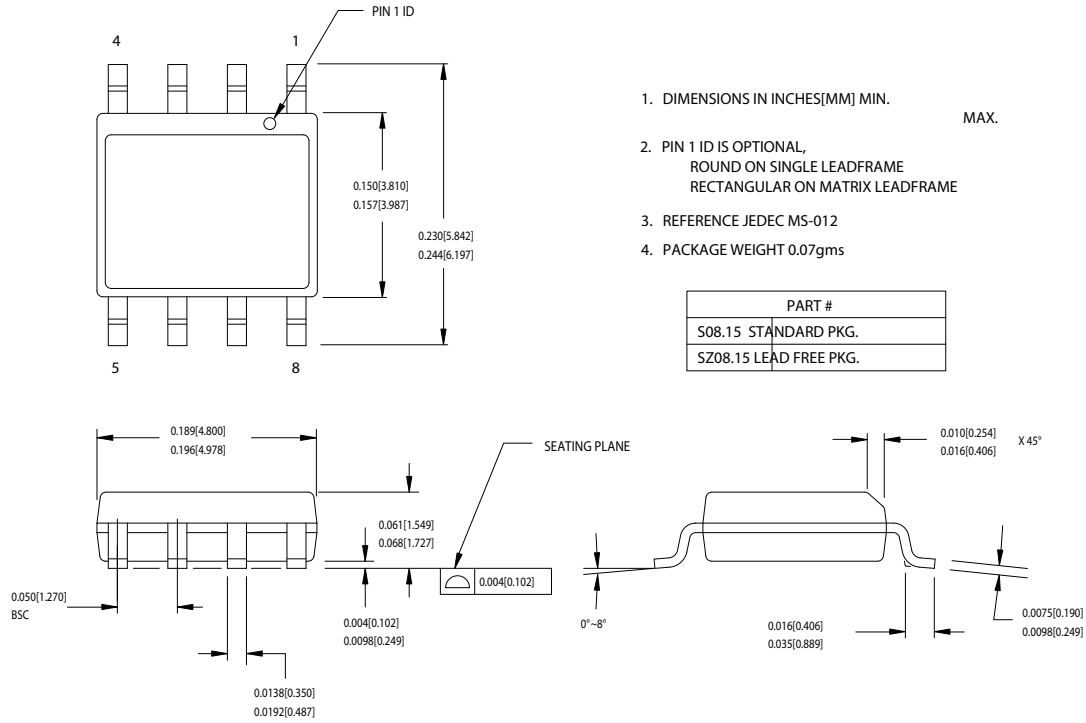
Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24212SC-1 <sup>[4]</sup>	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-1T <sup>[4]</sup>	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-2 <sup>[4]</sup>	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-2T <sup>[4]</sup>	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-3 <sup>[4]</sup>	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-3T <sup>[4]</sup>	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-5 <sup>[4]</sup>	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-5T <sup>[4]</sup>	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
<b>Pb-free</b>				
CY24212SXC-5 <sup>[4]</sup>	S8	8-Pin SOIC	Commercial	3.3V
CY24212SXC-5T <sup>[4]</sup>	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212KSXC-5	S8	8-Pin SOIC	Commercial	3.3V

**Note**

4. Not recommended for new designs.

**Package Drawing and Dimensions**

**Figure 4. 8-lead (150-Mil) SOIC S8**



51-85066-°C

**Document History Page**

Document Title: CY24212 MediaClock™ MPEG Clock Generator with VCXO Document Number: 38-07402				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117089	09/09/02	CKN	New Data Sheet
*A	120888	12/06/02	CKN	Added -3
*B	123064	02/19/03	CKN	Added -5
*C	345540	See ECN	RGL	Added Pb-free for -5 part
*D	2447126	See ECN	AESA	Updated template. Added Note "Not recommended for new designs." Added part number CY24212KSXC-5 in ordering information table.

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