

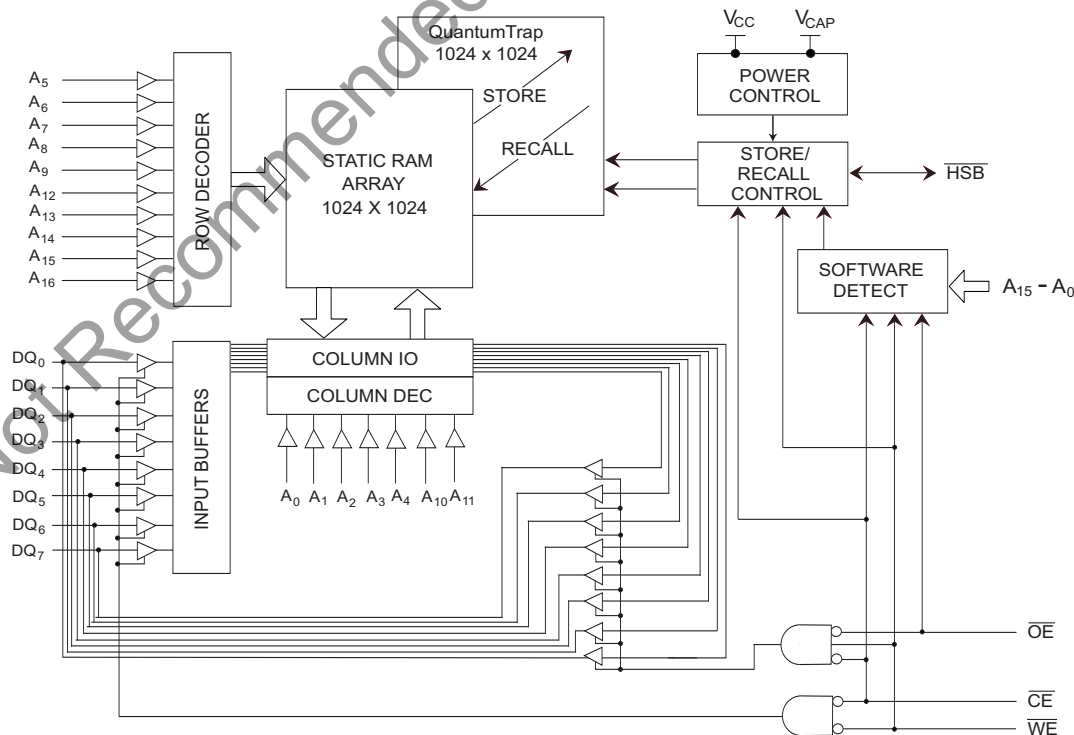
## Features

- 25 ns, 35 ns, and 45 ns Access Times
- Pin compatible with STK14CA8
- Hands off Automatic STORE on Power Down with only a small Capacitor
- STORE to QuantumTrap Nonvolatile Elements is initiated by software, hardware, or AutoStore on Power Down
- RECALL to SRAM initiated by Software or Power Up
- Unlimited READ, WRITE, and RECALL Cycles
- 200,000 STORE Cycles to QuantumTrap
- 20 year Data Retention at 55°C
- Single 3V +20%, -10% Operation
- Commercial and Industrial Temperature
- 32-pin (300 mil) SOIC and 48-pin (300 mil) SSOP packages
- RoHS Compliance

## Functional Description

The Cypress CY14B101L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

## Logic Block Diagram

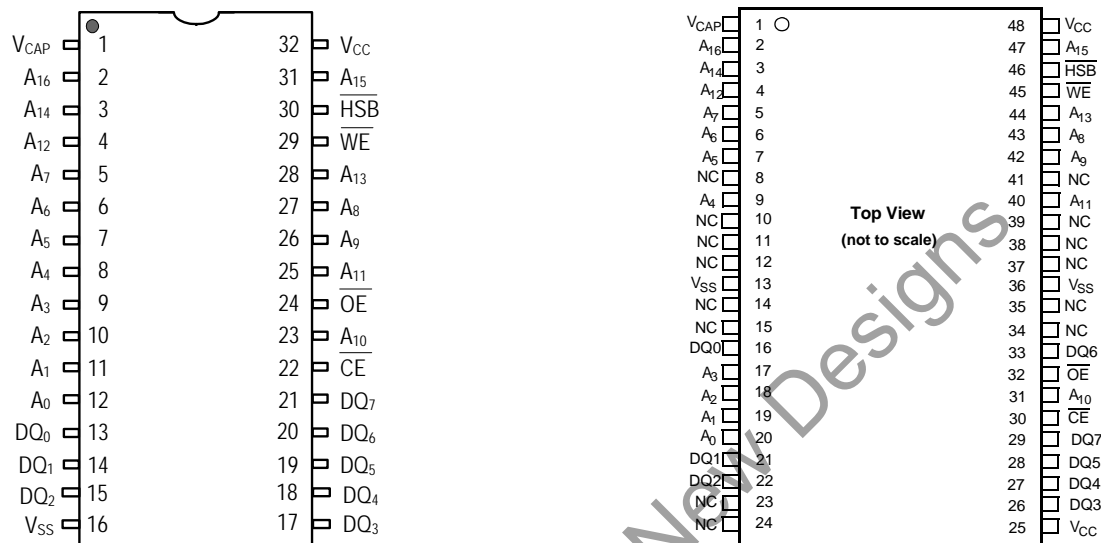


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## Pinouts

**Figure 1. Pin Diagram - 32-Pin SOIC and 48-Pin SSOP**



**Table 1. Pin Definitions**

| Pin Name                         | Alt            | I/O Type        | Description   |
|----------------------------------|----------------|-----------------|---|
| A <sub>0</sub> -A <sub>16</sub>  |                | Input           | <b>Address Inputs.</b> Used to select one of the 131,072 bytes of the nvSRAM.   |
| DQ <sub>0</sub> -DQ <sub>7</sub> |                | Input or Output | <b>Bidirectional Data IO Lines.</b> Used as input or output lines depending on operation.   |
| $\overline{WE}$                  | $\overline{W}$ | Input           | <b>Write Enable Input, Active LOW.</b> When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location.  |
| $\overline{CE}$                  | $\overline{E}$ | Input           | <b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.  |
| $\overline{OE}$                  | $\overline{G}$ | Input           | <b>Output Enable, Active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.  |
| V <sub>SS</sub>                  |                | Ground          | <b>Ground for the Device.</b> The device is connected to ground of the system.  |
| V <sub>CC</sub>                  |                | Power Supply    | <b>Power Supply Inputs to the Device.</b>   |
| HSB                              |                | Input or Output | <b>Hardware Store Busy (HSB).</b> When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional). |
| VCAP                             |                | Power Supply    | <b>AutoStore Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.   |
| NC                               |                | No Connect      | <b>No Connect.</b> This pin is not connected to the die.  |

## Device Operation

The CY14B101L nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14B101L supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

## SRAM Read

The CY14B101L performs a READ cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW while WE and HSB are HIGH. The address specified on pins A<sub>0-16</sub> determines the 131,072 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of  $t_{AA}$  (READ cycle 1). If the READ is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at  $t_{ACE}$  or at  $t_{DOE}$ , whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the  $t_{AA}$  access time without the need for transitions on any control input pins, and remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or WE or HSB is brought LOW.

## SRAM Write

A WRITE cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{CE}$  or WE goes HIGH at the end of the cycle.

The data on the common IO pins DQ<sub>0-7</sub> are written into the memory if it has valid  $t_{SD}$ , before the end of a WE controlled WRITE or before the end of an  $\overline{CE}$  controlled WRITE. Keep  $\overline{OE}$  HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If  $\overline{OE}$  is left LOW, internal circuitry turns off the output buffers  $t_{HZWE}$  after WE goes LOW.

## AutoStore Operation

The CY14B101L stores data to nvSRAM using one of three storage operations:

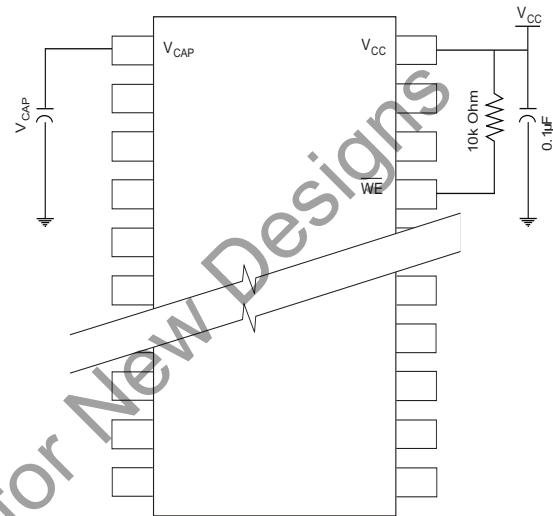
1. Hardware store activated by  $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101L.

During normal operation, the device draws current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part automatically disconnects the  $V_{CAP}$  pin from  $V_{CC}$ . A STORE operation is initiated with power provided by the  $V_{CAP}$  capacitor.

Figure 2 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for automatic store operation. Refer to the [DC Electrical Characteristics](#) on page 8 for the size of  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on WE to hold it inactive during power up.

**Figure 2. AutoStore Mode**



To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored, unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to HSB. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

## Hardware STORE ( $\overline{HSB}$ ) Operation

The CY14B101L provides the  $\overline{HSB}$  pin for controlling and acknowledging the STORE operations. The  $\overline{HSB}$  pin is used to request a hardware STORE cycle. When the  $\overline{HSB}$  pin is driven LOW, the CY14B101L conditionally initiates a STORE operation after  $t_{DELAY}$ . An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The  $\overline{HSB}$  pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. This pin should be externally pulled up if it is used to drive other inputs.

SRAM READ and WRITE operations, that are in progress when  $\overline{HSB}$  is driven LOW by any means, are given time to complete before the STORE operation is initiated. After  $\overline{HSB}$  goes LOW, the CY14B101L continues SRAM operations for  $t_{DELAY}$ . During  $t_{DELAY}$ , multiple SRAM READ operations take place. If a WRITE is in progress when  $\overline{HSB}$  is pulled LOW, it allows a time,  $t_{DELAY}$  to complete. However, any SRAM WRITE cycles requested after  $\overline{HSB}$  goes LOW are inhibited until  $\overline{HSB}$  returns HIGH.

If  $\overline{HSB}$  is not used, it is left unconnected.

## Hardware RECALL (Power Up)

During power up or after any low power condition ( $V_{CC} < V_{SWITCH}$ ), an internal RECALL request is latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a RECALL cycle is automatically initiated and takes  $t_{HRECALL}$  to complete.

## Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B101L software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x4E38, Valid READ
2. Read address 0xB1C7, Valid READ
3. Read address 0x83E0, Valid READ
4. Read address 0x7C1F, Valid READ
5. Read address 0x703F, Valid READ
6. Read address 0x8FC0, Initiate STORE cycle

The software sequence is clocked with  $\overline{CE}$  controlled READs or  $\overline{OE}$  controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that  $\overline{OE}$  is LOW for a valid sequence. After the  $t_{STORE}$  cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

## Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled READ operations is performed:

1. Read address 0x4E38, Valid READ
2. Read address 0xB1C7, Valid READ
3. Read address 0x83E0, Valid READ
4. Read address 0x7C1F, Valid READ
5. Read address 0x703F, Valid READ
6. Read address 0x4C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

## Data Protection

The CY14B101L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ .

If the CY14B101L is in a WRITE mode (both  $\overline{CE}$  and  $\overline{WE}$  are low) at power up after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on  $\overline{CE}$  or  $\overline{WE}$  is detected. This protects against inadvertent writes during power up or brown out conditions.

## Noise Considerations

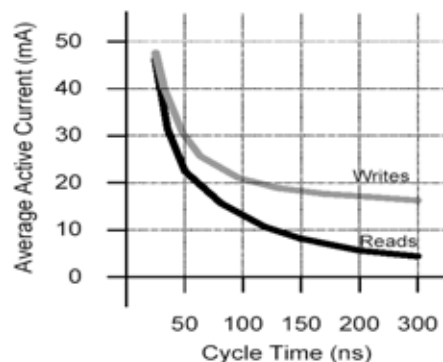
The CY14B101L is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1  $\mu F$  connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

## Low Average Active Power

CMOS technology provides the CY14B101L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 shows the relationship between  $I_{CC}$  and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 3.6V$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B101L depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of READs to WRITEs
- CMOS versus TTL input levels
- The operating temperature
- The  $V_{CC}$  level
- IO loading

**Figure 3. Current Versus Cycle Time**



## Preventing Store

Disable the AutoStore function by initiating an AutoStore Disable sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, perform the following sequence of CE controlled READ operations:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8B45 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, perform the following sequence of CE controlled READ operations:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) is issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, the best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- If AutoStore is firmware disabled, it does not reset to "autostore enabled" on every power down event captured by the nvSRAM. The application firmware should re-enable or re-disable autostore on each reset sequence based on the behavior desired.
- The  $V_{CAP}$  value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum  $V_{CAP}$  value because higher inrush currents may reduce the reliability of the internal pass transistor. Customers that want to use a larger  $V_{CAP}$  value to make sure there is extra store charge should discuss their  $V_{CAP}$  size selection with Cypress to understand any impact on the  $V_{cap}$  voltage level at the end of a  $t_{RECALL}$  period.

**Table 2. Hardware Mode Selection**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\text{A}_{15} - \text{A}_0$                             | Mode  | IO   | Power   |
|------------------------|------------------------|------------------------|--|---|--|---|
| H                      | X                      | X                      | X  | Not Selected  | Output High Z  | Standby   |
| L                      | H                      | L                      | X  | Read SRAM   | Output Data  | Active <sup>[3]</sup>                               |
| L                      | L                      | X                      | X  | Write SRAM  | Input Data   | Active  |
| L                      | H                      | L                      | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8B45 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Disable  | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data   | Active <sup>[1, 2, 3]</sup>                         |
| L                      | H                      | L                      | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4B46 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Enable   | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data   | Active <sup>[1, 2, 3]</sup>                         |
| L                      | H                      | L                      | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8FC0 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile Store  | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active $\text{I}_{\text{CC2}}$ <sup>[1, 2, 3]</sup> |
| L                      | H                      | L                      | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4C63 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile Recall | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active <sup>[1, 2, 3]</sup>                         |

**Notes**

1. The six consecutive address locations are in the order listed.  $\overline{\text{WE}}$  is HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 17 address lines on the CY14B101L, only the lower 16 lines are used to control software modes.
3. IO state depends on the state of  $\overline{\text{OE}}$ . The IO table shown is based on  $\overline{\text{OE}}$  Low.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  Relative to GND ..... -0.5V to 4.1V

Voltage Applied to Outputs  
in High Z State ..... -0.5V to  $V_{CC} + 0.5V$

Input Voltage ..... -0.5V to  $V_{CC} + 0.5V$

Transient Voltage (<20 ns) on  
Any Pin to Ground Potential ..... -2.0V to  $V_{CC} + 2.0V$

Package Power Dissipation

Capability ( $T_A = 25^\circ\text{C}$ ) ..... 1.0W

Surface Mount Lead Soldering

Temperature (3 Seconds) ..... +260°C

DC output Current (1 output at a time, 1s duration) .... 15 mA

Static Discharge Voltage ..... > 2001V  
(MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$     |
|------------|---------------------|--------------|
| Commercial | 0°C to +70°C        | 2.7V to 3.6V |
| Industrial | -40°C to +85°C      | 2.7V to 3.6V |

## DC Electrical Characteristics

Over the operating range ( $V_{CC} = 2.7V$  to  $3.6V$ ) [4, 5]

| Parameter | Description   | Test Conditions   | Min            | Max            | Unit          |
|-----------|---|---|----------------|----------------|---------------|
| $I_{CC1}$ | Average $V_{CC}$ Current  | $t_{RC} = 25\text{ ns}$   | Commercial     | 65             | mA            |
|           |   | $t_{RC} = 35\text{ ns}$   |                | 55             | mA            |
|           |   | $t_{RC} = 45\text{ ns}$   |                | 50             | mA            |
|           |   | Dependent on output loading and cycle rate.<br>Values obtained without output loads.<br>$I_{OUT} = 0\text{ mA}$ .   | Industrial     | 70             | mA            |
|           |   |   |                | 60             | mA            |
|           |   |   |                | 55             | mA            |
| $I_{CC2}$ | Average $V_{CC}$ Current during STORE                                   | All Inputs Do Not Care, $V_{CC} = \text{Max}$<br>Average current for duration $t_{STORE}$   |                | 6              | mA            |
| $I_{CC3}$ | Average $V_{CC}$ Current at $t_{RC} = 200\text{ ns}$ , 5V, 25°C Typical | $\overline{WE} \geq (V_{CC} - 0.2V)$ . All other inputs cycling.<br>Dependent on output loading and cycle rate. Values obtained without output loads.   |                | 10             | mA            |
| $I_{CC4}$ | Average $V_{CAP}$ Current during AutoStore Cycle                        | All Inputs Do Not Care, $V_{CC} = \text{Max}$<br>Average current for duration $t_{STORE}$   |                | 3              | mA            |
| $I_{SB}$  | $V_{CC}$ Standby Current  | $\overline{CE} \geq (V_{CC} - 0.2V)$ . All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ .<br>Standby current level after nonvolatile cycle is complete.<br>Inputs are static. $f = 0\text{ MHz}$ . |                | 3              | mA            |
| $I_{IX}$  | Input Leakage Current   | $V_{CC} = \text{Max}$ , $V_{SS} \leq V_{IN} \leq V_{CC}$  | -1             | +1             | $\mu\text{A}$ |
| $I_{OZ}$  | Off State Output Leakage Current  | $V_{CC} = \text{Max}$ , $V_{SS} \leq V_{IN} \leq V_{CC}$ , $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$  | -1             | +1             | $\mu\text{A}$ |
| $V_{IH}$  | Input HIGH Voltage  |   | 2.0            | $V_{CC} + 0.5$ | V             |
| $V_{IL}$  | Input LOW Voltage   |   | $V_{SS} - 0.5$ | 0.8            | V             |
| $V_{OH}$  | Output HIGH Voltage   | $I_{OUT} = -2\text{ mA}$  | 2.4            |                | V             |
| $V_{OL}$  | Output LOW Voltage  | $I_{OUT} = 4\text{ mA}$   |                | 0.4            | V             |
| $V_{CAP}$ | Storage Capacitor   | Between $V_{CAP}$ pin and $V_{SS}$ , 6V rated.  | 17             | 120            | $\mu\text{F}$ |

## Data Retention and Endurance

| Parameter | Description                  | Min | Unit  |
|-----------|------------------------------|-----|-------|
| $DATA_R$  | Data Retention at 55°C       | 20  | Years |
| $NV_C$    | Nonvolatile STORE Operations | 200 | K     |

### Notes

4. The HSB pin has  $I_{OUT} = -10\text{ }\mu\text{A}$  for  $V_{OH}$  of 2.4 V. This parameter is characterized but not tested.

5.  $V_{IH}$  changes by 100 mV when  $V_{CC} > 3.5V$ .

## Capacitance

In the following table, the capacitance parameters are listed.<sup>[6]</sup>

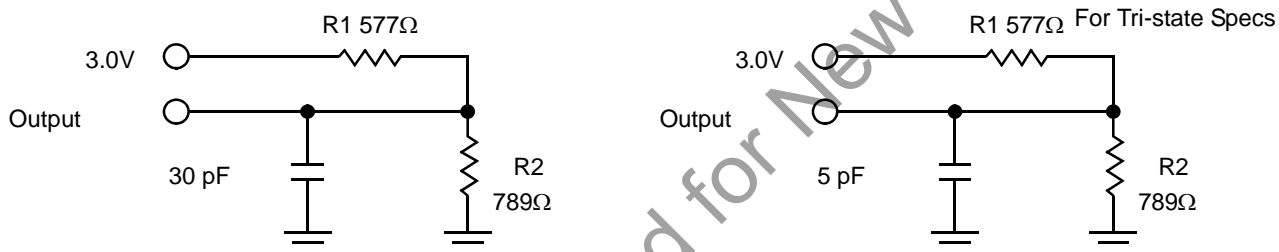
| Parameter | Description        | Test Conditions   | Max | Unit |
|-----------|--------------------|---|-----|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,<br>$V_{CC} = 0\text{ to }3.0\text{V}$ | 7   | pF   |
| $C_{OUT}$ | Output Capacitance |   | 7   | pF   |

## Thermal Resistance

In the following table, the thermal resistance parameters are listed.<sup>[6]</sup>

| Parameter     | Description                                 | Test Conditions  | 32-SOIC | 48-SSOP | Unit               |
|---------------|---|--|---------|---------|--------------------|
| $\Theta_{JA}$ | Thermal Resistance<br>(Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 33.64   | 32.9    | $^\circ\text{C/W}$ |
| $\Theta_{JC}$ | Thermal Resistance<br>(Junction to Case)    |  | 13.6    | 16.35   | $^\circ\text{C/W}$ |

**Figure 4. AC Test Loads**



## AC Test Conditions

Input Pulse Levels ..... 0V to 3V  
 Input Rise and Fall Times (10% to 90%) .....  $\leq 5\text{ ns}$   
 Input and Output Timing Reference Levels ..... 1.5V

### Note

6. These parameters are guaranteed by design and are not tested.

## AC Switching Characteristics

### SRAM Read Cycle

| Parameter         |                      | Description                       | 25 ns |     | 35 ns |     | 45 ns |     | Unit |
|-------------------|----------------------|-----------------------------------|-------|-----|-------|-----|-------|-----|------|
| Cypress Parameter | Alt                  |                                   | Min   | Max | Min   | Max | Min   | Max |      |
| $t_{ACE}$         | $t_{ELQV}$           | Chip Enable Access Time           |       | 25  |       | 35  |       | 45  | ns   |
| $t_{RC}^{[7]}$    | $t_{AVAV}, t_{ELEH}$ | Read Cycle Time                   | 25    |     | 35    |     | 45    |     | ns   |
| $t_{AA}^{[8]}$    | $t_{AVQV}$           | Address Access Time               |       | 25  |       | 35  |       | 45  | ns   |
| $t_{DOE}^{[8]}$   | $t_{GLQV}$           | Output Enable to Data Valid       |       | 12  |       | 15  |       | 20  | ns   |
| $t_{OHA}^{[8]}$   | $t_{AXQX}$           | Output Hold After Address Change  | 3     |     | 3     |     | 3     |     | ns   |
| $t_{LZCE}^{[9]}$  | $t_{ELQX}$           | Chip Enable to Output Active      | 3     |     | 3     |     | 3     |     | ns   |
| $t_{HZCE}^{[9]}$  | $t_{EHQZ}$           | Chip Disable to Output Inactive   |       | 10  |       | 13  |       | 15  | ns   |
| $t_{LZOE}^{[9]}$  | $t_{GLQX}$           | Output Enable to Output Active    | 0     |     | 0     |     | 0     |     | ns   |
| $t_{HZOE}^{[9]}$  | $t_{GHQZ}$           | Output Disable to Output Inactive |       | 10  |       | 13  |       | 15  | ns   |
| $t_{PU}^{[6]}$    | $t_{ELICCH}$         | Chip Enable to Power Active       | 0     |     | 0     |     | 0     |     | ns   |
| $t_{PD}^{[6]}$    | $t_{EHICCL}$         | Chip Disable to Power Standby     |       | 25  |       | 35  |       | 45  | ns   |

### Switching Waveforms

Figure 5. SRAM Read Cycle 1: Address Controlled [7, 8, 10]

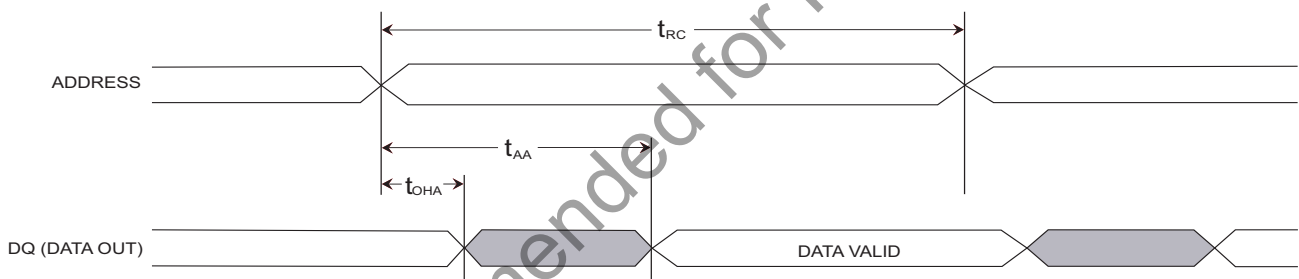
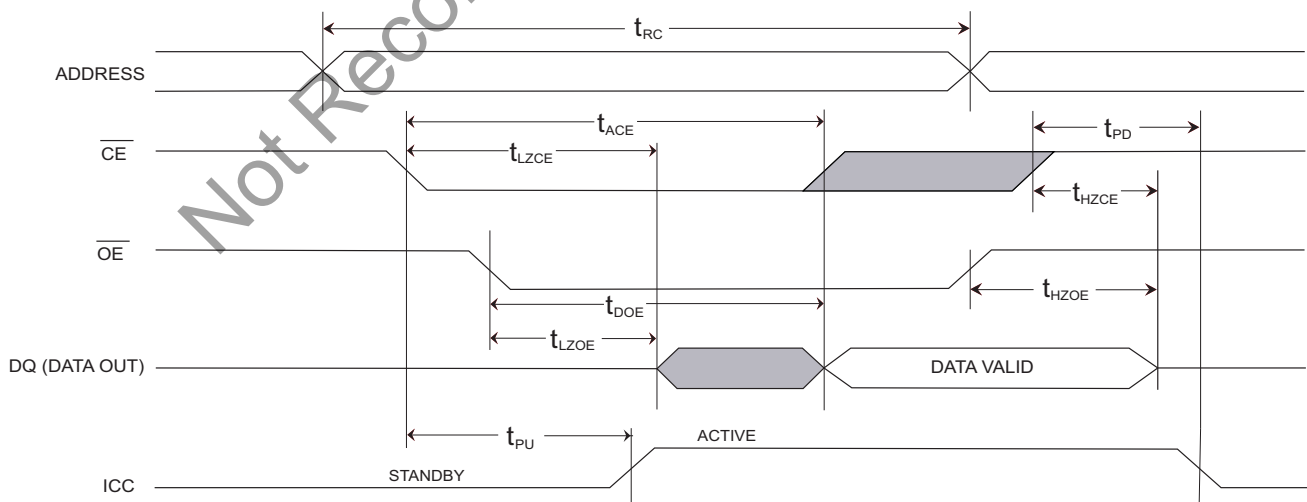


Figure 6. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled [7, 10]



#### Notes

7.  $\overline{WE}$  and  $\overline{HSB}$  must be HIGH during SRAM READ cycles.
8. Device is continuously selected with  $\overline{CE}$  and  $\overline{OE}$  both Low.
9. Measured  $\pm 200$  mV from steady state output voltage.
10.  $\overline{HSB}$  must remain high during READ and WRITE cycles.

## SRAM Write Cycle

| Parameter           |                         | Description                      | 25 ns |     | 35 ns |     | 45 ns |     | Unit |
|---------------------|-------------------------|----------------------------------|-------|-----|-------|-----|-------|-----|------|
| Cypress Parameter   | Alt                     |                                  | Min   | Max | Min   | Max | Min   | Max |      |
| $t_{WC}$            | $t_{AVAV}$              | Write Cycle Time                 | 25    |     | 35    |     | 45    |     | ns   |
| $t_{PWE}$           | $t_{WLWH}$ , $t_{WLEH}$ | Write Pulse Width                | 20    |     | 25    |     | 30    |     | ns   |
| $t_{SCE}$           | $t_{ELWH}$ , $t_{ELEH}$ | Chip Enable To End of Write      | 20    |     | 25    |     | 30    |     | ns   |
| $t_{SD}$            | $t_{DVWH}$ , $t_{DVEH}$ | Data Setup to End of Write       | 10    |     | 12    |     | 15    |     | ns   |
| $t_{HD}$            | $t_{WHDX}$ , $t_{EHDX}$ | Data Hold After End of Write     | 0     |     | 0     |     | 0     |     | ns   |
| $t_{AW}$            | $t_{AVWH}$ , $t_{AVEH}$ | Address Setup to End of Write    | 20    |     | 25    |     | 30    |     | ns   |
| $t_{SA}$            | $t_{AVWL}$ , $t_{AVEL}$ | Address Setup to Start of Write  | 0     |     | 0     |     | 0     |     | ns   |
| $t_{HA}$            | $t_{WHAX}$ , $t_{EHAX}$ | Address Hold After End of Write  | 0     |     | 0     |     | 0     |     | ns   |
| $t_{HZWE}^{[9,11]}$ | $t_{WLQZ}$              | Write Enable to Output Disable   |       | 10  |       | 13  |       | 15  | ns   |
| $t_{LZWE}^{[9]}$    | $t_{WHQX}$              | Output Active After End of Write | 3     |     | 3     |     | 3     |     | ns   |

## Switching Waveforms

Figure 7. SRAM Write Cycle 1:  $\overline{WE}$  Controlled <sup>[11, 12]</sup>

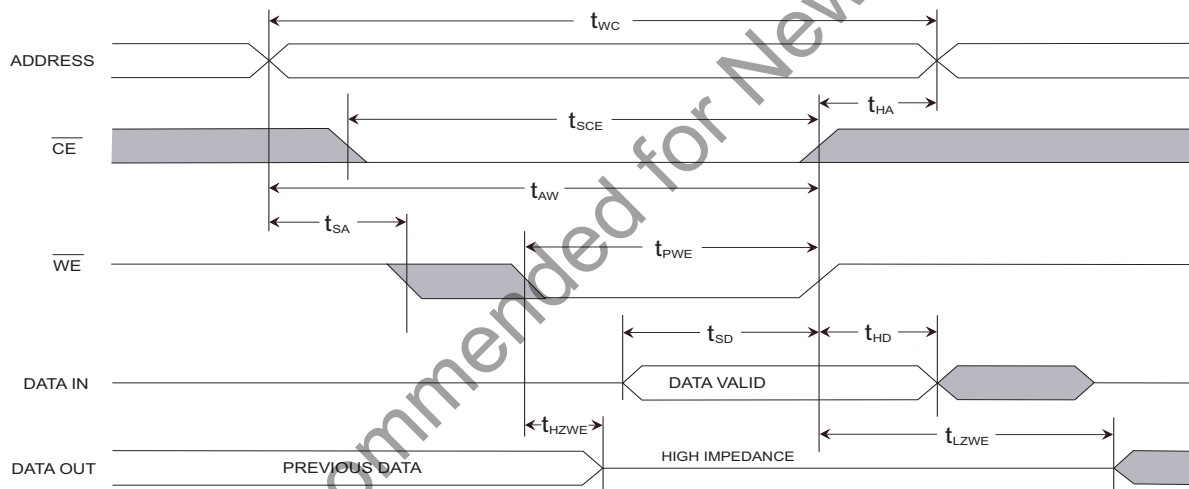
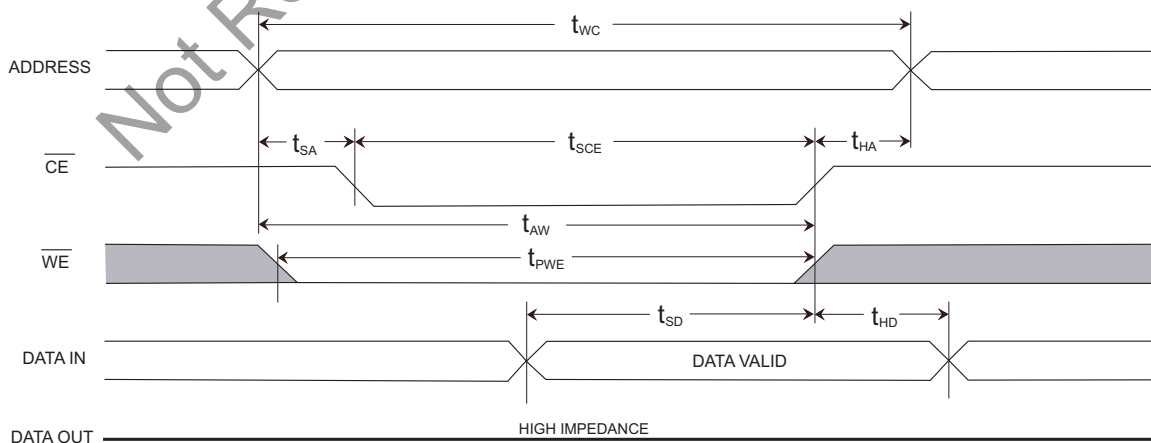


Figure 8. SRAM Write Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled <sup>[11, 12]</sup>



### Notes

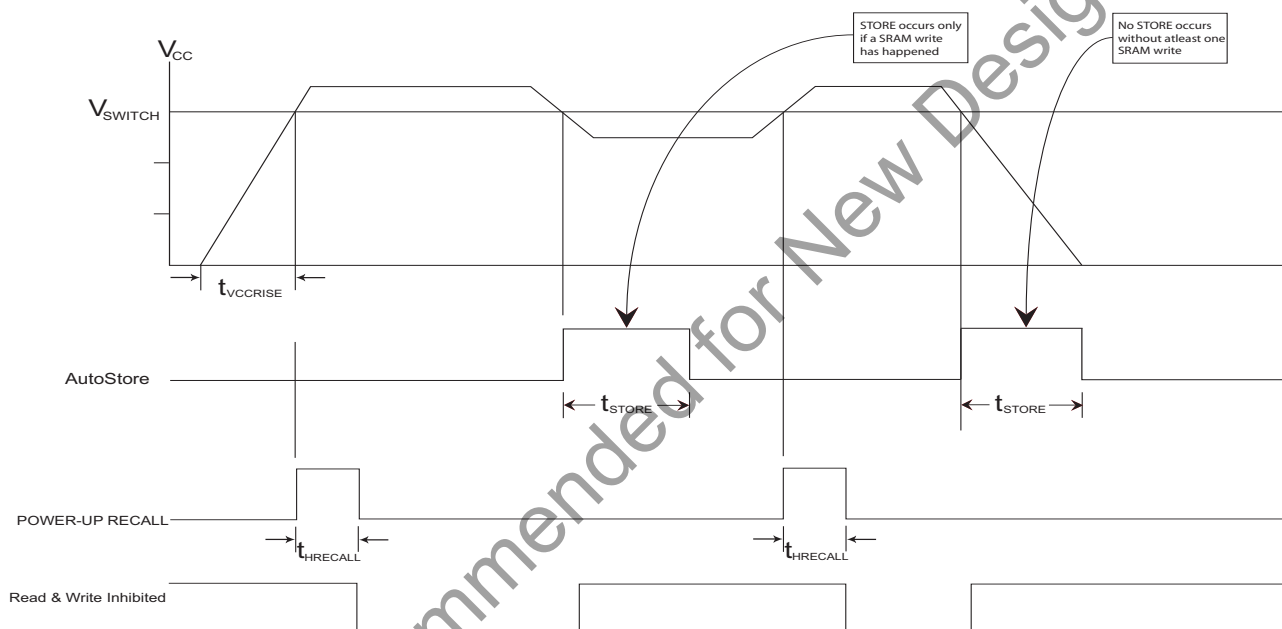
11. If  $\overline{WE}$  is Low when  $\overline{CE}$  goes Low, the outputs remain in the high impedance state.
12.  $\overline{CE}$  or  $\overline{WE}$  must be greater than  $V_{IH}$  during address transitions.

## AutoStore or Power Up RECALL

| Parameter            | Alt           | Description               | CY14B101L |      | Unit    |
|----------------------|---------------|---------------------------|-----------|------|---------|
|                      |               |                           | Min       | Max  |         |
| $t_{HRECALL}$ [13]   | $t_{RESTORE}$ | Power up RECALL Duration  |           | 20   | ms      |
| $t_{STORE}$ [14, 15] | $t_{HLHZ}$    | STORE Cycle Duration      |           | 12.5 | ms      |
| $V_{SWITCH}$         |               | Low Voltage Trigger Level |           | 2.65 | V       |
| $t_{VCCRISE}$        |               | $V_{CC}$ Rise Time        | 150       |      | $\mu$ s |

## Switching Waveforms

Figure 9. AutoStore/Power Up RECALL



**Note** Read and Write cycles are ignored during STORE, RECALL, and while  $V_{CC}$  is below  $V_{SWITCH}$

### Notes

13.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
14. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE will take place.
15. Industrial Grade devices requires 15 ms max.

## Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [16, 17]

| Parameter       | Alt                  | Description                        | 25 ns |     | 35 ns |     | 45 ns |     | Unit    |
|-----------------|----------------------|------------------------------------|-------|-----|-------|-----|-------|-----|---------|
|                 |                      |                                    | Min   | Max | Min   | Max | Min   | Max |         |
| $t_{RC}^{[17]}$ | $t_{AVAV}$           | STORE/RECALL Initiation Cycle Time | 25    |     | 35    |     | 45    |     | ns      |
| $t_{SA}$        | $t_{AVEL}$           | Address Setup Time                 | 0     |     | 0     |     | 0     |     | ns      |
| $t_{CW}$        | $t_{ELEH}$           | Clock Pulse Width                  | 20    |     | 25    |     | 30    |     | ns      |
| $t_{HA}$        | $t_{GHAX}, t_{ELAX}$ | Address Hold Time                  | 1     |     | 1     |     | 1     |     | ns      |
| $t_{RECALL}$    |                      | RECALL Duration                    |       | 120 |       | 120 |       | 120 | $\mu s$ |

## Switching Waveforms

Figure 10.  $\overline{CE}$  Controlled Software STORE/RECALL Cycle [17]

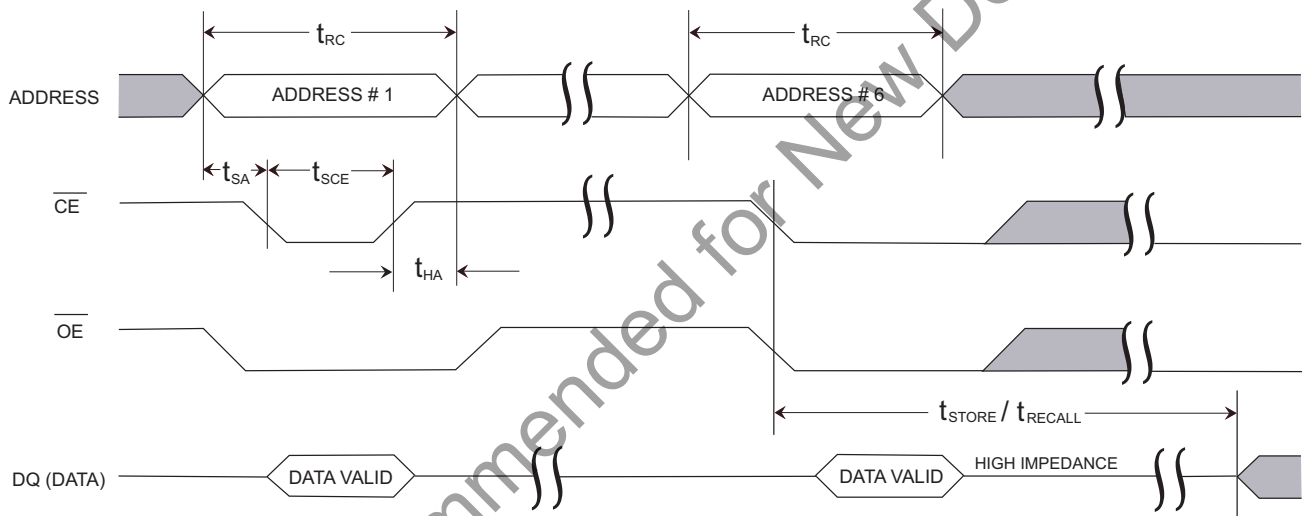
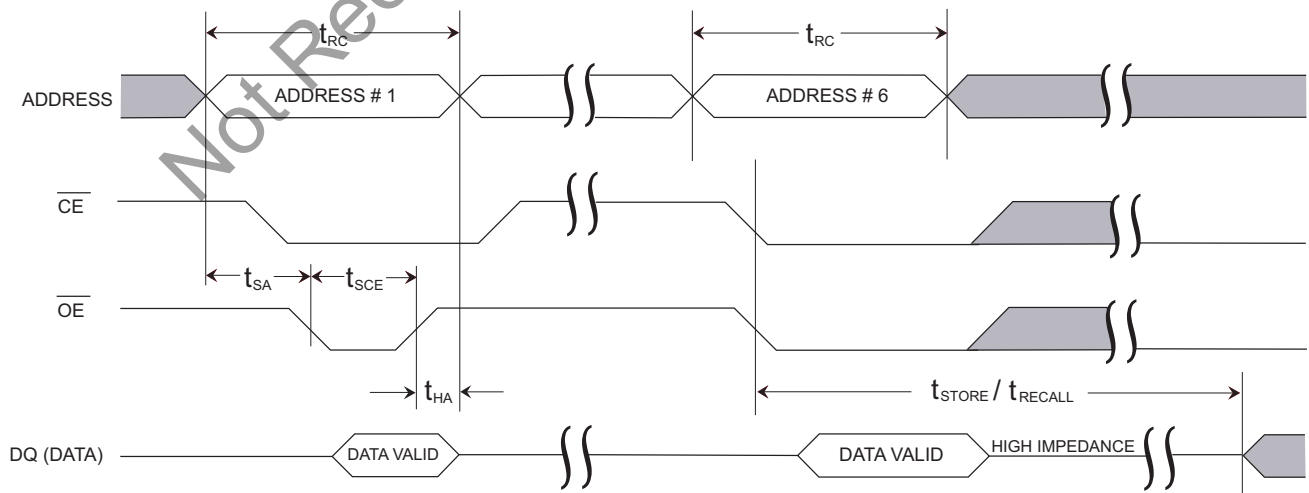


Figure 11.  $\overline{OE}$  Controlled Software STORE/RECALL Cycle [17]



### Notes

16. The software sequence is clocked on the falling edge of  $\overline{CE}$  controlled READs or  $\overline{OE}$  controlled READs.

17. The six consecutive addresses must be read in the order listed in the Mode Selection table. WE must be HIGH during all six consecutive cycles.

## Hardware STORE Cycle

| Parameter           | Alt                  | Description                         | CY14B101L |     | Unit    |
|---------------------|----------------------|-------------------------------------|-----------|-----|---------|
|                     |                      |                                     | Min       | Max |         |
| $t_{PHSB}$          | $t_{HLHX}$           | Hardware STORE Pulse Width          | 15        |     | ns      |
| $t_{DELAY}^{[18]}$  | $t_{HLQZ}, t_{BLQZ}$ | Time Allowed to Complete SRAM Cycle | 1         | 70  | $\mu s$ |
| $t_{ss}^{[19, 20]}$ |                      | Soft Sequence Processing Time       |           | 70  | us      |

## Switching Waveforms

Figure 12. Hardware STORE Cycle

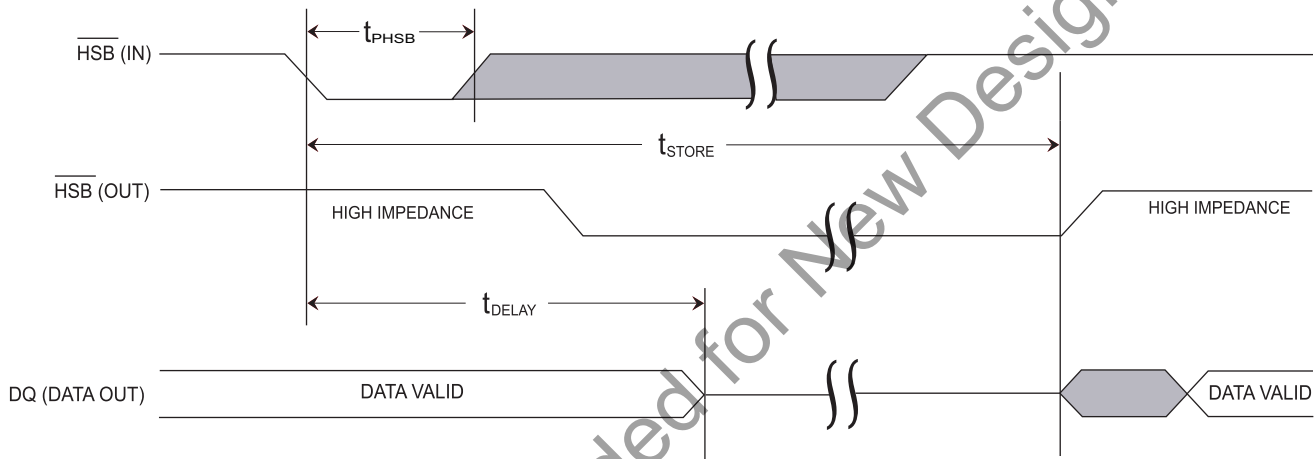
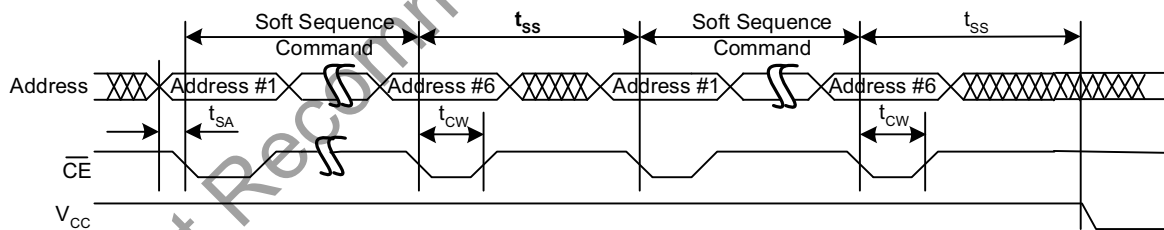


Figure 13. Soft Sequence Processing<sup>[19, 20]</sup>

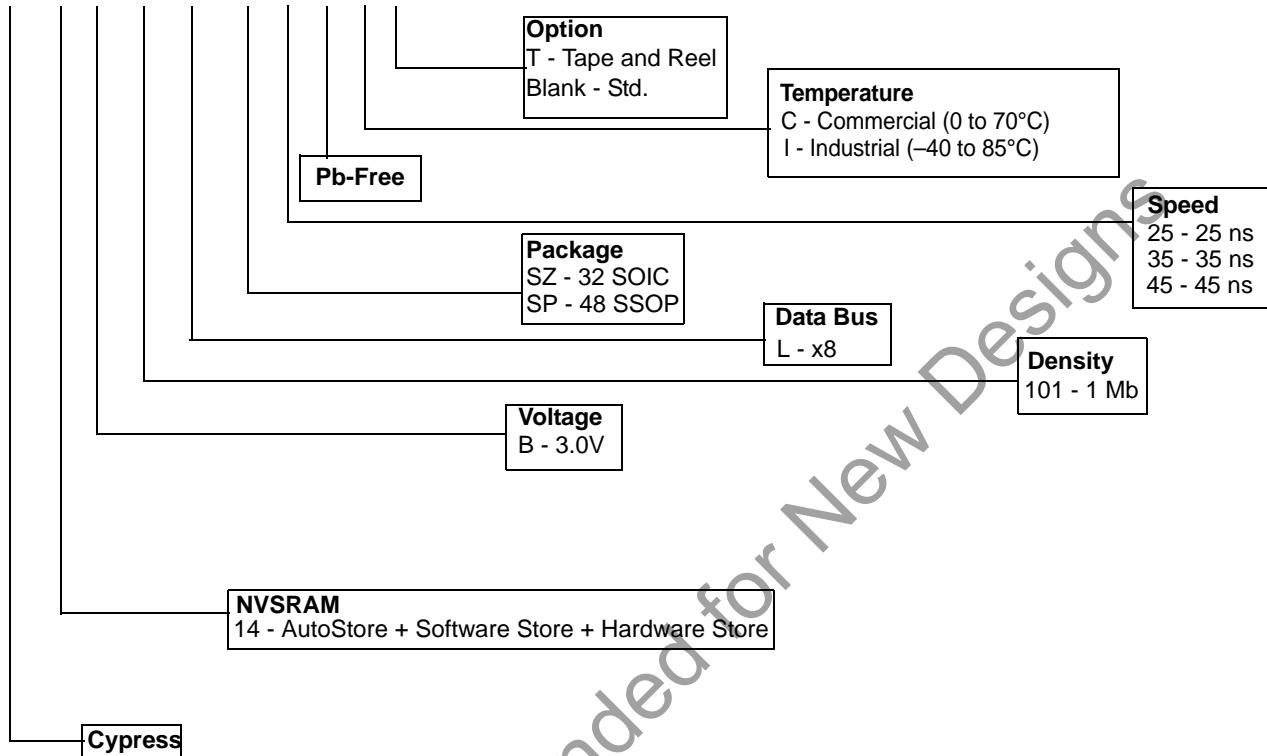


### Notes

18. On a hardware STORE initiation, SRAM operation continues to be enabled for time  $t_{DELAY}$  to allow read and write cycles to complete.
19. This is the amount of time to take action on a soft sequence command. Vcc power must remain high to effectively register command.
20. Commands such as Store and Recall lock out I/O until operation is complete which further increases this time. See specific command.

## Part Numbering Nomenclature

**CY 14 B 101 L - SZ 25 X C T**



## Ordering Information

These parts are not recommended for new designs.

| Speed (ns) | Ordering Code      | Package Diagram | Package Type | Operating Range |
|------------|--------------------|-----------------|--------------|-----------------|
| 25         | CY14B101L-SZ25XCT  | 51-85127        | 32-pin SOIC  | Commercial      |
|            | CY14B101L-SZ25XC   | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101LL-SP25XCT | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101LL-SP25XC  | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SZ25XIT  | 51-85127        | 32-pin SOIC  | Industrial      |
|            | CY14B101L-SZ25XI   | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101L-SP25XIT  | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SP25XI   | 51-85061        | 48-pin SSOP  |                 |

## Ordering Information

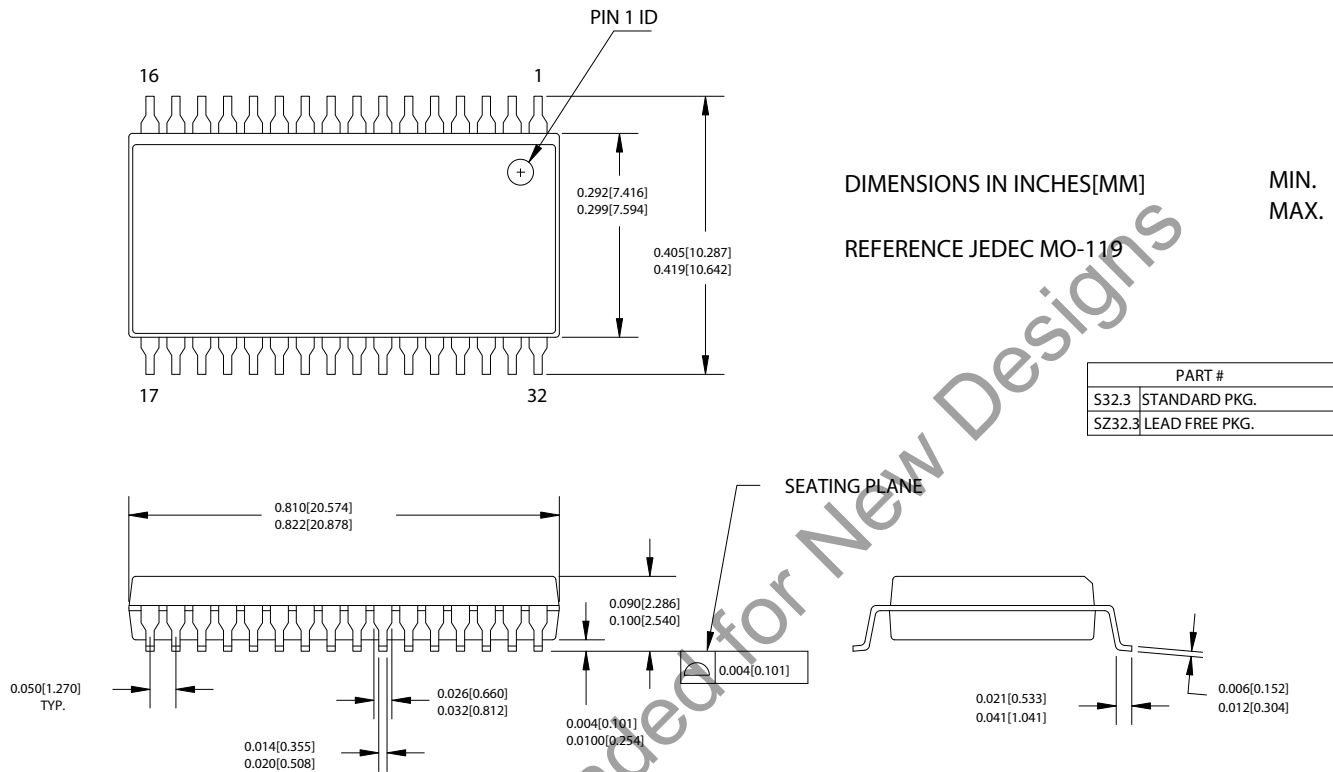
These parts are not recommended for new designs.

| Speed (ns) | Ordering Code     | Package Diagram | Package Type | Operating Range |
|------------|-------------------|-----------------|--------------|-----------------|
| 35         | CY14B101L-SZ35XCT | 51-85127        | 32-pin SOIC  | Commercial      |
|            | CY14B101L-SZ35XC  | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101L-SP35XCT | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SP35XC  | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SZ35XIT | 51-85127        | 32-pin SOIC  | Industrial      |
|            | CY14B101L-SZ35XI  | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101L-SP35XIT | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SP35XI  | 51-85061        | 48-pin SSOP  |                 |
| 45         | CY14B101L-SZ45XCT | 51-85127        | 32-pin SOIC  | Commercial      |
|            | CY14B101L-SZ45XC  | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101L-SP45XCT | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SP45XC  | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SZ45XIT | 51-85127        | 32-pin SOIC  | Industrial      |
|            | CY14B101L-SZ45XI  | 51-85127        | 32-pin SOIC  |                 |
|            | CY14B101L-SP45XIT | 51-85061        | 48-pin SSOP  |                 |
|            | CY14B101L-SP45XI  | 51-85061        | 48-pin SSOP  |                 |

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

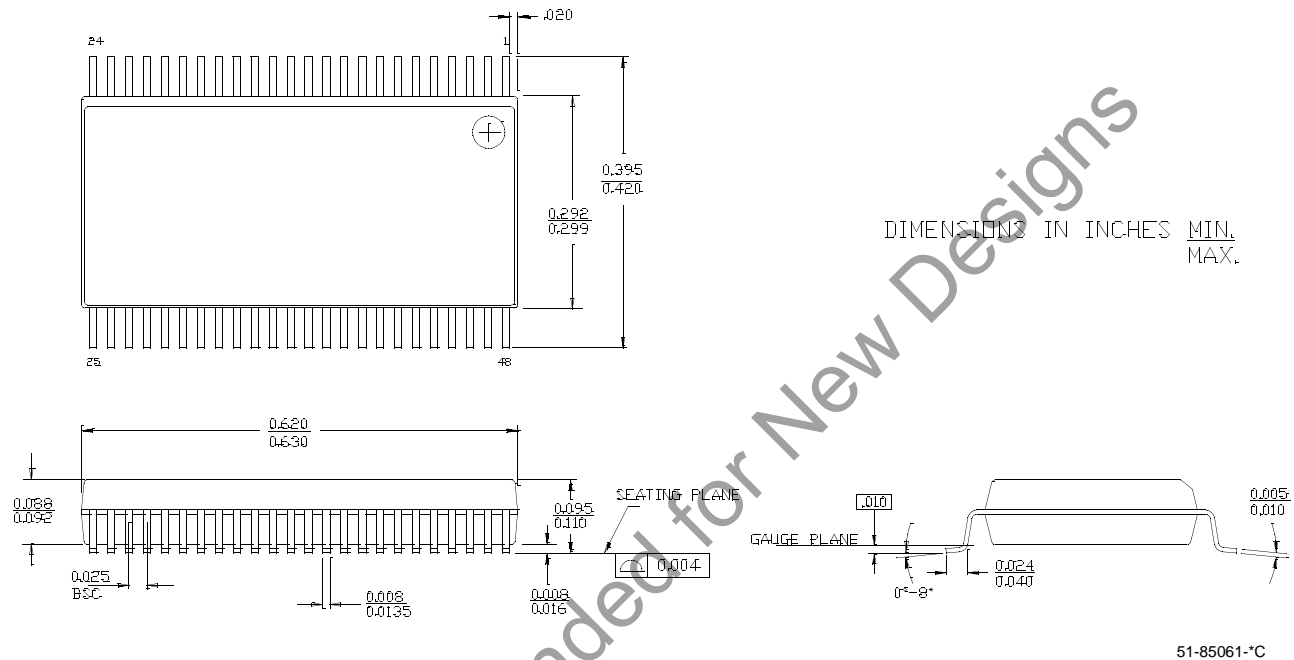
## Package Diagrams

Figure 14. 32-Pin (300 Mil) SOIC (51-85127)



51-85127-\*A

**Figure 15. 48-Pin Shrunk Small Outline Package (51-85061)**



**Document History Page**

| Document Title: CY14B101L 1 Mbit (128K x 8) nvSRAM<br>Document Number: 001-06400 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change  |
| **   | 425138  | TUP             | See ECN         | New data sheet   |
| *A   | 437321  | TUP             | See ECN         | Show data sheet on External Web  |
| *B   | 471966  | TUP             | See ECN         | Changed $I_{CC3}$ from 5 mA to 10 mA<br>Changed ISB from 2 mA to 3 mA<br>Changed $V_{IH(min)}$ from 2.2V to 2.0V<br>Changed $t_{RECALL}$ from 40 $\mu$ s to 50 $\mu$ s<br>Changed Endurance from 1 million Cycles to 500K Cycles<br>Changed Data Retention from 100 years to 20 years<br>Added Soft Sequence Processing Time Waveform<br>Updated Part Numbering Nomenclature and Ordering Information  |
| *C   | 503272  | PCI             | See ECN         | Changed from Advance to Preliminary<br>Changed the term "Unlimited" to "Infinite"<br>Changed Endurance from 500K Cycles to 200K Cycles<br>Added temperature specification to Data Retention - 20 years at 55°C<br>Removed $I_{CC1}$ values from the DC table for 25 ns and 35 ns industrial grade<br>Changed $I_{CC2}$ value from 3 mA to 6 mA in the DC table<br>Added a footnote on $V_{IH}$<br>Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V<br>Added footnote 17 related to using the software command<br>Updated Part Nomenclature Table and Ordering Information Table |
| *D   | 597002  | TUP             | See ECN         | Removed $V_{SWITCH(min)}$ specification from the AutoStore/Power Up RECALL table<br>Changed $t_{GLAX}$ specification from 20 ns to 1 ns<br>Added $t_{DELAY(max)}$ specification of 70 $\mu$ s in the hardware STORE cycle table<br>Removed $t_{HLBL}$ specification<br>Changed $t_{SS}$ specification from 70 $\mu$ s (min) to 70 $\mu$ s (max)<br>Changed $V_{CAP(max)}$ from 57 $\mu$ F to 120 $\mu$ F   |
| *E   | 688776  | VKN             | See ECN         | Added footnote related to HSB<br>Changed $t_{GLAX}$ to $t_{GHAX}$  |
| *F   | 1349963 | UHA/SFV         | See ECN         | Changed from Preliminary to Final<br>Updated Ordering Information table  |
| *G   | 2427986 | GVCH            | See ECN         | Move to external web   |
| *H   | 2546756 | GVCH/AESA       | 08/01/2008      | Aligned part number nomenclature<br>Corrected typo in ordering information<br>Changed pin definition of NC pin<br>Updated data sheet template  |

| Document Title: CY14B101L 1 Mbit (128K x 8) nvSRAM<br>Document Number: 001-06400 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change  |
| *I   | 2625139 | GVCH/PYRS       | 01/30/09        | Updated "features"<br>Added data retention at 55°C<br>Updated WE pin description<br>Added best practices<br>Added I <sub>CC1</sub> spec for 25ns and 35ns access speed for industrial temperature<br>Updated V <sub>IH</sub> from V <sub>CC</sub> +0.3 to V <sub>CC</sub> +0.5<br>Removed footnote 4 and 5<br>Added Data retention and Endurance Table<br>Added Thermal resistance values<br>Changed parameter t <sub>AS</sub> to t <sub>SA</sub><br>Changed t <sub>RECALL</sub> from 50us to 120us (including t <sub>SS</sub> of 70us)<br>Renamed t <sub>GLAX</sub> to t <sub>HA</sub><br>Updated figure 11 and 12<br>Renamed t <sub>HLHX</sub> to t <sub>PHSB</sub><br>Updated Figure 13 |
| *J   | 2695908 | GVCH/AESA       | 04/20/2009      | Removed part numbers CY14B101L-SP25XC and CY14B101L-SP25XCT.<br>Added part numbers CY14B101LL-SP25XC and CY14B101LL-SP25XCT.   |
| *K   | 2814390 | GVCH            | 11/25/2009      | Added Note in the Ordering information section mentioning that these parts are not recommended for new designs.<br>Added "Not recommended for new designs" watermark in the PDF..  |

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