CYPRESS PERFORM

CYRS1049DV33

4-Mbit (512 K × 8) Static RAM with RadStop™ Technology

Radiation Performance

Radiation Data

- Total dose = 300 Krad
- Soft error rate (both heavy ion and proton) Heavy ions ≤ 1×10^{-10} upsets/bit-day with single-error correction, double error detection error detection and correction (SEC-DED EDAC)
- Neutron = 2.0×10^{14} N/cm^2
- Dose rate ≥ 2.0×10^9 (rad(Si)/s)
- Latch up immunity LET = 120 MeV.cm^2/mg (125 °C)

Processing Flows

- Q Grade - Class Q flow in compliance with MIL-PRF 38535
- V Grade - Class V flow in compliance with MIL-PRF 38535

Prototyping Options

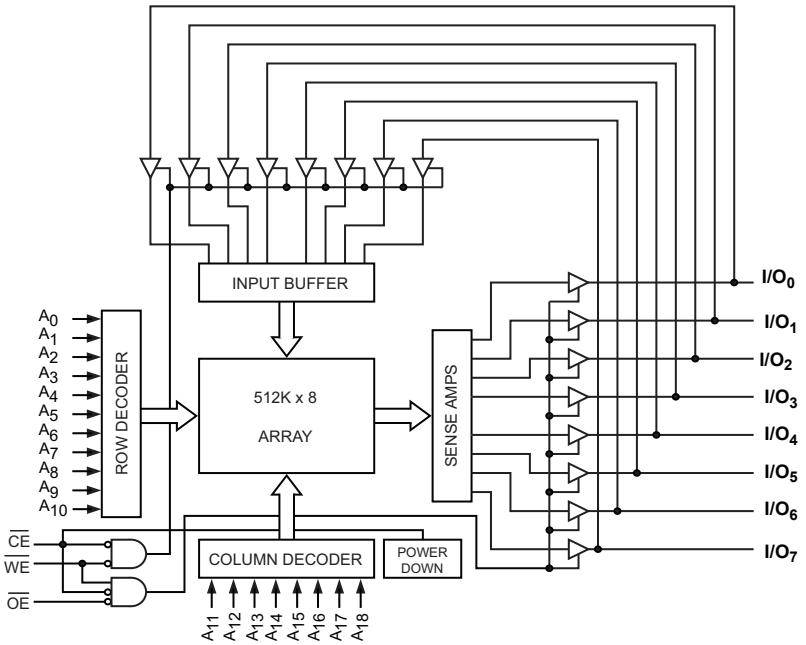
- CYPT1049DV33 protos with same functional and timing as flight units using non-radiation hardened die
- Characteristics in a 36-pin ceramic flat package

Features

- Temperature ranges
  - Military/Space: –55 °C to 125 °C
- High speed
  - t_{AA} = 12 ns
- Low active power
  - I_{CC} = 95 mA at 12 ns (P_{MAX} = 315 mW)
- Low CMOS standby power
  - I_{SB2} = 15 mA
- 2.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 36-pin ceramic flat package

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Functional Description

The CYRS1049DV33 is a high-performance complementary metal oxide semiconductor (CMOS) static RAM organized as 512 K words by 8 bits with RadStop™ technology. Cypress's state-of-the-art RadStop technology is radiation hardened through proprietary design and process hardening techniques. The 4-Mbit fast asynchronous SRAM with RadStop technology is also QML V certified with Defense Logistics Agency Land and Maritime (DLAM).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See the Truth Table on page 11 for a complete description of read and write modes.

The eight input or output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW)

The CYRS1049DV33 is available in a ceramic 36-pin Flat package with center power and ground (revolutionary) pinout.

Easy memory expansion is provided by utilizing $\overline{OE}$, $\overline{CE}$, and tri-state drivers.

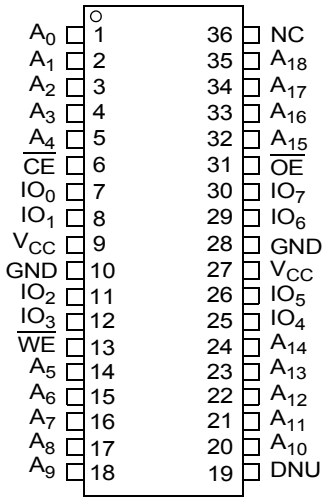
For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Selection Guide

Description	Military/Space	Unit
Maximum access time	12	ns
Maximum operating current	95	mA
Maximum CMOS standby current	15	mA

Pin Configuration

Figure 1. 36-pin Ceramic Flat Package pinout (Top View) [1]



Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [2] .....–0.3 V to +4.6 V

DC voltage applied to outputs in High Z state [2] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Military/Space	–55 °C to +125 °C	3.3 V ± 0.3 V	12 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Military/Space		Unit
				Min	Max	
V_{OH}	Output high voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output low voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH} [2]	Input high voltage			2.0	V_{CC} + 0.3	V
V_{IL} [2]	Input low voltage			–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, output disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	83 MHz	–	95	mA
			66 MHz	–	85	mA
			40 MHz	–	75	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0		–	15	mA

Note

2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

Capacitance

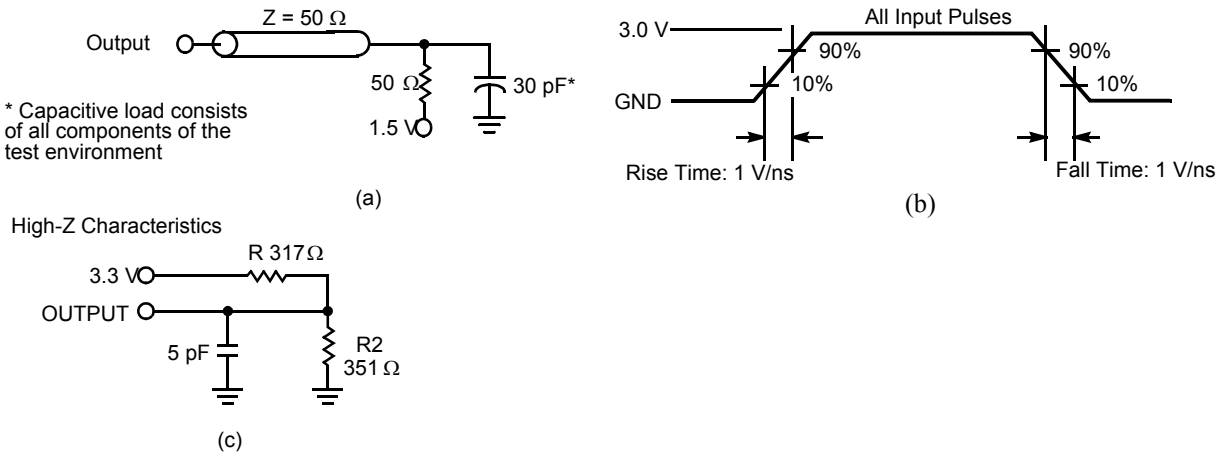
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	Ceramic Flat Package	Unit
Θ_{JC}	Thermal resistance (junction to case)	Test according to MIL-PRF 38538	3.6	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

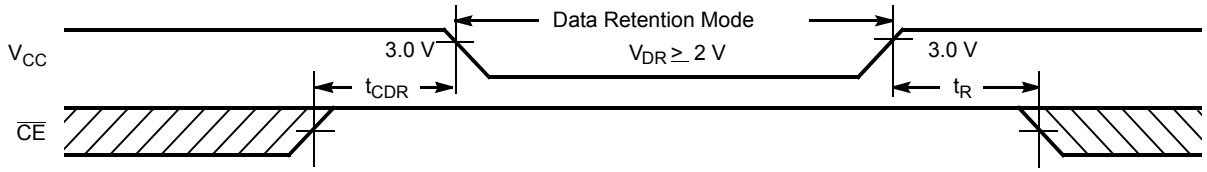
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [5]	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	15	mA
t_{CDR}[6]	Chip deselect to data retention time	–	0	–	ns
t_R[7]	Operation recovery time	–	12	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
5. No input may exceed V_{CC} + 0.3 V.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

AC Switching Characteristics

Over the Operating Range

Parameter [8]	Description	Military/Space		Unit
		Min	Max	
Read Cycle				
t_{power} [9]	V_{CC} (typical) to the first access	100	–	µs
t_{RC}	Read cycle time	12	–	ns
t_{AA}	Address to data valid	–	12	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	12	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [10]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [10, 11]	–	6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [10]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [10, 11]	–	6	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power-down	–	12	ns
Write Cycle [12, 13]				
t_{WC}	Write cycle time	12	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	–	ns
t_{AW}	Address setup to write end	8	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	8	–	ns
t_{SD}	Data setup to write end	6	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [10]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [10, 11]	–	6	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write and the transition of either of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 [14, 15]

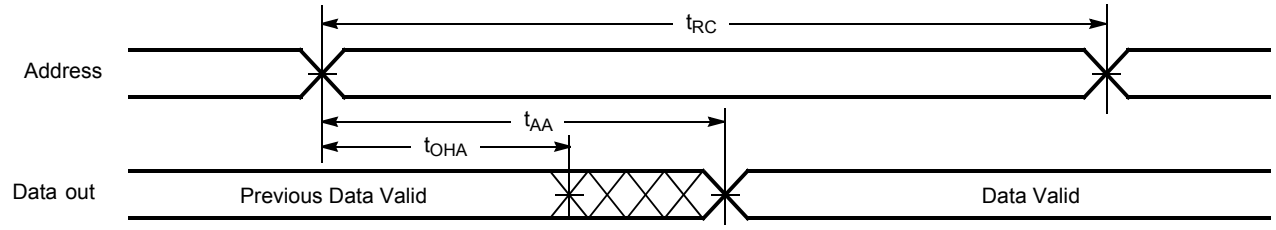
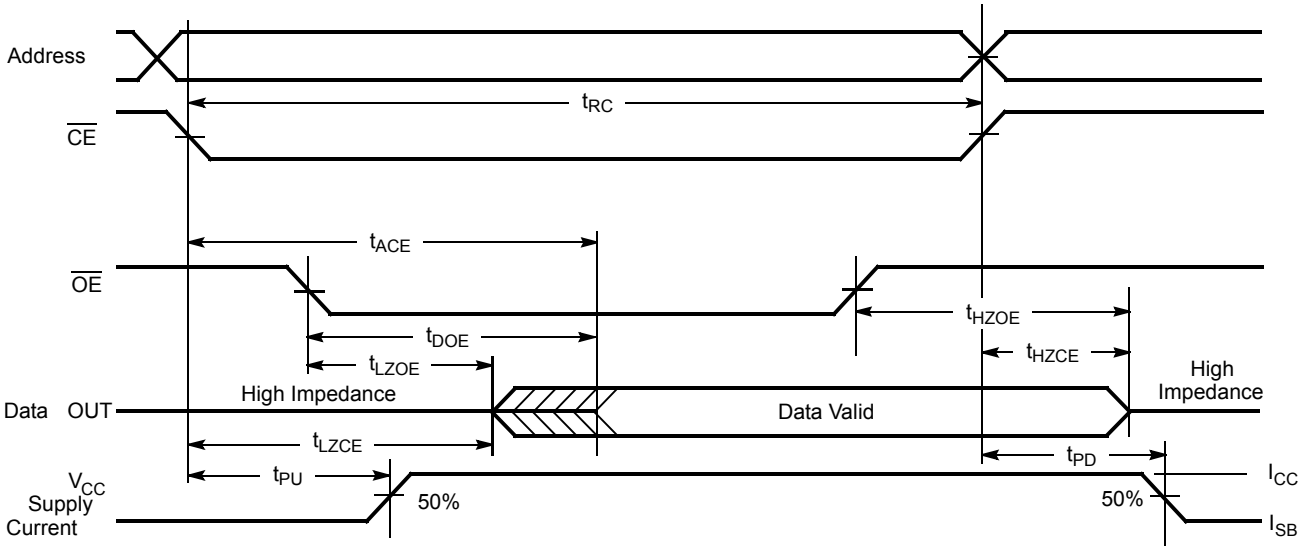


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]

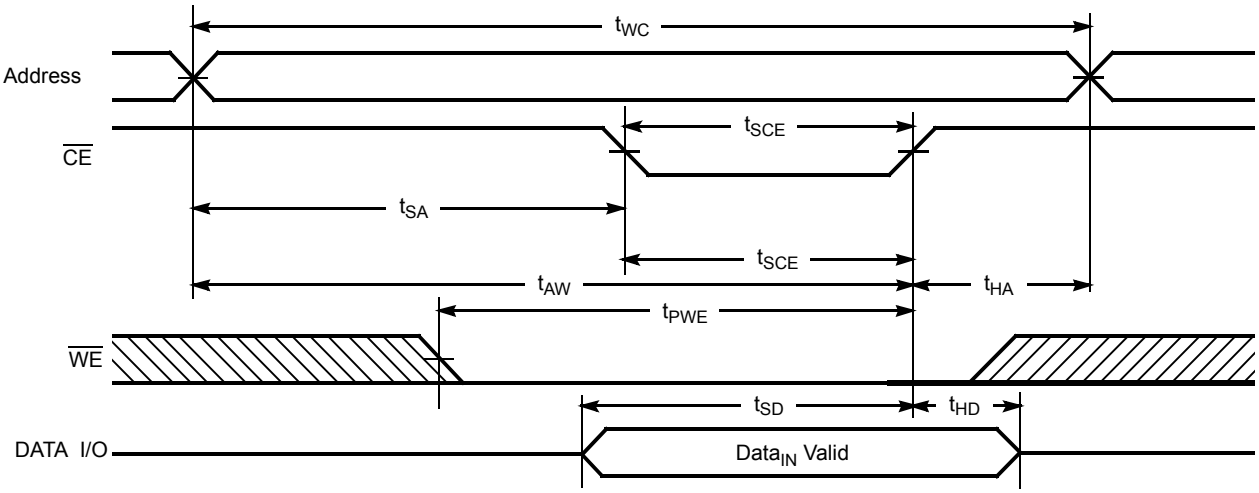
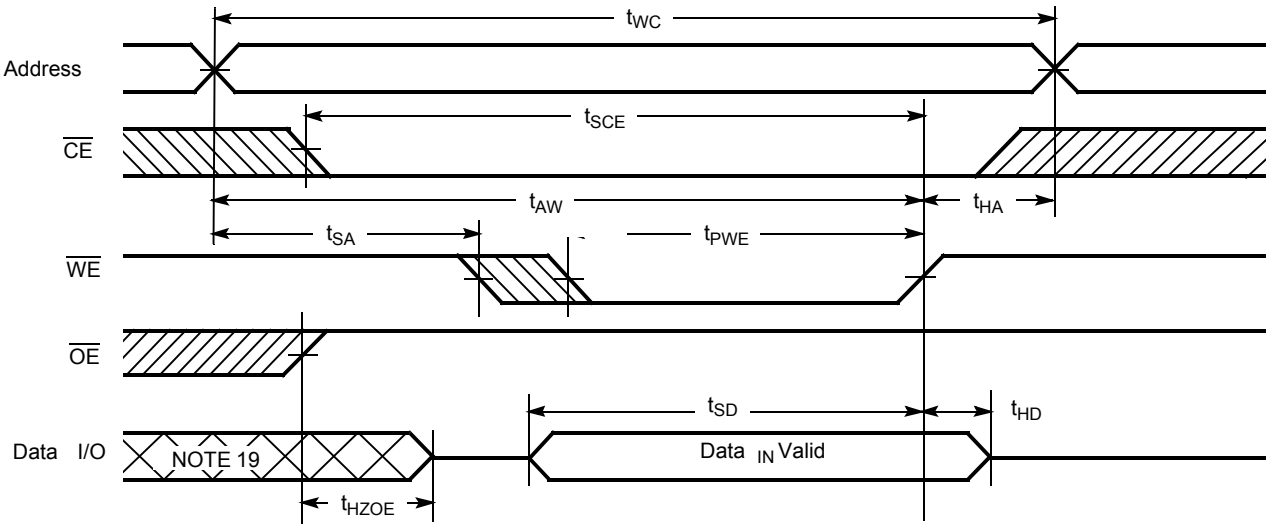


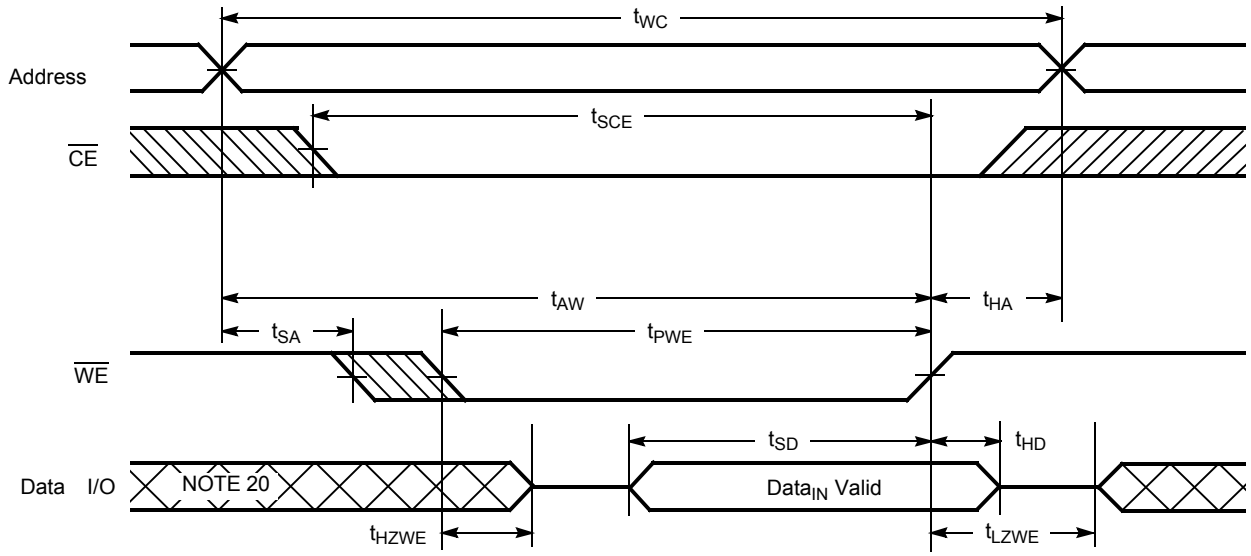
Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [17, 18]



Notes
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Note
20. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB1}or I_{SB2})
L	L	H	Data out	Read	Active (I_{CC})
L	X	L	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs disabled	Active (I_{CC})

Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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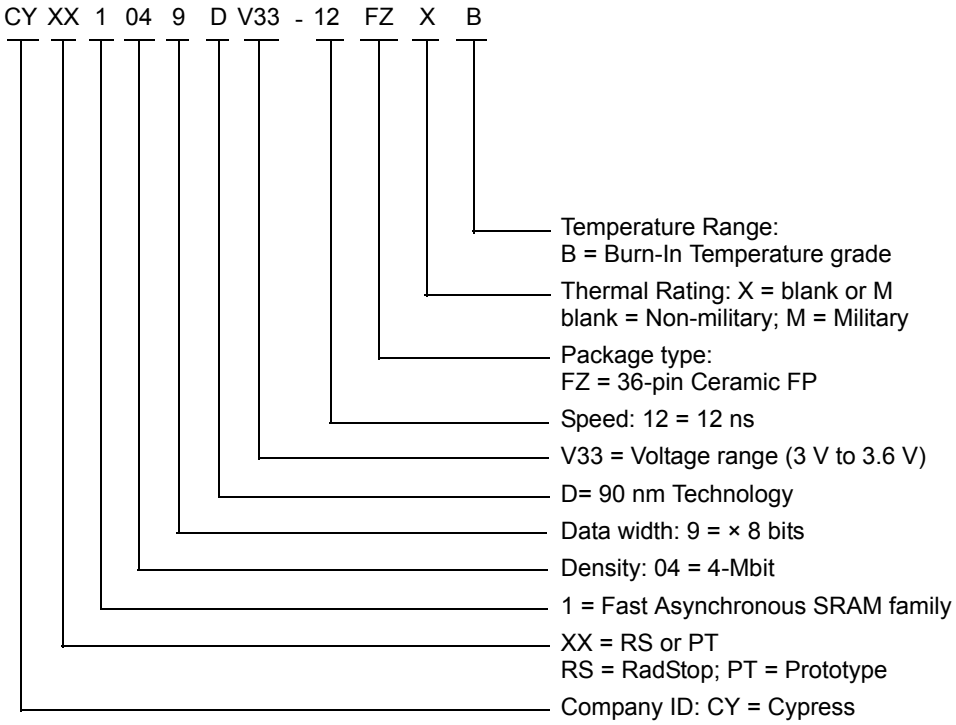
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CYRS1049DV33-12FZMB	001-67583	36-pin ceramic flat package	Burn-In
12	CYPT1049DV33-12FZMB	001-67583	36-pin ceramic flat package, Prototype part	Burn-In
12	5962F1123501QXA	001-67583	36-pin ceramic flat package, DLAM part	Burn-In
12	5962F1123501VXA	001-67583	36-pin ceramic flat package, DLAM part	Burn-In

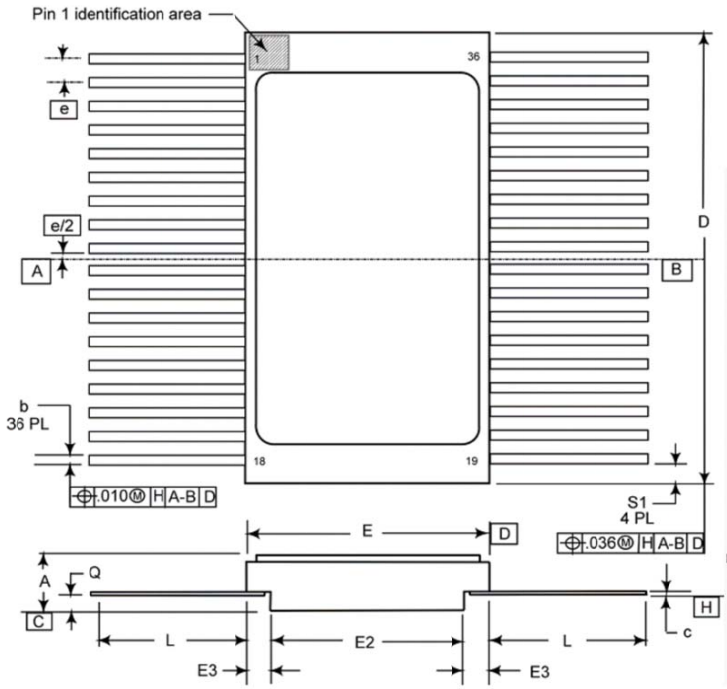
Contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



Package Diagram

Figure 9. 36-pin Ceramic Flat Pack (Solder Seal Lid) Package Outline, 001-67583



Case outline X

SYMBOL	Millimeters		Inches	
	Min	Max	Min	Max
A	2.40	2.99	0.094	0.118
b	0.38	0.48	0.015	0.019
c	0.102	0.152	0.004	0.006
D	23.12	23.62	0.910	0.930
E	11.99	12.39	0.472	0.488
E2	9.96	10.36	0.392	0.408
E3	0.082	1.22	0.003	0.048
e	1.19	1.35	0.047	0.053
L	10.19	10.64	0.401	0.419
Q	0.64	---	0.025	---
S1	0.13	---	0.51	---

NOTES:
1. Item was originally designed in millimeters.
2. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
3. The sealring and lid are not electrically connected to V_{SS} (isolated).
4. Lead finish is in accordance with MIL-PRF-38535.
5. Package material: opaque 90% minimum Alumina ceramic.

001-67583 *C

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
DLAM	Defense Logistics Agency Land and Maritime
DNU	Do Not Use
EDAC	Error Detection and Correction
I/O	Input/Output
LET	Linear Energy Transfer
$\overline{OE}$	Output Enable
QML	Qualified Manufacturers List
SEC-DED	Single Error Correction – Double Error Detection
SEL	Single-Event Latch-up
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Glossary

Total Dose	Permanent device damage due to ions over device life
Heavy Ion	Instantaneous device latch up due to single ion
LET	Linear energy transfer (measured in MeVcm^2)
Krad	Unit of measurement to determine device life in radiation environments.
Neutron	Permanent device damage due to energetic neutrons or protons
Prompt Dose	Data loss of permanent device damage due to X-rays and gamma rays <20 ns
RadStop Technology	Cypress's patented Rad Hard design methodology
QML V	Space level certification from DSCC.
DLAM	Defense Logistics Agency Land and Maritime
LSBU	Logical Single Bit Upset. Single bits in a single correction word are in error.
LMBU	Logical Multi Bit Upset. Multiple bits in a single correction word are in error

Document History Page

Document Title: CYRS1049DV33, 4-Mbit (512 K × 8) Static RAM with RadStop™ Technology Document Number: 001-64292				
Rev.	**ECN No.**	**Origin of Change**	**Submission Date**	**Description of Change**
**	3098986	HRP	12/01/2010	New data sheet.
*A	3181475	PRAS	02/24/2011	Updated Package Diagram (Replaced 44-pin TSOP II package with 36-pin flat package).
*B	3438781	HRP	11/14/2011	Updated Package Diagram (to current revision).
*C	3554946	HRP	03/19/2012	Changed status from Preliminary to Final. Updated Radiation Performance (Updated Radiation Data, Prototyping Options). Updated Features (Added (P_{MAX} = 315 mW)). Updated Functional Description (Added the paragraph “Easy memory expansion is provided by utilizing $\overline{OE}$, $\overline{CE}$, and tri-state drivers.”). Updated Maximum Ratings (DC voltage applied to outputs in High Z state, DC input voltage). Updated AC Switching Characteristics(Changed the maximum value of t_{DOE} parameter from 7 ns to 6 ns). Updated Ordering Information (Additional part numbers added).
*D	3887928	HRP	02/07/2013	Updated Radiation Performance (Updated Processing Flows (Replaced V grade with Q grade), Prototyping Options (Added non-radiation hard, replaced V grade with Q grade)). Updated Ordering Information (Updated part numbers).
*E	4208547	VINI	12/03/2013	Updated Radiation Performance: Updated Processing Flows: Added “V Grade - Class V flow in compliance with MIL-PRF 38535”. Updated Prototyping Options: Updated the first bullet as “CYPT1049DV33 protos with same functional and timing as flight units using non-radiation hardened die”. Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 001-67583 – Changed revision from *A to *B. Updated in new template. Completing Sunset Review.
*F	4571914	VINI	11/17/2014	Added related documentation hyperlink in page 1. Updated Figure 9 in Package Diagram (spec 001-67583 *B to *C).

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