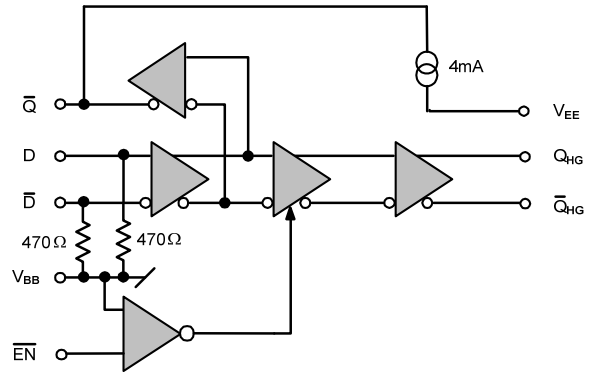


**FEATURES**

- Minimizes External Components
- High Bandwidth for  $\geq 1\text{GHz}$
- Similar Operation as CTSLVEL16VR
  - Except in Disabled Condition
  - $Q_{HG}$  is High
- $-147\text{ dBc/Hz}$  Typical Noise Floor

**BLOCK DIAGRAM**



**DESCRIPTION**

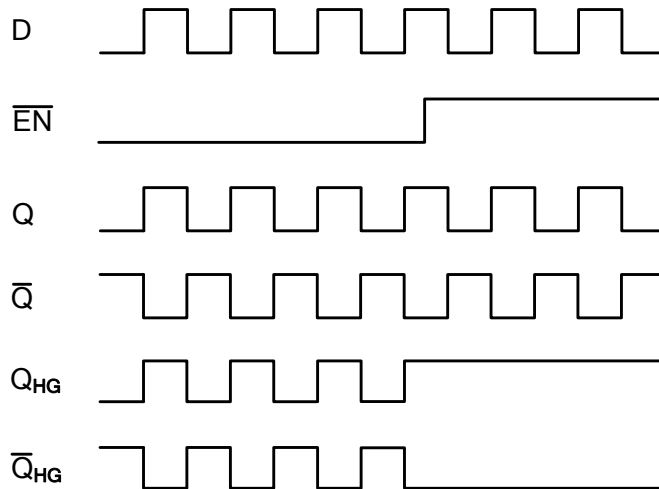
The CTSLVEL16VT is a specialized oscillator gain stage with a high gain output buffer including an enable function. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have voltage gain several times greater than the  $\bar{Q}$  output. It provides a  $Q_{HG}/\bar{Q}_{HG}$  enable that allows continuous oscillator operation via the  $\bar{Q}$  outputs.

The CTSLVEL16VT also provides a 4mA internal pull-down current source for  $\bar{Q}$  outputs. Internal input biasing further reduces the number of needed external components.

**ENGINEERING NOTES**

The CTSLVEL16VT is a specialized oscillator gain stage with a high gain output buffer including an enable. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have a voltage gain several times greater than the  $\bar{Q}$  output. When the  $\bar{EN}$  input is LOW, the  $\bar{Q}$  and  $Q_{HG}/\bar{Q}_{HG}$  outputs follow the data inputs. When  $\bar{EN}$  is HIGH, the  $Q_{HG}$  output is forced high and the  $\bar{Q}_{HG}$  output is forced low.

In the CTSLVEL16VT, the  $\bar{D}$  input is internally tied directly to the  $V_{BB}$  pin and the D input is tied to the  $V_{BB}$  pin through a  $470\Omega$  internal bias resistor. Bypassing  $V_{BB}$  to ground with a  $0.01\ \mu\text{F}$  capacitor is recommended.

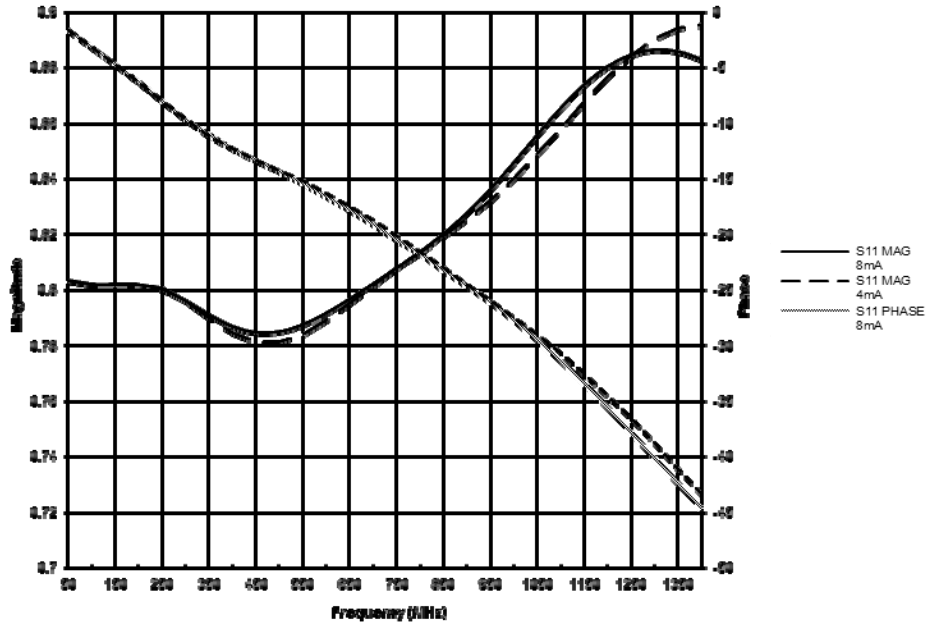


**Timing Diagram**

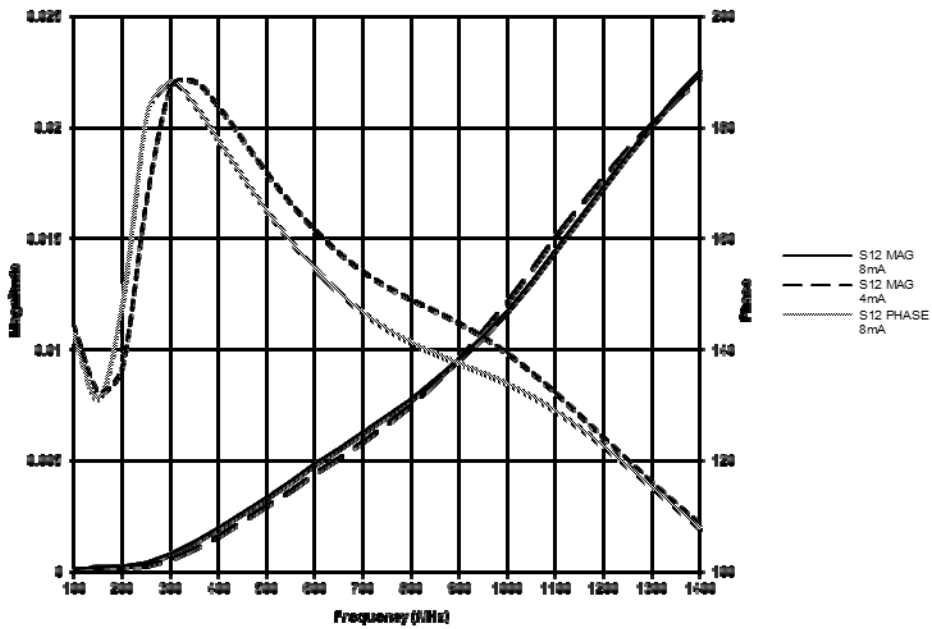
CTSLVEL16VT

PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

MLP8



S11

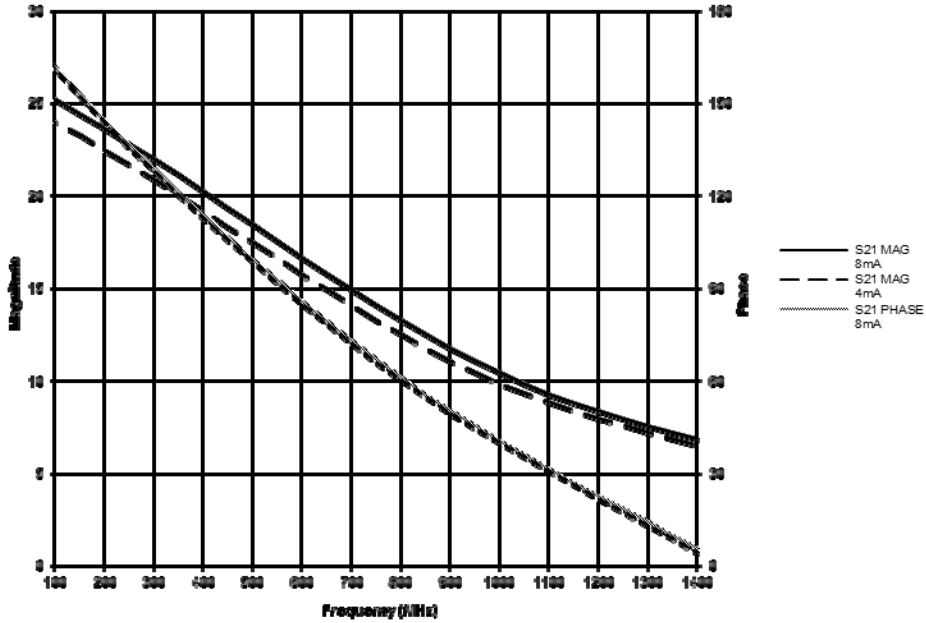


S12

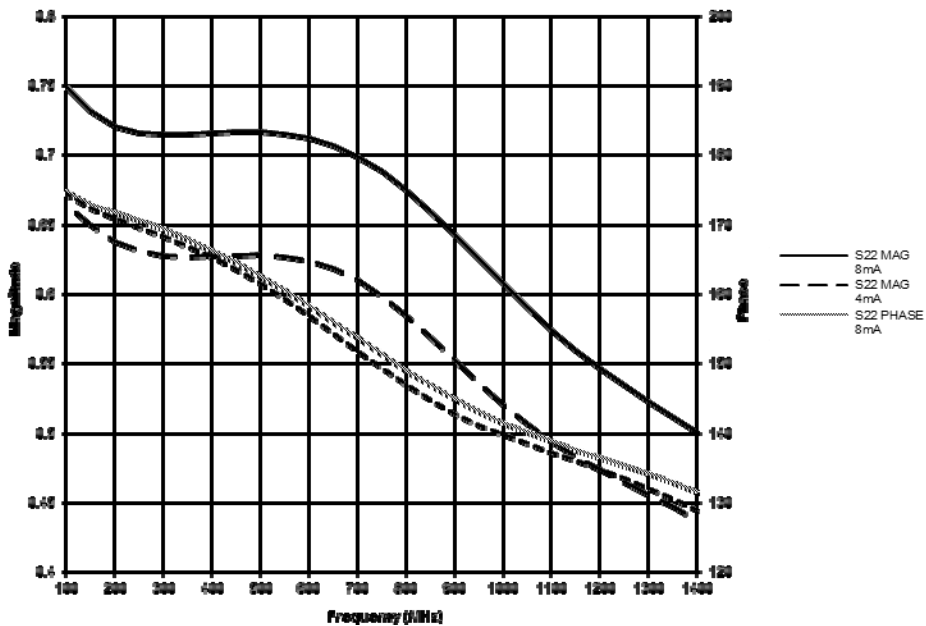
CTSLVEL16VT

PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

MLP8



S21



S22

## ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
$V_{CC}$	PECL Power Supply	$V_{EE} = 0V$	0 to + 6.0	V
$V_{D\_PECL}$	PECL D Input Voltage	Referenced to $V_{BB}$	$\pm 0.75$	V
$V_{EN\_PECL}$	PECL D Input Voltage	$V_{EE} = 0V$	0 to + 6.0	V
$V_{EE}$	ECL Power Supply	$V_{CC} = 0V$	-6.0 to 0	V
$V_{D\_ECL}$	ECL D Input Voltage	Referenced to $V_{BB}$	$\pm 0.75$	V
$V_{EN\_ECL}$	ECL D Input Voltage	$V_{CC} = 0V$	-6.0 to 0	V
$I_{OUT}$	Output Current	Continuous Q	25	mA
		Surge Q	50	
		Continuous $Q_{HG}$	50	
		Surge $Q_{HG}$	100	
$T_A$	Operating Temperature Range	-	-40 to +85	$^{\circ}C$
$T_{STG}$	Storage Temperature Range	-	-65 to +150	$^{\circ}C$
ESD <sub>HBM</sub>	Human Body Model Electro Static Discharge	-	2500	V
ESD <sub>MM</sub>	Machine Model Electro Static Discharge	-	200	V
ESD <sub>CDM</sub>	Charged Device Model Electro Static Discharge	-	2000	V

### ECL DC Characteristics ( $V_{EE} = -3.0V$ to $-5.5V$ , $V_{CC} = GND$ )

Symbol	Characteristic	$-40^{\circ}C$		$0^{\circ}C$		$25^{\circ}C$		$85^{\circ}C$		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1</sup>	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
$V_{OL}$	Output LOW Voltage <sup>1</sup>	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
$V_{IH}$	Input HIGH Voltage D,EN	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
$V_{IL}$	Input LOW Voltage D,EN	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
$V_{BB}$	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	$\mu A$
$I_{IL}$	Input LOW Current EN	0.5		0.5		0.5		0.5		$\mu A$
$I_{EE}$	Power Supply Current <sup>1</sup>		48		48		48		54	mA

<sup>1</sup> Specified with each output terminated through 50 $\Omega$  resistors to  $V_{CC} - 2V$ .

**LVPECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +3.3\text{V}$ )**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	2255	2465	2275	2465	2275	2465	2275	2465	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	1375	1745	1400	1680	1400	1680	1400	1680	mV
$V_{IH}$	Input HIGH Voltage D,EN	2135	2560	2135	2560	2135	2560	2135	2560	mV
$V_{IL}$	Input LOW Voltage D,EN	1400	1825	1400	1825	1400	1825	1400	1825	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN	0.5		0.5		0.5		0.5		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2 Specified with each output terminated through 50 Ω resistors to  $V_{CC} - 2\text{V}$ .

**PECL DC Characteristics ( $V_{EE} = \text{GND}$ ,  $V_{CC} = +5.0\text{V}$ )**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	3955	4165	3975	4165	3975	4165	3975	4165	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	3075	3445	3100	3380	3100	3380	3100	3380	mV
$V_{IH}$	Input HIGH Voltage D,EN	3835	4260	3835	4260	3835	4260	3835	4260	mV
$V_{IL}$	Input LOW Voltage D,EN	3100	3525	3100	3525	3100	3525	3100	3525	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IH}$	Input HIGH Current EN		150		150		150		150	μA
$I_{IL}$	Input LOW Current EN	0.5		0.5		0.5		0.5		μA
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

1 For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

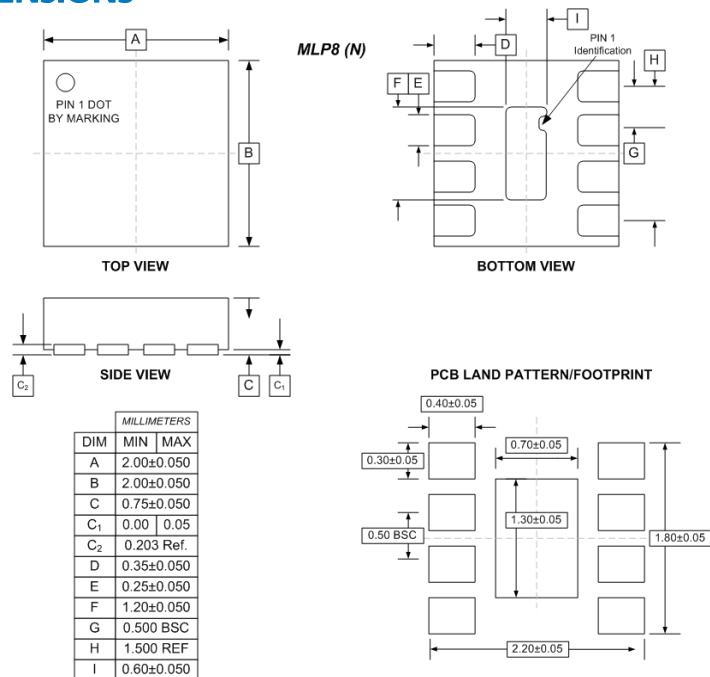
2 Specified with each output terminated through 50Ω resistors to  $V_{CC} - 2\text{V}$ .

**AC Characteristics ( $V_{EE} = -3.0V$  to  $-5.5V$ ;  $V_{CC}=GND$  or  $V_{EE}=GND$ ;  $V_{CC} = +3.0V$  to  $+5.5V$ )**

Symbol	Characteristic	40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH}/t_{PHL}$	Propagation Delay													
	D to $Q^1$			350			350			350			350	ps
	D to $Q_{HG}^2$			450			450			450			450	ps
$t_{SKEW}$	Duty Cycle Skew <sup>3</sup>		5	20		5	20		5	20		5	20	ps
$V_{pp}$ (AC)	Input Swing <sup>4</sup> Differential	80		1000	80		1000	80		1000	80		1000	mV
	Input Swing <sup>4</sup> Single Ended	160		1500	160		1500	160		1500	160		1500	
$t_r/t_f$	Output Rise/Fall <sup>1,2</sup> (20% - 80%)	100		240	100		240	100		240	100		240	ps

- <sup>1</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} -2V$ .
- <sup>2</sup> Specified with each output terminated through 50Ω resistors to  $V_{CC} -2V$ .
- <sup>3</sup> Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
- <sup>4</sup> The peak-to-peak input swing is the range for which AC parameters are guaranteed. D and  $\bar{D}$  must remain within the range of  $\pm 750$  mV with respect to  $V_{BB}$ . The device has a voltage gain of  $\sim 20$  to the  $\bar{Q}$  outputs and a voltage gain of  $\sim 100$  to the  $Q_{HG}/\bar{Q}_{HG}$  outputs.

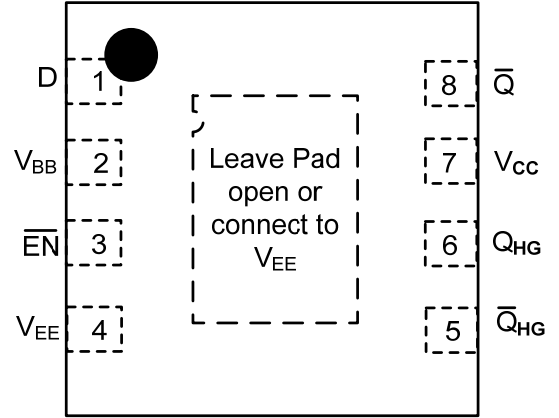
**PACKAGE DIMENSIONS**



**Pin Description and Configuration**

**Pin Assignments for CTSLVEL16VTNNG**

Pin	Name	Type	Function
1	D	Input	Data Input
2	V <sub>BB</sub>	Output	Reference Voltage
3	EN	Input	Output Enable
4	V <sub>EE</sub>	Power	Negative Supply
5	$\bar{Q}_{HG}$	Output	High Gain Inverting PECL Output
6	Q <sub>HG</sub>	Output	High Gain PECL Output
7	V <sub>CC</sub>	Power	Positive Supply
8	$\bar{Q}$	Output	Inverting PECL Output
9	NC	-	N/A



**CTSLVEL16VTNNG**

**PART ORDERING NUMBER**

Part Number	Package	Marking
CTSLVEL16VTNNG	MLP8	P8G YYWW