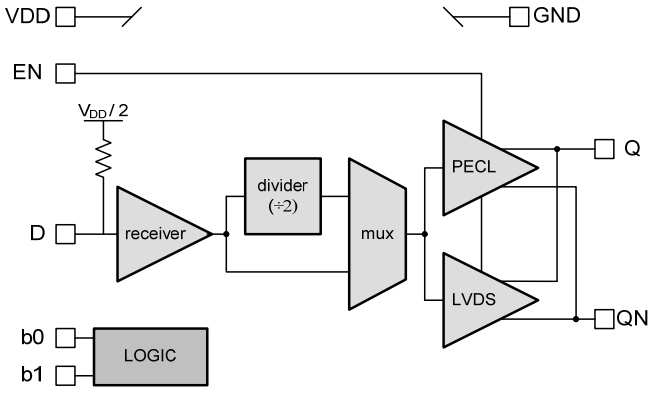
Ultra-Low Phase Noise LVPECL, LVDS Buffer and Translator with Gain

SON8, MSOP8

FEATURES

- 2.5V-3.3V Operation
- Ultra-Low Phase Noise Floor
  - LVPECL -167dBc/Hz
  - LVDS -165dBc/Hz
- Configurable
  - LVPECL or LVDS Output
  - ÷1 or ÷2
  - Enable Active High or Low
- 1GHz+ Bandwidth
- RoHS Compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

- The CTSLV315 is a configurable LVPECL, LVDS buffer & translator IC that is optimized for ultra-low phase noise and 2.5V-3.3V nominal supply voltage. It is particularly useful in converting crystal or SAW based oscillators into LVPECL and LVDS outputs for up to 1GHz of bandwidth.

- Recommended for applications with signal levels below 0.6 Vp-p. For applications with higher signal levels that do not require gain, refer to the CTSLV310. CTS encourages the user to try both devices to determine which is best suited for a particular application.

- A configurable IC design capable of providing LVPECL or LVDS outputs, ÷1 or ÷2 function, and active high or active low enable selection. See Table 1 for details of the configurations options that provide designers with a single IC buffer/translator solution that is extremely compact, flexible and high performance.

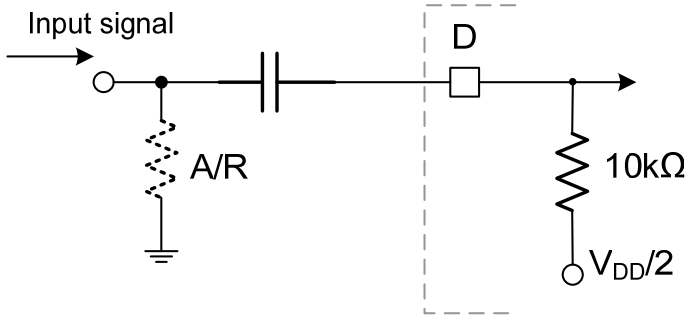
- 8 configurations which are determined by the static voltage levels of b-0 and b-1. Table 1 details the configurations.

Table 1 - Possible IC Configuration

Configuration Bits		Functional Configuration		
b-0	**b-1**	**Output Type**	**Enable Polarity**	**Division**
Open	Open	LVPECL	Active High	÷1
Open	Low	LVPECL	Active High	÷2
Open	High	LVPECL	Active Low	÷1
Low	Open	LVPECL	Active Low	÷2
Low	Low	LVDS	Active High	÷1
Low	High	LVDS	Active High	÷2
High	Open	LVDS	Active Low	÷1
High	Low	LVDS	Active Low	÷2
High	High	Not Used	Not Used	Not Used

Input Termination

The D input bias is $V_{DD}/2$ fed through an internal 10kΩ resistor. For clock applications, an input signal of at least 750m V_{PP} ensures the CTSLV15 meets AC specifications. The input should also be AC coupled to maintain a 50% duty cycle on the outputs. The input can be driven to any voltage between 0V and V_{DD} without damage or waveform degradation.

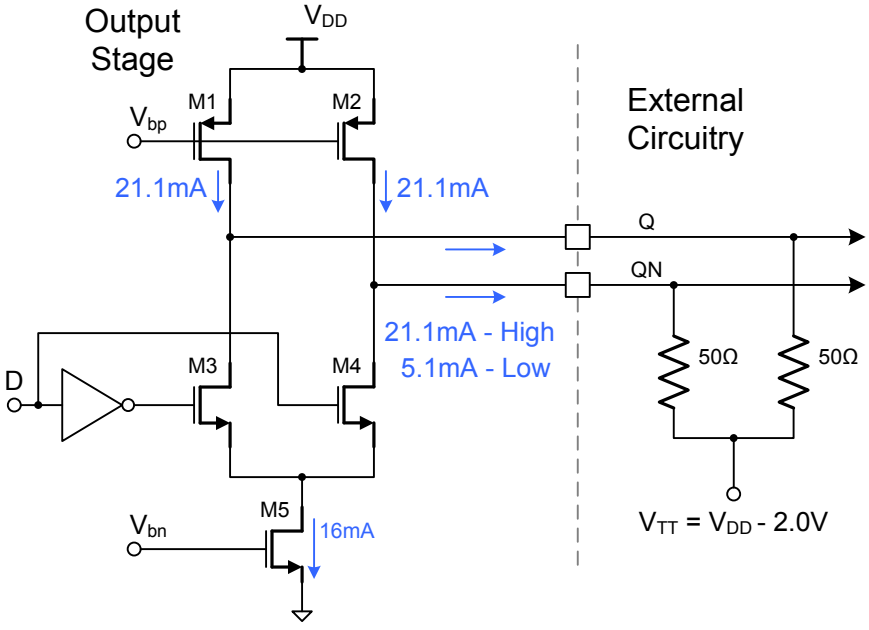


LVPECL Output Termination Techniques

DC Coupling

The LVPECL compatible output stage of the CTSLV315 uses a current drive topology to maximize switching speed as illustrated below. Two current source PMOS transistors (M1-M2) feed the output pins. M5 is an NMOS current source which is switched by M3 and M4. When M4 is on, M5 takes current from M2. This produces an output current of 5.1mA (low output state). M3 is off, and the entire 21.1mA flows through the output pin. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs.

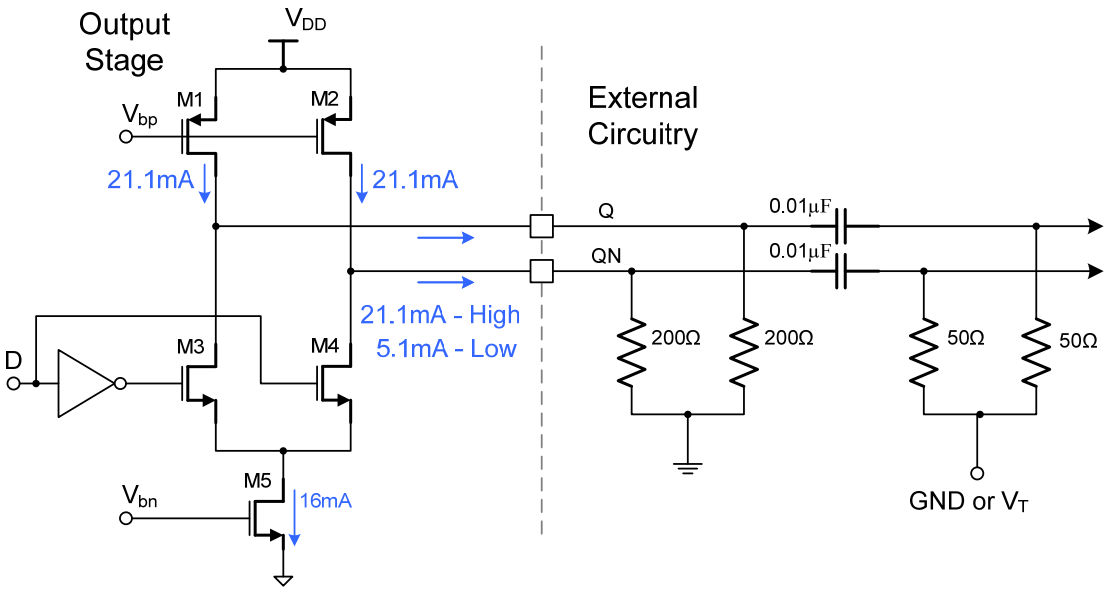
Both Q and QN should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.



Typical Output Termination

AC Coupling

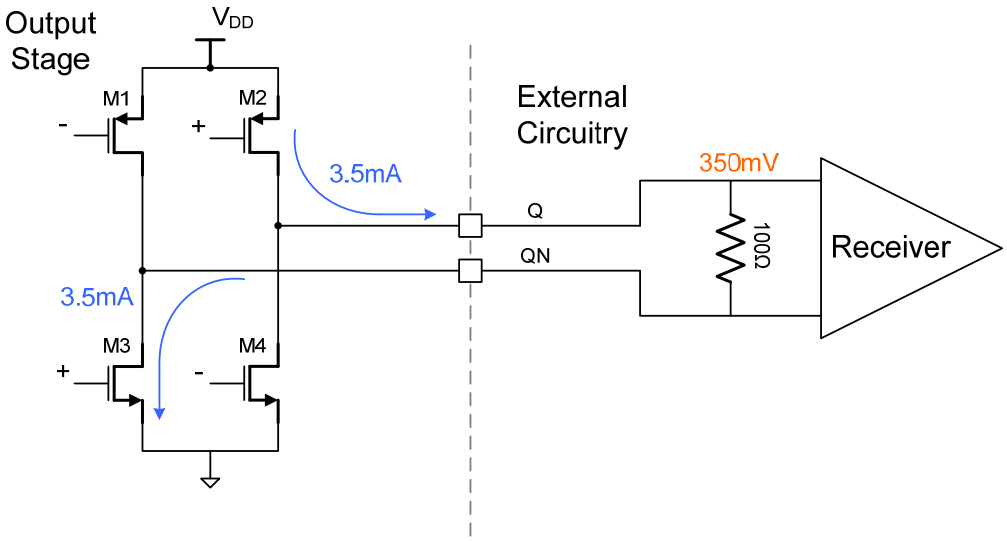
Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. The illustration below shows the AC coupling technique. The 200Ω resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination of the 200Ω and 50Ω resistors results in a net 40Ω AC load termination. In many cases this will work well. If necessary, the 50Ω resistors can be increased to about 56Ω. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.



AC Termination

LVDS Output Termination Technique

The following LVDS termination is compliant to the LVDS specification *TIA/EIA-644A*.



LVDS Termination

ELECTRICAL SPECIFICATIONS

Absolute Maximum Rating

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		2.375	2.5		V
				3.3	3.6	
$V_{ABSOLUTE}$	Absolute Max Power Supply	Continuous			3.6	V
		t ≤ 1s			5.5	
T_{OP}	Operating Temperature Range		-40		85	°C
$T_{STORAGE}$	Storage Temperature Range		-65		150	°C
V_{I_MAX}	Maximum Input Voltages	D	-0.5		V_{DD} +0.5	V
		EN	-0.5		V_{DD} + 0.5	
		b0	-0.5		V_{DD} + 0.5	
		b1	-0.5		V_{DD} + 0.5	
$I_{b0,b1}$	b-0, b-1 Input High Current	b-0, b-1 = V_{DD}			11	uA
	b-0, b-1 Input Low Current	b-0, b-1 = GND	-11			
$Vt_{b0,b1}$	b-0, b-1 Input High Voltage Threshold		V_{DD} -0.5		V_{DD}	V
	b-0, b-1 Input Low Voltage Threshold		0		0.5	
I_{EN}	EN Input Current		-4		3	uA
Vt_{EN}	EN Input High Voltage Threshold		V_{DD} -0.5		V_{DD}	V
	EN Input Low Voltage Threshold		0		0.5	
ESD	ESD Ratings	Human Body Model	2000			V
		Machine Model	200			
		Charged Device Model	2000			

LVPECL Performance Specifications

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
f_{MAX}	Max Input Frequency	÷1 mode	1000			MHz
		÷2 mode	1600			
R_L	Output Loading			50		Ω
R_{BIAS}	Input Bias Resistor	D input to $V_{DD}/2$ ref		10k		Ω
V_{IN_SWING}[1]	Input Voltage Swing		0.2			V_{PP}
V_{OUT}	Voltage Output Levels	V_{DD} = 2.5V, HIGH	V_{DD} -1.25		V_{DD} -0.88	V
		V_{DD} = 2.5V, LOW	V_{DD} -1.86		V_{DD} -1.66	V
		V_{DD} = 3.3V, HIGH	V_{DD} -1.15		V_{DD} -0.88	V
		V_{DD} = 3.3V, LOW	V_{DD} -1.86		V_{DD} -1.75	V
V_{OD}	Differential Output Voltage	V_{DD} = 2.5V	0.54		0.93	V_{PP}, Q/QN
			0.75		5.47	dBm, Q/QN
		V_{DD} = 3.3V	0.74		0.93	V_{PP}, Q/QN
			3.49		5.47	dBm, Q/QN
t_R / t_F	Output Rise/Fall Time	80%-20%	100		205	ps
PN	Phase Noise Floor	1MHz Offset	-167			dBc/Hz
J_{INTEG}	Integrated Jitter: 12kHz-20MHz	155MHz Carrier	26			ƒs
T_{ENABLE}	Enable Time[2]	EN = active			15	us
$T_{DISABLE}$	Disable Time[2]	EN = disabled			0.5	us
T_{PROP}	Propagation Delay[3]		0.9		2.2	ns
I_{DD}	Power Supply Current	EN = active[4]		28.5		mA
		EN = disabled[5]			5	

1 Phase noise floor performance is dependent upon input voltage swing.

2 Into and out of tri-state condition.

3 Time from D crossing $V_{DD}/2$ to Q=QN.

4 V_{DD} =3.3V, F_{IN} @ 200MHz.

5 D = 0V.

LVDS Performance Specifications

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
f_{MAX}	Max Input Frequency	÷1 mode	1000			MHz
		÷2 mode	1600			
R_L	Output Loading			100		Ω
R_{BIAS}	Input Bias Resistor	D input to V_{DD}/2 ref		10k		Ω
V_{IN_SWING}[1]	Input Voltage Swing		0.2			V_{PP}
V_{OUT}	Voltage Output Levels	V_{DD} = 2.5V	290		454	mV
		V_{DD} = 3.3V	290		454	
V_{OD}	Differential Output Voltage		-50		50	mV
V_{OC}	Common Mode Output Voltage		1.125		1.375	V
ΔV_{OC}	Delta in Common Mode Output Voltage[2]		-50		50	mV
$V_{OC,PP}$	Peak-to-Peak Common Mode Output Voltage				100	mV
t_R / t_F	Output Rise/Fall Time	80%-20%	120		220	ps
PN	Phase Noise Floor	1MHz Offset	-165			dBc/Hz
J_{INTEG}	Integrated Jitter: 12kHz - 20MHz	155MHz Carrier	36			ƒs
T_{ENABLE}	Enable Time[3]	EN = active			4	us
$T_{DISABLE}$	Disable Time[3]	EN = disabled			0.5	us
T_{PROP}	Propagation Delay[4]		0.8		1.7	ns
I_{DD}	Power Supply Current	EN = active[5]		12.9		mA
		EN = disabled[6]			5	

1 Phase noise floor performance is dependent upon input voltage swing.

2 Between logics states.

3 Into and out of tri-state condition.

4 Time from D crossing V_{DD}/2 to Q=QN.

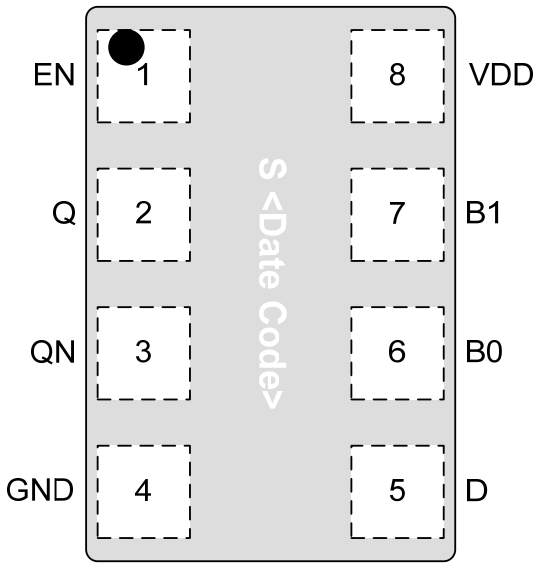
5 V_{DD} =3.3V, F_{in} @ 200MHz.

6 D = 0V.

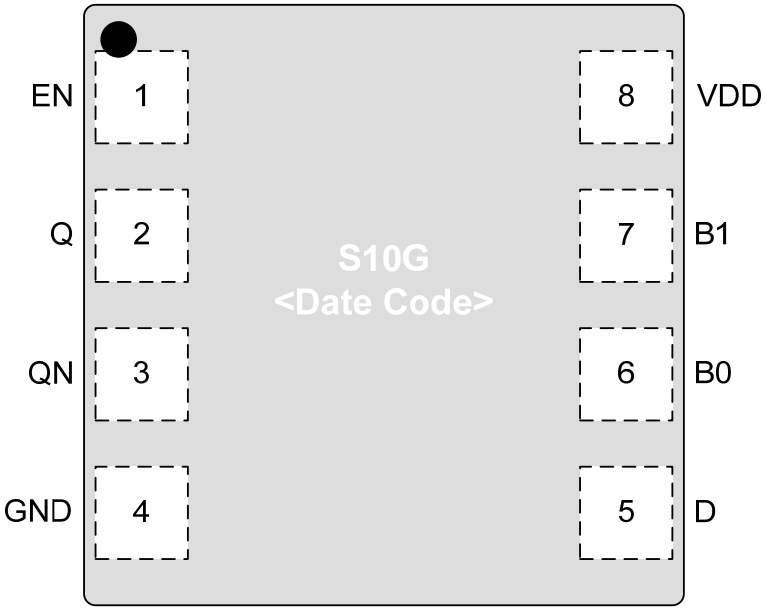
Pin Description and Configuration

Pin Assignments

Pin	Name	I/O/P	Function	Properties
1	EN	I	Enable	Configurable functionality
2	Q	O	Output Signal	Configurable (LVPECL, LVDS)
3	QN	O	Output Signal	Configurable (LVPECL, LVDS)
4	GND	P	Negative Supply	0V
5	D	I	Input Signal	
6	B0	I	Configuration Bit	Tertiary Levels
7	B1	I	Configuration Bit	Tertiary Levels
8	V_{DD}	P	Positive Supply	2.375V - 3.6V



SON8



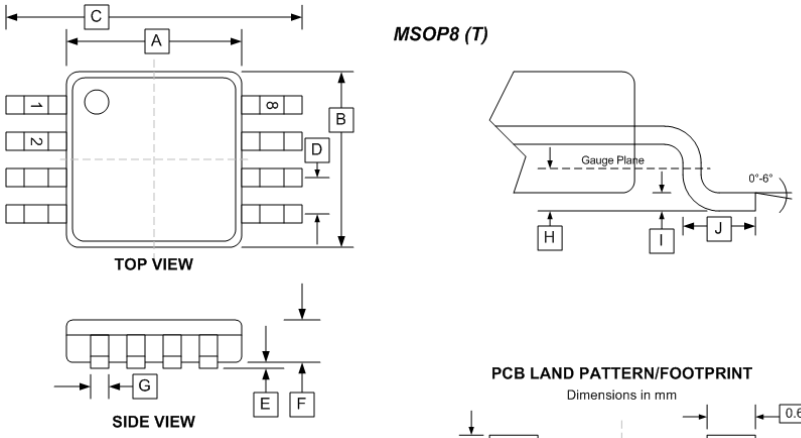
MSOP8

PART ORDERING INFORMATION

Part Number	Package	Marking
CTSLV315QG	SON8	RYW
CTSLV315TG	MSOP8	BE5G / YYWW

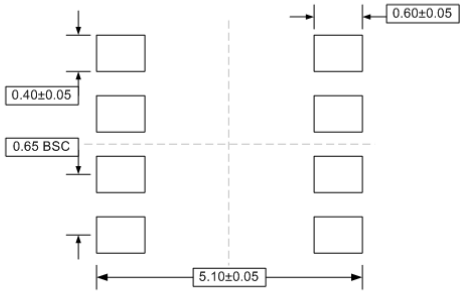
PACKAGE DIMENSIONS

MSOP8 (T)

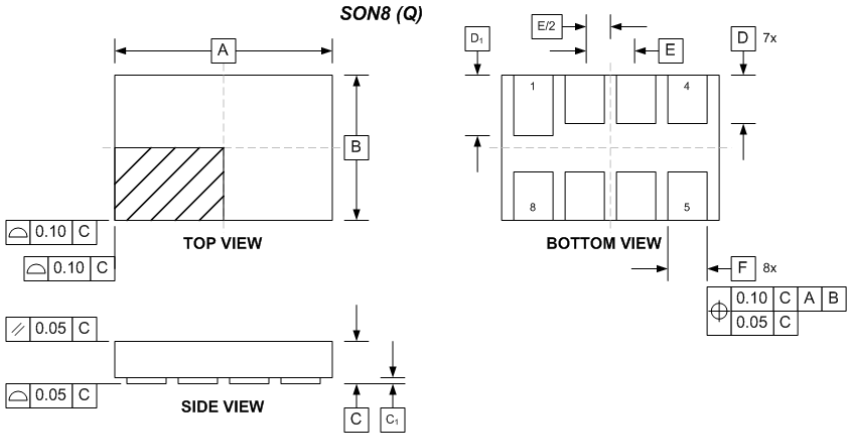


DIM	INCHES MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

PCB LAND PATTERN/FOOTPRINT
Dimensions in mm



SON8 (Q)



DIM	MILLIMETERS MIN	MAX
A	1.50 BSC	
B	1.00 BSC	
C	---	0.40
C_1	0.00	0.05
D	0.25	0.35
D_1	0.30	0.40
E	0.35 BSC	
F	0.15	0.25

PCB LAND PATTERN/FOOTPRINT