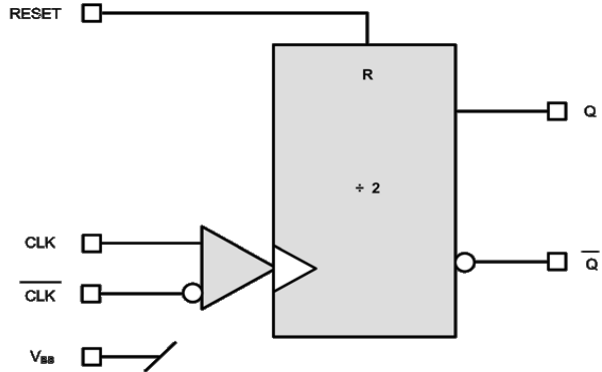


FEATURES

- 3.0+ GHz Toggle Frequency
- 470ps Propagation Delay
- Internal Input Pull-down Resistors
- 3.0V to 5.5V Power Supply
- RoHS Compliant Pb Free Packages

BLOCK DIAGRAM



DESCRIPTION

The CTS100LVEL32 is an integrated ÷2 divider. The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random logic state; the reset allows for the synchronization of multiple CTS100LVEL32's in a system.

The CTS100LVEL32 is a direct replacement for the On Semiconductor MC100EL/LVEL32.

ENGINEERING NOTES

The CTS100LVEL32 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/ \overline{CLK} differential input pair. The input signal is then fed to the other CLK/ \overline{CLK} input. The V_{BB} pin should be used only as a bias for the CTS100LVEL32 as its sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μ F capacitor.

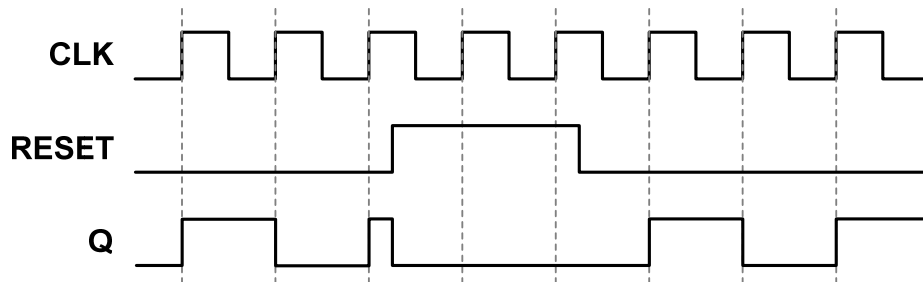


Figure 1 - Timing Diagram

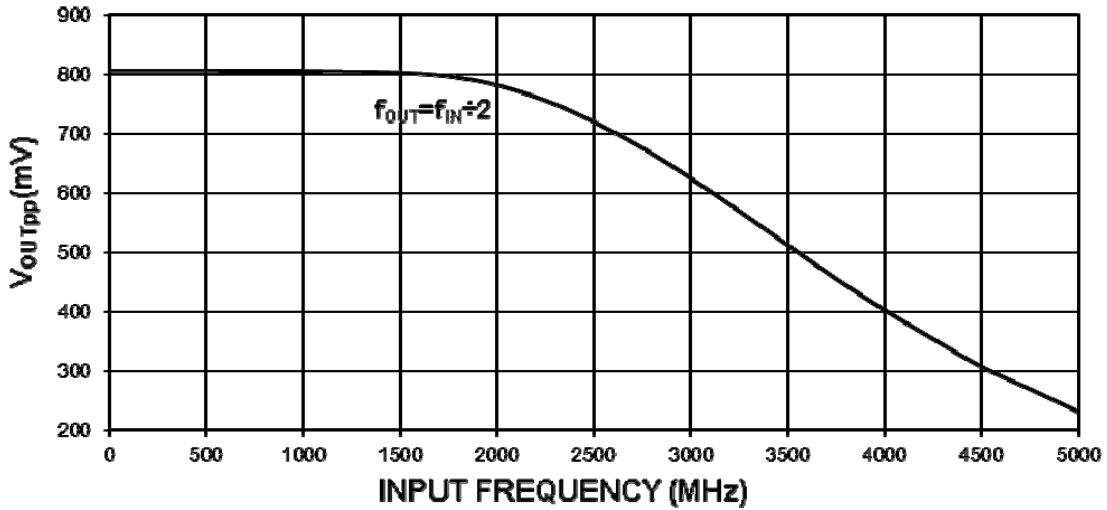


Figure 2 - Typical Large Signal Output Swing
Measured with 750mV input, output terminated to $V_{CC}-2V$ via 50Ω resistors.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	$V_{EE} = 0V$	0 to + 6.0	V
V_{I_PECL}	PECL Input Voltage	$V_{EE} = 0V$	0 to + 6.0	V
V_{EE}	ECL Power Supply	$V_{CC} = 0V$	-6.0 to 0	V
V_{I_ECL}	ECL Input Supply	$V_{CC} = 0V$	-6.0 to 0	V
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range	-	-40 to +85	$^{\circ}C$
T_{STG}	Storage Temperature Range	-	-65 to +150	$^{\circ}C$
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

ECL DC Characteristics (VEE = -3.0V to -5.5V, VCC = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ¹	-1085	-880	-1025	-880	-1025	-880	-1025	-880	mV
V _{OL}	Output LOW Voltage ¹	-1830	-1555	-1810	-1620	-1810	-1620	-1810	-1620	mV
V _{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	-1165	-880	mV
V _{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475	-1810	-1475	mV
V _{BB}	Reference Voltage	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV
I _{IH}	Input HIGH Current		150		150		150		150	μA
I _{IL}	Input LOW Current CLK	-150		-150		-150		-150		μA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I _{EE}	Power Supply Current		30		30		30		35	mA

¹ Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

LVPECL DC Characteristics (VEE = GND, VCC = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2215	2420	2275	2420	2275	2420	2275	2420	mV
V _{OL}	Output LOW Voltage ^{1,2}	1470	1745	1490	1680	1490	1680	1490	1680	mV
V _{IH}	Input HIGH Voltage ¹	2135	2420	2135	2420	2135	2420	2135	2420	mV
V _{IL}	Input LOW Voltage ¹	1490	1825	1490	1825	1490	1825	1490	1825	mV
V _{BB}	Reference Voltage ¹	1920	2040	1920	2040	1920	2040	1920	2040	mV
I _{IH}	Input HIGH Current		150		150		150		150	μA
I _{IL}	Input LOW Current CLK	-150		-150		-150		-150		μA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I _{EE}	Power Supply Current		30		30		30		35	mA

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

² Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

PECL DC Characteristics (VEE = GND, VCC = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3915	4120	3975	4120	3975	4120	3975	4120	mV
V _{OL}	Output LOW Voltage ^{1,2}	3170	3445	3190	3380	3190	3380	3190	3380	mV
V _{IH}	Input HIGH Voltage ¹	3835	4120	3835	4120	3835	4120	3835	4120	mV
V _{IL}	Input LOW Voltage ¹	3190	3525	3190	3525	3190	3525	3190	3525	mV
V _{BB}	Reference Voltage ¹	3620	3740	3620	3740	3620	3740	3620	3740	mV
I _{IH}	Input HIGH Current		150		150		150		150	μA
I _{IL}	Input LOW Current CLK	-150		-150		-150		-150		μA
	Input LOW Current RESET	0.5		0.5		0.5		0.5		
I _{EE}	Power Supply Current		30		30		30		35	mA

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

² Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

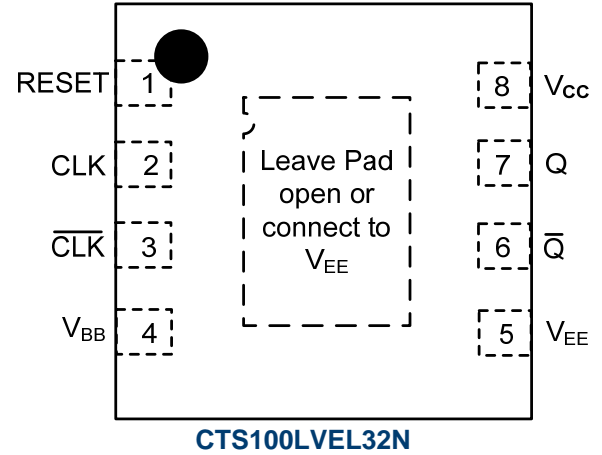
AC Characteristics (VEE = -3.0V to -5.5V; VCC=GND or VEE=GND; VCC = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Toggle Frequency	2.6			2.6			2.6			2.6			GHz
t _{PLH} /t _{PHL}	CLK to Q̄	360	450	540	370	460	550	380	470	560	400	490	580	ps
	RESET to Q̄	390	540	690	440	540	640	440	540	640	450	550	650	ps
t _{SKREW}	Duty Cycle Skew		5	20		5	20		5	20		5	20	ps
V _{PP} (AC)	Input Swing													
	Differential	150		1000	150		1000	150		1000	150		1000	mV
	Single Ended	300		2000	300		2000	300		2000	300		2000	mV
V _{CMR}	Common Mode Range	V _{EE+}		V _{CC-}	V _{EE+}		V _{CC-}	V _{EE+}		V _{CC-}	V _{EE+}		V _{CC-}	
	V _{PP} < 500mV	1.2		0.4	1.1		0.4	1.1		0.4	1.1		0.4	V
	V _{PP} ≥ 500mV	1.4		0.4	1.3		0.4	1.3		0.4	1.3		0.4	V
t _R /t _F	Output Rise/Fall (20%-80%)	100		260	100		260	100		260	100		260	ps

Pin Description and Configuration

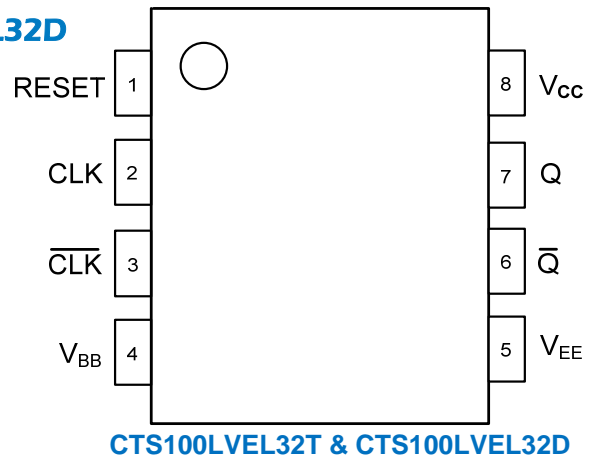
Pin Assignments for CTS100LVEL32N

Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{\text{CLK}}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	\overline{Q}	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply

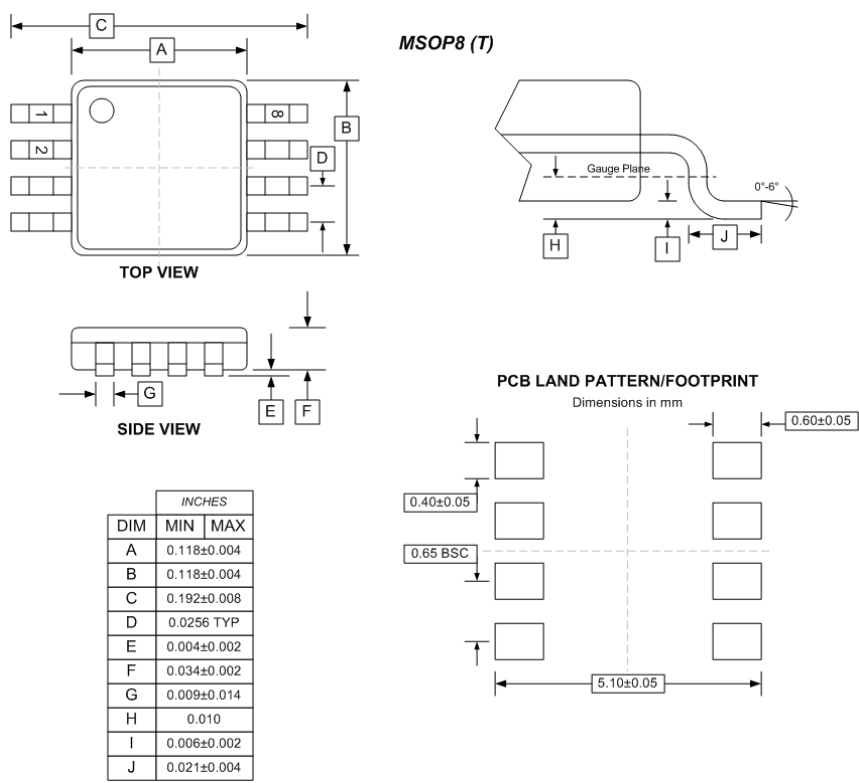
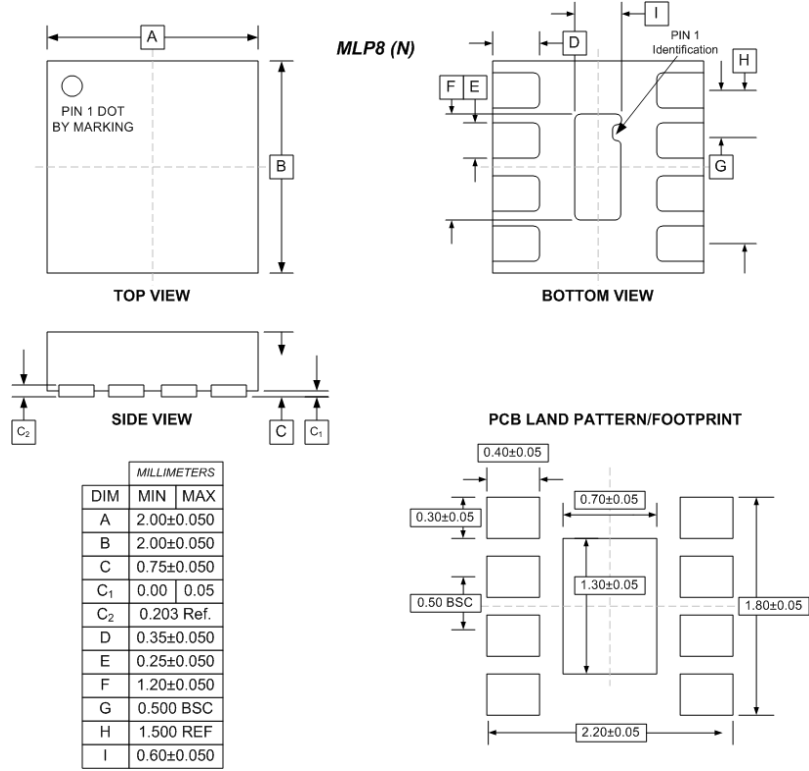


Pin Assignments for CTS100LVEL32T & CTS100LVEL32D

Pin	Name	Type	Function
1	RESET	Input	Asynchronous Reset
2	CLK	Input	Clock Input
3	$\overline{\text{CLK}}$	Input	Inverting Clock Input
4	V_{BB}	Output	Reference Voltage
5	V_{EE}	Power	Negative Supply
6	\overline{Q}	Output	Inverting PECL Output
7	Q	Output	PECL Output
8	V_{CC}	Power	Positive Supply



PACKAGE DIMENSIONS

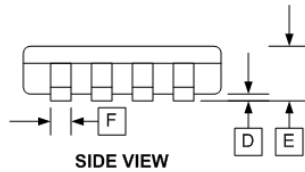
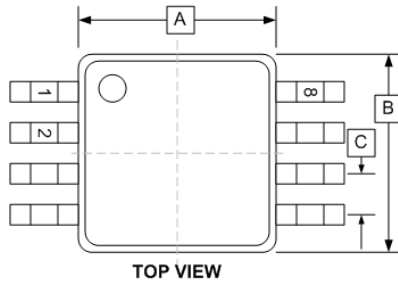


CTS100LVEL32

LVPECL Divide by 2 Divider
MLP8, MSOP8, SOIC8

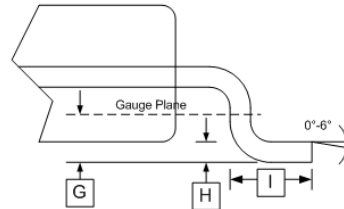
Not recommended for new designs

PACKAGE DIMENSIONS

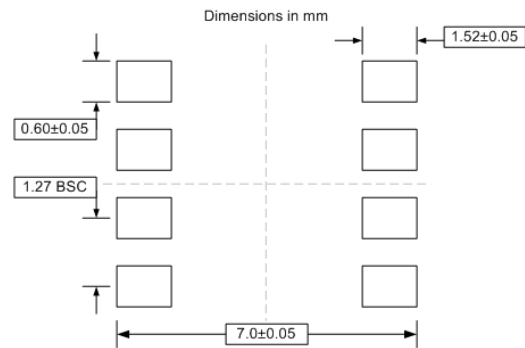


DIM	mm	
	MIN	MAX
A	3.81	3.99
B	4.80	4.98
C	1.27 BSC	
D	0.10	0.25
E	1.37	1.68
F	0.36	0.48
G	0.25	
H	0.19	0.25
I	0.41	0.86

SOIC8 (D)



PCB LAND PATTERN/FOOTPRINT



PART ORDERING INFORMATION

Part Number	Package	Marking
CTS100LVEL32NG	MLP8	C2G / YWW
CTS100LVEL32TG	MSOP8	HL32G / YYWW
CTS100LVEL32DG	SOIC8	CTS100G / LVEL32 / YYWW