WM9082

PDM Input Mono 3W Class D Speaker Driver

DESCRIPTION

The WM9082 is a high-performance sigma-delta Class D speaker driver. Audio input is supported using a stereo PDM interface; clock and control-code detection circuitry supports all of the audio and control functions via a 2-wire interface.

The digital audio interface provides excellent noise immunity, eliminating traditional input-filtering components. The flexible 2-wire interface minimises the PCB footprint and simplifies software development.

The combined audio and control interface configuration is ideal for enabling the WM9082 to be located close to the speaker; this reduces the length of the output connections, giving good EMC performance and removing the need for output filter components.

The sigma-delta architecture provides good power efficiency and improved EMI performance with respect to traditional PWM Class D designs.

A first-order high-pass filter can be selected on the input signal to remove DC offsets and help to prevent speaker damage. Other features include a low-power mute state, and output slew-rate control.

Short-circuit and thermal protection is provided.

The WM9082 is supplied in a 9-ball 1.56 x 1.46mm CSP package, with 0.5mm ball pitch.

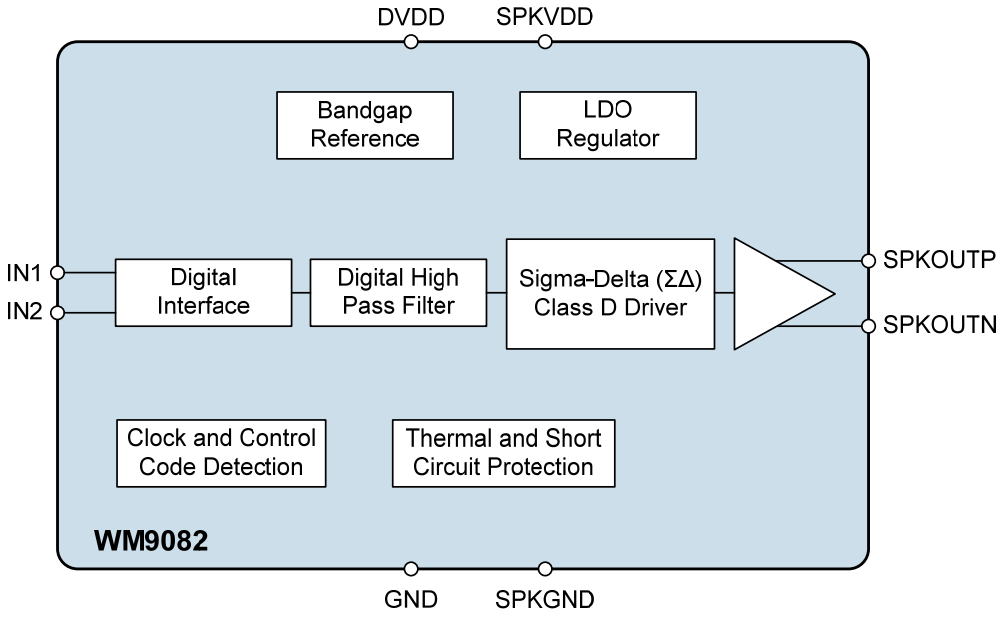
FEATURES

- Sigma-Delta Class-D speaker driver
  - 92dB SNR - 'A' weighted
  - 2.5W into 4Ω (5V supply, 1% THD)
  - 1.3W into 4Ω (3.6V supply, 1% THD)
  - 1.25W into 8Ω (5V supply, 1% THD)
  - 650mW into 8Ω (3.6V supply, 1% THD
- Stereo PDM digital audio input
- Supports 32kHz, 44.1kHz, 48kHz sample rates (128fs input)
- Automatic Left/Right channel selection
- First-order high pass filter (HPF)
- RF noise suppression
- Pop and click suppression
- Programmable output slew rates for low EMI
- Short-circuit and thermal protection
- 9-ball CSP package

APPLICATIONS

- Mobile Handsets
- Portable Media Players (PMP)
- Notebooks / Laptop computers
- LCD televisions

BLOCK DIAGRAM



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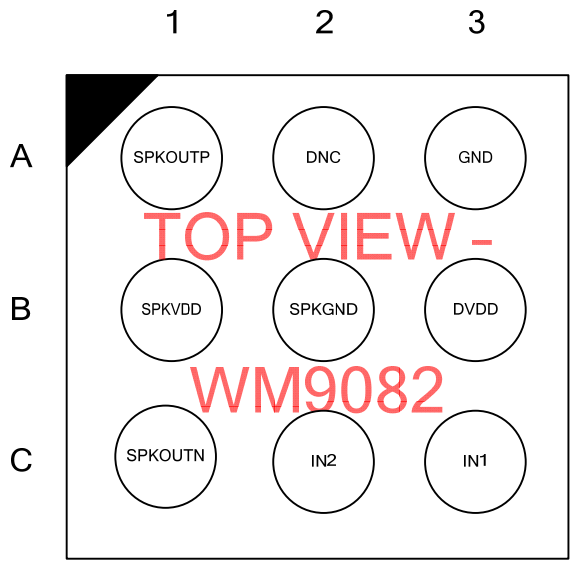
PIN CONFIGURATION

The WM9082 is supplied in a 9-ball CSP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9082ECSN/R	-40°C to +85°C	9-ball CSP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 5,000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKOUTP	Analogue Output	Positive BTL speaker output
A2	DNC		Do not connect
A3	GND	Supply	Ground
B1	SPKVDD	Supply	Class D output driver supply
B2	SPKGND	Supply	Ground
B3	DVDD	Supply	Digital supply
C1	SPKOUTN	Analogue Output	Negative BTL speaker output
C2	IN2	Digital Input	PDM input (CLK or Left DATA input)
C3	IN1	Digital Input	PDM input (CLK or Right DATA input)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Class D output driver supply voltage (SPKVDD)	-0.3V	7.0V
Digital supply voltage (DVDD)	-0.3V	2.5V
Voltage range digital inputs	GND - 0.3V	DVDD +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Class D output driver supply	SPKVDD	3.2	3.6	5.5	V
Digital supply	DVDD	1.35	1.8	2.0	V
Ground	SPKGND, GND		0		V

Note:

1. All digital and analogue grounds must always be within 0.3V of each other.

ELECTRICAL CHARACTERISTICS

Test Conditions

SPKVDD = 3.6V, DVDD = 1.8V, SPKGND=GND = 0V, T_A = +25°C, Load = 4Ω+33µH,
1kHz signal, CLK=6.144MHz (128fs), fs=48kHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Driver						
Signal to Noise ratio	SNR	A-weighted		92		dB
Idle channel noise		A-weighted		66		μV_{RMS}
Total Harmonic Distortion + Noise	THD+N	P_O = 625mW		-70		dB
Output Power (THD+N = 1%)	P_O	R_L = 4Ω, SPKVDD = 3.6V		1.3		W
		R_L = 4Ω, SPKVDD = 5.0V		2.5		
		R_L = 8Ω, SPKVDD = 3.6V		0.65		
		R_L = 8Ω, SPKVDD = 5.0V		1.25		
Speaker Load resistance (see note 1)			3			Ω
Speaker Load capacitance (see note 1)		Direct connection to SPKOUTP+SPKOUTN			200	pF
PSRR (SPKVDD)	PSRR	200mV (peak-peak) 217Hz Idle digital audio input while in the ON state		70		dB
Power efficiency		R_L = 4Ω, P_O = 625mW, SPKVDD = 3.6V		82		%
		R_L = 8Ω, P_O = 625mW, SPKVDD = 3.6V		86		
Clocking (IN1 or IN2)						
CLK input		fs = 48kHz		6.144		MHz
		fs = 44.1kHz		5.6448		
		fs = 32kHz		4.096		
Digital Input (IN1 or IN2)						
Input high level (see note 1)			0.7 x DVDD			V
Input low level (see note 1)					0.3 x DVDD	V
Input capacitance (see note 1)					10	pF
Input leakage			-0.9		0.9	µA
Other Parameters						
Pop-free start-up time		'OFF' state to 'ON' state (see Figure 3)		1		ms
Shutdown time		'ON' state to 'OFF' state (see Figure 3)		1		ms

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Consumption						
Quiescent current	I_{DVDD}			0.6		mA
(WM9082 in the 'ON' state; CLK enabled; DATA input is idle channel data.)	I_{SPKVDD}	$R_L = 4\Omega$		8		mA
		$R_L = 8\Omega$		8		
Standby current	I_{DVDD}			250		µA
(WM9082 in the 'STANDBY' state; CLK enabled; DATA input is repeated Control Code.)	I_{SPKVDD}			200		µA
Shutdown current	I_{DVDD}			0.6		µA
(WM9082 in the OFF state; CLK and DATA inputs disabled.)	I_{SPKVDD}			0.05		µA

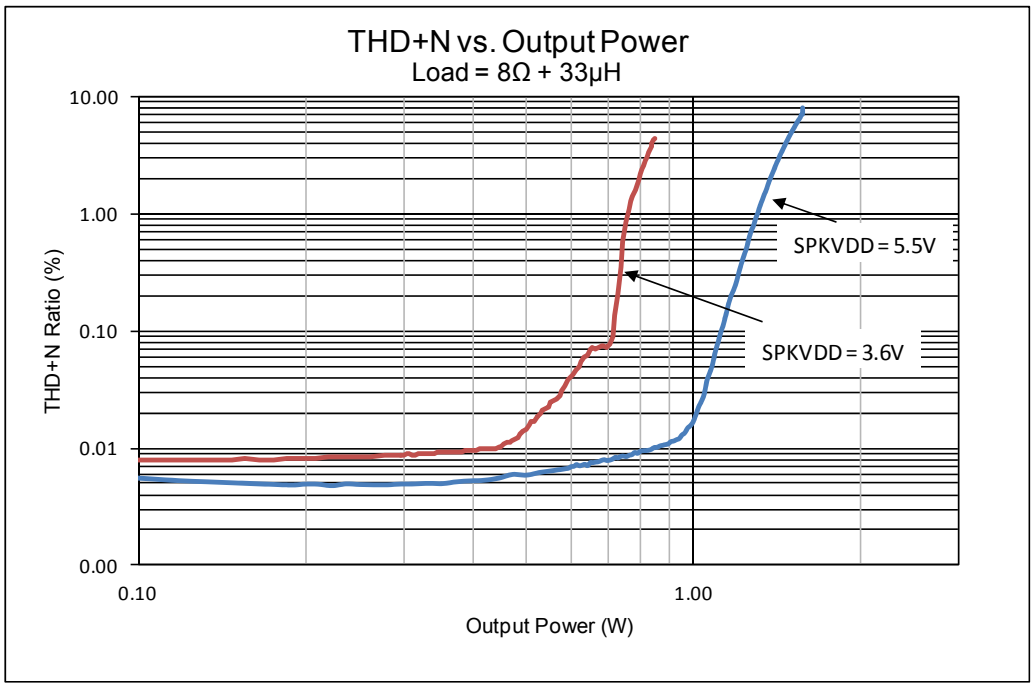
Note 1: Guaranteed by design; not production-tested.

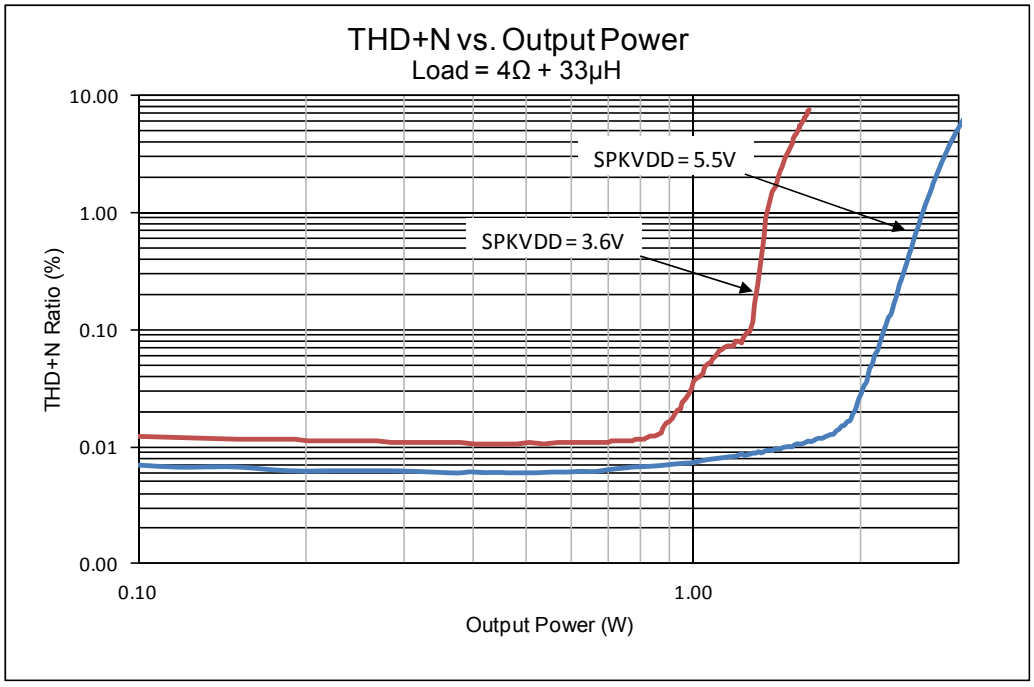
TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the sum of the harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the sum of the harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
5. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

TYPICAL PERFORMANCE

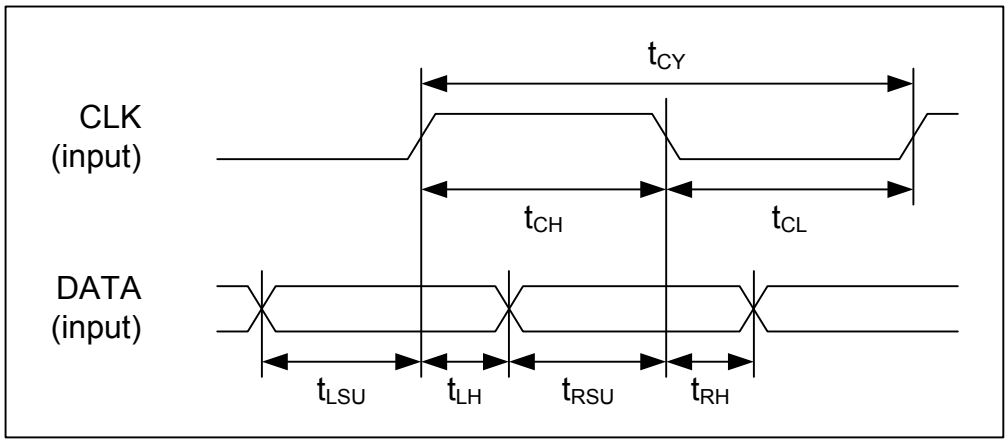
Typical speaker driver THD+N performance is shown below for 8Ω and 4Ω load conditions. Plots are shown for typical SPKVDD supply voltage conditions. (DVDD=1.8V in all cases.)





SIGNAL TIMING REQUIREMENTS

PDM AUDIO INTERFACE TIMING



Test Conditions

SPKVDD=3.6V, DVDD=1.8V, SPKGND=GND=0V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
CLK cycle time	t_{CY}	140	162	250	ns
CLK pulse width high	t_{CH}	60	81		ns
CLK pulse width low	t_{CL}	60	81		ns
DATA set-up time to CLK rising edge (Left channel data)	t_{LSU}	10			ns
DATA hold time from CLK rising edge (Left channel data)	t_{LH}	7			ns
DATA set-up time to CLK falling edge (Right channel data)	t_{RSU}	10			ns
DATA hold time from CLK falling edge (Right channel data)	t_{RH}	7			ns

DEVICE DESCRIPTION

INTRODUCTION

The WM9082 is a high performance sigma-delta Class D speaker driver designed for a range of high performance, low-power audio applications. It is packaged in a 9-ball CSP.

The device comprises two digital input pins, which support the CLK and DATA inputs of the PDM audio interface. Automatic Left/Right channel selection is provided using automatic detection of the input configuration. The PDM audio interface also supports decoding of silent Control Codes which can be used to configure the WM9082 or to select the low power, Standby operating state.

The WM9082 incorporates a selectable first-order high-pass filter for removing DC offsets and to help prevent speaker damage. Input sample rates of 32kHz, 44.1kHz and 48kHz are supported.

The sigma-delta architecture of the Class D output driver provides good power efficiency and improved EMI performance with respect to traditional PWM Class D designs.

The Class D speaker driver is powered from SPKVDD in the range 3.2V to 5.5V. The driver can deliver 2.5W output into a 4Ω load. The WM9082 is suitable for positioning very close to the external loudspeaker. The differential (BTL) outputs can connect directly to the loudspeaker with no other external components required.

Short-circuit and thermal protection is also provided.

The WM9082 is supplied in a 9-ball 1.56 x 1.46mm CSP package, with 0.5mm ball pitch.

PDM AUDIO INTERFACE

The WM9082 supports a stereo PDM audio interface, comprising a CLK wire and a DATA wire. Two channels of audio data are multiplexed on the DATA wire; the WM9082 speaker driver selects either the Left channel data or the Right channel data depending on the hardware configuration of the interface connection.

Each channel of PDM audio data consists of a stream of 1-bit data samples; the bit rate is 128 x fs, where fs is the sample frequency of the received audio signal. Note that PDM is a 'pulse density modulation' coding, where the signal amplitude is represented by the density of logic 1's in any window of consecutive data bits.

Two audio channels are interleaved on the PDM interface as illustrated in Figure 1. The Left channel data is read at the rising edge of CLK; the Right channel data is read at the falling edge of CLK. See "Signal Timing Requirements" for specific timing requirements.

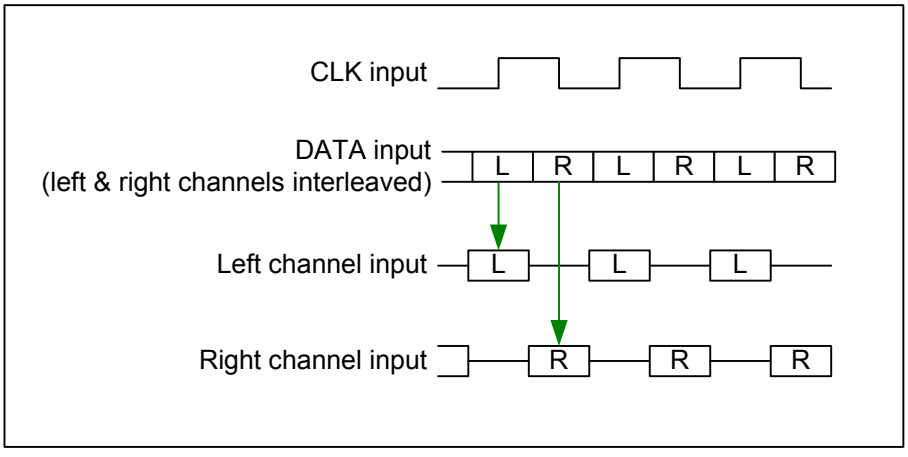


Figure 1 PDM Audio Interface

The channel selection for the WM9082 speaker driver is implemented automatically by sensing which of the inputs pins is CLK and which pin is DATA, as defined in Table 1.

To ensure correct channel selection, it must be ensured that the DATA input is disabled whenever the CLK input is disabled. If the DATA input signal is present when CLK is disabled, this may result in incorrect channel selection.

INPUT CONFIGURATION		SPEAKER CHANNEL
CLK = IN1	DATA = IN2	Left
CLK = IN2	DATA = IN1	Right

Table 1 PDM Channel Selection

If stereo operation is required, using two WM9082 speaker drivers, then this can be implemented very easily, by cross-connecting the CLK and DATA wires on the two speaker drivers, as illustrated in Figure 2.

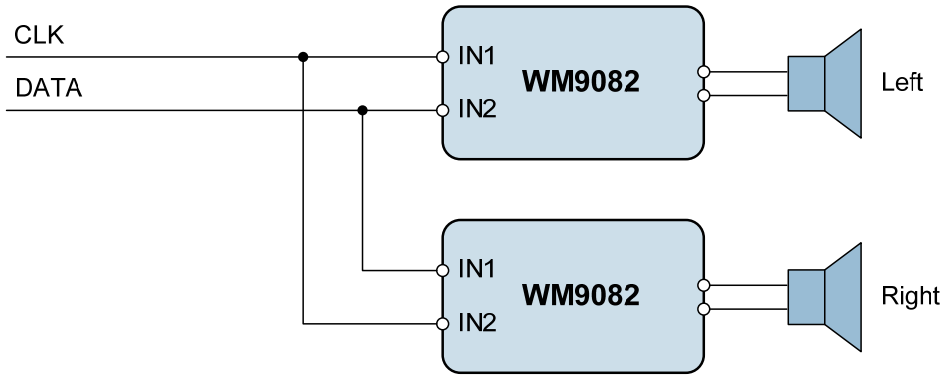


Figure 2 Stereo PDM Operation

The channel detection is determined automatically at device start-up, and also after any period when the CLK input has stopped.

DEVICE CONTROL CODES

When power supplies are present (see “Recommended Operating Conditions”), and audio data is input at the audio interface, the WM9082 powers up and the Class D speaker driver is enabled. The WM9082 selects either the Left or Right channel data as described in “PDM Audio Interface”.

The WM9082 can be controlled using specific data sequences, known as Control Codes, received over the PDM audio interface. Each Control Code is a “zero” code when decoded as audio data. Therefore, the Control Codes can be transmitted to the WM9082 in the form of silent audio data, but the codes will be recognised by the WM9082 as control instructions.

The WM9082 Control Codes are defined in Table 2 and Table 3.

The Control Codes are 8-bit codes, which must be transmitted LSB first.

The Page 1 Control Codes (see Table 2) are valid when transmitted consecutively for the required number of times. The Page 2 Control Codes (see Table 3) are valid only when preceded by the “Page 2 access” instruction (ie. Page 1, Code 6).

In most cases, the Control Codes are only valid if they are received more than 32 times consecutively (see below for further details). For greatest reliability, however, it is recommended that the host device always transmits Control Codes at least 64 times whenever it is desired to send a control instruction to the WM9082.

If the WM9082 is configured to receive Left channel data, then it will only respond to Control Codes received on the Left channel of the PDM interface. Similarly, if the WM9082 is configured to receive Right channel data, then it will only respond to Control Codes received on the Right channel.

ID	FUNCTION	DESCRIPTION	CONTROL CODE
Code 1	Start Up (3.6V SPKVDD)	Fast Start-Up for default SPKVDD	AA
Code 2	Standby	Disable Class D output	66
Code 3	EMI control 1	Invert SR[1]	F0
Code 4	32kHz mode control	Select 32kHz sample rate mode	8B
Code 5	High Pass Filter control	Disable 2Hz High Pass Filter	39
Code 6	Page 2 access	Enable Page 2 Control Codes	56
Code 7	Reserved		D1
Code 8	Reserved		D2
Code 9	Start Up (3.6V SPKVDD)	Start-Up for SPKVDD = 3.6V	D4
Code 10	Start Up (5.0V SPKVDD)	Start-Up for SPKVDD = 5.0V	D8

Table 2 WM9082 Page 1 Control Codes

ID	FUNCTION	DESCRIPTION	CONTROL CODE
Code 1	Reserved		AA
Code 2	Reserved		66
Code 3	Performance control 1	Invert PC1[0]	F0
Code 4	Reserved		8B
Code 5	Reserved		39
Code 6	Reserved		56
Code 7	Reserved		D1
Code 8	Reserved		D2
Code 9	EMI control 2	Invert SR[0]	D4
Code 10	Performance control 2	Increment PC2[1:0]	D8

Table 3 WM9082 Page 2 Control Codes

The output driver slew-rate control is configurable using the SR[1] and SR[0] bits. These fields are defined in Table 4. The slew-rate Control Code sequences are described in Table 6.

SR[1]	SR[0]	OUTPUT SLEW RATE (OUTPUT RISE / FALL TIME)
0	0	5ns (Default)
0	1	10ns
1	0	20ns
1	1	40ns

Table 4 Output Slew Rate Control bits

The output driver operating mode is configurable using the PC1[0] and PC2[1:0] bits. These fields are defined in Table 5. Selected operating mode Control Code sequences are described in Table 6.

PC1[0]	PC2[1:0]	DESCRIPTION		
1	00	Best PSRR		
1	01	↑	↓	(default)
1	10	↑	↓	
1	11	↑	↓	
0	XX		Best SNR	

Table 5 Operating Mode Control bits

As noted above, the WM9082 Control Codes are only valid when they are transmitted consecutively for the required number of times. The valid Control Codes can be used to control the operating state of the WM9082 and also to select different operating modes.

The “Page 2 access” Control Code enables the Page 2 Control Codes for the next control code only; the Page 1 codes will apply again for any subsequent control code(s).

The state transitions and operating modes are described below.

INITIAL POWER-UP

When a valid CLK signal is first detected on IN1 or IN2, the WM9082 powers up to the “STANDBY” state. The WM9082 will remain in this state until a “Start-up Event” is detected, or until the CLK signal is removed.

CONFIGURATION EVENTS

In the STANDBY state, the WM9082 can be configured (if required) using the Control Code sequences listed in Table 6.

Note that these Control Code sequences are only valid when the WM9082 is in the STANDBY state; it is not possible to configure the device whilst simultaneously sending audio data.

The following features are configurable in the STANDBY state:

- Sample rate (33kHz, 44.1kHz or 48kHz)
- Input path High Pass Filter (HPF)
- Output slew rate control
- Operating Mode (PSRR vs SNR control)

The cut-off frequency of the input path HPF, when enabled, is around 2Hz, assuming a 48kHz audio sample rate (CLK = 6.144MHz).

The operating mode selections provide different options for SNR vs PSRR optimisation.

The Control Code sequences are listed in Table 6.

DESCRIPTION	CONTROL CODE
Select 32kHz sample rate	32 x Code 4
Disable the input path HPF	32 x Code 5
Select 10ns output slew rate	32 x Code 6 32 x Code 9
Select 20ns output slew rate	32 x Code 3
Select 40ns output slew rate	32 x Code 3 32 x Code 6 32 x Code 9
Select 'Best PSRR' mode	32 x Code 6 32 x Code 10 32 x Code 6 32 x Code 10 32 x Code 6 32 x Code 10
Select 'Best SNR' mode	32 x Code 6 32 x Code 3

Table 6 WM9082 Configuration Events

If none of these Control Code sequences is received, then the WM9082 is configured for the following default operating conditions:

- Sample rate is 44.1kHz or 48kHz
- Input path High Pass Filter (HPF) enabled
- Output slew rate is 10ns
- Default PSRR and SNR (see "Electrical Characteristics")

Note that the default operating conditions are only restored on power-up or following a period when the CLK input is stopped.

START-UP EVENTS

The WM9082 Class D output is enabled whenever PDM audio data is detected at the input pins, or when a valid Start-Up Control Code is detected. The WM9082 Start-Up is selected under any of the conditions described in Table 7. Each of these conditions results in a transition to the "ON" state.

Note that, if SPKVDD > 4.3V, then it is recommended to start up the WM9082 using Code 10; this ensures that the device is optimally configured for the higher SPKVDD level.

Note that, when the start-up transition occurs as a result of PDM audio data, then the WM9082 will be enabled in whichever mode had previously been selected (if any). In the case where the "ON" state has not previously been selected, then the default (SPKVDD = 3.6V) mode is chosen.

CONDITION	DESCRIPTION
4 x Code 1	Fast start-up for default SPKVDD condition (SPKVDD = 3.6V)
32 x Code 9	Start-up for SPKVDD = 3.6V
32 x Code 10	Start-up for SPKVDD = 5.0V
PDM audio data	Fast start-up

Table 7 WM9082 Start-Up Events

STANDBY EVENTS

The WM9082 Class D output is disabled whenever the PDM input data is interrupted, or when a valid Standby Control Code is detected. The WM9082 Standby transition is selected during normal operation (ie. from the "ON" state") under any of the conditions described in Table 8. Each of these conditions results in a transition to the "STANDBY" state.

CONDITION	DESCRIPTION
32 x Code 2	Standby command - selects STANDBY state
64 x Any Control Code	Selects STANDBY state
Error condition	Selects STANDBY state (An error condition is detected if >24 consecutive 1's or >24 consecutive 0's is received on the PDM audio interface.)

Table 8 WM9082 Standby Events

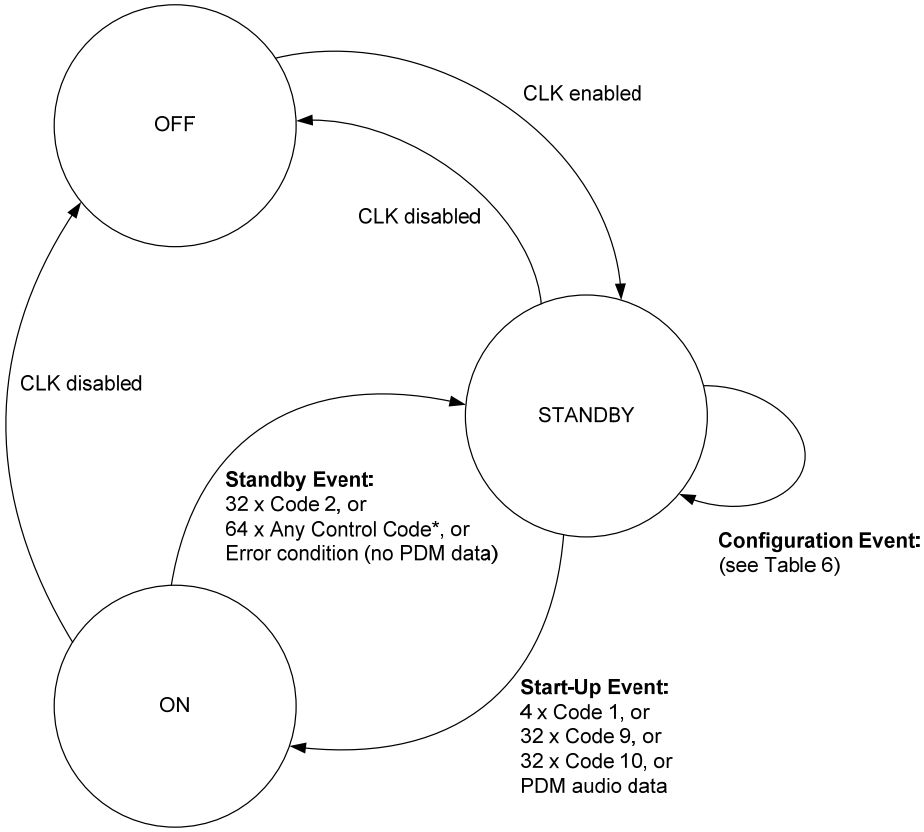
Note that repeated instances of any Control Code will not cause more than one state transition until audio data or a different Control Code has been received. This prevents the WM9082 from cycling between the "ON" state and the "STANDBY" state in the event of repeated Control Codes.

SHUTDOWN EVENTS

If the CLK input is not present at any time, this results in a transition to the "OFF" state. The WM9082 will remain in the "OFF" state until the CLK input restarts.

STATE TRANSITION DIAGRAM

The WM9082 operating states and transitions are illustrated in Figure 3.



* Note that repeated instances of any Control Code will not cause more than one state transition until audio data or a different Control Code has been received. This prevents the WM9082 from cycling between the "ON" state and the "STANDBY" state in the event of repeated Control Codes.

Figure 3 State Transition Diagram

SPEAKER DRIVER

The speaker outputs SPKOUTP and SPKOUTN operate in a BTL configuration. These pins provide a differential output for direct connection to the loudspeaker. In a typical application, no other external components are required for the loudspeaker connection.

The sigma-delta architecture of the Class D driver is more linear and power efficient than traditional PWM implementations, resulting in reduced power consumption and improved EMI characteristics.

The speaker driver is disabled during start-up and following receipt of selected Control Codes which can be used to configure the WM9082. The driver is automatically re-enabled on receipt of any audio data.

RESETS AND SHUTDOWN

A power on reset circuit ensures correct start-up and shut-down when the DVDD supply rail is enabled or disabled.

The WM9082 is held in the “OFF” state when there is no CLK signal detected on the IN1 or IN2 pins; the Shutdown current in the “OFF” state is noted in the “Electrical Characteristics” section.

Short circuit and thermal protection is also provided. In the event of an output short-circuit or an over-temperature condition, the WM9082 will protect itself by disabling the Class D speaker driver. The WM9082 will automatically recover and continue normal operation when the fault condition is cleared.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behaviour in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower-frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM9082, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM9082 are listed below in Table 9.

POWER SUPPLY	DECOUPLING CAPACITOR
DVDD	0.1μF ceramic
SPKVDD	4.7μF ceramic

Table 9 Power Supply Decoupling Capacitors

All decoupling capacitors should be placed as close as possible to the WM9082 device.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

CLASS D SPEAKER CONNECTIONS

The WM9082 incorporates a Class D speaker driver, which offers high amplifier efficiency at large signal levels. As the Class D output is a sigma-delta modulated signal, the choice of speakers and tracking of signals is important for ensuring good performance and reducing EMI.

The efficiency of the speaker drivers is affected by the series resistance between the WM9082 and the speaker (e.g. PCB track loss and inductor ESR) as shown in Figure 4. This resistance should be as low as possible to maximise efficiency.

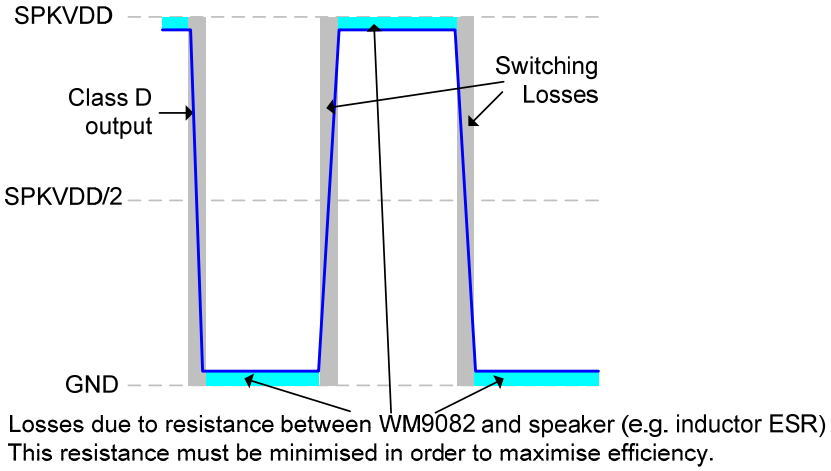


Figure 4 Speaker Connection Losses

The Class D output requires external filtering in order to recreate the audio signal. This may be implemented using a 2nd order LC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

A suitable LC filter implementation is illustrated in Figure 5.

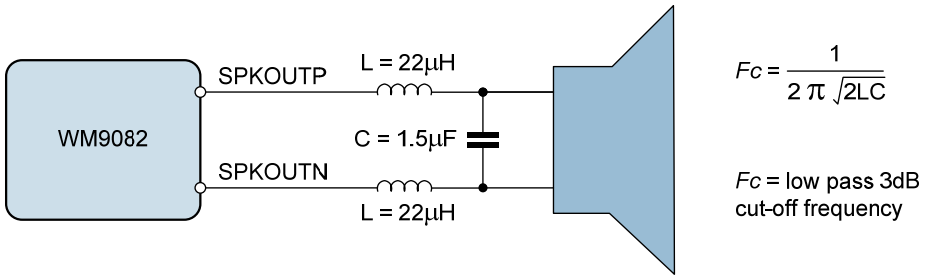


Figure 5 Class D Output Filter Components

A simple equivalent circuit of a loudspeaker consists of a serially connected resistor and inductor, as shown in Figure 6. This circuit provides a low pass filter for the speaker output. If the loudspeaker characteristics are suitable, then the loudspeaker itself can be used in place of the filter components described earlier. This is known as 'filterless' operation.

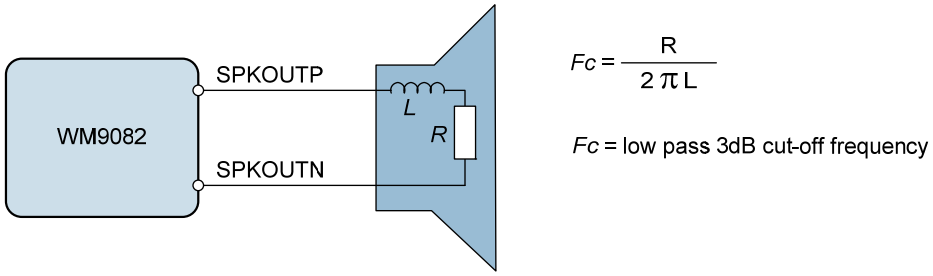


Figure 6 Speaker Equivalent Circuit for Filterless Operation

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8Ω and the desired cut-off frequency is 20kHz, then the optimum speaker inductance may be calculated as:

$$L = \frac{R}{2\pi Fc} = \frac{8\Omega}{2\pi * 20kHz} = 64\mu H$$

8Ω loudspeakers typically have an inductance in the range 20μH to 100μH, however, it should be noted that a loudspeaker inductance will not be constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency).

The Class D outputs of the WM9082 operate at much higher frequencies than is recommended for most speakers; care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high frequency energy of the Class D switching and, in so doing, to prevent speaker damage.

A simple test can be used to confirm if the loudspeaker is compatible with filterless operation. Under quiescent input conditions (idle digital audio input while in the ON state), the SPKVDD current is measured with the speaker disconnected, and measured again with the speaker connected. If the SPKVDD current increases by more than 10mA when the speaker is connected, then the speaker alone is not effective as a filter, and it is recommended to consider changing the speaker or adding LC filter components.

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 7 provides a summary of recommended external components for WM9082. Note that the actual requirements may differ according to the specific target application.

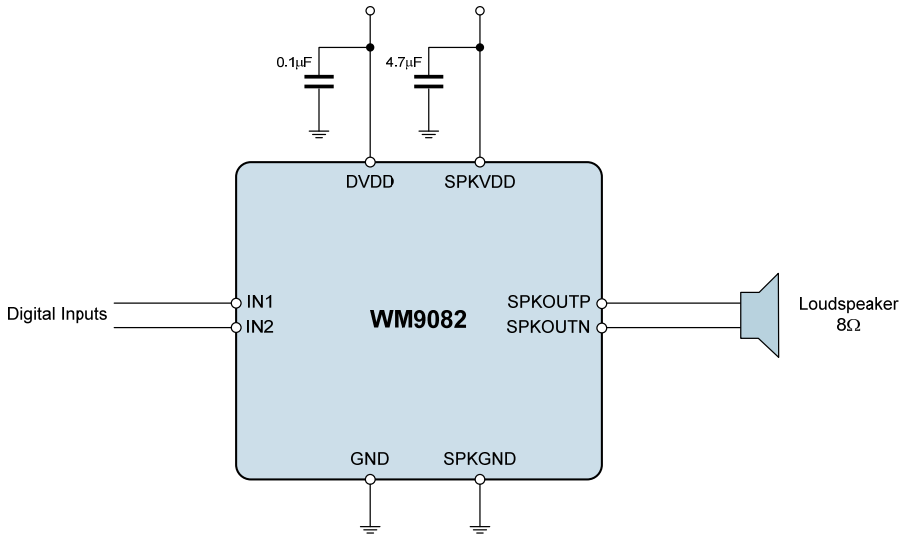


Figure 7 WM9082 Recommended External Components Diagram

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM9082 device as possible, with current loop areas kept as small as possible.

CLASS D LOUDSPEAKER CONNECTION

Long, exposed PCB tracks or connection wires will emit EMI. The distance between the WM9082 and the loudspeaker should therefore be kept as short as possible. Where speakers are connected to the PCB via a cable form, it is recommended that a shielded twisted pair cable is used. The shield should be connected to the main system, with care taken to ensure ground loops are avoided.

Further reduction in EMI can be achieved using PCB ground (or VDD) planes and also by using passive LC components to filter the Class D switching waveform. When passive filtering is used, low ESR components should be chosen in order to minimise the series resistance between the WM9082 and the speaker, maximising the power efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads can also be used. These should be positioned as close to the device as possible.

These techniques for EMI reduction are illustrated in Figure 8.

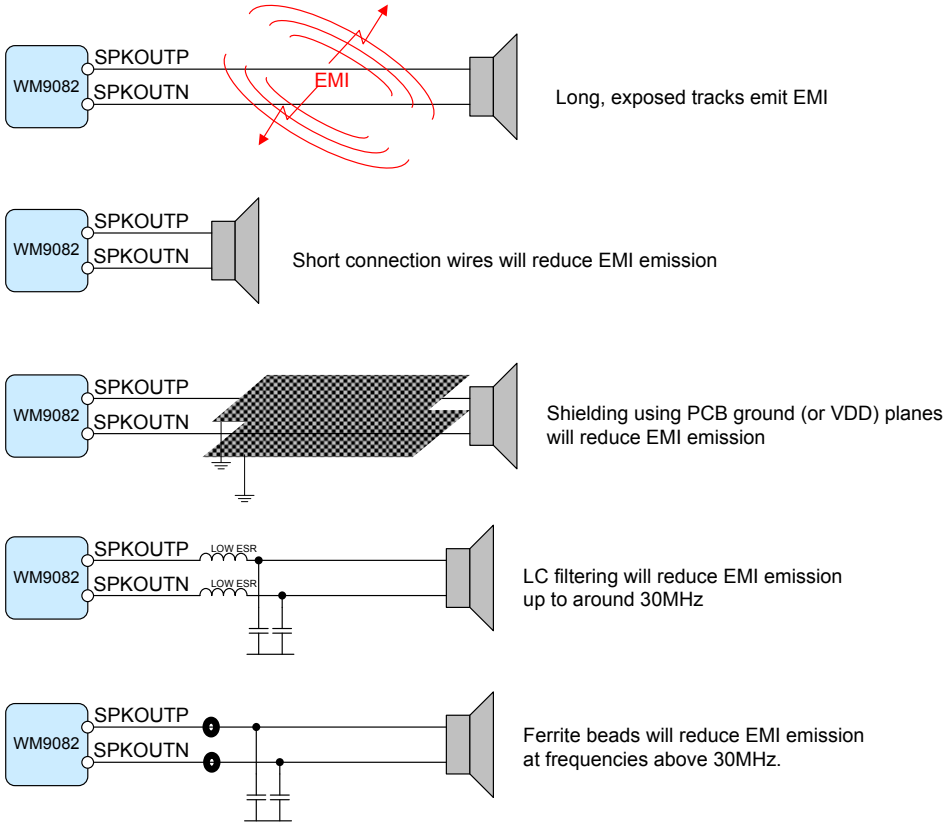
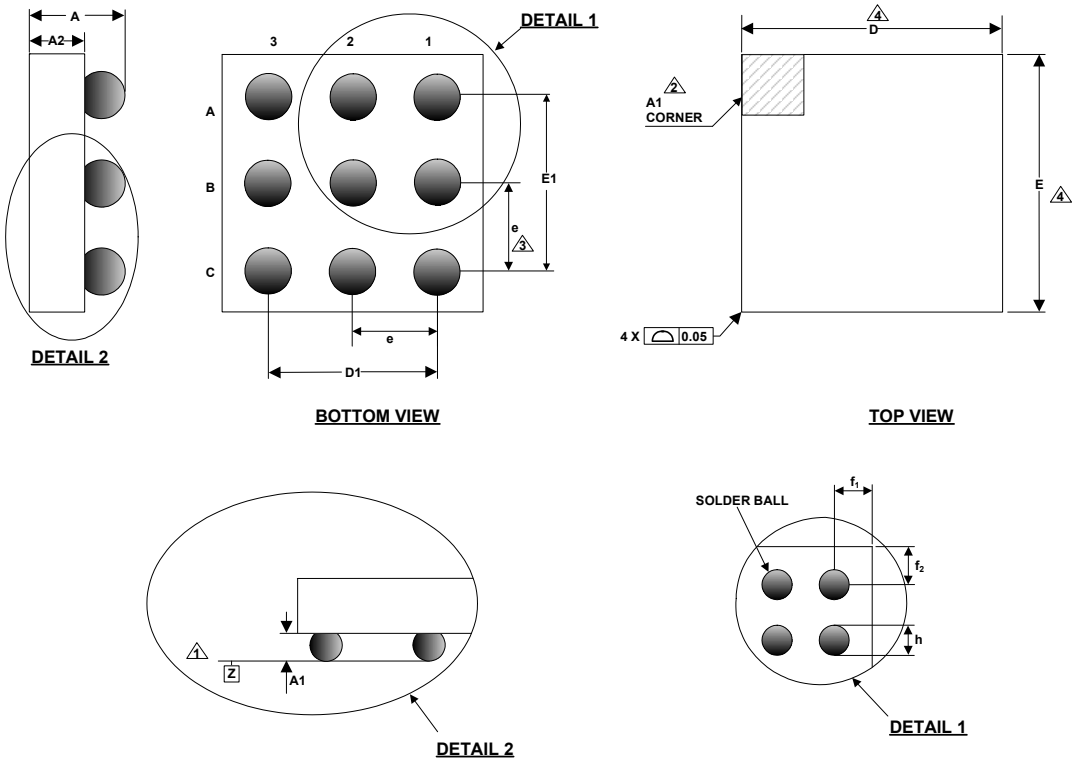


Figure 8 EMI Reduction Techniques

PACKAGE DIMENSIONS

PACKAGE DIAGRAM FOR DEVICES MARKED LT9

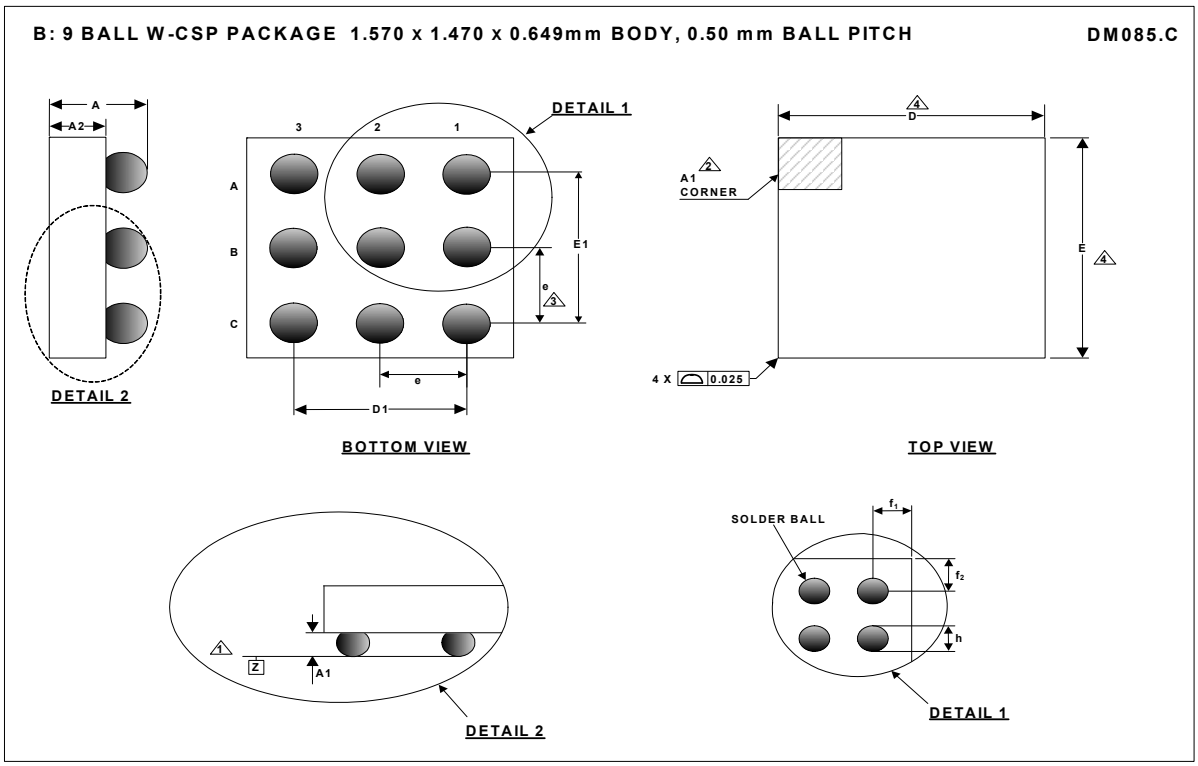
B: 9 BALL W-CSP PACKAGE 1.560 x 1.460 x 0.635mm BODY, 0.50 mm BALL PITCH **DM085.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.618	0.635	0.652	
A1	0.230	0.235	0.240	
A2	0.388	0.400	0.412	
D	1.550	1.560	1.570	
D1		1.000 BSC		
E	1.450	1.460	1.470	
E1		1.000 BSC		
e		0.500 BSC		3
f_1	0.275			
f_2	0.225			
h		0.320		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
3. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
4. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
5. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

PACKAGE DIAGRAM FOR DEVICES MARKED JC5



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.610	0.649	0.688	
A1	0.212	0.249	0.286	
A2	0.387	0.400	0.413	
D	1.545	1.570	1.595	
D1		1.000 BSC		
E	1.445	1.470	1.495	
E1		1.000 BSC		
e		0.500 BSC		3
f_1	0.273			
f_2	0.223			
h	0.261	0.311	0.361	

NOTES:
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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
05/07/10	1.0	First Release		
20/04/11	2.0	Product status updated to preliminary technical data		
21/04/11	2.0	Updated pinout changing VREFC to DNC. All associated diagrams and tables also updated to reflect the change	1, 4, 16, 18	WF
28/04/11	2.0	PSRR typical electrical characteristics values added	5	BM
03/05/11	2.0	In Description, removed 'The recommended configuration requires only 3 external capacitors'	1	WF
12/08/11	2.1/2.2	Electrical Characteristics updated. Additional Control Codes defined for slew rate control & performance mode. Updates to filterless speaker description & recommendations		PH
15/09/11	2.2	Electrical Characteristics updated Default slew rate / operating mode conditions updated		PH
25/10/11	3.0	Product status updated to pre-production		JMacD
18/05/12	4.0	Electrical Characteristics updated Typical performance graphs added		PH
10/08/12	4.1	Package Diagram DM085C added.		JMacD