CS3301

Low-noise, Programmable Gain, Differential Amplifier

Features

- Signal Bandwidth: DC to 2 kHz
- Selectable Gain: x1, x2, x4, x8, x16, x32, x64
- Differential Inputs, Differential Outputs
  - Multiplexed inputs: INA, INB, 800Ω termination
  - Rough / fine charge outputs for CS5371/72
  - Max signal amplitude: 5 V_{pp} differential
  - Low input bias: 500 pA
- Outstanding Noise Performance
  - 0.20 μV_{p-p} between 0.1 Hz and 10 Hz
  - 8.5 $nV/\sqrt{Hz}$ from 0.1 Hz to 2 kHz
- Low Total Harmonic Distortion
  - -118 dB THD typical (0.000126%)
  - -112 dB THD maximum (0.000251%)
- Low Power Consumption
  - Normal/LPWR/PWDN: 5.5 mA, 3.5 mA, 10 µA
- Single or Dual Power Supply Configurations
  - VA+ = +5 V; VA- = 0 V; VD = +3.3 V to +5 V
  - VA+ = +2.5 V;VA- = -2.5 V;VD = +3.3 V

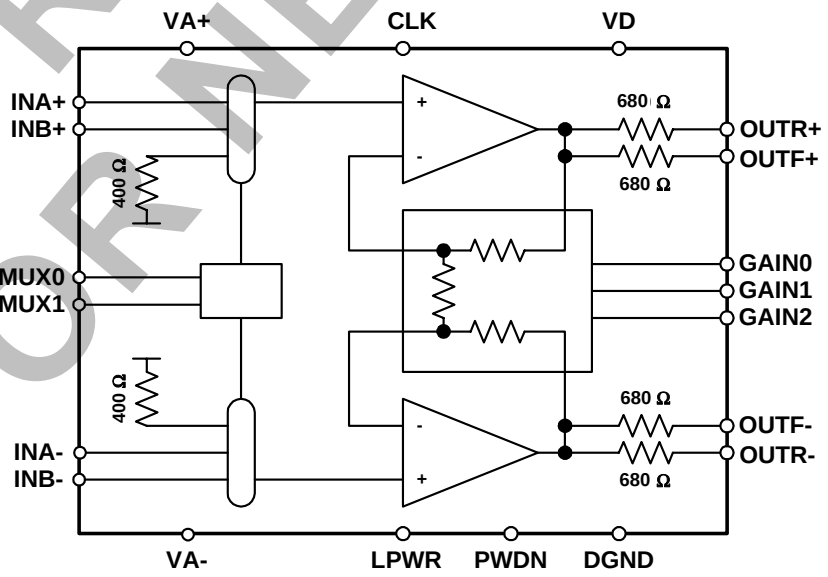
Description

The CS3301 is a low-noise differential input, differential output amplifier with programmable gain, optimized for amplifying signals from low-impedance sensors such as geophones. The gain settings are binary weighted (x1, x2, x4, x8, x16, x32, x64) and are selected using simple pin settings. Two sets of external inputs, INA and INB, simplify system design as inputs from a sensor and test DAC. An internal 800 Ω termination can also be selected for noise tests.

Amplifier noise performance is outstanding with a noise density of 8.5 $nV/\sqrt{Hz}$ over the 0.1 Hz to 2 kHz bandwidth. Distortion performance is also extremely good, typically -118 dB THD. Flat noise down to 0.1 Hz and low total harmonic distortion make this amplifier ideal for low-frequency, low-amplitude, differential signals requiring maximum dynamic range.

ORDERING INFORMATION

See page 15.



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REVISION HISTORY

Revision	Date	Changes
PP2	JUL 2003	Final preliminary release.
F1	AUG 2005	Updated legal notice. Added MSL data.
F2	SEP 2005	Updated anti-alias resistor values, relative gain accuracy, CS4373A part number.
F3	DEC 2007	Added watermark to indicate device is not recommended for new designs.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**

1. CHARACTERISTICS AND SPECIFICATIONS

- Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- DGND = 0 V, all voltages with respect to 0 V.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Unipolar Power Supplies						
Positive Analog		VA+	4.75	5.0	5.25	V
Negative Analog	(Note 1)	VA-	-0.25	0	0.25	V
Positive Digital	(Note 2)	VD	3.135	3.3	5.25	V
Bipolar Power Supplies						
Positive Analog		VA+	2.375	2.5	2.625	V
Negative Analog	(Note 1)	VA-	-2.625	-2.5	-2.375	V
Positive Digital	(Note 2)	VD	3.135	3.3	3.465	V
Thermal						
Ambient Operating Temperature	Industrial (-IS)	T_A	-40	-	85	°C

Notes: 1. VA- must be the most negative voltage to avoid potential SCR latch-up conditions.
2. VD must conform to Digital Supply Differential under Absolute Maximum Ratings.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Parameter
DC Power Supplies	Positive Analog Negative Analog Digital	VA+ VA- VD	-0.3 -6.8 -0.3	6.8 0.3 6.8	V V V
Analog Supply Differential	[(VA+) - (VA-)]	VA_{DIFF}	-	6.8	V
Digital Supply Differential	[(VD) - (VA-)]	VD_{DIFF}	-	6.8	V
Input Current, Any Pin Except Supplies	(Note 3)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 3)	I_{IN}	-	±50	mA
Output Current	(Note 3)	I_{OUT}	-	±25	mA
Power Dissipation		PDN	-	500	mW
Analog Input Voltages		V_{INA}	(VA-)-0.5	(VA+)+0.5	V
Digital Input Voltages		V_{IND}	-0.5	(VD)+0.5	V
Ambient Operating Temperature (Power Applied)		T_A	-40	85	ºC
Storage Temperature Range		T_{STG}	-65	150	ºC

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 3. Transient currents up to 100 mA will not cause SCR latch-up.

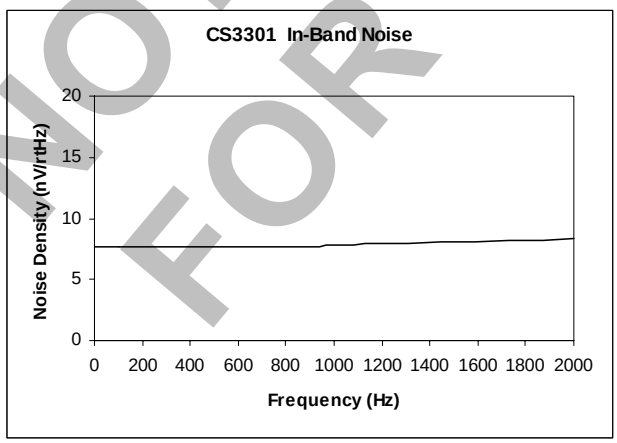
THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	ºC
Junction to Ambient Thermal Impedance	Θ_{JA}	-	65	-	ºC / W
Ambient Operating Temperature (Power Applied)	T_A	-40	-	+85	ºC

ANALOG CHARACTERISTICS

Parameter		Symbol	CS3301 Min	CS3301 Typ	CS3301 Max	Unit
Noise Performance, Normal						
Input Voltage Noise	f_0 = 0.1 Hz to 10 Hz	VN_{PP}	-	0.20	0.40	μV_{p-p}
Input Voltage Noise Density	f_0 = 0.1 Hz to 2 kHz	VN_D	-	8.5	12.0	$nV/\sqrt{Hz}$
Input Current Noise Density	(Note 4)	IN_D	-	200	-	$fA/\sqrt{Hz}$
Noise Performance, Low Power (LPWR=1)						
Input Voltage Noise	f_0 = 0.1 Hz to 10 Hz	VN_{PP}	-	0.25	0.50	μV_{p-p}
Input Voltage Noise Density	f_0 = 0.1 Hz to 2 kHz	VN_D	-	10.0	15.0	$nV/\sqrt{Hz}$
Input Current Noise Density	(Note 4)	IN_D	-	100	-	$fA/\sqrt{Hz}$
Distortion Performance, Normal						
Total Harmonic Distortion	(Note 5, 6)	THD	-	-118	-112	dB
Linearity	(Note 5, 6)	LIN	-	0.000126	0.000251	%
Distortion Performance, Low Power (LPWR=1)						
Total Harmonic Distortion	(Note 5, 6)	THD	-	-118	-110	dB
Linearity	(Note 5, 6)	LIN	-	0.000126	0.000316	%

Notes: 4. Guaranteed by design and/or characterization.
5. Tested with a full scale input signal of 31.25 Hz.
6. Noise in the harmonic bins dominates THD and linearity measurements for x16, x32, x64 gains.



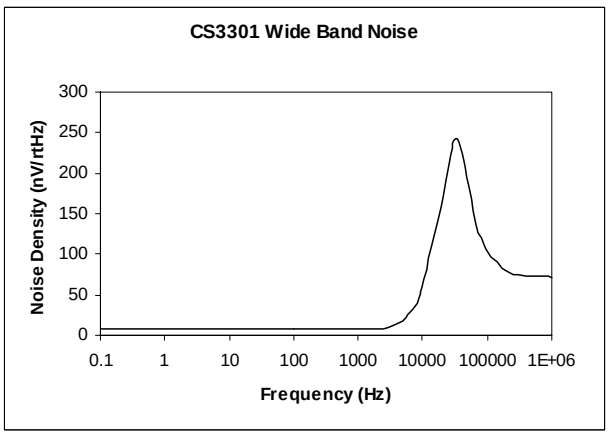


Figure 1. CS3301 Noise Performance

ANALOG CHARACTERISTICS (CONT.)

Parameter		Symbol	CS3301 Min	CS3301 Typ	CS3301 Max	Unit
Gain						
Gain, Differential		GAIN	x1	-	x64	
Gain, Common Mode	(Note 7)	$GAIN_{CM}$	-	x1	-	
Gain Accuracy, Absolute	(Note 8)	$GAIN_{ABS}$	-	±1	±2	%
Gain Accuracy, Relative	(Note 9)	$GAIN_{REL}$	-	±0.2	±0.5	%
Gain Drift	(Note 4, 10)	$GAIN_{TC}$	-	5	-	ppm / ºC
Offset						
Offset Voltage, Input Referred	(Note 11)	OFST	-	±5	±15	µV
Offset After Calibration, Absolute	(Note 12)	$OFST_{CAL}$	-	±1	-	µV
Offset Calibration Range	(Note 13)	$OFST_{RNG}$	-	100	-	% F.S.
Offset Voltage Drift	(Note 4, 10)	$OFST_{TC}$	-	0.1	-	µV / ºC

7. Common mode signals pass through the differential amplifier architecture.
8. Absolute gain accuracy tests the matching of x1 gain across multiple CS3301 devices.
9. Relative gain accuracy tests the tracking of x1,x2,x4,x16,x32,x64 gain relative to x8 gain on a single CS3301 device.
10. Specification is for the parameter over the specified temperature range and is for the CS3301 device only. It does not include the effects of external components.
11. Offset voltage is tested with the amplifier inputs connected to the internal 800Ω termination.
12. The absolute offset after calibration specification applies to the effective offset voltage of the CS3301 output when used with the CS5371/72 modulator and CS5376A digital filter, and is measured from the digitally calibrated output codes of the CS5376A.
13. The CS3301 offset calibration is performed digitally with the CS5371/72 modulator and CS5376A digital filter and includes the full scale signal range. Calibration offsets of greater than ± 5% of full scale will begin to subtract from system dynamic range.

ANALOG CHARACTERISTICS (CONT.)

Parameter		Symbol	CS3301 Min	CS3301 Typ	CS3301 Max	Unit
Analog Input Characteristics						
Input Signal Frequencies		BW	DC	-	2000	Hz
Input Voltage Range (Signal + Vcm) (Note 14)	x1	V_{IN}	(VA-)+0.7	-	(VA+)-1.25	V
	x2 - x64		(VA-)+0.7	-	(VA+)-1.75	
Full Scale Input, Differential	x1	V_{INFS}	-	-	5	V_{p-p}
	x2		-	-	2.5	V_{p-p}
	x4		-	-	1.25	V_{p-p}
	x8		-	-	625	mV_{p-p}
	x16		-	-	312.5	mV_{p-p}
	x32		-	-	156.25	mV_{p-p}
	x64		-	-	78.125	mV_{p-p}
Input Impedance, Differential		Z_{INDIFF}	-	1, 50	-	GΩ, pF
Input Impedance, Common Mode		Z_{INCM}	-	1	-	MΩ
Input Bias Current		I_{IN}	-	500	1200	pA
Crosstalk, Multiplexed Inputs	(Note 4)	XT	-	-130	-	dB
Common to Differential Mode Rejection	(Note 4, 15)	CDMR	90	100	-	dB
Analog Output Characteristics						
Full Scale Output, Differential		V_{OUT}	-	-	5	V_{p-p}
Output Voltage Range (Signal + Vcm)		V_{RNG}	(VA-)+0.5	-	(VA+)-0.5	V
Output Impedance	(Note 16)	Z_{OUT}	-	680	-	Ω
Output Impedance Drift	(Note 16)	Z_{TC}	-	0.24	-	Ω/°C
Output Current		I_{OUT}	-	-	3.33	mA
Load Capacitance		C_L	-	-	100	nF

Notes: 14. No signals operating from external power supplies should be applied to pins of the device prior to its own supplies being established. Connecting any terminal to voltages greater than VA+ or less than VA- may cause destructive latch-up.

15. Ratio of common mode input amplitude vs. differential mode output amplitude for a perfectly matched common mode input signal. Characterized with a 50 Hz, 500 mV_{peak} common mode sine wave applied to the analog inputs.

16. Output impedance characteristics are primarily determined by the integrated anti-alias resistors. Values are approximate and can vary up to +/- 10% depending on process parameters.

DIGITAL CHARACTERISTICS

Parameter	Symbol	CS3301 Min	Typ	Max	Unit
Digital Characteristics					
High Level Input Drive Voltage (Note 17)	V_{IH}	0.6*VD	-	VD	V
Low Level Input Drive Voltage (Note 17)	V_{IL}	0.0	-	0.8	V
Input Leakage Current	I_{IN}	-	±1	±10	µA
Digital Input Capacitance	C_{IN}	-	9	-	pF
Rise Times, Digital Inputs Except CLK	t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs Except CLK	t_{FALL}	-	-	100	ns
Master Clock Specifications					
Master Clock Frequency (Note 18)	f_{CLK}	2.0	2.048	2.2	MHz
Master Clock Duty Cycle	f_{DTY}	40	-	60	%
Master Clock Rise Time	t_{RISE}	-	-	25	ns
Master Clock Fall Time	t_{FALL}	-	-	25	ns
Master Clock Jitter (In-Band or Aliased In-Band)	JTR_{IB}	-	-	300	ps
Master Clock Jitter (Out-of-Band)	JTR_{OB}	-	-	1	ns

Notes: 17. Device is intended to be driven with CMOS logic levels.

18. When CLK is tied to DGND, an internal oscillator provides a master clock at approximately 2 MHz. CLK should be driven for synchronous system operation.

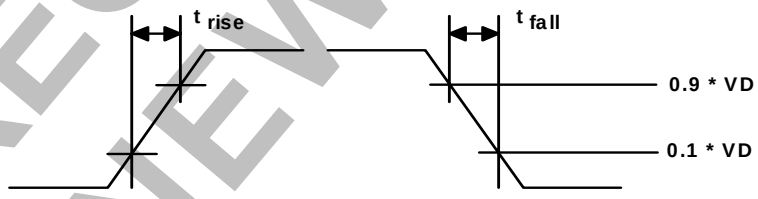


Figure 2. Digital Input Rise and Fall Times

Input Selection	MUX1	MUX0
800 Ω termination	0	0
INA only	1	0
INB only	0	1
INA + INB	1	1

Gain Selection	GAIN2	GAIN1	GAIN0
x1	0	0	0
x2	0	0	1
x4	0	1	0
x8	0	1	1
x16	1	0	0
x32	1	0	1
x64	1	1	0
reserved	1	1	1

Table 1. Digital Selections for Gain and Input Mux Control

POWER SUPPLY CHARACTERISTICS

Parameter		Symbol	CS3301 Min	Typ	Max	Unit
Power Supply Current, Normal						
Analog Power Supply Current	(Note 19)	I_A	-	5.25	6.8	mA
Digital Power Supply Current	(Note 19)	I_D	-	0.2	0.25	mA
Power Supply Current, Low Power (LPWR=1)						
Analog Power Supply Current	(Note 19)	I_A	-	3.5	4.75	mA
Digital Power Supply Current	(Note 19)	I_D	-	0.2	0.25	mA
Power Supply Current, Power Down (PWDN=1)						
Analog Power Supply Current	(Note 19)	I_A	-	9	11	µA
Digital Power Supply Current	(Note 19)	I_D	-	2	8	µA
Power Supply Rejection						
Power Supply Rejection Ratio	(Note 4, 20)	PSRR	95	120	-	dB

Notes: 19. All outputs unloaded. Analog inputs connected to the internal 800 Ω termination. Digital inputs forced to VD or DGND respectively.

20. Power supply rejection characterized with a 50 Hz, 400 mVp-p sine wave applied separately to each supply.

2. GENERAL DESCRIPTION

The CS3301 is a low-noise chopper-stabilized CMOS differential input, differential output amplifier for precision analog signals between DC and 2 kHz. It has multiplexed inputs, rough/fine charge outputs, and programmable gains of x1, x2, x4, x8, x16, x32, and x64.

The amplifier's performance makes it ideal for low-frequency, high dynamic range applications requiring low distortion and minimal power consumption. It's optimized for use in acquisition systems designed around the CS5371/72 single/dual ΔΣ modulators and the CS5376A quad digital filter. Figure 3 shows the system architecture of a 4-channel acquisition system using four CS3301, two CS5372, one CS4373A, and one CS5376A.

2.1 Analog Signals

2.1.1 Analog Inputs

The amplifier analog inputs are designed for differential sensors. Input multiplexing simplifies system connections by providing separate inputs for a sensor and test DAC (INA, INB) as well as an internal termination for noise tests. The MUX0, MUX1 digital pins determine which multiplexed input is connected to the amplifier.

2.1.2 Analog Outputs

The amplifier analog outputs are separated into rough charge / fine charge signals to easily connect to the CS5371/72 inputs. Each output also includes a series resistor, requiring only two differential capacitors to create the CS5371/72 input anti-alias filter.

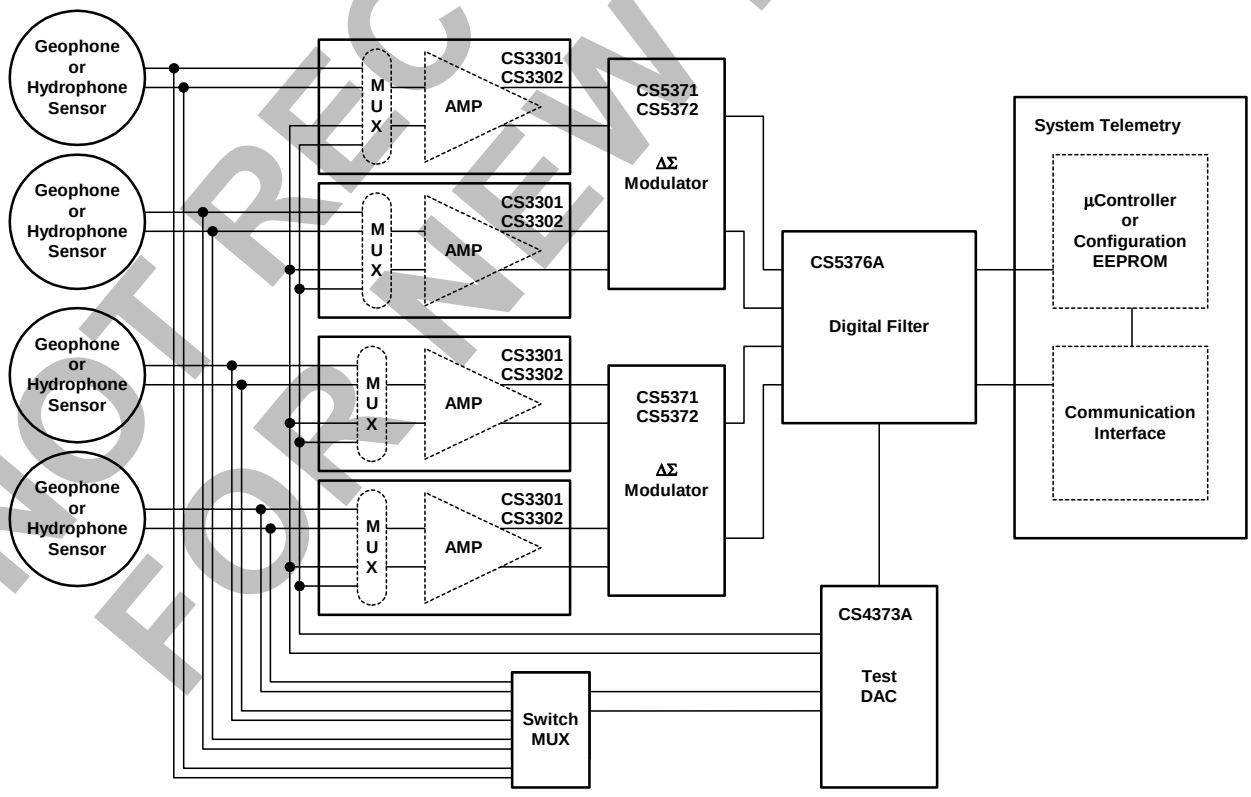


Figure 3. Multi-Channel System Architecture

2.1.3 Differential Signals

Analog signals into and out of the CS3301 are differential, consisting of two halves with equal but opposite magnitude varying about a common mode voltage.

A full scale 5 Vpp differential signal centered on a -0.15 V common mode can have:

SIG+ = -0.15 V + 1.25 V = 1.1 V

SIG- = -0.15 V - 1.25 V = -1.4 V

SIG+ is +2.5 V relative to SIG-

For the reverse case:

SIG+ = -0.15 V - 1.25 V = -1.4 V

SIG- = -0.15 V + 1.25 V = 1.1 V

SIG+ is -2.5 V relative to SIG-

The total swing for SIG+ relative to SIG- is (+2.5 V) - (-2.5 V) = 5 V_{pp}. A similar calculation can be done for SIG- relative to SIG+. Note that a 5 V_{pp} differential signal centered on a -0.15 V common mode voltage never exceeds 1.1 V and never drops below -1.4 V on either half of the signal.

By definition, differential voltages are to be measured with respect to the opposite half, not relative to ground. A multimeter differentially measuring between SIG+ and SIG- in the above example would properly read 1.767 V_{rms}, or 5 V_{pp}.

2.2 Digital Signals

2.2.1 Clock Input

The clock signal is used by the chopper-stabilization circuitry of the amplifier analog inputs. The CLK pin can be driven by an external clock source for synchronous operation, or CLK can be grounded to run from its own internally generated clock signal. The CLK pin is connected to a clock detect circuit which will disable the internal clock and use an external clock if one is supplied. If the internal clock signal is to be used, the CLK pin should be connected to DGND.

2.2.2 Gain Selection

The CS3301 supports gain ranges of x1, x2, x4, x8, x16, x32, and x64. They are selected using the GAIN0, GAIN1, and GAIN2 pins as shown in Table 1 on page 8.

2.2.3 Mux Selection

The analog inputs to the amplifier are multiplexed, with external signals applied to the INA+, INA- or INB+, INB- pins. An internal termination is also available for noise tests. Input mux selection is made using the MUX0 and MUX1 pins as shown in Table 1 on page 8.

Although a mux selection is provided to enable the INA and INB switches simultaneously, significant current should not be driven through them in this mode. The CS3301 mux switches will maintain good linearity only with minimal signal currents.

2.2.4 Low Power Selection

For applications where power is critical, a low-power mode can be selected. This mode reduces amplifier power consumption at the expense of slightly degraded performance. Low power mode is selected using the LPWR pin, which is active high.

2.2.5 Power Down Selection

A power-down mode is available to shut down the amplifier when not in use. When enabled, all internal circuitry is disabled, the analog inputs and outputs go high-impedance, and the device enters a micro-power state. Power down mode is selected using the PWDN pin, which is active high.

2.3 Power Supplies

2.3.1 Analog Power Supplies

The analog power pins of the CS3301 are to be supplied with a total of 5 V between VA+ and VA-. This voltage is typically from a bipolar ±2.5 V power supply. When using bipolar power supplies, the analog signal common mode voltage should be biased to 0 V. The analog power supplies are rec-

ommended to be bypassed to system ground using 0.1 µF X7R type capacitors.

The VA- supply is connected to the CMOS substrate and as such must remain the most negative applied voltage to prevent potential latch-up conditions. Care should be taken to ensure analog input voltages do not drop more than -0.3 V below the VA- supply. Care should also be taken to establish the VA- supply before analog signals are applied to the device. It is recommended to clamp the VA- supply to system ground using a reversed biased Schottky diode to prevent possible latch-up conditions related to mismatched supply rail initialization.

2.3.2 Digital Power Supplies

The digital power supply across the VD and DGND pins is flexible and can be set to interface with 3.3V or 5V logic. The digital power supply should be bypassed to system ground using a 0.01 µF X7R type capacitor.

2.4 Connection Diagram

Figure 4 shows a connection diagram for the CS3301 amplifier when used with the CS5372 dual ΔΣ modulator and CS5376A digital filter. The diagram shows differential sensors, a test DAC, and analog outputs with anti-alias capacitors; power supply connections including recommended by-passing; and digital control connections back to the CS5376A GPIO pins.

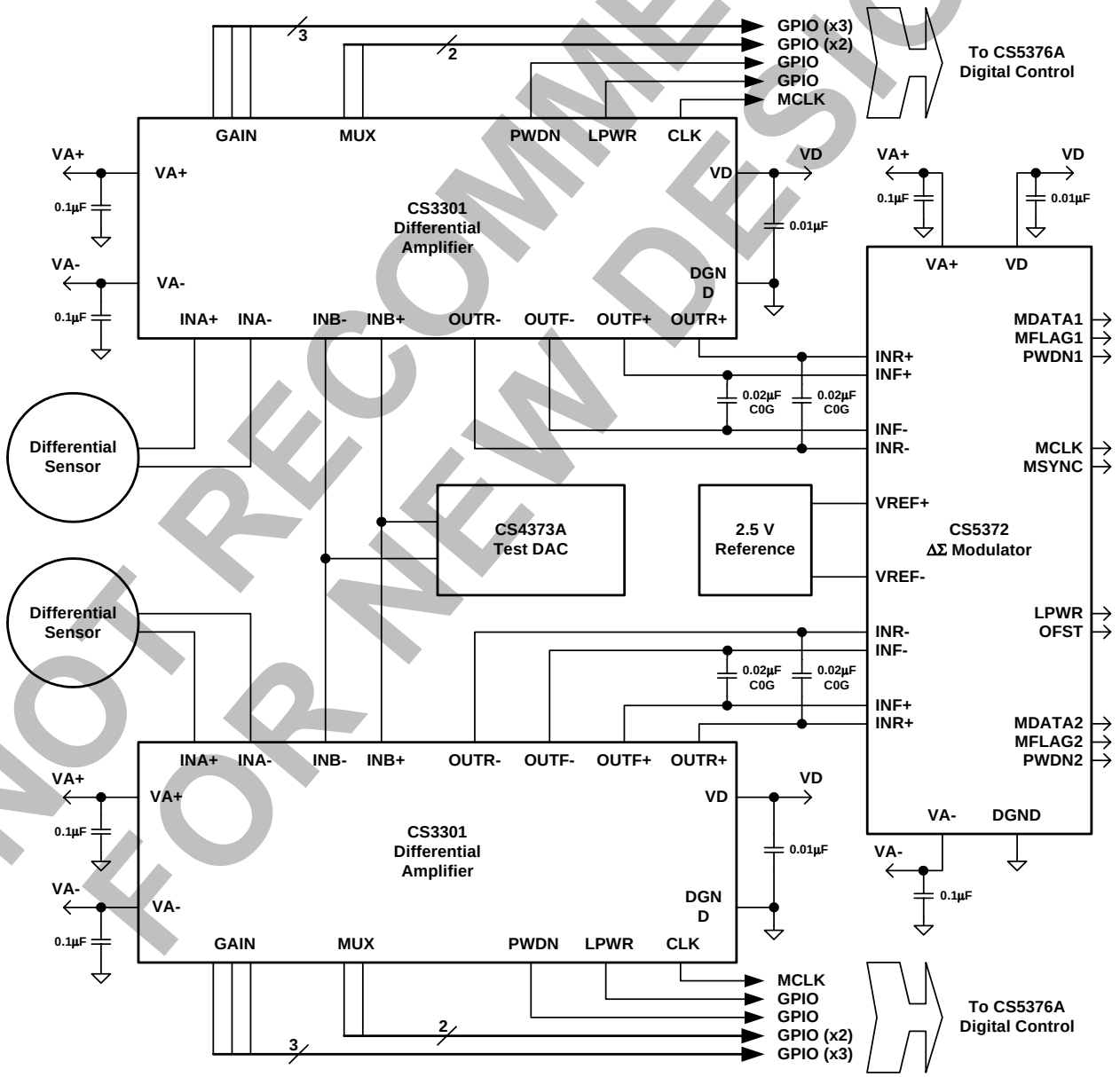


Figure 4. CS3301 Amplifier Connections

3. PIN DESCRIPTION

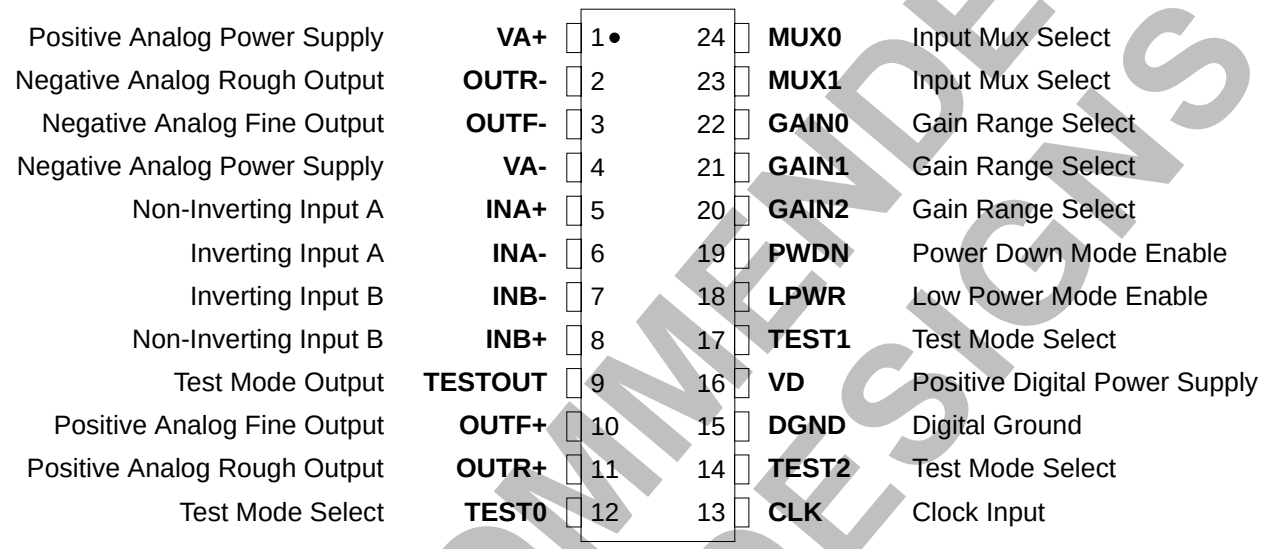


Figure 5. CS3301 Pin Assignments

Pin Name	Pin #	I/O	Pin Description
VA+	1	I	Positive analog supply voltage.
VA-	4	I	Negative analog supply voltage.
VD	16	I	Positive digital supply voltage.
DGND	15	I	Digital ground.
INA+, INA-	5, 6	I	Channel A differential analog inputs. Selected via MUX pins.
INB+, INB-	8, 7	I	Channel B differential analog inputs. Selected via MUX pins.
OUTR+, OUTR-	11, 2	O	Rough charge differential analog outputs.
OUTF+, OUTF-	10, 3	O	Fine charge differential analog outputs.
GAIN0, GAIN1, GAIN2	22, 21, 20	I	Gain range select. See Gain Selection table in Digital Characteristics section.
CLK	13	I	Master clock input. Connect to DGND to use internal oscillator.
LPWR	18	I	Low power mode enable. Active high.
PWDN	19	I	Power down mode enable. Active high.
MUX0, MUX1	24, 23	I	Analog input select. See Input Selection table in Digital Characteristics section.
TEST0	12	I	Test mode select, factory use only. Connect to VA- during normal operation.
TEST1, TEST2	17, 14	I	Test mode select, factory use only. Connect to DGND during normal operation.
TESTOUT	9	O	Test mode output, factory use only. Connect to VA- during normal operation.

Table 2. Pin Descriptions

4. ORDERING INFORMATION

Model	Temperature	Package
CS3301-IS	-40 to +85 °C	24-pin SSOP
CS3301-ISZ (lead free)		

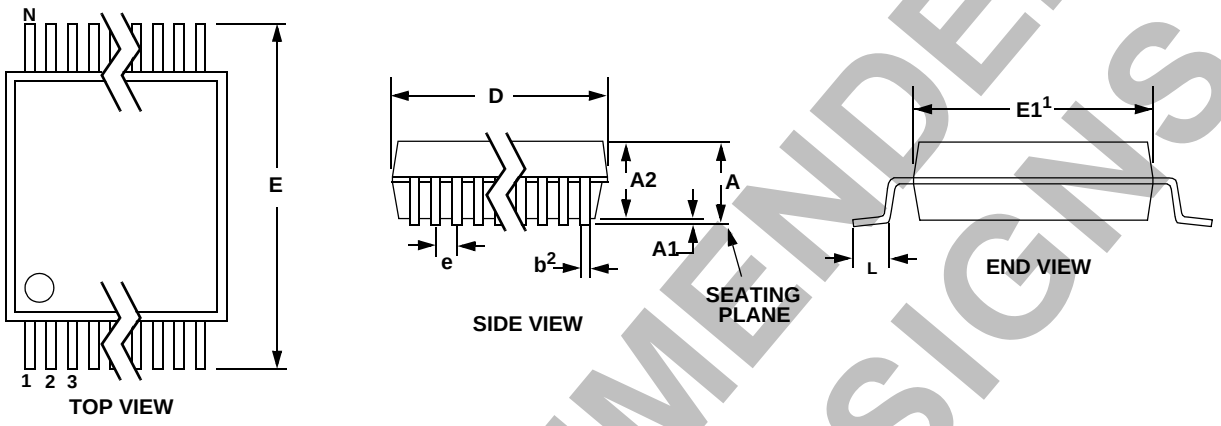
5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS3301-IS	240 °C	2	365 Days
CS3301-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

6. PACKAGE DIMENSIONS

24 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.311	0.335	7.90	8.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.