CRD35L01

1 x 1.7 W CS35L01 Amplifier Reference Design Kit

Features

- Four boards provided in the CS35L01 Amplifier Reference Design Kit
- Separate boards for each mode configuration
  - SD, FSD, HD, and FHD
- CS35L01 produces a default +6-dB Gain
- Delivers 1.4 W/Ch into 8 Ω at 1% THD+N
- Delivers 1.7 W/Ch into 8 Ω at 10% THD+N
- Differential mono analog inputs
- Demonstrates recommended 4-layer layout and grounding arrangements
  - Optional output filter connections
  - Optional gain adjustment resistors
- Powered by a single 2.5- to 5.5-V power supply
- Device shutdown control

Description

The CRD35L01 demonstrates the CS35L01 high-efficiency Hybrid Class-D audio amplifier. This reference design implements a single-channel amplifier that delivers 1.7 W per full-bridge channel into 8-Ω loads using a single +5-V supply.

Differential audio inputs can easily be connected through the J1 header. If desired, the gain can be adjusted through the optional input resistors.

The -SD, -FSD, -HD, or -FHD suffix designates the CS35L01's operational mode. Each of the four boards is configured to operate in each of the four corresponding modes of the CS35L01 device.

Device shutdown control is available through the J2 header.

ORDERING INFORMATION

CRD35L01	CS35L01 Reference Design

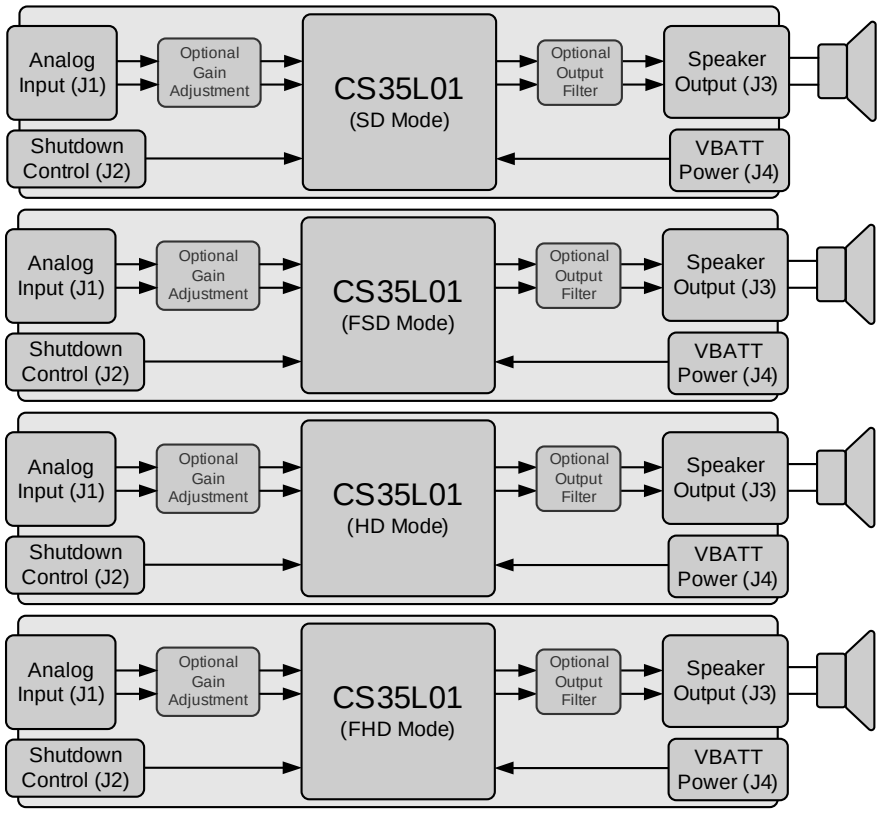


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SYSTEM OVERVIEW

The CRD35L01 reference design is a practical means for evaluating the CS35L01 high-efficiency Class-D audio amplifier with idle current consumption. A differential mono analog input signal interface is provided. Optional input gain and output filtering component placeholders are provided for easy modification to custom tune the CS35L01 for the user's specific system requirements.

1.1 CS35L01 Hybrid Class-D Amplifier

The CS35L01 Hybrid Class-D amplifier is a mono, full-bridge, closed-loop, +6-dB gain, audio amplifier available in a 9-ball, WLCSP package. A complete description of the CS35L01 device is included in the CS35L01 product data sheet.

1.2 Power Supply

A single +2.5 to +5.5 VDC power supply is required to power the CRD35L01. The supply must be capable of delivering sufficient current for the intended power output. The supply provides power to the CS35L01. The power supply connection to the board is provided by the header J4. The positive terminal is labeled VBATT. The ground terminal is labeled GND.

1.3 Operational Modes

The CS35L01 device has four operational modes, each of which require slightly different hardware connections. Four boards are available to illustrate the hardware design differences between each of the four modes. More information on the specifics of each operational mode can be found in the CS35L01/03 product datasheet. The CRD names listed below are populated with a CS35L01 device.

- CRD35L01-SD: Standard Class-D Mode
- CRD35L01-FSD: Reduced-Frequency Standard Class-D Mode
- CRD35L01-HD: Hybrid Class-D Mode
- CRD35L01-FHD: Reduced-Frequency Hybrid Class-D Mode

The CRD35L01-SD schematic is shown in Figure 2 on page 8. The CRD35L01-FSD schematic is shown in Figure 3 on page 8. The CRD35L01-HD schematic is shown in Figure 5 on page 8. The CRD35L01-FHD schematic is shown in Figure 5 on page 8.

1.4 Shutdown Control

The J2 header contains shutdown control for the CS35L01 device. Placing a jumper across the J2 header pulls the $\overline{SD}$ line LOW and shuts down the amplifier. When no jumper is present, the $\overline{SD}$ line is pulled HIGH by the R3 resistor, enabling normal operation.

1.5 Amplifier Gain

The amplifier gain of the CS35L01 device is +6 dB by default. The amplifier gain can be reduced through the use of the optional input gain adjustment resistors on the CRD35L01.

1.5.1 Optional Input Gain Adjustment Resistors

The CRD35L01 contains optional gain adjustment resistor placeholders (R1 and R2). By default, these placeholders are not populated and are bypassed with a signal trace configuring the CS35L01 to operate at its default gain. The gain adjustment resistors are necessary only when a gain of +6 dB is not desired.

By adding series resistance to the input, the signal amplitude to the CS35L01 will be reduced, and will reduce the overall system gain. The typical input impedance values of the CS35L01 can be found in the device datasheet.

In order to use the optional gain adjustment resistors, the traces between the R1 pads and the traces between the R2 pads must be cut to break the bypass circuit, before populating R1 and R2 with the desired resistance values. The location of these required cuts are shown in Figure 1. After the trace between the pads has been broken, the gain adjustment resistors can be added to the board.

1.6 Differential Analog Inputs

The differential audio inputs into the CS35L01 are provided by the 3-pin header (J1) through DC blocking capacitors (C1 and C2). The C1 and C2 capacitors allow for an analog source to connect directly to the CS35L01 regardless of any DC bias that may be present between the analog audio source's outputs and CS35L01 inputs.

1.7 Speaker Outputs

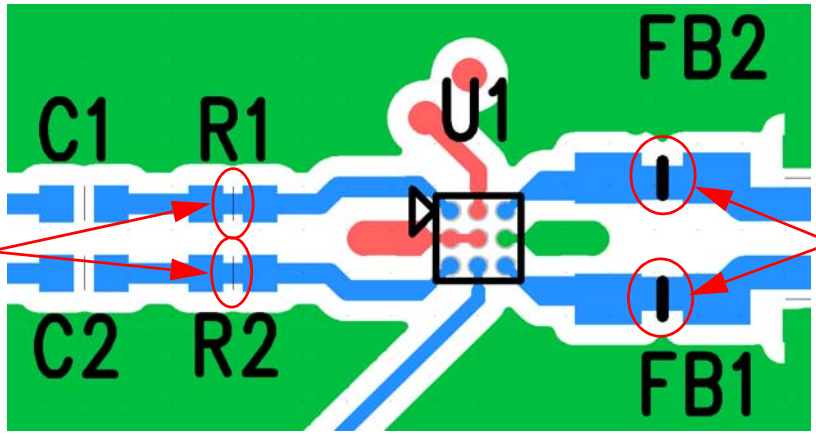
The CS35L01 power outputs are configured for a full-bridge, single audio channel. The outputs are routed through an optional EMI output filter and then presented at the J3 header (OUT- and OUT+).

1.7.1 Optional Speaker Output EMI Filter Components

As mentioned above, the CS35L01 contains optional placeholders for a series ferrite bead and shunt capacitor output filter. For most applications with very short speaker leads between the CS35L01 and the speaker, use of these components will not be necessary. However, if there is a long signal path between the CS35L01 and the speaker or if the system requires connecting to cables off the PCB, it is suggested that the ferrite bead and capacitor are populated with the recommended values shown in Figure 3 on page 9.

In order to use the optional output filter ferrite beads, the traces between the L1 pads and the traces between the L2 pads must be cut to break the bypass circuit, before populating L1 and L2 with the desired component values. The location of these required cuts are shown in Figure 1.

Cut the bypass traces before inserting the optional input gain adjustment resistors



Cut the bypass traces before inserting the optional output filter ferrite beads

Figure 1. Optional Bypass Trace Cut Locations

2. GROUNDING AND POWER SUPPLY DECOUPLING

The CS35L01 requires careful attention to power supply and grounding arrangements to optimize performance and minimize radiated emissions. The decoupling capacitors should be located as close to the CS35L01 as possible. This can be optimized by using both top and bottom side component population as demonstrated by the CRD35L01 boards.

2.1 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Figure 6 and Figure 7 on page 10 show the component placement for the CRD35L01-SD board. Figure 18 and Figure 19 on page 12 shows the component side placement for the CRD35L01-HD board. Note the addition of the C8 capacitor connected to the LFILT+ pin. This pin is used as decoupling for the internal LDO regulator when operating in HD or FHD modes.

The small value decoupling capacitors are placed as close as possible to the power pins of the CS35L01 on the CRD35L01 boards. For the WLCSP package it is recommended that the power supply decoupling capacitors reside on the opposite side of the board from which the CS35L01 is populated on. This allows for very close placement of the decoupling capacitors to the power supply pins of the CS35L01 without interfering with the differential audio inputs or differential audio outputs. This placement keeps the high-frequency current loop small to minimize power supply variations and EMI. These capacitors are not required to be expensive low-ESR capacitors.

2.2 Electromagnetic Interference (EMI)

This reference design is a board-level solution that is meant to control emissions by minimizing and suppressing them at the source, in contrast to containing them in an enclosure.

2.2.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout to minimize high-frequency fields in the immediate vicinity of the high-power components. Specific techniques include the following:

- As mentioned in Section 2.1, effective power supply decoupling of high-frequency currents and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Differential input and output signals should be routed differentially whenever possible.
- A solid ground plane on the adjacent PCB layer underneath all high-frequency traces to minimize the loop area of the return path.
- Optional output EMI filter component landings are available as described in Section 1.7.1, if emissions need to be further reduced.
- Keeping the switching output filter components as close to the amplifier as possible.

3. SYSTEM CONNECTORS AND JUMPERS

Connector Name	Reference Designator	Pin	Signal Direction	Connector Function
IN+	J1	1	Input	Differential analog input (+) to CS35L01.
IN-	J1	2	Input	Differential analog input (-) to CS35L01.
GND	J1	3	GND	GND reference connection.
$\overline{SD}$	J2	1	Input	Device shutdown control.
GND	J2	2	GND	GND reference connection.
OUT+	J3	1	Output	Analog output (+) from CS35L01.
OUT-	J3	2	Output	Analog output (-) from CS35L01.
VBATT	J4	1	Input	Positive connection from power supply, +2.5 to +5.5 VDC.
GND	J4	2	Input	GND connection from power supply.

Table 1. System Input and Output Connections

Control Name	Function	Function Selected
$\overline{SD}$	Shutdown	Low = CS35L01 shutdown enabled High = CS35L01 shutdown disabled

Table 2. J2 Shutdown Control Settings

4. CRD SCHEMATIC

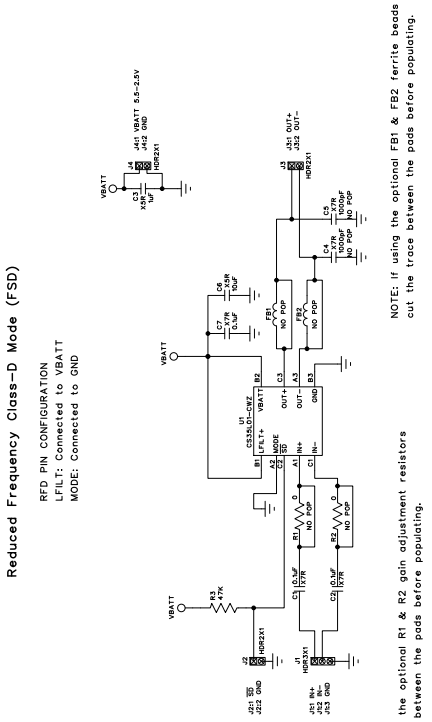


Figure 3. CRD35L01-FSD Schematic

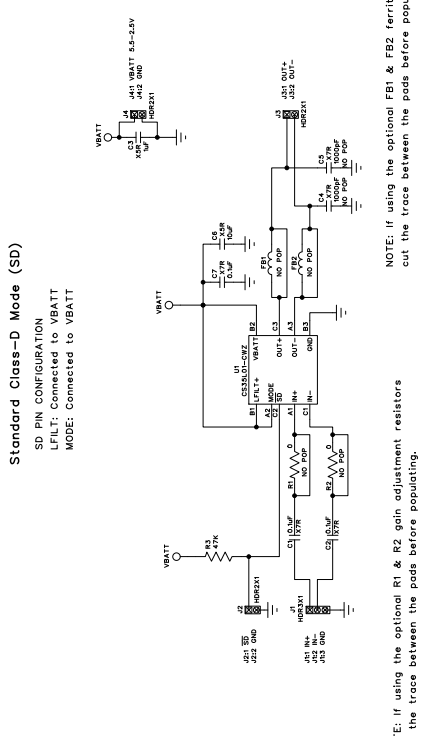


Figure 2. CRD35L01-SD Schematic

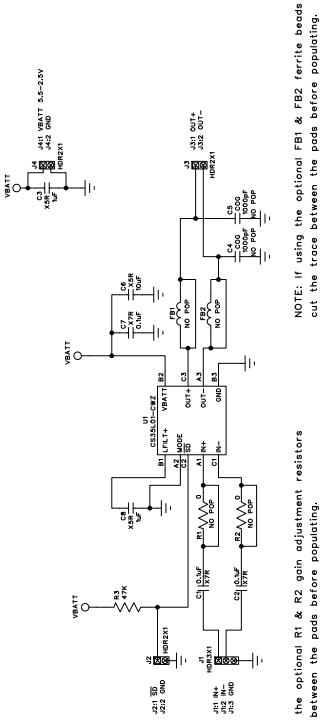


Figure 5. CRD35L01-FHD Schematic

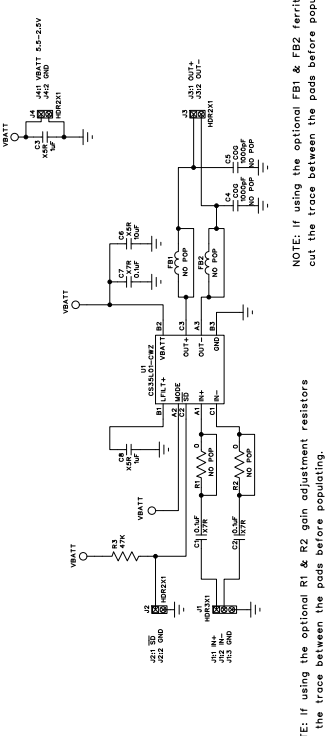


Figure 4. CRD35L01-HD Schematic

4.1 Bill of Materials

The component listing below is shown for the four CRD35L01 board variations (-SD, -FSD, -HD, and -FHD). Unpopulated (DNP) components are listed with recommended components for reference purposes.

Qty	Reference Designator(s)	CRD35L01 Boards	Description	MFG / Part Number
2	C1, C2	-SD, -FSD, -HD, -FHD	Capacitor, 0.1 µF, X7R, 16 V	Kemet / C0402C104K4RAC
1	C3	-SD, -FSD, -HD, -FHD	Capacitor, 1 µF, X5R, 10 V	Kemet / C0603C105K8PAC
1	C6	-SD, -FSD, -HD, -FHD	Capacitor, 10 µF, X5R, 6.3 V	Kemet / C0603C106M9PAC
1	C7	-SD, -FSD, -HD, -FHD	Capacitor, 0.1 µF, X7R, 16 V	Kemet / C0402C104K4RAC
1	C8	-HD, -FHD (Note 1)	Capacitor, 1 µF, X5R, 10 V	Kemet / C0603C105K8PAC
1	R3	-SD, -FSD, -HD, -FHD	Resistor 47k Ω, 1/16 W	Dale / CRCW040247K0JNED
1	U1	-SD, -FSD, -HD, -FHD	Hybrid Class-D WLCSP Amp	Cirrus Logic / CS35L01-CWZ
(DNP)	C4, C5	-SD, -FSD, -HD, -FHD	Capacitor, 1 nF, X7R, 50 V	Murata / GRM155R71H102KA01D
(DNP)	FB1, FB2	-SD, -FSD, -HD, -FHD	Ferrite Bead, 220 Ω @ 100 MHz	TDK / MPZ1608S221A
(DNP)	R1, R2	-SD, -FSD, -HD, -FHD	Resistor, 0 Ω, 1/16 W	Yageo / RC0402JR-070RL

Table 3. Bill of Materials Listing

Note:

1. C8 is not present on SD or FSD boards. LFILT+ (B1) is connected directly to VBATT.

5. CRD LAYOUT

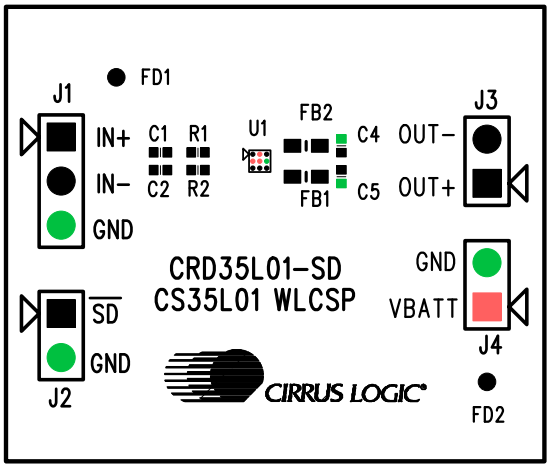


Figure 6. CRD35L01-SD Top Side Component Placement

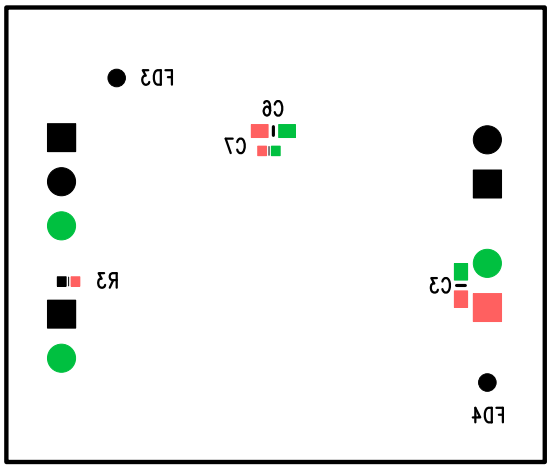


Figure 7. CRD35L01-SD Bottom Side Component Placement

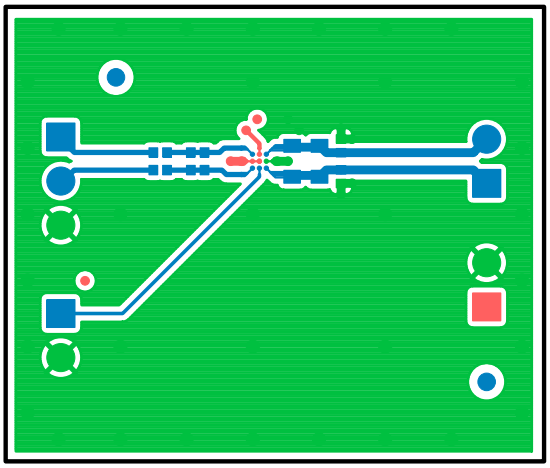


Figure 8. CRD35L01-SD Layer 1 Copper

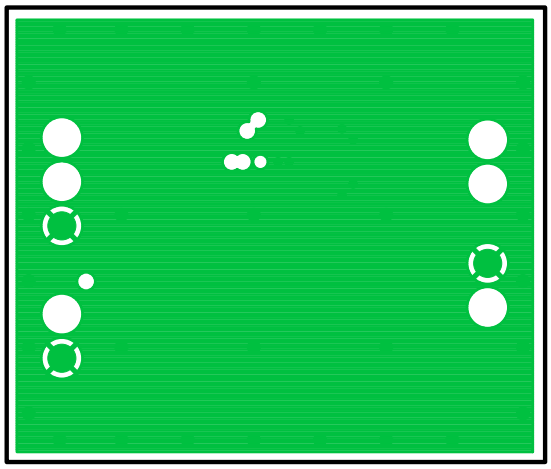


Figure 9. CRD35L01-SD Layer 2 Copper

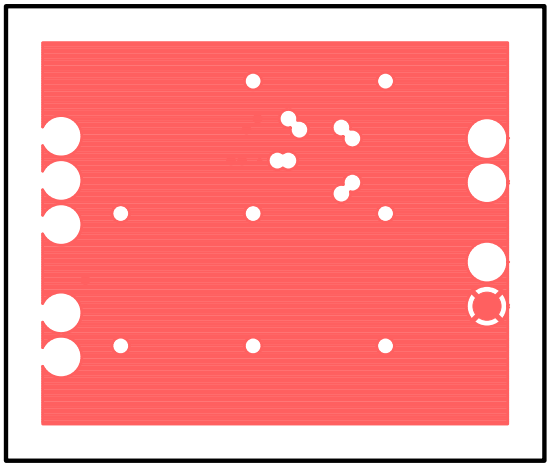


Figure 10. CRD35L01-SD Layer 3 Copper

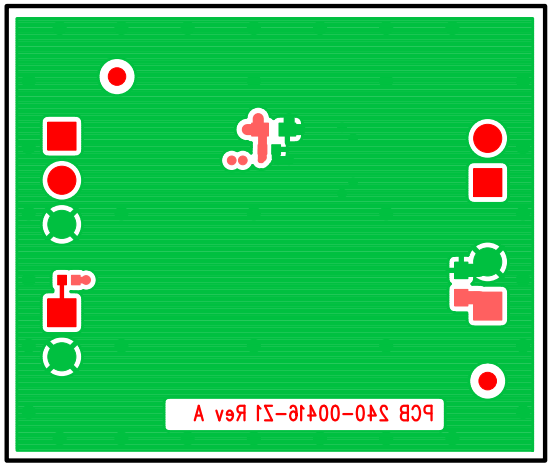


Figure 11. CRD35L01-SD Layer 4 Copper

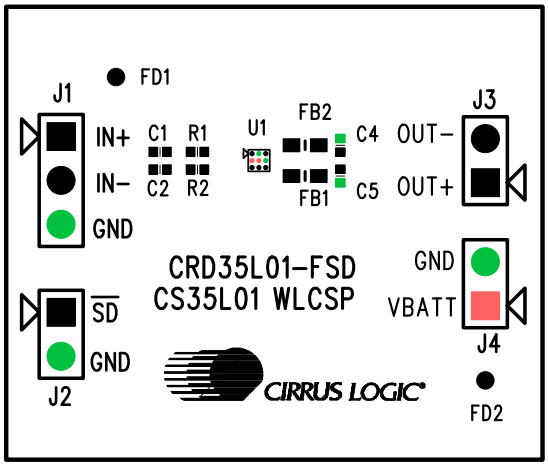


Figure 12. CRD35L01-FSD Top Side Component Placement

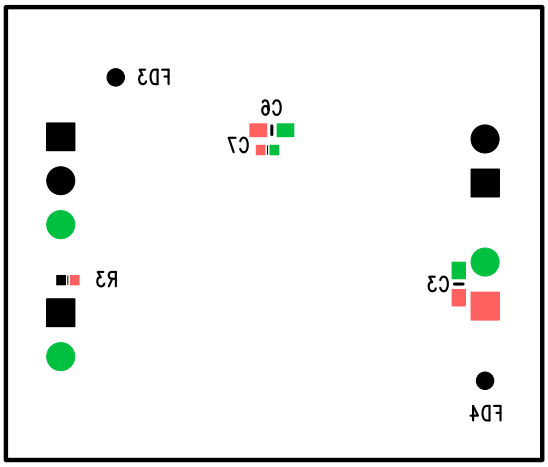


Figure 13. CRD35L01-FSD Bottom Side Component Placement

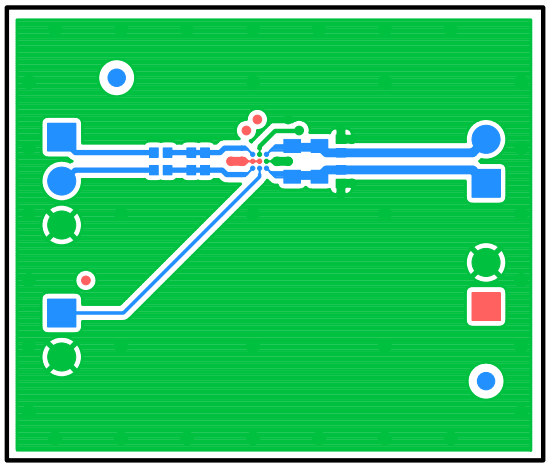


Figure 14. CRD35L01-FSD Layer 1 Copper

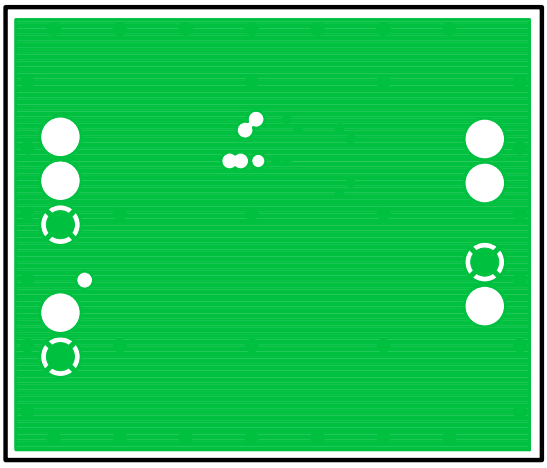


Figure 15. CRD35L01-FSD Layer 2 Copper

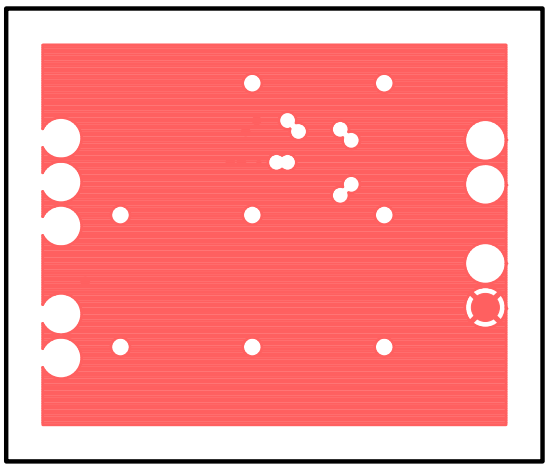


Figure 16. CRD35L01-FSD Layer 3 Copper

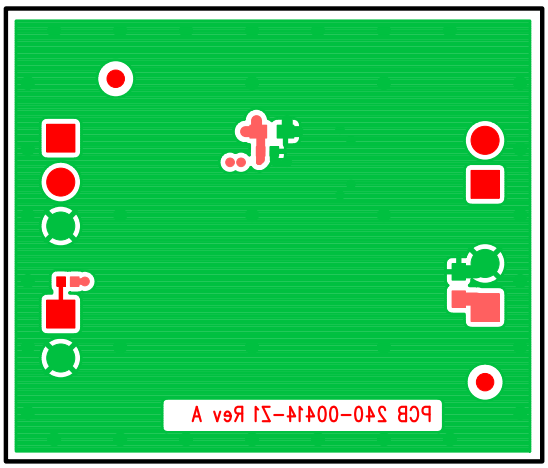


Figure 17. CRD35L01-FSD Layer 4 Copper

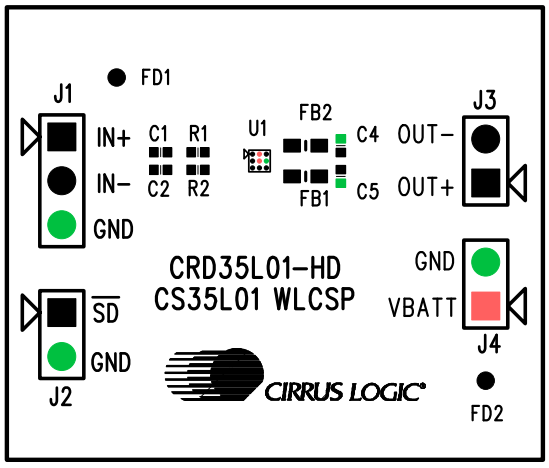


Figure 18. CRD35L01-HD Top Side Component Placement

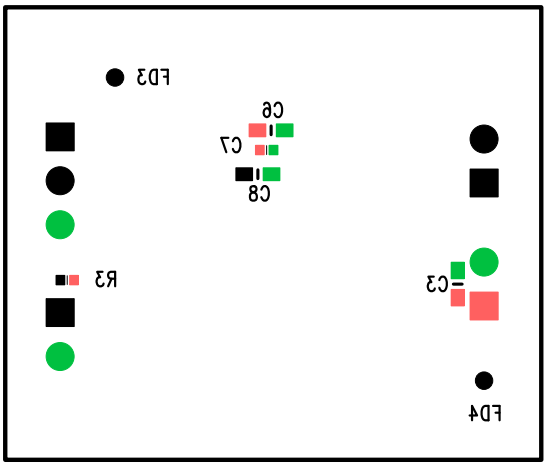


Figure 19. CRD35L01-HD Bottom Side Component Placement

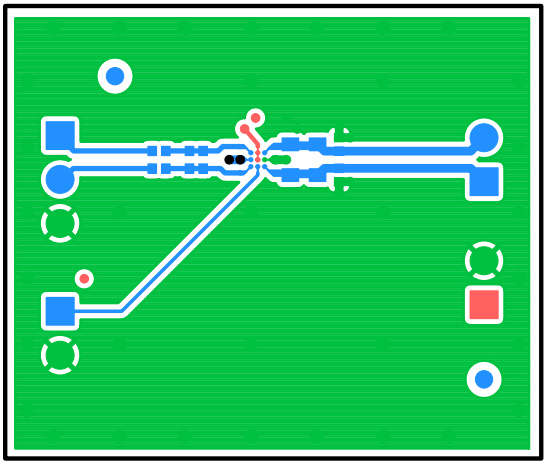


Figure 20. CRD35L01-HD Layer 1 Copper

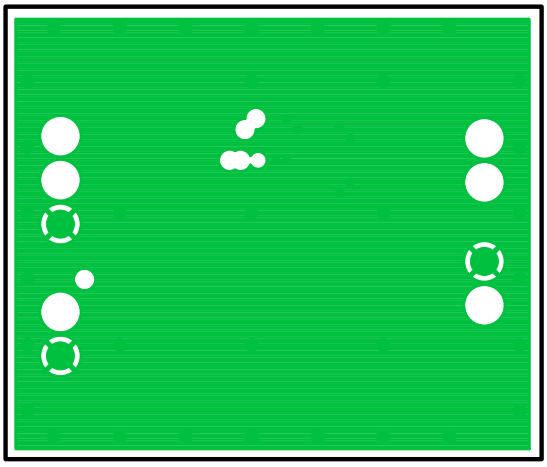


Figure 21. CRD35L01-HD Layer 2 Copper

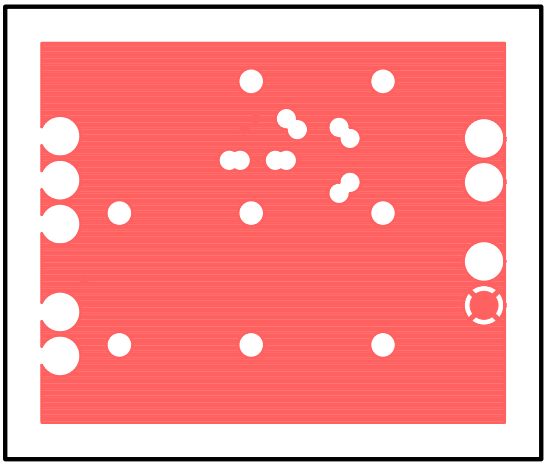


Figure 22. CRD35L01-HD Layer 3 Copper

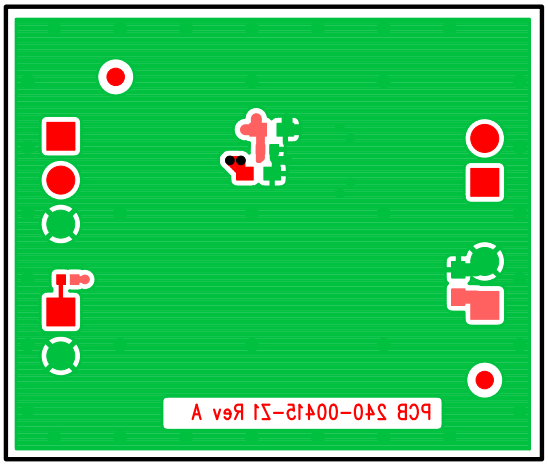


Figure 23. CRD35L01-HD Layer 4 Copper

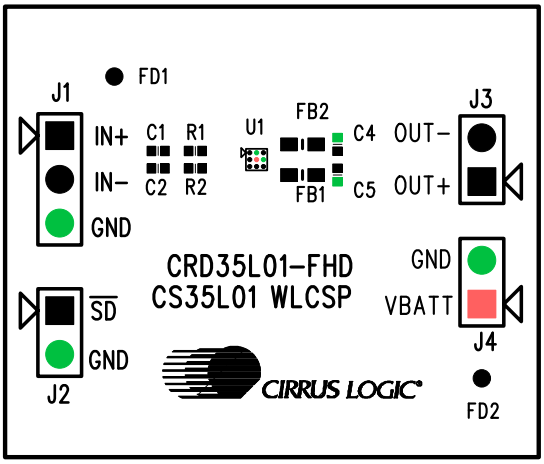


Figure 24. CRD35L01-FHD Top Side Component Placement

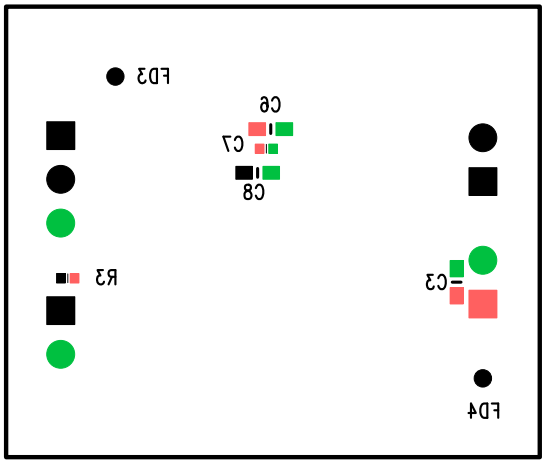


Figure 25. CRD35L01-FHD Bottom Side Component Placement

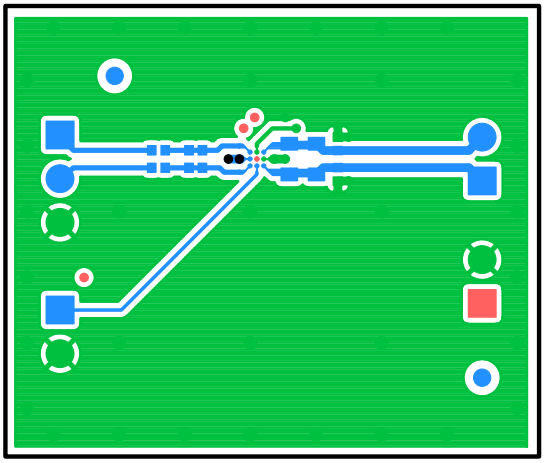


Figure 26. CRD35L01-FHD Layer 1 Copper

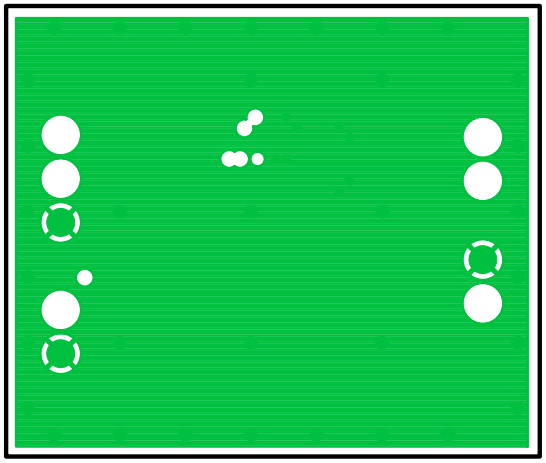


Figure 27. CRD35L01-FHD Layer 2 Copper

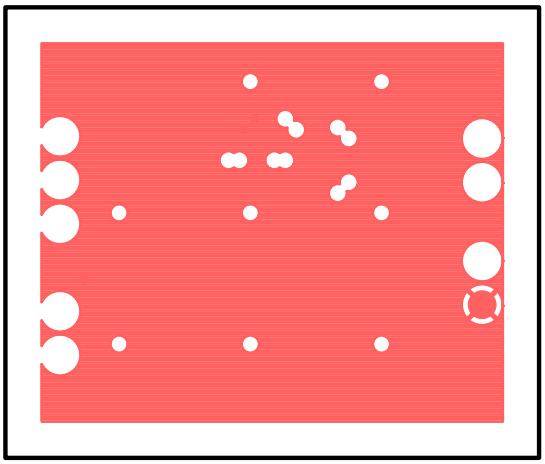


Figure 28. CRD35L01-FHD Layer 3 Copper

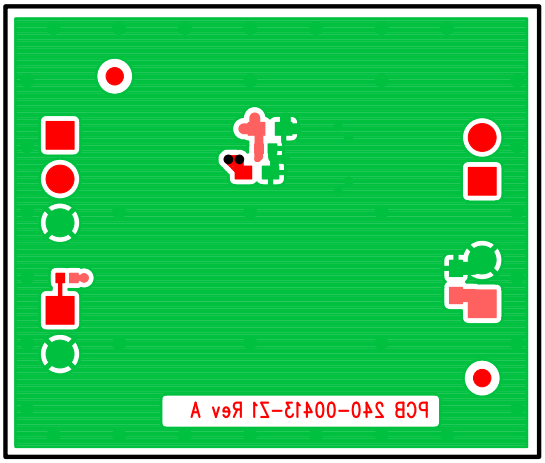


Figure 29. CRD35L01-FHD Layer 4 Copper

6. REVISION HISTORY

Release	Changes
RD1	– Initial Release
RD2	– Updated front page 1% and 10% output power numbers to match DS909A2 datasheet. – Updated Figure 2 on page 8 to match the updated CRD35L01-SD Rev A1 schematic. – Updated Figure 3 on page 8 to match the updated CRD35L01-FSD Rev A1 schematic. – Updated Figure 4 on page 8 to match the updated CRD35L01-HD Rev A1 schematic. – Updated Figure 5 on page 8 to match the updated CRD35L01-FHD Rev A1 schematic. – Updated BOM values for C6 & C7 in Table 3 on page 9 to match the updated Rev A1 schematics and the typical connection diagram in the DS909A2 datasheet. All CRD35L01-SD, -FSD, -HD, and -FHD boards with an assembly date of 02/15/10 or earlier contain components from the Rev A0 BOM.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest to you, go to www.cirrus.com.