

# WS1103

## CDMA Cell 3x3 Power Amplifier Module (824-849 MHz)



### Data Sheet

#### Description

The WS1103 is a CDMA(Code Division Multiple Access) power amplifier module designed for handsets operating in the 824-849 MHz bandwidth.

The WS1103 features CoolPAM circuit technology that offers state-of-the-art reliability, temperature stability and ruggedness.

Digital mode control of CoolPAM reduces current consumption, which enables extended talk time of mobile devices.

The WS1103 meets stringent CDMA linearity requirements to and beyond 28 dBm output power. The 3 mm x 3 mm form factor 8-pin surface mount package is self contained, incorporating 50 ohm input and output matching networks.

#### Features

- Excellent linearity
- Low quiescent current
- High efficiency
  - PAE at 28 dBm: 41.2%
  - PAE at 16 dBm: 17.7%
- 8-pin surface mounting package  
3 mm x 3 mm x 1.0 mm
- Internal 50 ohm matching networks for both RF input and output
- RoHS compliant

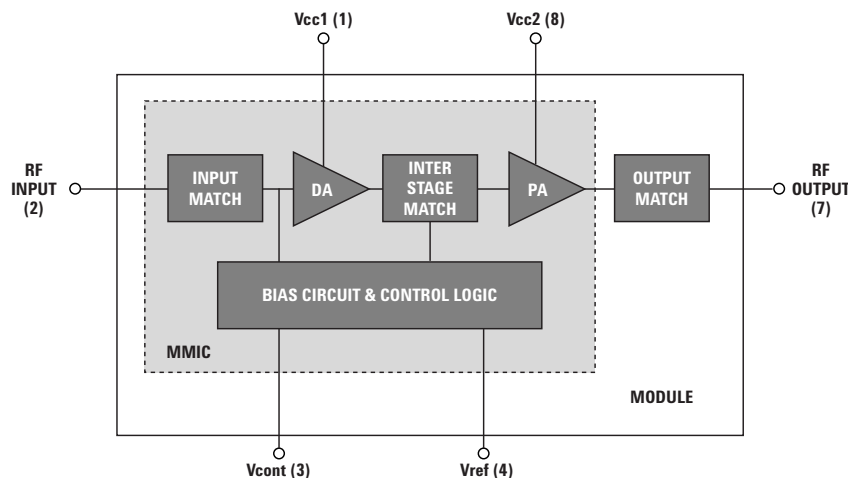
#### Applications

- Digital CDMA Cellular
- Wireless local loop

#### Order Information

Part Number	No. of Devices	Container
WS1103-TR1	1,000	7" Tape and Reel
WS1103-BLK	100	BULK

#### Functional Block Diagram



**Table 1. Absolute Maximum Ratings<sup>[1]</sup>**

Parameter	Symbol	Min.	Nominal	Max.	Unit
RF Input Power	Pin	–	–	10.0	dBm
DC Supply Voltage	Vcc	0	3.4	5.0	V
Reference Voltage	Vref	0	2.85	3.3	V
Control Voltage	Vcont	0	2.85	3.3	V
Storage Temperature	Tstg	-55	–	+125	°C

**Table 2. Recommended Operating Conditions**

Parameter	Symbol	Min.	Nominal	Max.	Unit
DC Supply Voltage	Vcc	3.2	3.4	4.2	V
DC Reference Voltage	Vref	2.75	2.85	2.95	V
Mode Control Voltage					
– High Power Mode	Vcont	0	0	0.5	V
– Low Power Mode	Vcont	2.0	2.85	3.0	V
Operating Frequency	Fo	824		849	MHz
Ambient Temperature	Ta	-30	25	85	°C

**Table 3. Power Range Truth Table**

Power Mode	Symbol	Vref	Vcont <sup>[2]</sup>	Range
High Power Mode	PR2	2.85	Low	~ 28 dBm
Low Power Mode	PR1	2.85	High	~ 16 dBm
Shut Down Mode	–	0	–	–

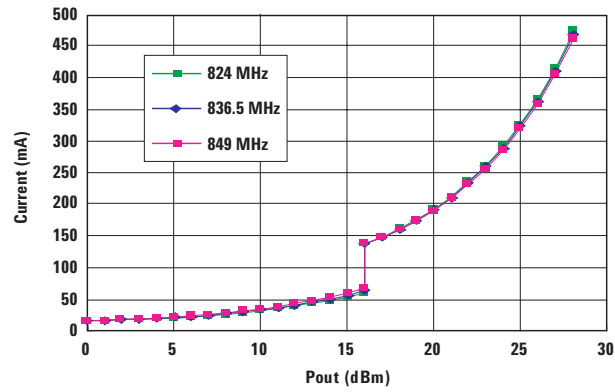
**Notes:**

1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (2.0 – 3.0 V), Low (0.0 V – 0.5 V).

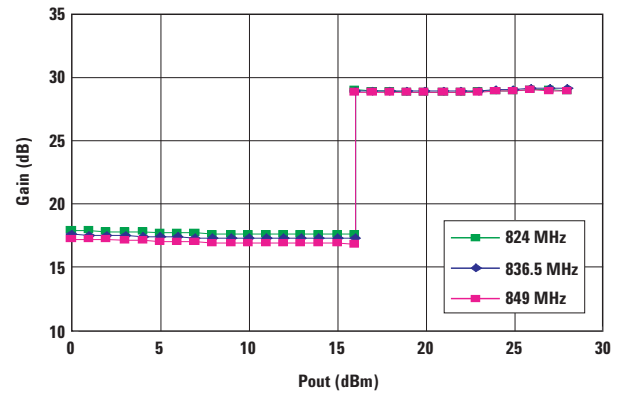
**Table 4. Electrical Characteristics for CDMA Mode (Vcc = 3.4 V, Vref = 2.85 V, T = 25°C, Zin/Zout = 50 ohm)**

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range		F		824	–	849	MHz
Gain		Gain_hi	High Power Mode, Pout = 28 dBm	24	29.5		dB
		Gain_low	Low Power Mode, Pout = 16 dBm	14	17.5		dB
Power Added Efficiency		PAE_hi	High Power Mode, Pout = 28 dBm	36	41.2		%
		PAE_low	Low Power Mode, Pout = 16 dBm	13.6	17.7		%
Total Supply Current		Icc_hi	High Power Mode, Pout = 28 dBm		450	515	mA
		Icc_low	Low Power Mode, Pout = 16 dBm		65	85	mA
Quiescent Current		Iq_hi	High Power Mode		93	125	mA
		Iq_low	Low Power Mode		13	25	mA
Reference Current		Iref_hi	High Power Mode, Pout = 28 dBm		2	7	mA
		Iref_low	Low Power Mode, Pout = 16 dBm		3	8	mA
Control Current		Icont	Low Power Mode, Pout = 16 dBm		0.2	1	mA
Total Current in Power-Down Mode		Ipd	Vref = 0 V		0.2	5	μA
Adjacent Channel Power Ratio	900 kHz offset	ACPR1_hi	High Power Mode, Pout = 28 dBm		-55	-47	dBc
	1.98 MHz offset	ACPR2_hi			-59	-57	dBc
	900 kHz offset	ACPR1_low	Low Power Mode, Pout = 16 dBm		-59	-47	dBc
	1.98 MHz offset	ACPR2_low			-66	-57	dBc
Harmonic Suppression	Second	2f0	High Power Mode, Pout = 28 dBm		-39	-30	dBc
	Third	3f0			-56	-40	dBc
Input VSWR		VSWR			2:1	2.5:1	
Stability (Spurious Output)		S	VSWR 6:1, All Phase			-60	dBc
Noise Power in Rx Band		RxBN			-136.5	-132	dBm/Hz
Ruggedness			No Damage				
		Ru	Pout < 28 dBm, Pin < 10 dBm, All Phase			10:1	VSWR
			High Power Mode				

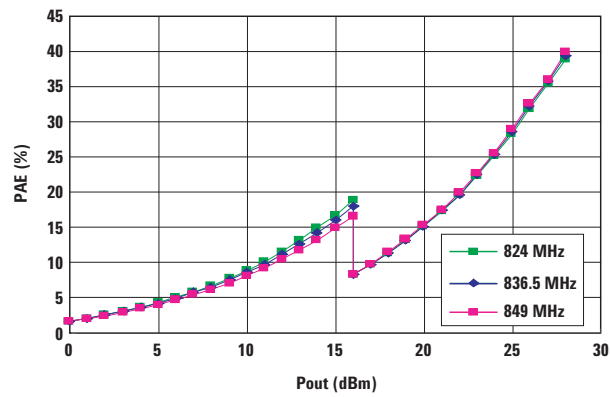
**Characteristics Data ( $V_{cc} = 3.4\text{ V}$ ,  $V_{ref} = 2.85\text{ V}$ ,  $T = 25^\circ\text{C}$ ,  $Z_{in}/Z_{out} = 50\text{ ohm}$ )**



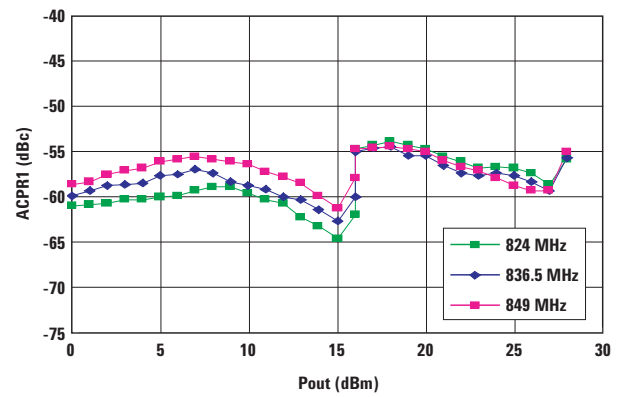
**Figure 1. Total current vs. output power**



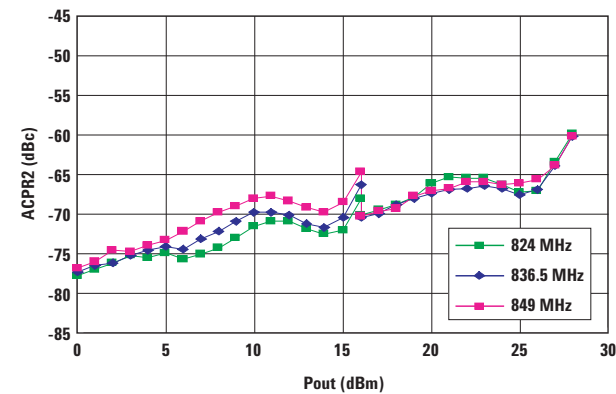
**Figure 2. Gain vs. output power**



**Figure 3. Power added efficiency vs. output power**



**Figure 4. Adjacent channel power ratio 1 vs. output power**



**Figure 5. Adjacent channel power ratio 2 vs. output power**

## Evaluation Board Description

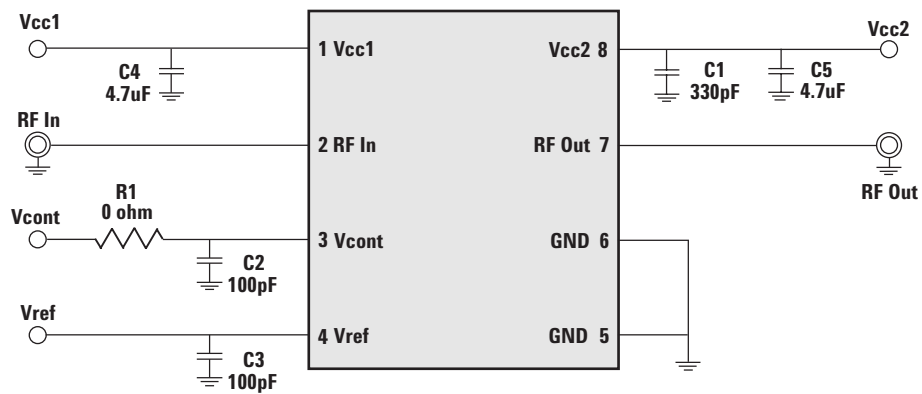


Figure 6. Evaluation board schematic

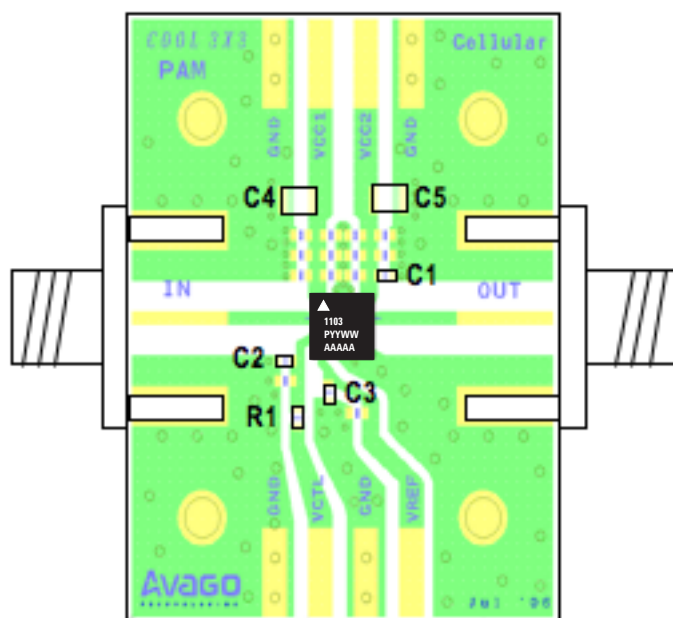


Figure 7. Evaluation board assembly diagram

Package Dimensions and Pin Descriptions

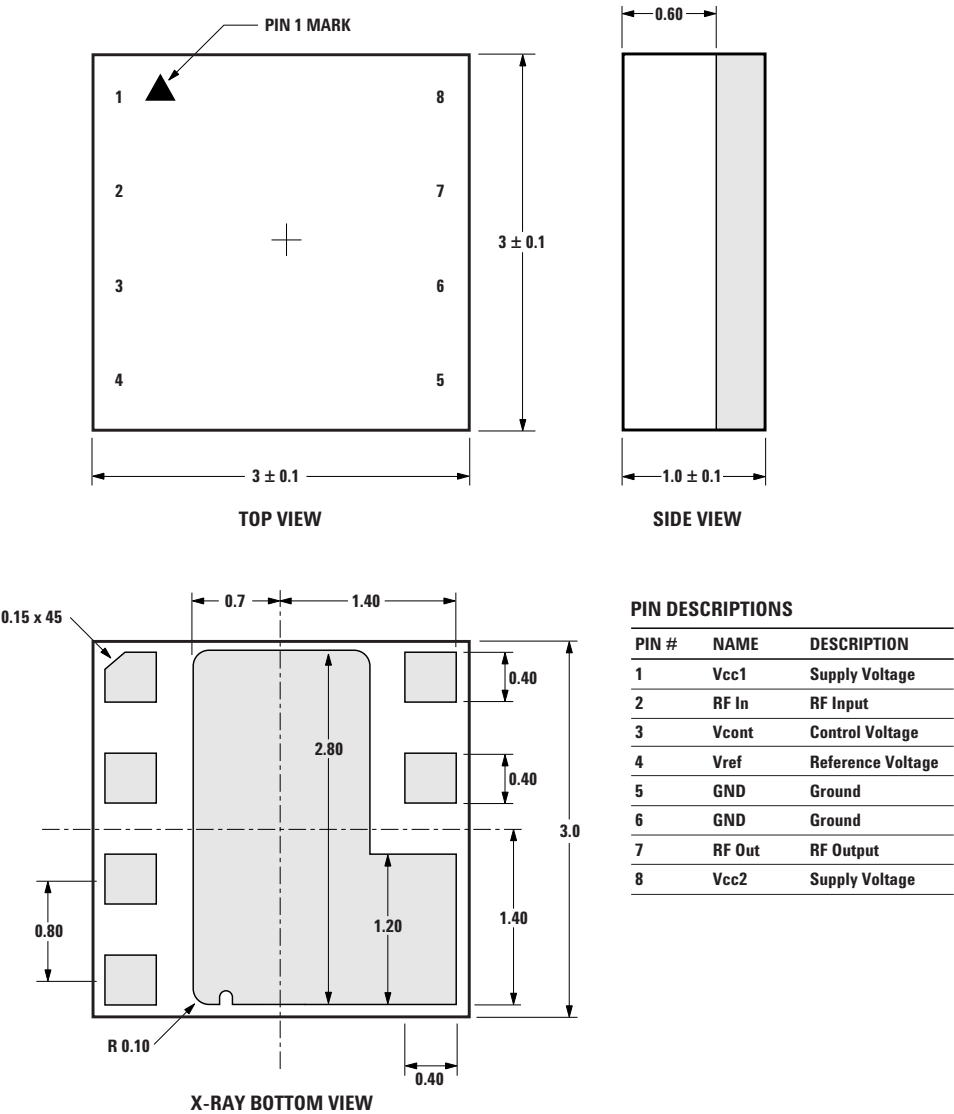


Figure 8. Package dimensional drawing and pin descriptions (all dimensions are in millimeters)

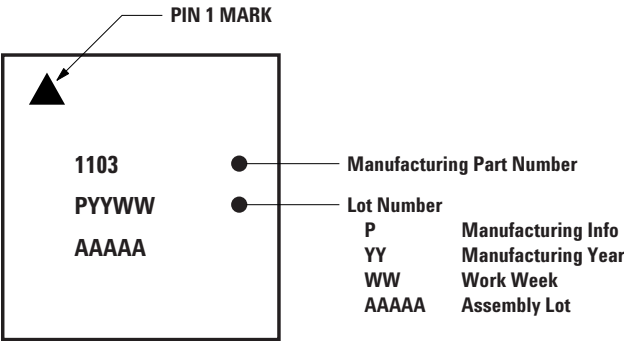
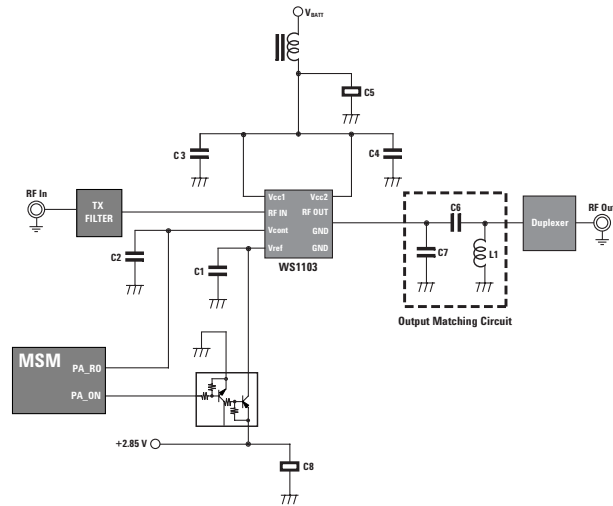


Figure 9. Marking specifications

## Peripheral Circuit in Handset



### Notes:

- Recommended voltage for Vref is 2.85 V.
- Place C1 near to Vref pin.
- Place C3 and C4 close to pin 1 (Vcc1) and pin 8 (Vcc2).  
These capacitors can affect the RF performance.
- Use 50  $\Omega$  transmission line between PAM and Duplexer and make it as short as possible to reduce conduction loss.
- $\pi$ -type circuit topology is good to use for matching circuit between PA and Duplexer.

Figure 10. Peripheral circuit

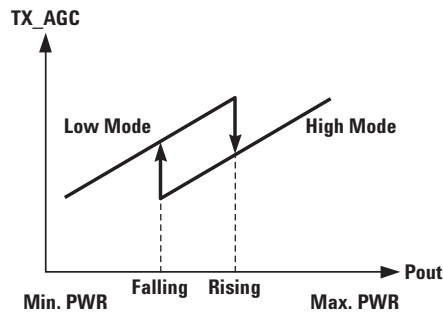


Figure 11. Calibration procedure

## Calibration

Calibration procedure is shown in Figure 11. Two calibration tables, high mode and low mode respectively, are required for Cool PAM, which is due to gain difference in each mode. For continuous output power at the mode change points, the input power should be adjusted according to gain step during the mode change.

### Offset Value (Difference between Rising Point and Falling Point)

Offset value, which is the difference between the rising point (output power where PA mode changes from low mode to high mode) and falling point (output power where PA mode changes from high mode to low mode), should be adopted to prevent system oscillation. 3 to 5 dB is recommended for hysteresis.

### Average Current & Talk Time

Probability Distribution Function implies that what is important for longer talk time is the efficiency of low or medium power range rather than the efficiency at full power. WS1103 idle current is 13 mA and operating current at 16 dBm is 65 mA at nominal condition. This PA with low current consumption prolongs talk time by no less than 30 minutes compared to other PAs.

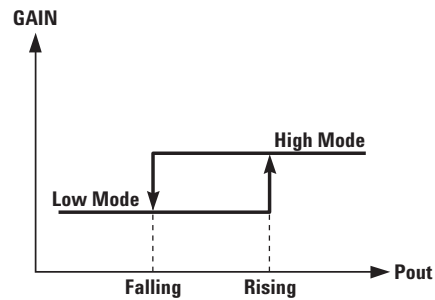


Figure 12. Setting of offset between rising and falling power

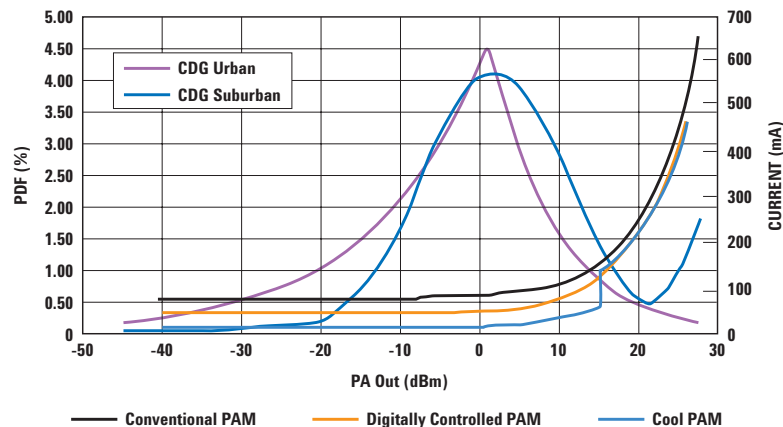


Figure 13. CDMA power distribution function

### PCB Design Guidelines

The recommended WS1403 PCB land pattern is shown in Figure 14 and Figure 15. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

### Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown in Figure 16. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100 mm (4 mils) or 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

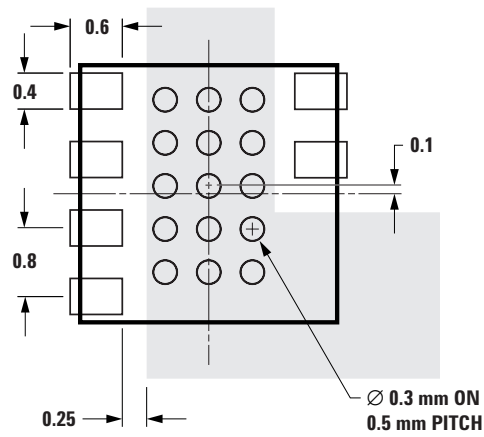


Figure 14. Metallization

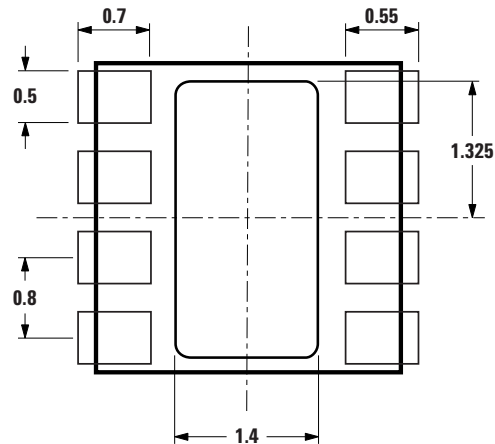


Figure 15. Solder mask opening

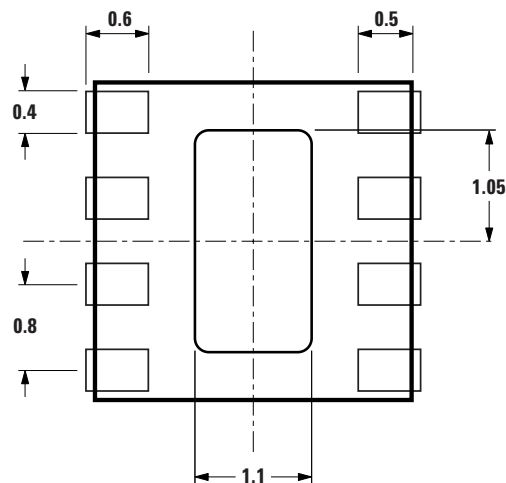
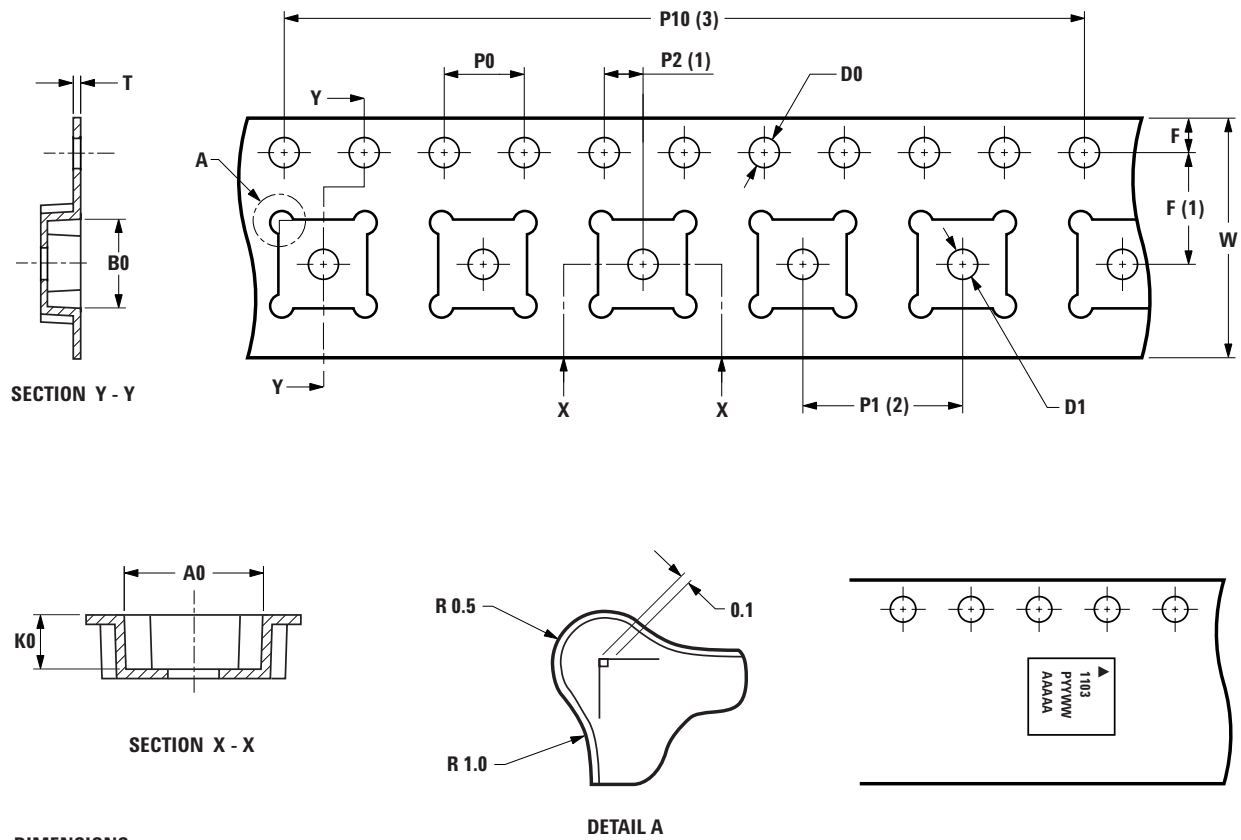


Figure 16. Solder paste stencil aperture



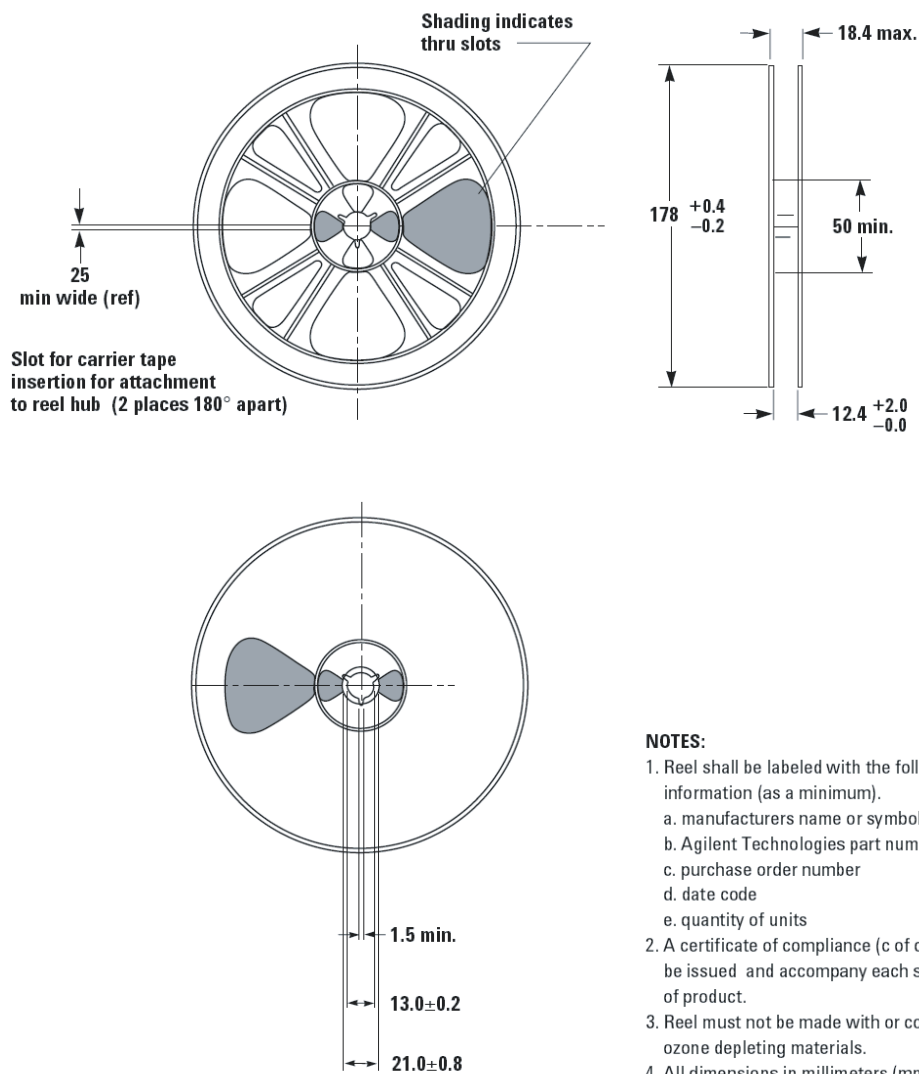
## Tape and Reel Information



DIMENSIONS	
NOTATION	MILLIMETERS
A0	$3.40 \pm 0.10$
B0	$3.40 \pm 0.10$
K0	$1.35 \pm 0.10$
D0	$1.55 \pm 0.05$
D1	$1.60 \pm 0.10$
P0	$4.00 \pm 0.10$
P1	$8.00 \pm 0.10$
P2	$2.00 \pm 0.05$
P10	$40.00 \pm 0.20$
E	$1.75 \pm 0.10$
F	$5.50 \pm 0.05$
W	$12.00 \pm 0.30$
T	$0.30 \pm 0.05$

Figure 17. Tape and reel format – 3 mm x 3 mm

## Reel Drawing



**Figure 18. Plastic reel format (all dimensions are in millimeters)**

## Handling and Storage

### ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

### MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for

moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS1103 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the WS1103 is targeted at 260°C +0/-5°C. Figure 19 and Table 7 show typical SMT profile for maximum temperature of 260 +0/-5°C.

**Table 5. ESD Classification**

Pin #	Name	Description	HBM	CDM	Classification
1	Vcc1	Supply Voltage	±2000 V	±200 V	Class 2
2	RFIn	RF Input	±2000 V	±200 V	Class 2
3	Vcont	Control Voltage	±2000 V	±200 V	Class 2
4	Vref	Reference Voltage	±2000 V	±200 V	Class 2
5	GND	Ground	±2000 V	±200 V	Class 2
6	GND	Ground	±2000 V	±200 V	Class 2
7	RF Out	RF Output	±2000 V	±200 V	Class 2
8	Vcc2	Supply Voltage	±2000 V	±200 V	Class 2

Note:

1. Module products should be considered extremely ESD sensitive.

**Table 6. Moisture Classification Level and Floor Life**

MSL Level	Floor Life (out of bag) at factory ambient = < 30°C/60% RH or as stated
1	Unlimited at = < 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note:

1. The MSL Level is marked on the MSL Label on each shipping bag.

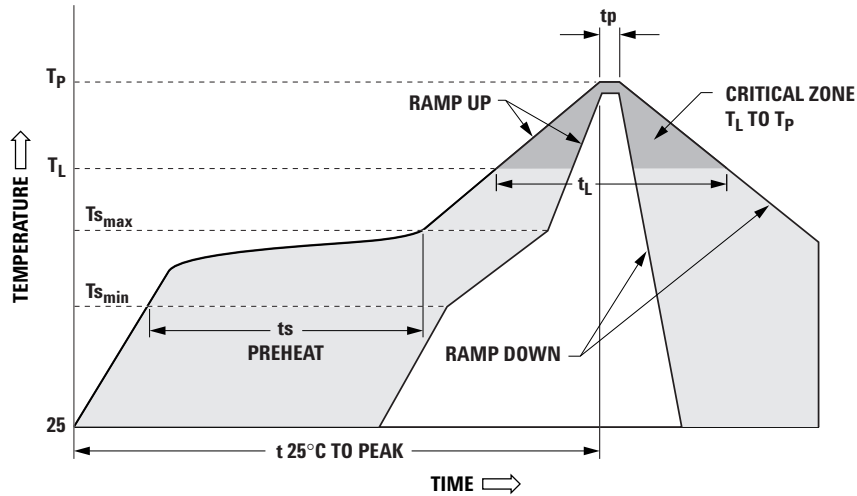


Figure 19. Typical SMT reflow profile for maximum temperature =  $260 \pm 5^\circ\text{C}$

Table 7. Typical SMT Reflow Profile for Maximum Temperature =  $260 \pm 5^\circ\text{C}$

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average Ramp-Up Rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat		
- Temperature Min (T <sub>smin</sub> )	100°C	150°C
- Temperature Max (T <sub>smax</sub> )	150°C	200°C
- Time (Min to Max) (ts)	60-120 sec	60-180 sec
T <sub>smax</sub> to TL		
- Ramp-Up Rate		3°C /sec max
Time Maintained Above:		
- Temperature (TL)	183°C	217°C
- Time (TL)	60-150 sec	60-150 sec
Peak Temperature (Tp)	240 $\pm 5^\circ\text{C}$	260 $\pm 5^\circ\text{C}$
Time Within 5°C of Actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-Down Rate	6°C /sec max	6°C /sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

## Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

## Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

## Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

## CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

## Board Rework

### Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

### Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

## Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

## Derating Due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 7. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table 8 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperatures, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 8:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity =  $0.121 \exp(-0.35\text{eV}/kT)$  mm<sup>2</sup>/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity =  $1.320 \exp(-0.35\text{eV}/kT)$  mm<sup>2</sup>/s (this used largest known Diffusivity @ 30°C).

**Table 8. Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C and 30°C for ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)**

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°C
		∞	∞	∞	78	53	42	36	14	10	8	25°C
		∞	∞	∞	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	2	3	20°C
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	27	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

For product information and a complete list of distributors, please go to our website: **[www.avagotech.com](http://www.avagotech.com)**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.  
Data subject to change. Copyright © 2005–2008 Avago Technologies. All rights reserved.  
AV02-0290EN - August 26, 2008

