ExpressLane PEX 8112-AA
PCI Express-to-PCI Bridge
Data Book

Version 1.2

October 2008

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Document Number: 8112-AA-SIL-DB-P1-1.2

Revision History

Version	Date	Description of Changes
1.0	October, 2007	Initial Production Data Book release, Silicon Revision AA. Added Section 19.6 - EEPROM and GPIO Specifications.
1.1	November, 2007	PCI Control Register (Offset 100Ch) in Forward Bridge Mode. Configuration Registers (Chapter 15): changed Bit 30 from Reserved to Short Discard Timer Timeout Select. Appendix A: Added Leaded package part number and description.
1.2	October, 2008	Chapter 2 – Clarified pull-up resistor information. Chapter 4, Section 4.1.1.1 – Revised PCIRST# assertion information. Chapter 5, Sections 5.1.1 and 5.2.1 – Revised the method for writing to Mailbox registers. Chapter 6, Section 6.1 – Revised listing of compatible serial EEPROMs. Chapters 15 and 16, register offset 42h[15:10] – Changed default value. Chapter 20 – Combined Table 20-1 and 20-2 into a single table (20-1), and renumbered all subsequent tables. Miscellaneous corrections and enhancements throughout data book.

Preface

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Scope

This data book describes the PEX 8112 bridge operation and provides operational data for customer use.

Audience

This data book provides the functional details of PLX Technology's ExpressLane PEX 8112-AA PCI Express-to-PCI Bridge, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the documents referenced below.

- PLX Technology, Inc. (PLX)

  870 W Maude Avenue, Sunnyvale, CA 94085 USA

  Tel: 800 759-3735 (domestic only) or 408 774-9060, Fax: 408 774-2169, www.plxtech.com

  The PLX PEX 8112 Toolbox includes this data book, as well as other PEX 8112 documentation, including the Errata and Schematic Design Checklist.

- PCI Special Interest Group (PCI-SIG)

  3855 SW 153rd Drive, Beaverton, OR 97006 USA

  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com

  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Local Bus Specification, Revision 2.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  - *PCI Bus Power Management Interface Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express Base Specification Errata, Revision 1.0a*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
  - *PCI Express Card Electromechanical Specification, Revision 1.0a*

- The Institute of Electrical and Electronics Engineers, Inc. (IEEE)

  445 Hoes Lane, Piscataway, NJ 08854-4141 USA

  Tel: 800 701-4333 (domestic only) or 732 981-0060, Fax: 732 981-9667, www.ieee.org

  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*

Supplemental Documentation Abbreviations

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI r2.2	*PCI Local Bus Specification, Revision 2.2*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Mgmt. r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PCI Express r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express r1.0a Errata	*PCI Express Base Specification Errata, Revision 1.0a*
PCI Express-to-PCI/PCI-X Bridge r1.0	*PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
PCI Express CEM r1.0a	*PCI Express Card Electromechanical Specification, Revision 1.0a*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*

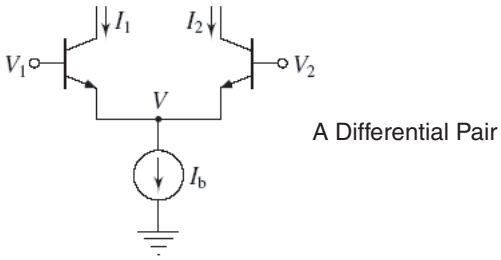
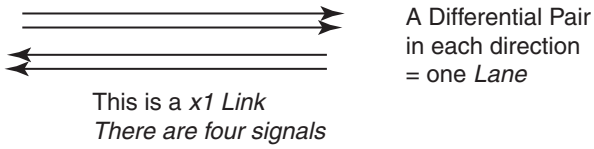
Data Assignment Conventions

Data Width	PEX 8112 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	DWORD/DWord/Dword

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express r1.0a* are not included in this table.

Terms and Abbreviations	Definition
#	Indicates an Active-Low signal.
ACK	Acknowledge Control Packet. Control packet used by a destination to acknowledge data packet receipt. Signal that acknowledges the signal receipt.
ADB	Allowable Disconnect Boundary.
ADQ	Allowable Disconnect Quantity. In PCI Express, the ADQ is a buffer size. Used to indicate memory requirements or reserves.
BAR	Base Address Register.
Byte	8-bit quantity of data.
CA	Completion with Completer Abort status.
CFG	Access initiated by PCI Configuration transactions on the primary bus.
Clock cycle	One period of the PCI Bus clock.
Completer	Device addressed by a *Requester*.
CRC	Cyclic Redundancy Check.
CRS	Configuration Retry Status.
CSR	Configuration Status register; Control and Status register; Command and Status register.
DAC	Dual Address cycle. A PCI transaction wherein a 64-bit address is transferred across a 32-bit data path in two Clock cycles.
Destination Bus	Target of a transaction that crosses a bridge is said to reside on the destination bus.
DLLP	Data Link Layer Packet (originates at the Data Link Layer); can contain Flow Control (FCx DLLPs) acknowledge packets (ACK and NAK DLLPs); and power management (PMx DLLPs).
Downstream	Transactions that are forwarded from the primary bus to the secondary bus of a bridge are said to be *flowing downstream*.
DWORD/DWord/Dword	Double-word. 32-bit quantity of data.
ECRC	End-to-end Cyclic Redundancy Check (CRC).
EE	Access initiated by the Serial EEPROM Controller during initialization.
Endpoints	Devices, other than the Root Complex and switches, that are Requesters or Completers of PCI Express transactions. • Endpoints can be PCI Express endpoints or Conventional PCI endpoints. • Conventional PCI endpoints can support I/O and Locked transaction semantics. PCI Express endpoints do not support I/O and Locked transaction semantics.
EP	Endpoint.
FC	Flow Control.
Field	Multiple register bits that are combined for a single function.
Forward Bridge mode	The primary bus is closest to the PCI Express Root Complex.

Terms and Abbreviations	Definition
Host	Computer that provides services to computers that connect to it on a network. Considered to be in charge of the other devices connected to the bus.
HwInit	Register bits are initialized by firmware or hardware mechanisms *such a*s ball strapping (on the BAR0ENB#, EXTARB, and FORWARD balls) or serial EEPROM. Bits are Read-Only after initialization and reset only with a Fundamental Reset.
I	CMOS Input.
I/O	CMOS Bidirectional Input Output.
JTAG	Joint Test Action Group.
Lane	Differential signal pair in each direction.
Layers	PCI Express defines three layers: • **Transaction Layer** – Provides assembly and disassembly of TLPs, the major components of which are Header, Data Payload, and an optional Digest field. • **Data Link Layer** – Provides link management and data integrity, including error detection and correction. Defines the data control for PCI Express. • **Physical Layer** – Appears to the upper layers as *PCI*. Connects the lower protocols to the upper layers.
Link	Physical connection between two devices that consists of x*N* ***lanes***. A x1 link consists of one Transmit and one Receive signal, where each signal is a differential pair. This is one lane. There are four lines or signals in a x1 link.  
LTSSM	Link Training and Status State Machine.
MM	Access initiated by PCI Memory transactions on the primary or secondary bus, using the address range defined by **PCI Base Address 0**.
MRL	Manually operated Retention Latch.
MSI	Message Signaled Interrupt.
NAK	Negative Acknowledge.
Non-Posted Transaction	A Memory Read, I/O Read or Write, or Configuration Read or Write that returns a Completion to the Master.
NS	No Snoop.

Terms and Abbreviations	Definition
O	CMOS Output.
OD	Open Drain Output.
Originating Bus	Master of a transaction that crosses a bridge is said to reside on the originating bus.
Packet Types	There are three packet types: • ***TLP***, Transaction Layer Packet • ***DLLP***, Data Link Layer Packet • ***PLP***, Physical Layer Packet
PCI	PCI Compliant.
PCI	Peripheral Component Interconnect. A PCI Bus is a high-performance bus that is 32 or 64 bits wide. It is designed to be used with devices that contain high-bandwidth requirements (*such as*, the display subsystem). PCI is an I/O Bus that has the ability to be dynamically configured.
PCI Master (Initiator)	Drives the Address phase and transaction boundary (FRAME#). Initiates a transaction and drives data handshaking (IRDY#) with the Target.
PCI Target	Claims the transaction by asserting DEVSEL# and handshakes the transaction (TRDY#) with the PCI Master.
PCI Transaction	Read, Write, Read Burst, or Write Burst operation on the PCI Bus. Includes an Address phase, followed by one or more Data phases.
PCI Transfer	During a transfer, data is moved from the source to the destination on the PCI Bus. TRDY# and IRDY# assertion indicates a Data transfer.
PEX	PCI Express.
PLL	Phase-Locked Loop.
PM	Power Management.
PME	Power Management Event.
Port	Interface between a PCI Express component and the link. Consists of Transmitters and Receivers. • An ***ingress*** port receives a packet. • An ***egress*** port transmits a packet.
Posted Transaction	Memory Write that does not return a Completion to the Master.
Primary Bus	Bus closest to the PCI Express Root Complex (Forward Bridge mode) or the PCI Host CPU (Reverse Bridge mode).
PU	Signal is internally pulled up.
QoS	Quality of Service.
RC	Root Complex.
RCB	Read Boundary Completion.
Request packet	A *Non-Posted Request packet* transmitted by a Requester has a Completion packet returned by the associated Completer. A *Posted Request packet* transmitted by a Requester has no Completion packet returned by the Completer.
Requester	Device that originates a transaction or puts a transaction sequence into the PCI Express fabric.
Reverse Bridge Mode	The primary bus is closest to the PCI Host CPU.

Terms and Abbreviations	Definition
RO	Read-Only register or register bit. Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8112 Hardware-Initialization mechanism or PEX 8112 Serial EEPROM register Initialization feature.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RsvdP	***Reserved* and Preserved.** ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve the value read, for writes to bits.
RsvdZ	***Reserved* and Zero.** ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.
RW	Read-Write register. Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	Read-Only Status. Write 1 to clear status register. Register bits indicate status when read; a set bit that is indicating a status event, is cleared by writing 1. Writing 0 to RW1C bits has no effect.
Rx	Receiver.
SC	Successful Completion.
Secondary Bus	The bus farthest from the PCI Express Root Complex (Forward Bridge mode) or the PCI Host CPU (Reverse Bridge mode).
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SPI	Serial Peripheral Interface.
STRAP	Strapping pads (*such as*, BAR0ENB#, FORWARD, and EXTARB) must be connected to H or L on the board.
STS	Sustained Tri-State Output, Driven High for One CLK before Float.
TC	Traffic Class.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
TP	Totem Pole.
TS	Tri-State Bidirectional.
Tx	Transmitter.
Upstream	Transactions that are forwarded from the secondary bus to the primary bus of a bridge are said to be *flowing upstream*.
UR	Unsupported Request.
VC	Virtual Channel.
WO	Write-Only register. Used to indicate that a register is written by the Serial EEPROM Controller.
Word	16-bit quantity of data.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
XXXn0 XXXp0	The lowercase “p” (positive) or “n” (negative) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a “#” appended to the term (*for example*, PERST#).
`Program/code samples`	`Monospace` font (program or code samples) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response K = 1,024 (2^{10}) is used for memory size references KB = 1,024 bytes M = meg = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to memory sizes (binary notation)
1Fh	h = suffix which identifies hex values. Each prefix term is equivalent to a 4-bit binary value (nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 or 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to “B” (*for example*, 4B = 4 bytes)
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	DWord (32 bits) is the primary register size in these devices.
Reserved	Do not modify ***reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.

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Registers

Forward Bridge Mode Configuration Registers

Reverse Bridge Mode Configuration Registers

Chapter 1 Introduction

1.1 Overview

PLX Technology's ExpressLane™ PEX 8112 PCI Express-to-PCI Bridge allows for the use of ubiquitous PCI silicon with the high-performance PCI Express Network. As PCI Express systems proliferate, there remain many applications that do not need the extensive bandwidth nor performance features of PCI Express. With the PEX 8112, many existing chips and entire subsystems can be used, without modification, with PCI Express motherboards.

1.1.1 PCI Express Endpoint Interface

- Full 2.5 Gbps per direction
- Single lane and single virtual channel operation
- Compatible with multi-lane and multi-virtual channel PCI Express chips
- Packetized serial traffic with PCI Express Split Completion protocol
- Data Link Layer Cyclic Redundancy Check (CRC) generator and checker
- Automatic Retry of bad packets
- Integrated low-voltage differential drivers
- 8b/10b signal encoding
- In-band interrupts and messages
- Message Signaled Interrupt (MSI) support

1.1.2 PCI Bus

- *PCI r3.0*-compliant 32-bit, 66 MHz PCI Bus
- PCI Master Controller allows PCI Express access to PCI Target devices
- PCI Target Controller
  - Allows full Transparent access to PCI Express resources
  - Allows Memory-Mapped access to shared RAM and Configuration registers
- Internal PCI Arbiter, supporting up to 4 external PCI Masters
- PM registers and PCI backplane PME# signal support
- Message Signaled Interrupts (MSI) support

1.1.3 Configuration Registers

- All internal registers are accessible from the PCI Express interface or PCI Bus
- All internal registers are set up through an external serial EEPROM
- Internal registers allow writes to and reads from an external serial EEPROM
- Internal registers allow control of GPIO balls

1.1.4 Data Transfer Pathways

- PCI Transparent bridge access to the PCI Express interface
- PCI Memory-Mapped Single access to internal Configuration registers
- PCI Memory-Mapped Single/Burst access to internal shared RAM
- Indexed Addressing Capability registers (offsets 84h and 88h)
- PCI Configuration access to PCI Configuration registers (Reverse Bridge mode only)
- PCI Express Transparent bridge access to PCI Bus Targets
- PCI Express Memory-Mapped Single access to internal Configuration registers
- PCI Express Memory-Mapped Single/Burst access to internal shared RAM
- PCI Express Configuration access to PCI Configuration registers (Forward Bridge mode only)

1.2 Block Diagrams

Figure 1-1. PEX 8112 Block Diagram

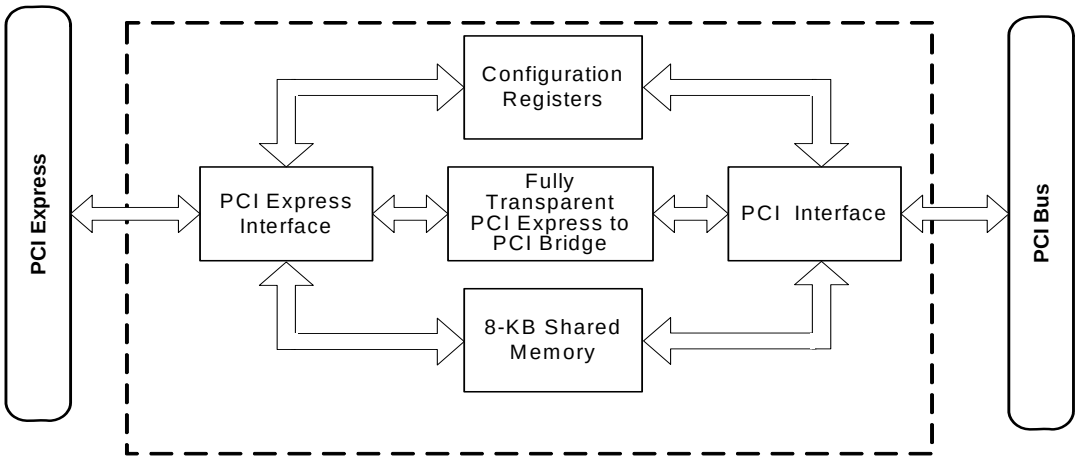


Figure 1-2. PEX 8112 Typical Forward Bridge Block Diagram

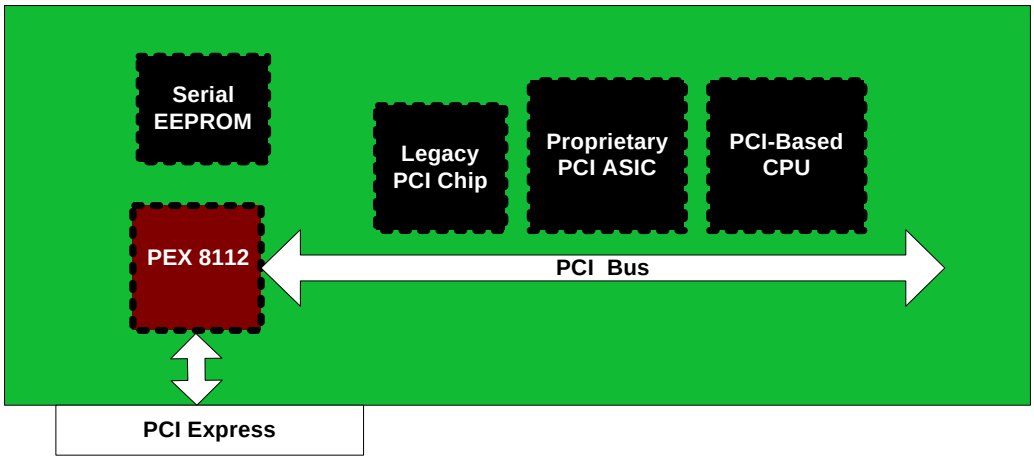
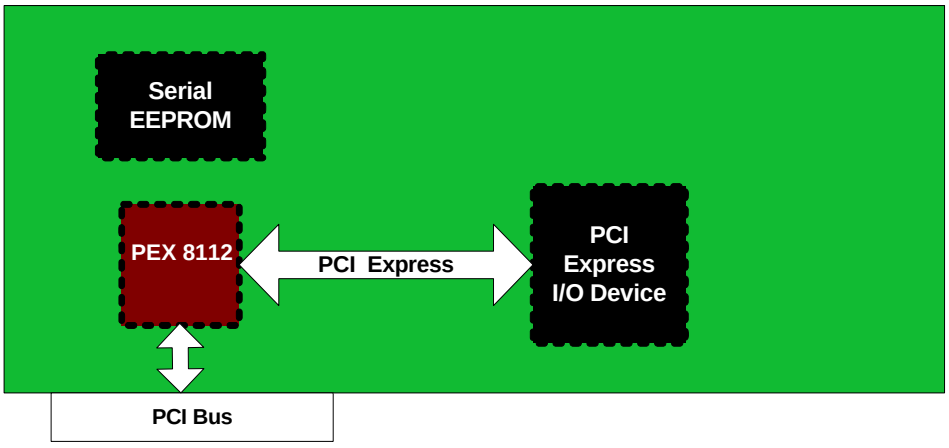


Figure 1-3. PEX 8112 Typical Reverse Bridge Block Diagram



1.3 Features

The PEX 8112 supports the following features:

- Forward and Reverse Transparent bridging between the PCI Express interface and PCI Bus
- PCI Express single-lane port (one Virtual Channel)
- PCI Express 2.5 Gbps per direction
- PCI Express full Split Completion protocol
- 32-bit, 66 MHz PCI Bus
- Internal PCI Arbiter, supporting up to 4 external PCI Masters
- Low power – 400 mW
- Serial Peripheral Interface (SPI) serial EEPROM port
- Internal 8-KB shared RAM available to the PCI Express interface and PCI Bus
- Four GPIO balls
- Low-power CMOS, in choice of two packages:
  - 144-ball, 13 x 13 mm^2 PBGA
  - 161-ball, 10 x 10 mm^2 FBGA
- 1.5V PCI Express interface operating voltage, 3.3V I/O, 5V tolerant PCI
- Power Management (PM)
  - Link PM states – L0, L0s, L1, L2 (Reverse Bridge mode only), L2/L3 Ready, and L3
  - PCI Bus Device PM states – D0 (D0_uninitialized and D0_active), D1, D2, and D3 (D3hot and D3cold)
- Maximum Payload Size – 128 bytes
- Lane polarity inversion
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1 (PCI-to-PCI Bridge r1.1)*
  - *PCI Bus Power Management Interface Specification, Revision 1.1 (PCI Power Mgmt. r1.1)*
  - *PCI Express Base Specification, Revision 1.0a (PCI Express r1.0a)*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 (PCI ExpressBridge r1.0)*
  - *PCI Express Card Electromechanical Specification, Revision 1.0a (PCI ExpressCard r1.0a*)

Chapter 2 Signal Ball Description

2.1 Introduction

This chapter provides descriptions of the PEX 8112 144-Ball PBGA and 161-Ball FBGA signal balls. The signals are divided into the groups listed in Table 2-1.

The signal name, type, location, and a brief description are provided for each signal ball, by package type. A list of signals by location and signal order, and a map of the PEX 8112's physical layout, are also provided.

Note: *If there is more than one ball per signal name, the ball numbers are ordered, in sequence, to follow signal name sequencing [n to 0].*

Table 2-1. PEX 8112 Signal Balls

144-Ball PBGA	161-Ball FBGA
• PCI Express Signals	• PCI Express Signals
• PCI Signals	• PCI Signals
• Clock, Reset, and Miscellaneous Signals	• Clock, Reset, and Miscellaneous Signals
• JTAG Interface Signals	• JTAG Interface Signals
• Test Signals	• Test Signals
• Power and Ground Signals	• No Connect Signals
	• Power and Ground Signals

2.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 2-2. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
DIFF	PCI Express Differential buffer
I	Input
I/O	Bidirectional (Input or Output)
O	Output
OD	Open Drain Output
PCI	PCI-Compatible buffer, 26-mA drive
PU	Weak (50KΩ) internal pull-up resistor
S	Schmitt Trigger
STS	Sustained Tri-State, driven High one Clock cycle before float
TP	Totem Pole
TS	Tri-State

2.3 Internal Pull-Up Resistors

2.3.1 Internal Pull-Up Resistors – Forward and Reverse Bridge Modes

The signals listed below have a weak internal 50KΩ pull-up resistor. However, if a signal with this notation is not used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace, the internal resistors might not be strong enough to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled High to VDD3.3 or Low to GND, as appropriate, through a 3KΩ to 10KΩ resistor.

- BAR0ENB#
- FORWARD
- GPIO[3:0]
- TDI
- TMS
- TRST#

2.3.2 PCI Signal Pull-Up Resistors – Forward Bridge Mode Only

The PCI balls discussed in this chapter are generic primary and secondary PCI Bus balls that do not have internal resistors. When designing motherboards, system slot boards, adapter boards, backplanes, and so forth, the termination of these balls must follow the guidelines detailed in the *PCI r3.0*. The following guidelines are not exhaustive and should be read in conjunction with the appropriate *PCI r3.0* sections.

PCI Control signals require a pull-up resistor on the motherboard, to ensure that these signals are always at valid values when a PCI Bus agent is not driving the bus. For a 32-bit PCI Bus, these Control signals include the following:

- DEVSEL#
- FRAME#
- INT[D:A]#
- IRDY#
- PERR#
- SERR#
- STOP#
- TRDY#

The INT[D:A]# balls require pull-up resistors, regardless of whether they are used.

Depending upon the application, M66EN can also require a pull-up resistor. The value of these pull-up resistors depends upon the bus loading. The *PCI r3.0* provides formulas for calculating the resistor values. When making adapter board devices where the PEX 8112 port is wired to the PCI connector, pull-up resistors are not required because they are pre-installed on the motherboard. Based upon the above, in an embedded design, pull-up resistors can be required for PCI Control signals on the bus.

2.4 Signal Ball Descriptions – 144-Ball PBGA

2.4.1 PCI Express Signals

Table 2-3. PCI Express Signals – 9 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
PERn0	I DIFF	B7	**Receive Minus** PCI Express Differential Receive signal.
PERp0	I DIFF	A8	**Receive Plus** PCI Express Differential Receive signal.
PERST#	I/O 6 mA 3.3V	B12	**PCI Express Reset** In Forward Bridge mode, PERST# is an input. Resets the entire PEX 8112 when asserted. In Reverse Bridge mode, PERST# is an output. Asserted when a PCI reset is detected.
PETn0	O DIFF	A4	**Transmit Minus** PCI Express Differential Transmit signal.
PETp0	O DIFF	B5	**Transmit Plus** PCI Express Differential Transmit signal.
REFCLK-	I DIFF	B6	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. In Forward Bridge mode, connected to the PCI Express interface REFCLK- ball. In Reverse Bridge mode, connected to an external differential clock driver.
REFCLK+	I DIFF	A6	**PCI Express Clock Input Plus** PCI Express differential, 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. In Forward Bridge mode, connected to the PCI Express interface REFCLK+ ball. In Reverse Bridge mode, connected to an external differential clock driver.
WAKEIN#	I 3.3V	C12	**Wake In Signal** In Forward Bridge mode, pull WAKEIN# High. In Reverse Bridge mode, WAKEIN# is an input, and indicates that the PCI Express Device requested a wakeup while the link remains in the L2 Link PM state.
WAKEOUT#	OD 6 mA 3.3V	A9	**Wake Out Signal** In Forward Bridge mode, WAKEOUT# is an Open Drain output, which is asserted when PMEIN# is asserted and the link remains in the L2 Link PM state.

2.4.2 PCI Signals

Table 2-4. PCI Signals – 63 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
AD[31:0]	I/O TS PCI	J10, J12, J11, K12, L9, M9, K8, L8, K7, L7, M7, J6, K6, M6, L6, J5, H2, H1, G3, G2, G1, F4, F3, F2, E4, E3, E2, E1, D2, D1, C1, D3	**Address/Data Bus (32 Balls)** The PCI address and data are multiplexed onto the same bus. During the Address phase, AD[31:0] contain the physical address of the transfer. During the Data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and Read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M8, K5, H3, F1	**Command/Byte Enable Bus (4 Balls)** The Bus command and Byte Enables are multiplexed onto the same bus. During the Address phase, CBE[3:0]# contain the Bus command. During the Data phase, CBE[3:0]# contain the Byte Enables. CBE0# corresponds to Byte 0 (AD[7:0]), and CBE3# corresponds to Byte 3 (AD[31:24]). 0000b = Interrupt Acknowledge 0001b = Special cycle 0010b = I/O Read 0011b = I/O Write 0110b = Memory Read 0111b = Memory Write 1010b = Configuration Read 1011b = Configuration Write 1100b = Memory Read Multiple 1101b = Dual Address Cycle 1110b = Memory Read Line 1111b = Memory Write and Invalidate All other encodings are ***reserved***.
DEVSEL#	I/O STS PCI	K4	**Device Select** Indicates that the Target (Bus Slave) decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus was selected.
FRAME#	I/O STS PCI	M5	**Frame** Driven by the PCI Master. Indicates access start and duration. When FRAME# is first asserted, the Address phase is indicated. When FRAME# is de-asserted, the transaction remains in the last Data phase.
GNT[3:0]#	I/O TS PCI	E11, F11, G9, G10	**Bus Grant (4 Balls)** Indicates that the Central Arbiter granted the bus to an agent. When the Internal PCI Arbiter is enabled, GNT[3:0]# are outputs used to grant the bus to external devices. When the Internal PCI Arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8112, and GNT[3:1]# are placed into a high-impedance state.
IDSEL	I PCI	K9	**Initialization Device Select** Valid only in Reverse Bridge mode. Used as a Chip Select during Configuration Read and Write cycles. Each PCI slot or device typically has an IDSEL connected to a signal address line, allowing the PCI Host to select individual sets of Configuration registers. In Forward Bridge mode, it is recommended to ground IDSEL, to prevent the signal from floating.

Table 2-4. PCI Signals – 63 Balls (144-Ball PBGA) *(Cont.)*

Signal	Type	Balls	Description
INTA# INTB# INTC# INTD#	I/O OD PCI	E12 E9 D11 E10	**Interrupt (4 Balls)** Asserted to request an interrupt. After assertion, must remain asserted until the device driver clears it. INT*x*# is level-sensitive and asynchronous to the CLK. In Forward Bridge mode, INT*x*# is an input from PCI devices. All INT*x*# signals are mapped into Assert_INT*x* and Deassert_INT*x* messages on the PCI Express interface. INT*x*# inputs must be pulled up externally. In Reverse Bridge mode, INTI# is an output to the PCI Central Resource Function. All Assert_INT*x* and Deassert_INT*x* PCI Express messages are translated to INT*x*# transitions on the PCI Bus.
IRDY#	I/O STS PCI	L5	**Initiator Ready** Indicates that the Initiator (PCI Master) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	M3	**Lock Atomic Operation** Indicates an atomic operation to a bridge that might require multiple transactions to complete. In Forward Bridge mode, LOCK# is an output. In Reverse Bridge mode, LOCK# is an input.
M66EN	I PCI	D10	**66 MHz Enable** Indicates whether the PCI Bus is operating at 33 or 66 MHz. When Low, and the PCLKO divisor value in the **Device Initialization** register *PCLKO Clock Frequency* field is set to 0011b, the PCLKO ball oscillates at 33 MHz, with a 50% Duty cycle. When High, and the PCLKO divisor value in the **Device Initialization** register *PCLKO Clock Frequency* field is set to 0011b, the PCLKO ball oscillates at 66 MHz, with a 33% to 60% Duty cycle, if the PCLKO62SEL# ball is pulled High or left disconnected. If the PCLKO62SEL# ball is pulled Low, the PCLKO ball is a low-jitter 62.5 MHz, with a 50% Duty cycle. Read M66EN, using the **PCI Control** register *M66EN* bit. M66EN must be grounded in 33 MHz systems.
PAR	I/O TS PCI	J1	**Parity** Even parity is generated across AD[31:0], and CBE[3:0]# [*that is*, the number of ones (1) on AD[31:0], CBE[3:0]#, and PAR is an even number]. PAR is valid one clock after the Address phase. For Data phases, PAR is valid one clock after IRDY# is asserted on Write cycles, and one clock after TRDY# is asserted on Read cycles. PAR has the same timing as AD[31:0], except it is delayed by one Clock cycle. The PCI Master drives PAR for Address and Write Data phases, and the Target drives PAR for Read Data phases.
PCIRST#	I/O TP PCI	F10	**PCI Reset** Asserted and de-asserted asynchronously to CLK, and used to bring a PCI device to an initial state. In Forward Bridge mode, PCIRST# is driven when a PCI Express reset is detected, or when the **Bridge Control** register *Secondary Bus Reset* bit is set. In Reverse Bridge mode, PCIRST# is an input that resets the entire PEX 8112. All PCI signals are asynchronously placed into a high-impedance state during reset.
PCLKI	I PCI	D12	**PCI Clock Input** All PCI signals, except RST# and interrupts, are sampled on the rising edge of PCLKI. The PCLKI frequency varies from 0 to 66 MHz, and it must oscillate during the serial EEPROM initialization sequence.

Table 2-4. PCI Signals – 63 Balls (144-Ball PBGA) *(Cont.)*

Signal	Type	Balls	Description
PERR#	I/O STS PCI	J3	**Parity Error** Indicates that a Data Parity error occurred. Driven active by the receiving agent two clocks following the data that contained bad parity.
PMEIN#	I S PCI	H12	**Power Management Event In** Valid only in Forward Bridge mode. Input used to monitor requests to change the system's Power state.
PMEOUT#	OD 24 mA 3.3V	L12	**Power Management Event Out** Valid only in Reverse Bridge mode. Open Drain output used to request a change in the Power state. PMEOUT# is ***not*** 5V tolerant. When used in systems with a 5V pull-up resistor on the PCI backplane PME# signal, an external voltage translation circuit is required.
REQ[3:0]#	I/O TS PCI	H11, G12, H9, G11	**Bus Request (4 Balls)** Indicates that an agent requires use of the bus. When the Internal PCI Arbiter is enabled, REQ[3:0]# are inputs used to service external bus requests. When the Internal PCI Arbiter is disabled, REQ0# is an output used to request bus control, and REQ[3:1]# are unused inputs.
SERR#	I/O OD PCI	J2	**System Error** Indicates that an Address Parity error, Data Parity error on the special cycle command, or other catastrophic error occurred. Driven active for one PCI clock period, and is synchronous to the CLK. Driven only in Reverse Bridge mode.
STOP#	I/O STS PCI	L4	**Stop** Indicates that the Target (bus slave) is requesting that the Master stop the current transaction. After STOP# is asserted, STOP# must remain asserted until FRAME# is de-asserted, whereupon STOP# must be de-asserted. Also, DEVSEL# and TRDY# cannot be changed until the current Data phase completes. STOP# must be de-asserted in the clock following the completion of the last Data phase, and must be placed into a high-impedance state in the next clock. Data is transferred when both IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI	M4	**Target Ready** Indicates that the Target (bus slave) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.

2.4.3 Clock, Reset, and Miscellaneous Signals

Table 2-5. Clock, Reset, and Miscellaneous Signals – 14 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	E8	**PCI Base Address 0 Register Enable** When Low, the **PCI Base Address 0** register (**BAR0**) is enabled. When High, the **PCI Base Address 0** register (**BAR0**) is enabled by the **Device-Specific Control** register *PCI Base Address 0 Enable* bit.
EECLK	O 3 mA TP 3.3V	B2	**Serial EEPROM Clock** Provides the clock to the serial EEPROM. Frequency is determined by the **Serial EEPROM Clock Frequency** register, and varies from 2 to 25 MHz.
EECS#	O 3 mA TP 3.3V	C4	**Serial EEPROM Chip Select** Active-Low Chip Select.
EERDDATA	I 3.3V	A1	**Serial EEPROM Read Data** Used to read data from the EEPROM. A 47KΩ pull-up resistor is required.
EEWRDATA	O 3 mA TP 3.3V	A2	**Serial EEPROM Write Data** Used to write data to the EEPROM.
EXTARB	I 3.3V	K11	**External Arbiter Enable** When Low, the Internal PCI Arbiter services requests from an external PCI device. When High, the PEX 8112 requests the PCI Bus from an External Arbiter.
FORWARD	I 3.3V PU	L11	**Bridge Select** When Low, the PEX 8112 acts as a PCI-to-PCI Express Bridge (Reverse Bridge). When High, the PEX 8112 acts as a PCI Express-to-PCI Bridge (Forward Bridge).
GPIO[3:0]	I/O 12 mA 3.3V PU	A11, B10, A10, C9	**General Purpose I/O (4 Balls)** Program as an Input or Output general-purpose ball. Internal device status is also an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **General-Purpose I/O Control** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is Low at the trailing edge of *reset*, the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. For Forward Bridge mode, *reset* is PERST#. For Reverse Bridge mode, *reset* is PCIRST#.

Table 2-5. Clock, Reset, and Miscellaneous Signals – 14 Balls (144-Ball PBGA) *(Cont.)*

<table>
<tr><th>Signal</th><th>Type</th><th>Balls</th><th>Description</th></tr>
<tr><td>PCLKO</td><td>O
26 mA
TP
PCI</td><td>H10</td><td>
PCI Clock Output
Buffered clock output, whose output frequency reference is selected by the values of the M66EN and PCLKO62SEL# Input balls, and the Device Initialization register PCLKO Clock Frequency field value. By default, the PCLKO Clock Frequency field is initialized to 0011b.
<table>
<tr><th>M66EN</th><th>PCLKO62SEL#</th><th>Clock Frequency</th><th>PCLKO</th><th>Duty Cycle</th></tr>
<tr><td>0</td><td>X</td><td>Any</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>1</td><td>Not 011b</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>1</td><td>011b</td><td>66 MHz</td><td>33%</td></tr>
<tr><td>1</td><td>0</td><td>Not 011b</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>0</td><td>011b</td><td>62.5 MHz</td><td>50%</td></tr>
</table>
Note: X is “Don’t Care.”

PCLKO is always driven and oscillates when all the following occur:

PCI Express REFCLK-/+ input balls are active
PCLKO Clock Frequency field is a non-zero value
PERST# (Forward Bridge mode) or PCIRST# (Reverse Bridge mode) is de-asserted

PCLKO can be connected to PCLKI as a source for the PCI input clock.
PCLKO is derived from the REFCLK-/+ inputs. As long as REFCLK-/+ is active, PCLKO is driven only when PERST# (Forward Bridge mode) or PCIRST# (Reverse Bridge mode) is de-asserted.
</td></tr>
<tr><td>PCLKO62SEL#</td><td>I
3.3V</td><td>C2</td><td>
PCI Clock Output 62.5 MHz Select
When pulled Low with M66EN High, causes the PCLKO clock to be derived from an internal low-jitter Phase-Locked Loop (PLL). PCLKO is 62.5 MHz, with a 50% Duty cycle. This provides an option for a low-jitter clock in situations where the REFCLK-/+ inputs can have jitter, which when used as a Reference Clock, would cause too much jitter on the output.
</td></tr>
<tr><td>PWR_OK</td><td>O
6 mA
3.3V</td><td>B9</td><td>
Power OK
Valid only in Forward Bridge mode. When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the Power register, PWR_OK is asserted.
</td></tr>
</table>

2.4.4 JTAG Interface Signals

Note: *The JTAG interface is described in Section 18.1, "JTAG Interface."*

Table 2-6. JTAG Interface Signals – 5 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
TCK	I	M2	**Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 10 MHz.
TDI	I PU	L3	**Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
TDO	O 12 mA 3.3V TS	L1	**Test Data Output** Serial output to the JTAG TAP Controller test instructions and data.
TMS	I PU	M12	**Test Mode Select** When High, JTAG Test mode is enabled. Input decoded by the JTAG TAP Controller, to control test operations.
TRST#	I PU	L10	**Test Reset** Active-Low input used to reset the Test Access Port. Tie to ground through a 1.5KΩ resistor, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation. When JTAG functionality is not used, the TRST# input should be pulled or driven Low, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's Instruction register to contain the *IDCODE* instruction, or by holding the TMS input High for at least five rising edges of the TCK input.

2.4.5 Test Signals

Table 2-7. Test Signals – 7 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
BTON	I	M11	**Test Enable** Connect to Ground for standard operation.
BUNRI	I	D8	**Test Mode Select** Connect to Ground for standard operation.
SMC	I	K1	**Scan Path Mode Control** Connect to Ground for standard operation.
TEST	I	A3	**Test Mode Select** Connect to Ground for standard operation.
TMC	I	C8	**Test Mode Control** Connect to Ground for standard operation.
TMC1	I	B1	**IDDQ Test Control Input** Connect to Ground for standard operation.
TMC2	I	M1	**I/O Buffer Control** Connect to Ground for standard operation.

2.4.6 Power and Ground Signals

Table 2-8. Power and Ground Signals – 46 Balls (144-Ball PBGA)

Signal	Type	Balls	Description
AVDD	Power	E7	**Analog Supply Voltage** Connect AVDD to the +1.5V power supply.
AVSS	Ground	C7	**Analog Ground** Connect AVSS to ground.
GND	Ground	A12, B4, C3, C11, D9, E6, F12, G5, H4, H7, J4, J8, K2, K10	**Ground (14 Balls)** Connect GND to ground.
VDD_P	Power	D5	**PLL Supply Voltage** Connect VDD_P to the +1.5V filtered PLL power supply.
VDD_R	Power	A7	**Receiver Supply Voltage** Connect VDD_R to the +1.5V power supply.
VDD_T	Power	A5	**Transmitter Supply Voltage** Connect VDD_T to the +1.5V power supply.
VDD1.5	Power	C10, D4, F6, F8, G6, G7, J9, K3	**PCI Express Interface Supply Voltage (8 Balls)** Connect VDD1.5 to the +1.5V power supply.
VDD3.3	Power	B3, B11, L2, M10	**I/O Supply Voltage (4 Balls)** Connect VDD3.3 to the +3.3V power supply.
VDD5	Power	F5, G8, H6	**PCI I/O Clamp Voltage (3 Balls)** Connect VDD5 to the +5.0V power supply for PCI buffers. In a 3.3V PCI environment, connect VDD5 to the 3.3V power supply.
VDDQ	Power	E5, F9, G4, H5, H8, J7	**I/O Supply Voltage (6 Balls)** Connect VDDQ to the +3.3V power supply for PCI buffers.
VSS_C	Ground	D7	**Common Ground** Connect VSS_C to ground.
VSS_P0	Ground	D6	**PLL Ground** Connect VSS_P0 to ground.
VSS_P1	Ground	C6	**PLL Ground** Connect VSS_P1 to ground.
VSS_R	Ground	B8	**Receiver Ground** Connect VSS_R to ground.
VSS_RE	Ground	F7	**Receiver Ground** Connect VSS_RE to ground.
VSS_T	Ground	C5	**Transmitter Ground** Connect VSS_T to ground.

2.4.7 Ball Assignments by Location and Signal Name – 144-Ball PBGA

Table 2-9. Ball Assignments by Location (144-Ball PBGA)

Location	Signal	Location	Signal	Location	Signal	Location	Signal
A1	EERDDATA	D1	AD2	G1	AD11	K1	SMC
A2	EEWRDATA	D2	AD3	G2	AD12	K2	GND
A3	TEST	D3	AD0	G3	AD13	K3	VDD1.5
A4	PETn0	D4	VDD1.5	G4	VDDQ	K4	DEVSEL#
A5	VDD_T	D5	VDD_P	G5	GND	K5	CBE2#
A6	REFCLK+	D6	VSS_P0	G6	VDD1.5	K6	AD19
A7	VDD_R	D7	VSS_C	G7		K7	AD23
A8	PERp0	D8	BUNRI	G8	VDD5	K8	AD25
A9	WAKEOUT#	D9	GND	G9	GNT1#	K9	IDSEL
A10	GPIO1	D10	M66EN	G10	GNT0#	K10	GND
A11	GPIO3	D11	INTC#	G11	REQ0#	K11	EXTARB
A12	GND	D12	PCLKI	G12	REQ2#	K12	AD28
B1	TMC1	E1	AD4	H1	AD14	L1	TDO
B2	EECLK	E2	AD5	H2	AD15	L2	VDD3.3
B3	VDD3.3	E3	AD6	H3	CBE1#	L3	TDI
B4	GND	E4	AD7	H4	GND	L4	STOP#
B5	PETp0	E5	VDDQ	H5	VDDQ	L5	IRDY#
B6	REFCLK-	E6	GND	H6	VDD5	L6	AD17
B7	PERn0	E7	AVDD	H7	GND	L7	AD22
B8	VSS_R	E8	BAR0ENB#	H8	VDDQ	L8	AD24
B9	PWR_OK	E9	INTB#	H9	REQ1#	L9	AD27
B10	GPIO2	E10	INTD#	H10	PCLKO	L10	TRST#
B11	VDD3.3	E11	GNT3#	H11	REQ3#	L11	FORWARD
B12	PERST#	E12	INTA#	H12	PMEIN#	L12	PMEOUT#
C1	AD1	F1	CBE0#	J1	PAR	M1	TMC2
C2	PCLKO62SEL#	F2	AD8	J2	SERR#	M2	TCK
C3	GND	F3	AD9	J3	PERR#	M3	LOCK#
C4	EECS#	F4	AD10	J4	GND	M4	TRDY#
C5	VSS_T	F5	VDD5	J5	AD16	M5	FRAME#
C6	VSS_P1	F6	VDD1.5	J6	AD20	M6	AD18
C7	AVSS	F7	VSS_RE	J7	VDDQ	M7	AD21
C8	TMC	F8	VDD1.5	J8	GND	M8	CBE3#
C9	GPIO0	F9	VDDQ	J9	VDD1.5	M9	AD26
C10	VDD1.5	F10	PCIRST#	J10	AD31	M10	VDD3.3
C11	GND	F11	GNT2#	J11	AD29	M11	BTON
C12	WAKEIN#	F12	GND	J12	AD30	M12	TMS

Table 2-10. Ball Assignments by Signal Name (144-Ball PBGA)

Signal	Location	Signal	Location	Signal	Location	Signal	Location
AD0	D3	CBE0#	F1	INTB#	E9	TMC2	M1
AD1	C1	CBE1#	H3	INTC#	D11	TMS	M12
AD2	D1	CBE2#	K5	INTD#	E10	TRDY#	M4
AD3	D2	CBE3#	M8	IRDY#	L5	TRST#	L10
AD4	E1	DEVSEL#	K4	LOCK#	M3	VDD_P	D5
AD5	E2	EECLK	B2	PCLKO62SEL#	C2	VDD_R	A7
AD6	E3	EECS#	C4	M66EN	D10	VDD_T	A5
AD7	E4	EERDDATA	A1	BAR0ENB#	E8	VDD1.5	C10
AD8	F2	EEWRDATA	A2	PAR	J1		D4
AD9	F3	EXTARB	K11	PCIRST#	F10		F6
AD10	F4	FORWARD	L11	PCLKI	D12		F8
AD11	G1	FRAME#	M5	PCLKO	H10		G6
AD12	G2	GND	A12	PERn0	B7		G7
AD13	G3		B4	PERp0	A8		J9
AD14	H1		C3	PERR#	J3		K3
AD15	H2		C11	PERST#	B12	VDD3.3	B3
AD16	J5		D9	PETn0	A4		B11
AD17	L6		E6	PETp0	B5		L2
AD18	M6		F12	PMEIN#	H12		M10
AD19	K6		G5	PMEOUT#	L12	VDD5	F5
AD20	J6		H4	PWR_OK	B9		G8
AD21	M7		H7	REFCLK-	B6		H6
AD22	L7		J4	REFCLK+	A6	VDDQ	E5
AD23	K7		J8	REQ0#	G11		F9
AD24	L8		K2	REQ1#	H9		G4
AD25	K8		K10	REQ2#	G12		H5
AD26	M9	GNT0#	G10	REQ3#	H11		H8
AD27	L9	GNT1#	G9	SERR#	J2		J7
AD28	K12	GNT2#	F11	SMC	K1	VSS_C	D7
AD29	J11	GNT3#	E11	STOP#	L4	VSS_P0	D6
AD30	J12	GPIO0	C9	TCK	M2	VSS_P1	C6
AD31	J10	GPIO1	A10	TDI	L3	VSS_R	B8
AVDD	E7	GPIO2	B10	TDO	L1	VSS_RE	F7
AVSS	C7	GPIO3	A11	TEST	A3	VSS_T	C5
BTON	M11	IDSEL	K9	TMC	C8	WAKEIN#	C12
BUNRI	D8	INTA#	E12	TMC1	B1	WAKEOUT#	A9

2.4.8 Physical Layout – 144-Ball PBGA

Figure 2-1. 144-Ball PBGA Physical Layout (Underside View)

M	L	K	J	H	G	F	E	D	C	B	A	
TMS	PMEOUT#	AD28	AD30	PMEIN#	REQ2#	GND	INTA#	PCLKI	WAKEIN#	PERST#	GND	12
BTON	FORWARD	EXTARB	AD29	REQ3#	REQ0#	GNT2#	GNT3#	INTC#	GND	VDD3.3	GPIO3	11
VDD3.3	TRST#	GND	AD31	PCLKO	GNT0#	PCIRST#	INTD#	M66EN	VDD1.5	GPIO2	GPIO1	10
AD26	AD27	IDSEL	VDD1.5	REQ1#	GNT1#	VDDQ	INTB#	GND	GPIO0	PWR_OK	WAKEOUT#	9
CBE3#	AD24	AD25	GND	VDDQ	VDD5	VDD1.5	BAR0ENB#	BUNRI	TMC	VSS_R	PERp0	8
AD21	AD22	AD23	VDDQ	GND	VDD1.5	VSS_RE	AVDD	VSS_C	AVSS	PERn0	VDD_R	7
AD18	AD17	AD19	AD20	VDD5	VDD1.5	VDD1.5	GND	VSS_P0	VSS_P1	REFCLK-	REFCLK+	6
FRAME#	IRDY#	CBE2#	AD16	VDDQ	GND	VDD5	VDDQ	VDD_P	VSS_T	PETp0	VDD_T	5
TRDY#	STOP#	DEVSEL#	GND	GND	VDDQ	AD10	AD7	VDD1.5	EECS#	GND	PETn0	4
LOCK#	TDI	VDD1.5	PERR#	CBE1#	AD13	AD9	AD6	AD0	GND	VDD3.3	TEST	3
TCK	VDD3.3	GND	SERR#	AD15	AD12	AD8	AD5	AD3	PCLKO62SEL#	EECLK	EEWRDATA	2
TMC2	TDO	SMC	PAR	AD14	AD11	CBE0#	AD4	AD2	AD1	TMC1	EERDDATA	1

2.5 Signal Ball Descriptions – 161-Ball FBGA

2.5.1 PCI Express Signals

Table 2-11. PCI Express Signals – 9 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
PERn0	I DIFF	B9	**Receive Minus** PCI Express Differential Receive signal.
PERp0	I DIFF	A8	**Receive Plus** PCI Express Differential Receive signal.
PERST#	I/O 6 mA 3.3V	C12	**PCI Express Reset** In Forward Bridge mode, PERST# is an input. Resets the entire PEX 8112 when asserted. In Reverse Bridge mode, PERST# is an output. Asserted when a PCI reset is detected.
PETn0	O DIFF	B5	**Transmit Minus** PCI Express Differential Transmit signal.
PETp0	O DIFF	A6	**Transmit Plus** PCI Express Differential Transmit signal.
REFCLK-	I DIFF	A7	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. In Forward Bridge mode, connected to the PCI Express interface REFCLK- ball. In Reverse Bridge mode, connected to an external differential clock driver.
REFCLK+	I DIFF	B7	**PCI Express Clock Input Plus** PCI Express differential, 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. In Forward Bridge mode, connected to the PCI Express interface REFCLK+ ball. In Reverse Bridge mode, connected to an external differential clock driver.
WAKEIN#	I 3.3V	D14	**Wake In Signal** In Forward Bridge mode, pull WAKEIN# High. In Reverse Bridge mode, WAKEIN# is an input, and indicates that the PCI Express Device requested a wakeup while the link remains in the L2 Link PM state.
WAKEOUT#	OD 6 mA 3.3V	A11	**Wake Out Signal** In Forward Bridge mode, WAKEOUT# is an Open Drain output, and asserted when PMEIN# is asserted and the link remains in the L2 Link PM state.

2.5.2 PCI Signals

Table 2-12. PCI Signals – 63 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
AD[31:0]	I/O TS PCI	L13, J11, K12, L12, M10, P11, P10, P9, L9, N8, P8, M8, M7, L6, N6, P7, K2, J3, J1, H2, H3, H1, G4, F3, F2, F1, E2, E3, E1, D3, D1, D2	**Address/Data Bus (32 Balls)** The PCI address and data are multiplexed onto the same bus. During the Address phase, AD[31:0] contain the physical address of the transfer. During the Data phase, AD[31:0] contain the data. AD31 is the most significant bit. Write data is stable when IRDY# is asserted, and Read data is stable when TRDY# is asserted. Data is transferred when both IRDY# and TRDY# are asserted.
CBE[3:0]#	I/O TS PCI	M9, P6, K1, G1	**Command/Byte Enable Bus (4 Balls)** The Bus command and Byte Enables are multiplexed onto the same bus. During the Address phase, CBE[3:0]# contain the Bus command. During the Data phase, CBE[3:0]# contain the Byte Enables. CBE0# corresponds to Byte 0 (AD[7:0]), and CBE3# corresponds to Byte 3 (AD[31:24]). 0000b = Interrupt Acknowledge 0001b = Special cycle 0010b = I/O Read 0011b = I/O Write 0110b = Memory Read 0111b = Memory Write 1010b = Configuration Read 1011b = Configuration Write 1100b = Memory Read Multiple 1101b = Dual Address Cycle 1110b = Memory Read Line 1111b = Memory Write and Invalidate All other encodings are ***reserved***.
DEVSEL#	I/O STS PCI	M4	**Device Select** Indicates that the Target (Bus Slave) decoded its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus was selected.
FRAME#	I/O STS PCI	L5	**Frame** Driven by the PCI Master, and indicates the access start and duration. When FRAME# is first asserted, the Address phase is indicated. When FRAME# is de-asserted, the transaction remains in the last Data phase.
GNT[3:0]#	I/O TS PCI	F12, G11, J13, J14	**Bus Grant (4 Balls)** Indicates that the Central Arbiter granted the bus to an agent. When the Internal PCI Arbiter is enabled, GNT[3:0]# are outputs used to grant the bus to external devices. When the Internal PCI Arbiter is disabled, GNT0# is an input used to grant the bus to the PEX 8112, and GNT[3:1]# are placed into a high-impedance state.

Table 2-12. PCI Signals – 63 Balls (161-Ball FBGA) *(Cont.)*

Signal	Type	Balls	Description
IDSEL	I PCI	N10	**Initialization Device Select** Valid only in Reverse Bridge mode. Used as a Chip Select during Configuration Read and Write cycles. Each PCI slot or device typically has an IDSEL connected to a signal address line, allowing the PCI Host to select individual sets of Configuration registers. In Forward Bridge mode, it is recommended to ground IDSEL, to prevent the signal from floating.
INTA# INTB# INTC# INTD#	I/O OD PCI	F14 F13 E14 E13	**Interrupt (4 Balls)** Asserted to request an interrupt. After assertion, must remain asserted until the device driver clears it. INT*x*# is level-sensitive and asynchronous to the CLK. In Forward Bridge mode, INT*x*# is an input from PCI devices. All INT*x*# signals are mapped into Assert_INT*x* and Deassert_INT*x* messages on the PCI Express interface. INT*x*# inputs must be pulled up externally. In Reverse Bridge mode, INT*x*# is an output to the PCI Central Resource Function. All Assert_INT*x* and Deassert_INT*x* PCI Express messages are translated to INT*x*# transitions on the PCI Bus.
IRDY#	I/O STS PCI	P5	**Initiator Ready** Indicates that the Initiator (PCI Master) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.
LOCK#	I/O STS PCI	P4	**Lock Atomic Operation** Indicates an atomic operation to a bridge that might require multiple transactions to complete. In Forward Bridge mode, LOCK# is an output. In Reverse Bridge mode, LOCK# is an input.
M66EN	I PCI	D13	**66 MHz Enable** Indicates whether the PCI Bus is operating at 33 or 66 MHz. When Low, and the PCLKO divisor value in the **Device Initialization** register *PCLKO Clock Frequency* field is set to 0011b, the PCLKO ball oscillates at 33 MHz, with a 50% Duty cycle. When High, and the PCLKO divisor value in the **Device Initialization** register *PCLKO Clock Frequency* field is set to 0011b, the PCLKO ball oscillates at 66 MHz, with a 33% to 60% Duty cycle if the PCLKO62SEL# ball is pulled High or left disconnected. If the PCLKO62SEL# ball is pulled Low, the PCLKO ball is a low-jitter 62.5 MHz, with a 50% Duty cycle. Read M66EN, using the **PCI Control** register *M66EN* bit. M66EN must be grounded in 33 MHz systems.
PAR	I/O TS PCI	J4	**Parity** Even parity is generated across AD[31:0], and CBE[3:0]# [*that is*, the number of ones (1) on AD[31:0], CBE[3:0]#, and PAR is an even number]. PAR is valid one clock after the Address phase. For Data phases, PAR is valid one clock after IRDY# is asserted on Write cycles, and one clock after TRDY# is asserted on Read cycles. PAR has the same timing as AD[31:0], except it is delayed by one Clock cycle. The PCI Master drives PAR for Address and Write Data phases, and the Target drives PAR for Read Data phases.

Table 2-12. PCI Signals – 63 Balls (161-Ball FBGA) *(Cont.)*

Signal	Type	Balls	Description
PCIRST#	I/O TP PCI	G14	**PCI Reset** Asserted and de-asserted asynchronously to CLK, and used to bring a PCI device to an initial state. In Forward Bridge mode, PCIRST# is driven when a PCI Express reset is detected, or when the **Bridge Control** register *Secondary Bus Reset* bit is set. In Reverse Bridge mode, PCIRST# is an input that resets the entire PEX 8112. All PCI signals are asynchronously placed into a high-impedance state during reset.
PCLKI	I PCI	E12	**PCI Clock Input** All PCI signals, except RST# and interrupts, are sampled on the rising edge of PCLKI. The PCLKI frequency varies from 0 to 66 MHz, and it must oscillate during the serial EEPROM initialization sequence.
PERR#	I/O STS PCI	L2	**Parity Error** Indicates that a Data Parity error occurred. Driven active by the receiving agent two clocks following the data that contained bad parity.
PMEIN#	I S PCI	L14	**Power Management Event In** Valid only in Forward Bridge mode. Input used to monitor requests to change the system Power state.
PMEOUT#	OD 24 mA 3.3V	M14	**Power Management Event Out** Valid only in Reverse Bridge mode. Open Drain output used to request a change in the Power state. PMEOUT# is ***not*** 5V tolerant. When used in systems with a 5V pull-up resistor on the PCI backplane PME# signal, an external voltage translation circuit is required.
REQ[3:0]#	I/O TS PCI	H11, H12, K13, K14	**Bus Request (4 Balls)** Indicates that an agent requires use of the bus. When the Internal PCI Arbiter is enabled, REQ[3:0]# are inputs used to service external bus requests. When the Internal PCI Arbiter is disabled, REQ0# is an output used to request bus control, and REQ[3:1]# are unused inputs.
SERR#	I/O OD PCI	L1	**System Error** Indicates that an Address Parity error, Data Parity error on the special cycle command, or other catastrophic error occurred. Driven active for one PCI clock period, and is synchronous to the CLK. Driven only in Reverse Bridge mode.
STOP#	I/O STS PCI	N4	**Stop** Indicates that the Target (bus slave) is requesting that the Master stop the current transaction. After STOP# is asserted, it must remain asserted until FRAME# is de-asserted, whereupon STOP# must be de-asserted. Also, DEVSEL# and TRDY# cannot be changed until the current Data phase completes. STOP# must be de-asserted in the clock following the completion of the last Data phase, and must be placed into a high-impedance state in the next clock. Data is transferred when both IRDY# and TRDY# are asserted, independent of STOP#.
TRDY#	I/O STS PCI	M5	**Target Ready** Indicates that the Target (bus slave) is ready to transfer data. Data phase is complete when both IRDY# and TRDY# are asserted.

2.5.3 Clock, Reset, and Miscellaneous Signals

Table 2-13. Clock, Reset, and Miscellaneous Signals – 14 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	A10	**PCI Base Address 0 Register Enable** When Low, the **PCI Base Address 0** register (**BAR0**) is enabled. When High, the **PCI Base Address 0** register (**BAR0**) is enabled by the **Device-Specific Control** register *PCI Base Address 0 Enable* bit.
EECLK	O 3 mA TP 3.3V	C2	**Serial EEPROM Clock** Provides the clock to the serial EEPROM. Frequency is determined by the **Serial EEPROM Clock Frequency** register, and varies from 2 to 25 MHz.
EECS#	O 3 mA TP 3.3V	C5	**Serial EEPROM Chip Select** Active-Low Chip Select.
EERDDATA	I 3.3V	B3	**Serial EEPROM Read Data** Used to read data from the PEX 8112. A 47KΩ pull-up resistor is required.
EEWRDATA	O 3 mA TP 3.3V	A3	**Serial EEPROM Write Data** Used to write data to the PEX 8112.
EXTARB	I 3.3V	M12	**External Arbiter Enable** When Low, the Internal PCI Arbiter services requests from an external PCI device. When High, the PEX 8112 requests the PCI Bus from an External Arbiter.
FORWARD	I 3.3V PU	M13	**Bridge Select** When Low, the PEX 8112 acts as a PCI-to-PCI Express Bridge (Reverse Bridge). When High, the PEX 8112 acts as a PCI Express-to-PCI Bridge (Forward Bridge).
GPIO[3:0]	I/O 12 mA 3.3V PU	B12, D11, A12, C10	**General Purpose I/O (4 Balls)** Program as an input or output general-purpose ball. Internal device status also has the ability to be an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **General-Purpose I/O Control** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is Low at the trailing edge of *reset*, the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. For Forward Bridge mode, *reset* is PERST#. For Reverse Bridge mode, *reset* is PCIRST#.

Table 2-13. Clock, Reset, and Miscellaneous Signals – 14 Balls (161-Ball FBGA) *(Cont.)*

<table>
<tr><th>Signal</th><th>Type</th><th>Balls</th><th>Description</th></tr>
<tr><td>PCLKO</td><td>O
26 mA
TP
PCI</td><td>H14</td><td>
PCI Clock Output
Buffered clock output, whose output frequency reference is selected by the values of the M66EN and PCLKO62SEL# Input balls, and the Device Initialization register PCLKO Clock Frequency field value. By default, the PCLKO Clock Frequency field is initialized to 0011b.
<table>
<tr><th>M66EN</th><th>PCLKO62SEL#</th><th>Clock Frequency</th><th>PCLKO</th><th>Duty Cycle</th></tr>
<tr><td>0</td><td>X</td><td>Any</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>1</td><td>Not 011b</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>1</td><td>011b</td><td>66 MHz</td><td>33%</td></tr>
<tr><td>1</td><td>0</td><td>Not 011b</td><td>Divisor of 100 MHz</td><td>50%</td></tr>
<tr><td>1</td><td>0</td><td>011b</td><td>62.5 MHz</td><td>50%</td></tr>
</table>
Note: X is “Don’t Care.”

PCLKO is always driven and oscillates when all the following occur:

PCI Express REFCLK-/+ input balls are active
PCLKO Clock Frequency field is a non-zero value
PERST# (Forward Bridge mode) or PCIRST# (Reverse Bridge mode) is de-asserted

PCLKO can be connected to PCLKI as a source for the PCI input clock.
PCLKO is derived from the REFCLK-/+ inputs. As long as REFCLK-/+ is active, PCLKO is driven only when PERST# (Forward Bridge mode) or PCIRST# (Reverse Bridge mode) is de-asserted.
</td></tr>
<tr><td>PCLKO62SEL#</td><td>I
3.3V</td><td>C3</td><td>
PCI Clock Output 62.5 MHz Select
When pulled Low with M66EN High, causes the PCLKO clock to be derived from an internal low-jitter Phase-Locked Loop (PLL). PCLKO is 62.5 MHz, with a 50% Duty cycle. This provides an option for a low-jitter clock in situations where the REFCLK-/+ inputs can have jitter, which when used as a Reference Clock, would cause too much jitter on the output.
</td></tr>
<tr><td>PWR_OK</td><td>O
6 mA
3.3V</td><td>B11</td><td>
Power OK
Valid only in Forward Bridge mode. When the available power indicated in the Set Slot Power Limit message is greater than or equal to the power requirement indicated in the Power register, PWR_OK is asserted.
</td></tr>
</table>

2.5.4 JTAG Interface Signals

Note: *The JTAG interface is described in Section 18.1, "JTAG Interface."*

Table 2-14. JTAG Interface Signals – 5 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
TCK	I	M2	**Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 10 MHz.
TDI	I PU	P3	**Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
TDO	O 12 mA TS 3.3V	M3	**Test Data Output** Serial output to the JTAG TAP Controller test instructions and data.
TMS	I PU	N12	**Test Mode Select** When High, JTAG Test mode is enabled. Input decoded by the JTAG TAP Controller, to control test operations.
TRST#	I PU	N11	**Test Reset** Active-Low input used to reset the Test Access Port. Tie to ground through a 1.5KΩ resistor, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation. When JTAG functionality is not used, the TRST# input should be pulled or driven Low, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's Instruction register to contain the *IDCODE* instruction, or by holding the TMS input High for at least five rising edges of the TCK input.

2.5.5 Test Signals

Table 2-15. Test Signals – 7 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
BTON	I	M11	**Test Enable** Connect to Ground for standard operation.
BUNRI	I	C9	**Test Mode Select** Connect to Ground for standard operation.
SMC	I	K3	**Scan Path Mode Control** Connect to Ground for standard operation.
TEST	I	C4	**Test Mode Select** Connect to Ground for standard operation.
TMC	I	D10	**Test Mode Control** Connect to Ground for standard operation.
TMC1	I	D4	**IDDQ Test Control Input** Connect to Ground for standard operation.
TMC2	I	M1	**I/O Buffer Control** Connect to Ground for standard operation.

2.5.6 No Connect Signals

Caution: ***Do not connect the following PEX 8112 balls to board electrical paths.***

Table 2-16. No Connect Signals – 17 Balls (161-Ball FBGA)

Signal Name	Type	Location	Description
NC	***Reserved***	A1, A2, A13, A14, B1, B2, B13, B14, E5, N1, N2, N13, N14, P1, P2, P13, P14	**No Connect (17 Balls)** Must remain open. Do not connect these balls to board electrical paths.

2.5.7 Power and Ground Signals

Table 2-17. Power and Ground Signals – 46 Balls (161-Ball FBGA)

Signal	Type	Balls	Description
AVDD	Power	C8	**Analog Supply Voltage** Connect AVDD to the +1.5V power supply.
AVSS	Ground	C6	**Analog Ground** Connect AVSS to ground.
GND	Ground	A4, C13, D5, D12, E4, E11, F11, J2, K4, K11, L4, M6, N9, P12	**Ground (14 Balls)** Connect GND to ground.
VDD_P	Power	B6	**PLL Supply Voltage** Connect VDD_P to the +1.5V filtered PLL power supply.
VDD_R	Power	C7	**Receiver Supply Voltage** Connect VDD_R to the +1.5V power supply.
VDD_T	Power	D6	**Transmitter Supply Voltage** Connect VDD_T to the +1.5V power supply.
VDD1.5	Power	B10, C1, C14, G2, G13, L3, L11, N7	**PCI Express Interface Supply Voltage (8 Balls)** Connect VDD1.5 to the +1.5V power supply.
VDD3.3	Power	B4, C11, L10, N3	**I/O Supply Voltage (4 Balls)** Connect VDD3.3 to the +3.3V power supply.
VDD5	Power	G3, H13, L7	**PCI I/O Clamp Voltage** Connect VDD5 to the +5.0V power supply for PCI buffers. In a 3.3V PCI environment, connect VDD5 to the 3.3V power supply.
VDDQ	Power	F4, G12, H4, J12, L8, N5	**I/O Supply Voltage (6 Balls)** Connect VDDQ to the +3.3V power supply for PCI buffers.
VSS_C	Ground	D9	**Common Ground** Connect VSS_C to ground.
VSS_P0	Ground	D7	**PLL Ground** Connect VSS_P0 to ground.
VSS_P1	Ground	D8	**PLL Ground** Connect VSS_P1 to ground.
VSS_R	Ground	A9	**Receiver Ground** Connect VSS_R to ground.
VSS_RE	Ground	B8	**Receiver Ground** Connect VSS_RE to ground.
VSS_T	Ground	A5	**Transmitter Ground** Connect VSS_T to ground.

2.5.8 Ball Assignments by Location and Signal Name – 161-Ball FBGA

Table 2-18. Ball Assignments by Location (161-Ball FBGA)

Location	Signal	Location	Signal	Location	Signal	Location	Signal
A1	NC	C14	VDD1.5	H2	AD12	M5	TRDY#
A2		D1	AD1	H3	AD11	M6	GND
A3	EEWRDATA	D2	AD0	H4	VDDQ	M7	AD19
A4	GND	D3	AD2	H11	REQ3#	M8	AD20
A5	VSS_T	D4	TMC1	H12	REQ2#	M9	CBE3#
A6	PETp0	D5	GND	H13	VDD5	M10	AD27
A7	REFCLK-	D6	VDD_T	H14	PCLKO	M11	BTON
A8	PERp0	D7	VSS_P0	J1	AD13	M12	EXTARB
A9	VSS_R	D8	VSS_P1	J2	GND	M13	FORWARD
A10	BAR0ENB#	D9	VSS_C	J3	AD14	M14	PMEOUT#
A11	WAKEOUT#	D10	TMC	J4	PAR	N1	NC
A12	GPIO1	D11	GPIO2	J11	AD30	N2	
A13	NC	D12	GND	J12	VDDQ	N3	VDD3.3
A14		D13	M66EN	J13	GNT1#	N4	STOP#
B1		D14	WAKEIN#	J14	GNT0#	N5	VDDQ
B2		E1	AD3	K1	CBE1#	N6	AD17
B3	EERDDATA	E2	AD5	K2	AD15	N7	VDD1.5
B4	VDD3.3	E3	AD4	K3	SMC	N8	AD22
B5	PETn0	E4	GND	K4	GND	N9	GND
B6	VDD_P	E5	NC	K11		N10	IDSEL
B7	REFCLK+	E11	GND	K12	AD29	N11	TRST#
B8	VSS_RE	E12	PCLKI	K13	REQ1#	N12	TMS
B9	PERn0	E13	INTD#	K14	REQ0#	N13	NC
B10	VDD1.5	E14	INTC#	L1	SERR#	N14	
B11	PWR_OK	F1	AD6	L2	PERR#	P1	
B12	GPIO3	F2	AD7	L3	VDD1.5	P2	
B13	NC	F3	AD8	L4	GND	P3	TDI
B14		F4	VDDQ	L5	FRAME#	P4	LOCK#
C1	VDD1.5	F11	GND	L6	AD18	P5	IRDY#
C2	EECLK	F12	GNT3#	L7	VDD5	P6	CBE2#
C3	PCLKO62SEL#	F13	INTB#	L8	VDDQ	P7	AD16
C4	TEST	F14	INTA#	L9	AD23	P8	AD21
C5	EECS#	G1	CBE0#	L10	VDD3.3	P9	AD24
C6	AVSS	G2	VDD1.5	L11	VDD1.5	P10	AD25
C7	VDD_R	G3	VDD5	L12	AD28	P11	AD26

Table 2-18. Ball Assignments by Location (161-Ball FBGA) *(Cont.)*

Location	Signal	Location	Signal	Location	Signal	Location	Signal
C8	AVDD	G4	AD9	L13	AD31	P12	GND
C9	BUNRI	G11	GNT2#	L14	PMEIN#	P13	NC
C10	GPIO0	G12	VDDQ	M1	TMC2	P14	
C11	VDD3.3	G13	VDD1.5	M2	TCK		
C12	PERST#	G14	PCIRST#	M3	TDO		
C13	GND	H1	AD10	M4	DEVSEL#		

Table 2-19. Ball Assignments by Signal Name (161-Ball FBGA)

Signal	Location	Signal	Location	Signal	Location	Signal	Location
AD0	D2	EECLK	C2		B1	TDO	M3
AD1	D1	EECS#	C5		B2	TEST	C4
AD2	D3	EERDDATA	B3		B13	TMC	D10
AD3	E1	EEWRDATA	A3		B14	TMC1	D4
AD4	E3	EXTARB	M12		E5	TMC2	M1
AD5	E2	FORWARD	M13		N1	TMS	N12
AD6	F1	FRAME#	L5	NC	N2	TRDY#	M5
AD7	F2		A4		N13	TRST#	N11
AD8	F3		C13		N14	VDD_P	B6
AD9	G4		D5		P1	VDD_R	C7
AD10	H1		D12		P2	VDD_T	D6
AD11	H3		E4		P13		B10
AD12	H2		E11		P14		C1
AD13	J1		F11	PCLKO62SEL#	C3		C14
AD14	J3		J2	M66EN	D13		G2
AD15	K2		K4	BAR0ENB#	A10	VDD1.5	G13
AD16	P7		K11	PAR	J4		L3
AD17	N6		L4	PCIRST#	G14		L11
AD18	L6		M6	PCLKI	E12		N7
AD19	M7		N9	PCLKO	H14		B4
AD20	M8		P12	PERn0	B9		C11
AD21	P8	GNT0#	J14	PERp0	A8	VDD3.3	L10
AD22	N8	GNT1#	J13	PERR#	L2		N3
AD23	L9	GNT2#	G11	PERST#	C12		G3
AD24	P9	GNT3#	F12	PETn0	B5	VDD5	H13
AD25	P10	GPIO0	C10	PETp0	A6		L7
AD26	P11	GPIO1	A12	PMEIN#	L14		F4
AD27	M10	GPIO2	D11	PMEOUT#	M14		G12
AD28	L12	GPIO3	B12	PWR_OK	B11		H4
AD29	K12	IDSEL	N10	REFCLK-	A7	VDDQ	J12
AD30	J11	INTA#	F14	REFCLK+	B7		L8
AD31	L13	INTB#	F13	REQ0#	K14		N5
AVDD	C8	INTC#	E14	REQ1#	K13	VSS_C	D9
AVSS	C6	INTD#	E13	REQ2#	H12	VSS_P0	D7
BTON	M11	IRDY#	P5	REQ3#	H11	VSS_P1	D8
BUNRI	C9	LOCK#	P4	SERR#	L1	VSS_R	A9

Table 2-19. Ball Assignments by Signal Name (161-Ball FBGA) *(Cont.)*

Signal	Location	Signal	Location	Signal	Location	Signal	Location
CBE0#	G1	NC	A1	SMC	K3	VSS_RE	B8
CBE1#	K1		A2	STOP#	N4	VSS_T	A5
CBE2#	P6		A13	TCK	M2	WAKEIN#	D14
CBE3#	M9		A14	TDI	P3	WAKEOUT#	A11
DEVSEL#	M4						

2.5.9 Physical Layout – 161-Ball FBGA

Figure 2-2. 161-Ball FBGA Physical Layout (Underside View)

P	N	M	L	K	J	H	G	F	E	D	C	B	A	
NC	NC	PMEOUT#	PMEIN#	REQ0#	GNT0#	PCLKO	PCIRST#	INTA#	INTC#	WAKEIN#	VDD1.5	NC	NC	14
NC	NC	FORWARD	AD31	REQ1#	GNT1#	VDD5	VDD1.5	INTB#	INTD#	M66EN	GND	NC	NC	13
GND	TMS	EXTARB	AD28	AD29	VDDQ	REQ2#	VDDQ	GNT3#	PCLKI	GND	PERST#	GPIO3	GPIO1	12
AD26	TRST#	BTON	VDD1.5	GND	AD30	REQ3#	GNT2#	GND	GND	GPIO2	VDD3.3	PWR_OK	WAKEOUT#	11
AD25	IDSEL	AD27	VDD3.3							TMC	GPIO0	VDD1.5	BAR0ENB#	10
AD24	GND	CBE3#	AD23							VSS_C	BUNRI	PERn0	VSS_R	9
AD21	AD22	AD20	VDDQ							VSS_P1	AVDD	VSS_RE	PERp0	8
AD16	VDD1.5	AD19	VDD5							VSS_P0	VDD_R	REFCLK+	REFCLK-	7
CBE2#	AD17	GND	AD18							VDD_T	AVSS	VDD_P	PETp0	6
IRDY#	VDDQ	TRDY#	FRAME#						NC	GND	EECS#	PETn0	VSS_T	5
LOCK#	STOP#	DEVSEL#	GND	GND	PAR	VDDQ	AD9	VDDQ	GND	TMC1	TEST	VDD3.3	GND	4
TDI	VDD3.3	TDO	VDD1.5	SMC	AD14	AD11	VDD5	AD8	AD4	AD2	PCLKO62SEL#	EERDDATA	EEWRDATA	3
NC	NC	TCK	PERR#	AD15	GND	AD12	VDD1.5	AD7	AD5	AD0	EECLK	NC	NC	2
NC	NC	TMC2	SERR#	CBE1#	AD13	AD10	CBE0#	AD6	AD3	AD1	VDD1.5	NC	NC	1

Chapter 3 Reset Summary

3.1 Forward Bridge Mode

Table 3-1 defines which device resources are reset when each of the Forward bridge reset sources are asserted.

Table 3-1. Forward Bridge Reset

Reset Sources	Device Resources			
	PCI Express Interface Logic	PCI Bus Logic	PCIRST# Ball	Configuration Registers
PCI Express PERST# ball	✔	✔	✔	✔
PCI Express Link Down	✔	✔	✔	✔[a]
PCI Express Hot Reset	✔	✔	✔	✔[a]
Secondary Bus Reset bit		✔	✔	

*a. The **General-Purpose I/O Control** register is not reset for Link Down nor Hot Reset.*

3.2 Reverse Bridge Mode

Table 3-2 defines which device resources are reset when each of the Reverse bridge reset sources are asserted.

Table 3-2. Reverse Bridge Reset

Reset Sources	Device Resources				
	PCI Express Interface Logic	PCI Bus Logic	PERST# Ball	PCI Express Hot Reset	Configuration Registers
PCIRST# ball	✔	✔	✔	✔	✔
Secondary Bus Reset bit	✔			✔	

3.3 Initialization Summary

Certain PEX 8112 initialization sequences are described as follows:

- No serial EEPROM, blank serial EEPROM, or invalid serial EEPROM
  - When the EERDDATA ball is always High, an invalid serial EEPROM is detected. In this case, the default PCI Device ID (8112h) is selected. A 47KΩ pull-up resistor ensures that EERDDATA is High when no serial EEPROM is installed.
  - Enable the PCI Express interface and PCI Bus, using default register values.
- Valid serial EEPROM with Configuration register data
  - Enable the PCI Express interface and PCI Bus, using register values loaded from the serial EEPROM. The **Device Initialization** register *PCI Express Enable* or *PCI Enable* bit should be the last bit set by the serial EEPROM.

Chapter 4 Initialization

4.1 Forward Bridge Initialization

The actions that the PEX 8112 takes upon receipt of certain reset timing and interface initialization requirements are described in the following sections.

4.1.1 Forward Bridge Reset Behavior

There are three types of reset that the PEX 8112 receives over the primary bus (PCI Express):

- Physical Layer resets that are platform-specific and referred to as *Fundamental Resets* (Cold/Warm Reset)
- PCI Express Physical Layer mechanism (Hot Reset)
- PCI Express Data Link transitioning to the *DL_Down* state of the primary bus (PCI Express)

These three primary bus reset sources are each described in the sections that follow. All primary bus reset events initiate a Secondary Bus Reset, which resets the PCI Bus. In addition to primary bus reset sources, the PEX 8112 supports a PCI Bus reset, by way of the **Bridge Control** register.

After reset is de-asserted, a device attempting a Configuration access to the PCI Bus behind the PEX 8112 must wait for at least *Trhfa* (2^{25}) PCI clocks.

4.1.1.1 Fundamental Reset (Cold/Warm Reset)

The PEX 8112 uses the PCI Express PERST# signal as a Fundamental Reset input. When PERST# assertion follows the power-on event, it is referred to as a *Cold Reset*. The PCI Express system also generates this signal without removing power; which is referred to as a *Warm Reset*. The PEX 8112 treats Cold and Warm Resets without distinction. The PEX 8112 state machines are asynchronously reset, and the Configuration registers are initialized to their default values when PERST# is asserted. The PEX 8112 also places its PCI outputs into a high-impedance state, unless it is configured as the PCI Bus parking agent.

The PEX 8112 propagates the Warm/Cold Reset from its primary bus (PCI Express) to PCI reset on the secondary bus (PCI). The PCIRST# signal is asserted while PERST# is asserted. PCIRST# is asserted for at least 2 ms after the power levels are valid.

PCIRST# is asserted concurrent with PERST# assertion, and remains asserted for 1 to 2 ms after the trailing edge of PERST#. If PERST# de-asserts during that time, PCIRST# remains active until 1 ms has elapsed from the time it asserted. If PERST# is de-asserted after this time, PCIRST# follows the PERST# de-assertion within two PCI 33-MHz clock cycles (approximately 60 ns).

4.1.1.2 Primary Reset Due to Physical Layer Mechanism (Hot Reset)

PCI Express supports the Link Training Control Reset (a training sequence with the *Hot Reset* bit set), or Hot Reset, for propagating Reset requests downstream. When the PEX 8112 receives a Hot Reset on its primary bus (PCI Express), it propagates that reset to the PCIRST# signal. In addition, the PEX 8112 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. Software is responsible for ensuring that the Link Reset assertion and de-assertion messages are timed such that the PEX 8112 adheres to proper reset assertion and de-assertion durations on the PCIRST# signal.

For details, refer to the *PCI r3.0*, Section 4.2.3.2, “Timing Parameters,” and Section 4.3.2, “Reset.”

4.1.1.3 Primary Reset Due to Data Link Down

When the PEX 8112 primary bus (PCI Express) remains in standard operation and, for whatever reason, the link is down, the Transaction and Data Link Layers enter the *DL_Down* state. The PEX 8112 discards all transactions being processed and returns all registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. In addition, the entry of the primary bus (PCI Express) into DL_Down status initiates a reset of the PCI Bus, using the PCIRST# signal.

4.1.1.4 Secondary Bus Reset by way of Bridge Control Register

A PCI Secondary Bus Reset is initiated by setting the **Bridge Control** register *Secondary Bus Reset* bit. This targeted reset is used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration. A Write to the *Secondary Bus Reset* bit forces the assertion of the secondary bus PCI Reset (RST#) signal without affecting the primary bus (PCI Express) or Configuration Space registers. Moreover, the logic associated with the secondary bus is re-initialized and transaction buffers associated with the secondary bus are cleared.

RST# is asserted when the *Secondary Bus Reset* bit is set; therefore, software must take care to observe proper PCI reset timing requirements. Software is responsible for ensuring that the PEX 8112 does not receive transactions that require forwarding to the secondary bus while the *Secondary Bus Reset* bit is set.

4.1.1.5 Bus Parking during Reset

The PEX 8112 drives the secondary bus PCI Bus AD[31:0], CBE[3:0]#, and PAR signals to a logic Low level (zero) when the secondary bus RST# is asserted.

4.2 Reverse Bridge Initialization

4.2.1 Reverse Bridge Reset Behavior

A PCI Express Hot Reset (PCI Express Link Training Sequence) is generated when the **Bridge Control** register *Secondary Bus Reset* bit is set.

PCIRST# assertion causes the PCI Express sideband Reset signal (PERST#) to assert.

4.2.2 Reverse Bridge Secondary Bus Reset by way of Bridge Control Register

A PCI Express Secondary Bus Reset is initiated by setting the **Bridge Control** register *Secondary Bus Reset* bit. This targeted reset is used for various reasons, including recovery from error conditions on the secondary bus, or to initiate re-enumeration.

A Write to the *Secondary Bus Reset* bit causes a PCI Express Link Reset Training Sequence to transmit, without affecting the primary bus or Configuration Space registers. Moreover, the logic associated with the secondary bus is re-initialized and transaction buffers associated with the secondary bus are cleared.

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Chapter 5 Interrupts

5.1 Forward Bridge PCI Interrupts

In Forward Bridge mode, the PCI INT*x*# signals are inputs to the PEX 8112. The interrupt is routed to the PCI Express interface, using Virtual Wire Interrupt messages. The PCI Express interface supports the INT*x* Virtual Wire Interrupt feature for Conventional PCI systems that still support the PCI INT*x*# Interrupt signals. PCI INT*x*# interrupts are "virtualized" in the PCI Express interface, using Assert_INT*x* and Deassert_INT*x* messages (where *x* is A, B, C, or D for the respective PCI INT*x*# Interrupt signals defined in the *PCI r3.0*). This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INT*x* and Deassert_INT*x* messages transmitted on the PCI Express link capture the asserting/de-asserting edge of the respective PCI INT*x*# signal.

The Requester ID used in the PCI Express Assert_INT*x* and Deassert_INT*x* messages transmitted by the PEX 8112 (irrespective of whether the source is internal or external to the PEX 8112) equals the PEX 8112's primary bus' Bus Number and Device Number. The Function Number sub-field is cleared to 0.

5.1.1 Forward Bridge Internally Generated Interrupts

The following internal events can be programmed to generate an interrupt:

- Serial EEPROM transaction completed
- Any GPIO bit that is programmed as an input
- **Mailbox** register written

When one of these interrupts occurs, a Virtual Wire or Message Signaled interrupt (MSI) is generated. Both generated-interrupt methods are described, in detail, in the following two sections.

The **Mailbox** registers can be written from the downstream side with Memory-Mapped transactions, using the Address range defined by the **PCI Base Address 0** register.

5.1.1.1 Virtual Wire Interrupts

When Message Signaled Interrupts (MSIs) are disabled, Virtual Wire interrupts are used to support internal interrupt events. Internal interrupt sources are masked by the **PCI Command** register *Interrupt Disable* bit and routed to one of the virtual interrupts using the **PCI Interrupt Pin** register. PCI Express Assert_INT*x* and Deassert_INT*x* messages are not masked by the **PCI Command** register *Bus Master Enable* bit. The internal interrupt is processed the same as the corresponding PCI Interrupt signal.

5.1.1.2 MSI

The PCI Express interface supports interrupts using MSIs. With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8112 uses the 64-bit Message Address version of the **MSI Capability** structure (**MSI Address** and **MSI Upper Address** registers), and clears the *No Snoop* and *Relaxed Ordering* bits in the Requester attributes.

Address and Data Configuration registers are associated with the MSI feature – **MSI Address**, **MSI Upper Address**, and **MSI Data**. When an internal interrupt event occurs, the value in the **MSI Data** Configuration register is written to the PCI Express address specified by the **MSI Address** and **MSI Upper Address** Configuration registers.

When MSI is enabled (**MSI Control** register *MSI Enable* bit is set to 1), the Virtual Wire Interrupt feature is disabled. MSIs are generated independently of the **PCI Command** register *Interrupt Disable* bit. MSIs are gated by the **PCI Command** register *Bus Master Enable* bit.

Notes: *The No Snoop and Relaxed Ordering bits are cleared, because the PEX 8112 does **not support** these features.*

PCI INTx interrupts are never translated to Message Signaled Interrupts, but are always forwarded using Virtual Wire interrupts.

5.2 Reverse Bridge PCI Interrupts

In Reverse Bridge mode, the PCI INT*x*# signals are outputs from the PEX 8112. Each INT*x*# signal is asserted or de-asserted when the corresponding PCI Express Assert_INT*x* or Deassert_INT*x* message is received. The INT*x*# signals are asserted independently of the **PCI Command** register *Interrupt Disable* bit, and only when the PEX 8112 remains in the D0 Device PM state.

5.2.1 Reverse Bridge Internally Generated Interrupts

The following internal events can be programmed to generate an interrupt:

- Serial EEPROM transaction completed
- Any GPIO bit that is programmed as an input
- **Mailbox** register written

When one of these interrupts occurs, either an INT*x*# signal interrupt or Message Signaled interrupt is generated. Both generated-interrupt methods are described, in detail, in the following two sections.

The **Mailbox** registers can be written from the downstream side with Memory-Mapped transactions, using the Address range defined by the **PCI Base Address 0** register.

5.2.1.1 INT*x*# Signals

When an internal interrupt event occurs, it causes a PCI INT*x*# signal to assert. Internal interrupt sources are masked by the **PCI Command** register *Interrupt Disable* bit and are routed to one of the INT*x*# signals, using the **PCI Interrupt Pin** register. The INT*x*# signals are asserted only when Message Signaled Interrupts are disabled.

5.2.1.2 MSI

The PCI Bus supports interrupts using MSIs. With this mechanism, a device signals an interrupt by writing to a specific memory location. The PEX 8112 uses the 64-bit Message Address version of the **MSI Capability** structure (**MSI Address** and **MSI Upper Address** registers).

Address and Data Configuration registers are associated with the MSI feature – **MSI Address**, **MSI Upper Address**, and **MSI Data**. When an internal interrupt event occurs, the value in the **MSI Data** Configuration register is written to the PCI Express address specified by the **MSI Address** and **MSI Upper Address** Configuration registers.

When MSI is enabled (**MSI Control** register *MSI Enable* bit is set to 1), the INT*x*# Interrupt signals for internally generated interrupts are disabled. MSIs are generated independently of the **PCI Command** register *Interrupt Disable* bit. MSIs are gated by the **PCI Command** register *Bus Master Enable* bit.

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Chapter 6 Serial EEPROM Controller

6.1 Overview

The PEX 8112 provides an interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs. This interface consists of a Chip Select, Clock, Write Data, and Read Data balls, and operates at up to 25 MHz. Compatible 128-byte serial EEPROMs include the Catalyst CAT25C01, ST Microelectronics M95010W, and the following Atmel part numbers – AT25080A, AT25160A, AT25320A, and AT25640A. The PEX 8112 supports up to a 16 MB serial EEPROM, using 1-, 2-, or 3-byte addressing. The PEX 8112 automatically determines the appropriate addressing mode.

6.2 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in Table 6-1. The Validation Signature byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the number of bytes of serial EEPROM data to be loaded. It is equal to the number of registers to be loaded times six (6 serial EEPROM bytes per register). For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8112 exits reset. Following the register data are two bytes that determine how many shared memory locations to load. The remaining locations in the EEPROM contain the data to be loaded into the shared memory.

Table 6-2 defines the Serial EEPROM Format Byte organization.

Table 6-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	Refer to Table 6-2	Serial EEPROM Format Byte
2h	REG_BYTE_COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG_BYTE_COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
…	…	…
REG_BYTE_COUNT + 4	MEM_BYTE_COUNT (LSB)	Shared memory Byte Count (LSB)
REG_BYTE_COUNT + 5	MEM_BYTE_COUNT (MSB)	Shared memory Byte Count (MSB)
REG_BYTE_COUNT + 6	SHARED_MEM (Byte 0)	1st byte Shared memory
REG_BYTE_COUNT + 7	SHARED_MEM (Byte 1)	2nd byte of Shared memory
…	…	…
FFFFh	SHARED_MEM (Byte *n*)	Last byte of Shared memory

Table 6-2. Serial EEPROM Format Byte

Bit(s)	Description
0	**Configuration Register Load** When cleared, and REG_BYTE_COUNT is non-zero, the Configuration data is read from the serial EEPROM and discarded. When set, Configuration registers are loaded from the serial EEPROM. The first Configuration Register address is located at Bytes 3 and 4 in the serial EEPROM.
1	**Shared Memory Load** When set, shared memory is loaded from the serial EEPROM, starting at location REG_BYTE_COUNT + 6. The byte number to load is determined by the value in serial EEPROM locations REG_BYTE_COUNT + 4 and REG_BYTE_COUNT + 5.
7:2	***Reserved***

6.3 Serial EEPROM Initialization

After the PEX 8112 Reset is de-asserted, the serial EEPROM's internal **Status** register is read to determine whether a serial EEPROM is installed. A pull-up resistor on the EERDDATA ball produces a value of FFh when there is no serial EEPROM installed. When a serial EEPROM is detected, the first byte (validation signature) is read. When a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8112. The serial EEPROM address width is determined while this first byte is read. When the first byte's value is not 5Ah, the serial EEPROM is assumed to be blank or programmed with invalid data. In this case, the PCI Express interface and PCI Bus are enabled with device default settings. Also, the **Serial EEPROM Control** register *Serial EEPROM Address Width* field reports a value of 00b (undetermined width).

When the serial EEPROM contains valid data, the second byte (Serial EEPROM Format Byte) is read to determine which serial EEPROM sections are loaded into the PEX 8112 Configuration registers and memory.

Bytes 2 and 3 determine the number of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address (bit 12 Low selects the PCI Configuration registers; bit 12 High selects the Memory-Mapped Configuration registers) and 4 bytes of register Write data. When bit 1 of the Serial EEPROM Format Byte is set, locations REG_BYTE_COUNT + 4 and REG_BYTE_COUNT + 5 are read to determine the number of bytes to transfer from the serial EEPROM into shared memory.

The REG_BYTE_COUNT must be a multiple of 6 and MEM_BYTE_COUNT must be a multiple of 4.

The EECLK ball frequency is determined by the **Serial EEPROM Clock Frequency** register *Serial EEPROM Clock Frequency* field. The default clock frequency is 2 MHz. At this clock rate, it takes approximately 24 µs per DWORD during Configuration register or shared memory initialization. For faster loading of large serial EEPROMs that support a faster clock, direct the first Configuration register load from the serial EEPROM to the **Serial EEPROM Clock Frequency** register. This increases the serial EEPROM clock frequency for subsequent DWORDs.

Note: *When operating in Forward Bridge mode, it is recommended that the serial EEPROM sets the* ***Device Initialization*** *register PCI Express Enable bit. When operating in Reverse Bridge mode, it is recommended that the serial EEPROM sets the* ***Device Initialization*** *register PCI Enable bit.*

6.4 Serial EEPROM Random Read/Write Access

A PCI Express or PCI Master uses the **Serial EEPROM Control (EECTL)** register to access the serial EEPROM. This register contains 8-bit Read and Write Data fields, Read and Write Start signals, and related Status bits.

The following "C" routines demonstrate the firmware protocol required to access the serial EEPROM through the **Serial EEPROM Control** register. An interrupt is usually generated when the **Serial EEPROM Control** register *Serial EEPROM Busy* bit goes from true to false.

6.4.1 Serial EEPROM Opcodes

```
READ_STATUS_EE_OPCODE = 5
WREN_EE_OPCODE = 6
WRITE_EE_OPCODE = 2
READ_EE_OPCODE = 3
```

6.4.2 Serial EEPROM Low-Level Access Routines

```
int EE_WaitIdle()
{
    int eeCtl, ii;
    for (ii = 0; ii < 100; ii++)
     {
        PEX 8112Read(EECTL, eeCtl);      = /* read current value in EECTL */
        if ((eeCtl & (1 << EEPROM_BUSY)) == 0) = /* loop until idle */
            return(eeCtl);
    }
    PANIC("EEPROM Busy timeout!\n");
}
void EE_Off()
{
    EE_WaitIdle();                          = /* make sure EEPROM is idle */
    PEX 8112Write(EECTL, 0);                = /* turn off everything
(especially EEPROM_CS_ENABLE)*/
}
int EE_ReadByte()
{
    int eeCtl = EE_WaitIdle();              = /* make sure EEPROM is idle */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_READ_START);
    PEX 8112Write(EECTL, eeCtl);            = /* start reading */
    eeCtl = EE_WaitIdle();                  = /* wait until read is done */
    return((eeCtl >> EEPROM_READ_DATA) & 0xff); = /* extract read data
from EECTL */
}
void EE_WriteByte(int val)
{
    int eeCtl = EE_WaitIdle();              = /* make sure EEPROM is idle */
    eeCtl &= ~(0xff << EEPROM_WRITE_DATA); = /* clear current WRITE value */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_WRITE_START) |
             ((val & 0xff) << EEPROM_WRITE_DATA);
    PEX 8112Write(EECTL, eeCtl);
}
```

6.4.3 Serial EEPROM Read Status Routine

```
...
EE_WriteByte(READ_STATUS_EE_OPCODE);   = /* read status opcode */
status = EE_ReadByte();                = /* get EEPROM status */
EE_Off();                              = /* turn off EEPROM */
...
```

6.4.4 Serial EEPROM Write Data Routine

```
...
EE_WriteByte(WREN_EE_OPCODE);          = /* must first write-enable */
EE_Off();                              = /* turn off EEPROM */
EE_WriteByte(WRITE_EE_OPCODE);         = /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM       = /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          = /* transmit High byte of address */
#endif
EE_WriteByte(addr >> 8);               = /* transmit next byte of address */
EE_WriteByte(addr);                    = /* transmit Low byte of address */
for (ii = 0; ii < n; ii++)
{
    EE_WriteByte(buffer[ii]);          = /* transmit data to be written */
}
EE_Off();                              = /* turn off EEPROM */
...
```

6.4.5 Serial EEPROM Read Data Routine

```
...
EE_WriteByte(READ_EE_OPCODE);          = /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM       = /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);          = /* transmit High byte of address */
#endif
EE_WriteByte(addr >> 8);               = /* transmit next byte of address */
EE_WriteByte(addr);                    = /* transmit Low byte of address */
for (ii = 0; ii < n; ii++)
{
   buffer[ii] = EE_ReadByte(buffer[ii]); /* store read data in buffer */
}
EE_Off();                              = /* turn off EEPROM */
```

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Chapter 7 Address Spaces

7.1 Introduction

The PEX 8112 supports the following Address spaces:

- PCI-compatible Configuration (00h to FFh; 256 bytes)
- PCI Express Extended Configuration (100h to FFFh)
- I/O (32-bit)
- Memory (32-bit Non-Prefetchable)
- Prefetchable Memory (64-bit)

The first two spaces are used for accessing Configuration registers. (Refer to Chapter 8, "Configuration Transactions," for details.)

PCI Express Extended Configuration space (100h to FFFh) is supported only in Forward Bridge mode.

Table 7-1 lists which bus is primary or secondary for the PEX 8112 Forward and Reverse Bridge modes.

The other three Address spaces determine which transactions are forwarded from the primary bus to the secondary bus, and from the secondary bus to the primary bus. The Memory and I/O ranges are defined by a set of **Base** and **Limit** registers in the Configuration Header. Transactions falling within the ranges defined by the **Base** and **Limit** registers are forwarded from the primary bus to the secondary bus. Transactions falling outside these ranges are forwarded from the secondary bus to the primary bus.

The PEX 8112 does not perform Address Translation (flat address space) when transactions cross the bridge.

Table 7-1. Primary and Secondary Bus Definitions for Forward and Reverse Bridge Modes

Bridge Mode	Primary Bus	Secondary Bus
Forward Bridge	PCI Express	PCI
Reverse Bridge	PCI	PCI Express

7.2 I/O Space

The I/O Address space determines whether to forward I/O Read or I/O Write transactions across the PEX 8112. PCI Express uses the 32-bit Short Address Format (DWORD-aligned) for I/O transactions.

7.2.1 Enable Bits

Five Configuration register bits control the PEX 8112's response to I/O transactions:

- **PCI Command** register *I/O Access Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *ISA Enable* bit
- **Bridge Control** register *VGA Enable* bit
- **Bridge Control** register *VGA 16-Bit Decode* bit

The *I/O Access Enable* bit must be set for I/O transactions to be forwarded downstream. When cleared:

- All I/O transactions on the secondary bus are forwarded to the primary bus
- Forward Bridge mode – All primary bus I/O requests are completed with Unsupported Request (UR) status
- Reverse Bridge mode – All I/O transactions are ignored (no DEVSEL# assertion) on the primary (PCI) bus

The *Bus Master Enable* bit must be set for I/O transactions to be forwarded upstream. When cleared:

- Forward Bridge mode – All I/O transactions on the secondary (PCI) bus are ignored
- Reverse Bridge mode – All I/O requests on the secondary (PCI Express) bus are completed with UR status

The *ISA Enable* bit is discussed in Section 7.2.3, "ISA Mode." The *VGA Enable* and *VGA 16-Bit Decode* bits are discussed in Section 7.2.4, "VGA Mode."

7.2.2 I/O Base and Limit Registers

The following **I/O Base** and **Limit** Configuration registers are used to determine whether to forward I/O transactions across the PEX 8112:

- **I/O Base** (upper four bits of 8-bit register correspond to Address bits [15:12])
- **I/O Base Upper 16 Bits** (16-bit register corresponds to Address bits [31:16])
- **I/O Limit** (upper four bits of 8-bit register correspond to Address bits [15:12])
- **I/O Limit Upper 16 Bits** (16-bit register correspond to Address bits [31:16])

The I/O Base consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit **I/O Base** register define bits [15:12] of the I/O Base address. The lower four bits of the 8-bit register determine the I/O address capability of this device. The 16 bits of the **I/O Base Upper 16 Bits** register define bits [31:16] of the I/O Base address.

The I/O Limit consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit **I/O Limit** register define bits [15:12] of the I/O Limit address. The lower four bits of the 8-bit register determine the I/O address capability of this device, and reflect the value of the same field in the **I/O Base** register. The 16 bits of the **I/O Limit Upper 16 Bits** register define bits [31:16] of the I/O Limit address.

Because Address bits [11:0] are not included in the Address space decoding, the I/O Address range has a granularity of 4 KB and is always aligned to a 4-KB Address Boundary space. The maximum I/O range is 4 GB.

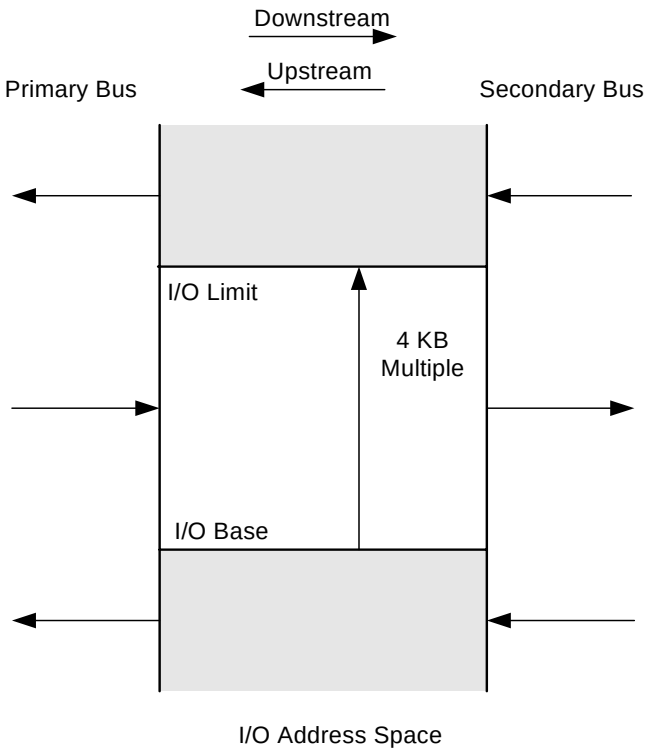
I/O transactions on the primary bus that fall within the range defined by the **I/O Base** and **Limit** registers are forwarded downstream to the secondary bus, and I/O transactions on the secondary bus that are within the range are ignored.

I/O transactions on the primary bus that do not fall within the range defined by the **I/O Base** and **Limit** registers are ignored, and I/O transactions on the secondary bus that do not fall within the range are forwarded upstream to the primary bus.

Figure 7-1 illustrates I/O forwarding.

For 16-bit I/O addressing, when the **I/O Base** has a value greater than the **I/O Limit**, the I/O range is disabled. For 32-bit I/O addressing, when the I/O base specified by the **I/O Base** and **I/O Base Upper 16 Bits** registers has a value greater than the I/O limit specified by the **I/O Limit** and **I/O Limit Upper 16 Bits** registers, the I/O range is disabled. In these cases, all I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

Figure 7-1. I/O Forwarding



7.2.3 ISA Mode

The **Bridge Control** register *ISA Enable* bit supports I/O forwarding in systems that have an ISA Bus. The *ISA Enable* bit only affects I/O addresses that are within the range defined by the **I/O Base** and **Limit** registers, and are in the first 64 KB of the I/O Address space.

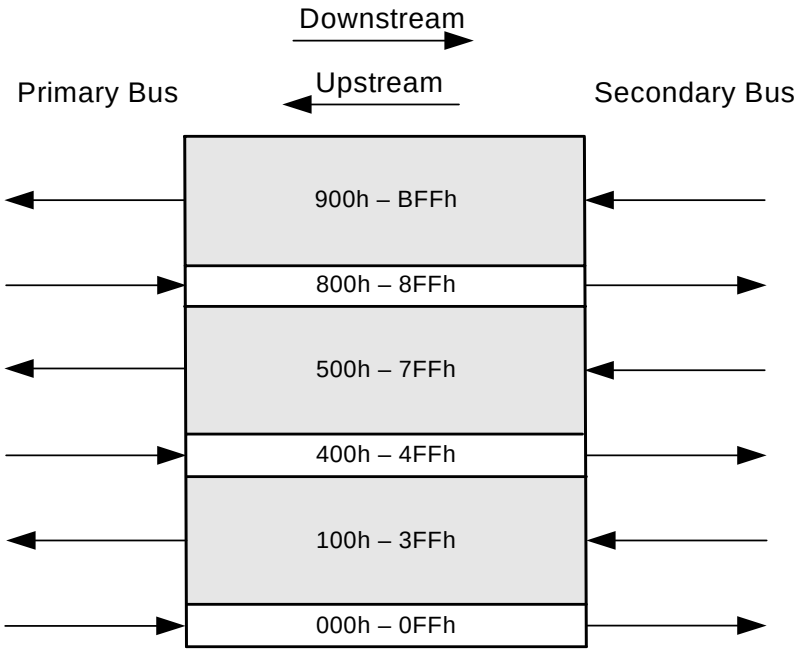
When the *ISA Enable* bit is set, the PEX 8112 does not forward downstream I/O transactions on the primary bus that are in the top 768 bytes of each 1-KB block within the first 64 KB of Address space. Only transactions in the bottom 256 bytes of each 1-KB block are forwarded downstream. When the *ISA Enable* bit is cleared, all addresses within the range defined by the **I/O Base** and **Limit** registers are forwarded downstream. I/O transactions with addresses above 64 KB are forwarded according to the range defined by the **I/O Base** and **Limit** registers.

When the *ISA Enable* bit is set, the PEX 8112 forwards upstream I/O transactions on the secondary bus that are in the top 768 bytes of each 1-KB block within the first 64 KB of Address space, although the address is within the I/O base and limit. All other transactions on the secondary bus are forwarded upstream when they fall outside the range defined by the **I/O Base** and **Limit** registers. When the *ISA Enable* bit is cleared, all secondary bus I/O addresses outside the range defined by the **I/O Base** and **Limit** registers are forwarded upstream.

As with all upstream I/O transactions, the **PCI Command** register *Bus Master Enable* bit must be set to enable upstream forwarding.

Figure 7-2 illustrates I/O forwarding with the *ISA Enable* bit set.

Figure 7-2. I/O Forwarding with *ISA Enable* Bit Set



7.2.4 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Register accesses to be forwarded downstream from the primary bus to the secondary bus, independent of the **I/O Base** and **Limit** registers.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O address decoding, and is applicable when the *VGA Enable* bit is set.

The *VGA Enable* and *VGA 16-Bit Decode* bits control the following VGA I/O addresses:

- 10-bit addressing – Address bits [9:0] = 3B0h through 3BBh, and 3C0h through 3DFh
- 16-bit addressing – Address bits [15:0] = 3B0h through 3BBh, and 3C0h through 3DFh

These ranges apply only to the first 64 KB of I/O Address space.

7.2.4.1 VGA Palette Snooping

Separate VGA palette snooping is ***not supported*** by PCI Express-to-PCI bridges; however, the PEX 8112 supports palette snooping in Reverse Bridge mode. In Forward Bridge mode, the **Bridge Control** register *VGA Enable* bit determines whether VGA Palette accesses are forwarded from PCI Express-to-PCI. The **PCI Command** register *VGA Palette Snoop* bit is forced to 0 in Forward Bridge mode.

The **Bridge Control** register *VGA 16-Bit Decode* bit selects between 10- and 16-bit VGA I/O palette snooping address decoding, and is applicable when the *VGA Palette Snoop* bit is set.

The *VGA Palette Snoop* and *VGA 16-Bit Decode* bits control the following VGA I/O Palette Snoop addresses:

- 10-bit addressing – Address bits [9:0] = 3C6h, 3C8h, and 3C9h
- 16-bit addressing – Address bits [15:0] = 3C6h, 3C8h, and 3C9h

The PEX 8112 supports the following three modes of palette snooping:

- Ignore VGA palette accesses when there are no graphics agents downstream that need to snoop or respond to VGA Palette Access cycles (Reads or Writes)
- Positively decode and forward VGA Palette Writes when there are graphics agents downstream of the PEX 8112 that require to Snoop Palette Writes (Reads are ignored)
- Positively decode and forward VGA Palette Reads and Writes when there are graphics agents downstream that require to snoop or respond to VGA Palette Access cycles (Reads or Writes)

The **Bridge Control** register *VGA Enable* bit and **PCI Command** register *VGA Palette Snoop* bit select the PEX 8112's response to Palette accesses, as defined in Table 7-2.

Table 7-2. PEX 8112 Response to Palette Access

VGA Enable Bit	VGA Palette Snoop Bit	PEX 8112 Response to Palette Accesses
0	0	Ignore all Palette accesses
0	1	Positively decode Palette Writes (ignore Reads)
1	X	Positively decode Palette Reads and Writes

Note: *X is "Don't Care."*

7.3 Memory-Mapped I/O Space

The Memory-Mapped I/O Address space determines whether to forward Non-Prefetchable Memory Read or Write transactions across the PEX 8112. Map devices that experience side effects during reads, *such as* buffers, into this space. For PCI-to-PCI Express reads, prefetching occurs in this space only when the Memory Read Line or Memory Read Multiple commands are issued on the PCI Bus. For PCI Express-to-PCI reads, the byte number to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this Address space are limited to a 32-bit range.

7.3.1 Enable Bits

Three Configuration register bits control the PEX 8112's response to Memory-Mapped I/O transactions:

- **PCI Command** register *Memory Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *VGA Enable* bit

The *Memory Space Enable* bit must be set for Memory transactions to be forwarded downstream. When cleared:

- All Memory transactions on the secondary bus are forwarded to the primary bus
- Forward Bridge mode – All Non-Posted Memory Requests are completed with UR status, and Posted Write data is discarded
- Reverse Bridge mode – All Memory transactions are ignored on the primary (PCI) bus

The *Bus Master Enable* bit must be set for Memory transactions to be forwarded upstream. When cleared:

- Forward Bridge mode – All Memory transactions on the secondary (PCI) bus are ignored
- Reverse Bridge mode – All Non-Posted Memory Requests on the secondary (PCI Express) bus are completed with UR status, and Posted Write data is discarded

The *VGA Enable* bit is discussed in Section 7.3.3, "VGA Mode."

7.3.2 Memory Base and Limit Registers

The following **Memory Base** and **Limit** Configuration registers are used to determine whether to forward Memory-Mapped I/O transactions across the PEX 8112:

- **Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])

Memory Base register bits [15:4] define Memory-Mapped I/O Base Address bits [31:20]. **Memory Limit** register bits [31:20] define Memory-Mapped I/O Limit bits [31:20]. Bits [3:0] of both registers are hardwired to 0h.

Because Address bits [19:0] are not included in the Address space decoding, the Memory-Mapped I/O Address range has a granularity of 1 MB and is always aligned to a 1-MB Address Boundary space. The maximum Memory-Mapped I/O range is 4 GB.

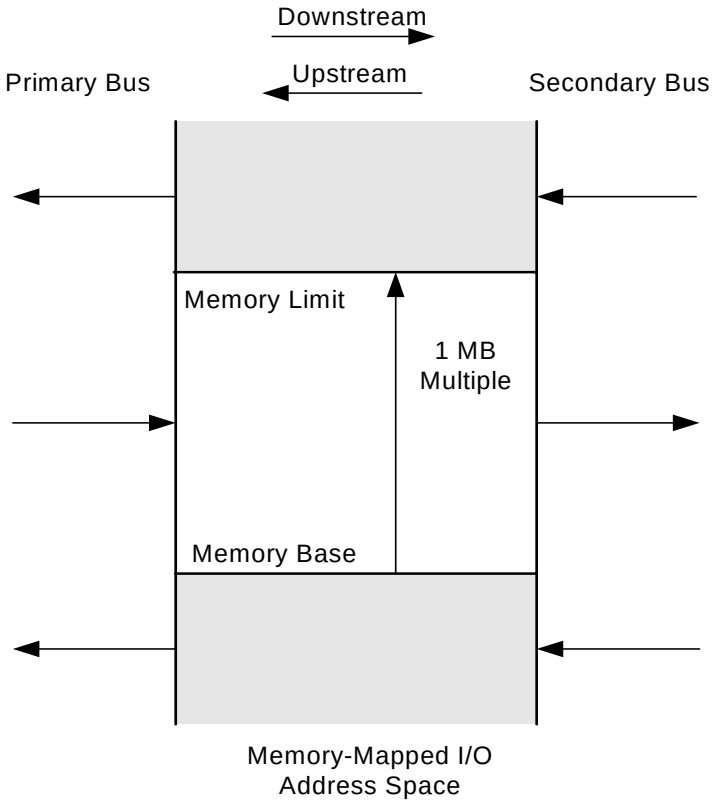
Memory transactions that fall within the range defined by the **Memory Base** and **Limit** registers are forwarded downstream from the primary bus to the secondary bus, and Memory transactions on the secondary bus that are within the range are ignored.

Memory transactions that do not fall within the range defined by the **Memory Base** and **Limit** registers are ignored on the primary bus, and forwarded upstream from the secondary bus (provided they are not in the Address range defined by the set of **Prefetchable Memory Address** registers or forwarded downstream by the VGA mechanism).

Figure 7-3 illustrates Memory-Mapped I/O forwarding.

When the **Memory Base** is programmed to have a value greater than the **Memory Limit**, the Memory-Mapped I/O range is disabled. In this case, all Memory transaction forwarding is determined by the **Prefetchable Base** and **Limit** registers and the **Bridge Control** register *VGA Enable* bit.

Figure 7-3. Memory-Mapped I/O Forwarding



7.3.3 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Frame Buffer accesses to be forwarded downstream from the primary bus to the secondary bus, independent of the **Memory Base** and **Limit** registers.

The *VGA Enable* bit controls VGA Memory addresses 0A_0000h through 0B_FFFFh.

7.4 Prefetchable Space

The Prefetchable Address space determines whether to forward Prefetchable Memory Read or Write transactions across the PEX 8112. Map devices that do not experience side effects during reads into this space.

- For PCI-to-PCI Express reads, prefetching occurs in this space for all Memory Read commands (Memory Read, Memory Read Line, and Memory Read Multiple) issued on the PCI Bus
- For Memory Read commands, the **Device-Specific Control** register *Blind Prefetch Enable* bit must be set for prefetching to occur
- For PCI Express-to-PCI reads, the byte number to read is determined by the Memory Read Request; therefore, prefetching does not occur

7.4.1 Enable Bits

Three Configuration register bits control the PEX 8112's response to Prefetchable Address space:

- **PCI Command** register *Memory Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *VGA Enable* bit

For further details, refer to Section 7.3.1, "Enable Bits."

7.4.2 Prefetchable Base and Limit Registers

The following **Prefetchable Memory Base** and **Limit** Configuration registers are used to determine whether to forward Prefetchable Memory transactions across the PEX 8112:

- **Prefetchable Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Base Upper 32 Bits** (32-bit register corresponds to Address bits [63:32])
- **Prefetchable Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Limit Upper 32 Bits** (32-bit register corresponds to Address bits [63:32])

Prefetchable Memory Base register bits [15:4] define Prefetchable Memory Base Address bits [31:20]. **Prefetchable Memory Limit** register bits [31:20] define Prefetchable Memory Limit bits [31:20]. For 64-bit addressing, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are also used to define the space.

Because Address bits [19:0] are not included in the Address space decoding, the Prefetchable Memory Address range has a granularity of 1 MB and is always aligned to a 1-MB Address Boundary space. The maximum Prefetchable Memory range is 4 GB with 32-bit addressing, and 2^{61} bytes with 64-bit addressing.

Memory transactions that fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are forwarded downstream from the primary bus to the secondary bus, and Memory transactions on the secondary bus that are within the range are ignored.

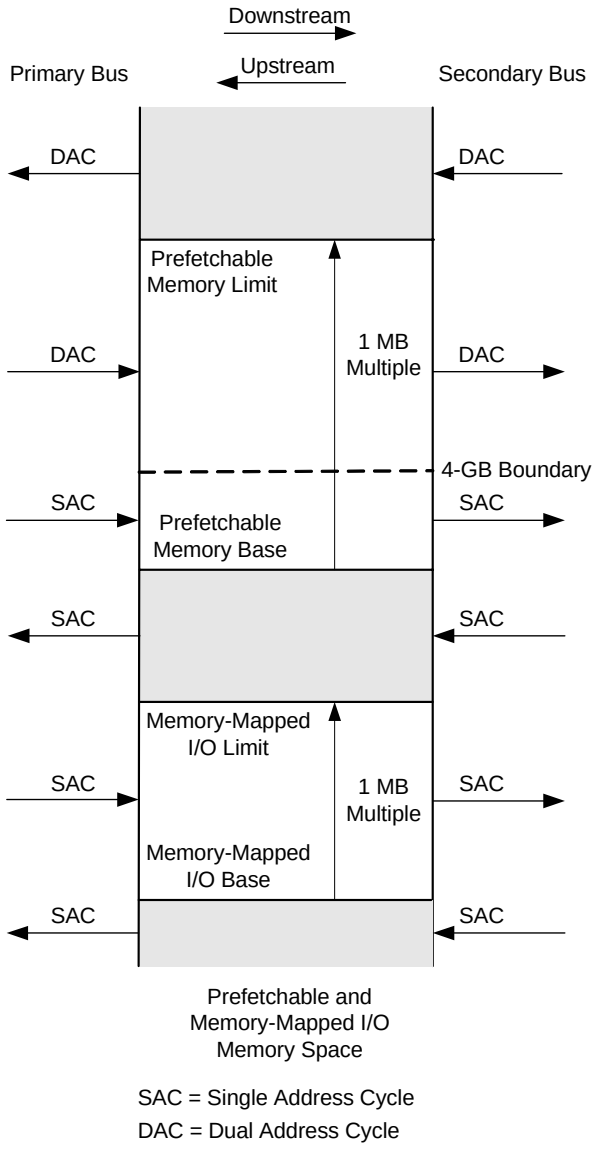
Memory transactions that do not fall within the range defined by the **Prefetchable Memory Base** and **Limit** registers are ignored on the primary bus, and forwarded upstream from the secondary bus (provided they are not in the Address range defined by the set of Memory-Mapped I/O Address registers or forwarded downstream by the VGA mechanism).

When the **Prefetchable Memory Base** is programmed to a value greater than the **Prefetchable Memory Limit**, the Prefetchable Memory range is disabled. In this case, all Memory transaction forwarding is determined by the **Memory Base** and **Limit** registers and the **Bridge Control** register *VGA Enable* bit.

Consider the four **Prefetchable Memory Base** and **Limit** registers when disabling the Prefetchable range.

Figure 7-4 illustrates both Memory-Mapped I/O and Prefetchable Memory forwarding. In the illustration, Dual Address cycles (DAC) indicate 64-bit addressing.

Figure 7-4. Memory-Mapped I/O and Prefetchable Memory Forwarding



7.4.3 64-Bit Addressing

Unlike Memory-Mapped I/O memory that must be below the 4-GB Address Boundary space, prefetchable memory is located below, above, or span the 4-GB Address Boundary space. Memory locations above the 4-GB Address Boundary space must be accessed using 64-bit addressing. PCI Express Memory transactions that use the Short Address (32-bit) format Target the Non-Prefetchable Memory space, or a Prefetchable Memory window below the 4-GB Address Boundary space. PCI Express Memory transactions that use the Long Address (64-bit) format Target locations anywhere in the 64-bit Memory space.

PCI Memory transactions that use Single Address cycles only Target locations below the 4-GB Address Boundary space. PCI Memory transactions that use Dual Address cycles Target locations anywhere in the 64-bit Memory space. The first Address phase of Dual Address transactions contains the lower 32 bits of the address, and the second Address phase contains the upper 32 bits of the address. When the upper 32 bits of the address are zero (0h), a Single Address transaction is always performed.

7.4.3.1 Enabling 64-Bit Address Capability

The **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field (offset 24h; PREBASE[3:0]) determines whether the PEX 8112 forwards transactions targeting memory above the 4-GB Address Boundary space. This field is programmed by serial EEPROM after device reset.

When the *Prefetchable Base Address Capability* field is cleared to 0000b (default), addresses over the 4-GB Address Boundary space are ***not supported***. In this case, PCI Express-to-PCI memory transactions to addresses at the 4-GB Address Boundary space and above are completed with UR status, and PCI-to-PCI Express DAC transactions are ignored (Master Abort).

When the *Prefetchable Base Address Capability* field is set to 0001b, 64-bit Address transactions are supported, according to the forwarding rules described in the sections that follow.

7.4.3.2 Forward Bridge Mode

Below 4-GB Address Boundary Space

If the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both cleared to 0, addresses above the 4-GB Address Boundary space are ***not supported***. In Forward Bridge mode, if a PCI Express Memory transaction is detected with an address above the 4-GB Address Boundary space, the transaction is completed with UR status. All Dual Address transactions on the PCI Bus are forwarded upstream to the PCI Express interface.

Above 4-GB Address Boundary Space

If the Prefetchable memory is located entirely above the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both set to non-zero values.

If a PCI Express Memory transaction is detected with an address below the 4-GB Address Boundary space, the transaction is completed with UR status, and all single address transactions on the PCI Bus are forwarded upstream to the PCI Express interface (unless the transactions fall within the Memory-Mapped I/O or VGA Memory range).

A PCI Express Memory transaction above the 4-GB Address Boundary space, that falls within the range defined by the **Prefetchable Memory Base**, **Prefetchable Memory Base Upper 32 Bits**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper 32 Bits** registers, is forwarded downstream and becomes a Dual Address cycle on the PCI Bus.

- If a Dual Address cycle, which is outside the range defined by these registers, is detected on the PCI Bus, the cycle is forwarded upstream to the PCI Express interface.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space does not fall within the range defined by these registers, the transaction is completed with UR status.
- If a PCI Dual Address cycle falls within the range determined by these registers, the cycle is ignored.

Spans 4-GB Address Boundary Space

- If the Prefetchable memory spans the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper 32 Bits** register is cleared to 0, and the **Prefetchable Memory Limit Upper 32 Bits** register is set to a non-zero value.
- If a PCI Express Memory transaction is detected with an address below the 4-GB Address Boundary space, and is greater than or equal to the Prefetchable Memory Base address, the transaction is forwarded downstream. If the address is less than the Prefetchable Memory Base address, a single address transaction on the PCI Bus is forwarded upstream to the PCI Express interface.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space is less than or equal to the **Prefetchable Memory Limit** register, it is forwarded downstream to the PCI Bus as a Dual Address cycle.
- If a Dual Address cycle on the PCI Bus is less than or equal to the **Prefetchable Memory Limit** register, it is ignored.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space is greater than the **Prefetchable Memory Limit** register, the transaction is completed with UR status.
- If a Dual Address cycle on the PCI Bus is greater than the **Prefetchable Memory Limit** register, the transaction is forwarded upstream to the PCI Express interface.

7.4.3.3 Reverse Bridge Mode

Below 4-GB Address Boundary Space

If the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both cleared to 0, addresses above the 4-GB Address Boundary space are ***not supported***. In Reverse Bridge mode, if a Dual Address transaction is detected on the PCI Bus, the transaction is ignored. If a PCI Express Memory transaction is detected with an address above the 4-GB Address Boundary space, the transaction is forwarded upstream to the PCI Bus as a Dual Address cycle.

Above 4-GB Address Boundary Space

If the Prefetchable memory is located entirely above the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper 32 Bits** and **Prefetchable Memory Limit Upper 32 Bits** registers are both set to non-zero values. The PEX 8112 ignores all Single Address Memory transactions on the PCI Bus, and forwards all PCI Express Memory transactions with addresses below the 4-GB Address Boundary space upstream to the PCI Bus (unless they fall within the Memory-Mapped I/O or VGA Memory range).

A Dual Address transaction on the PCI Bus that falls within the range defined by the **Prefetchable Memory Base**, **Prefetchable Memory Base Upper 32 Bits**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper 32 Bits** registers is forwarded downstream to the PCI Express interface.

- If a PCI Express Memory transaction is above the 4-GB Address Boundary space and falls outside the range defined by these registers, it is forwarded upstream to the PCI Bus as a Dual Address cycle. Dual Address transactions on the PCI Bus that do not fall within the range defined by these registers are ignored.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space falls within the range defined by these registers, it is completed with UR status.

Spans 4-GB Address Boundary Space

- If the Prefetchable memory spans the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper 32 Bits** register is cleared to 0, and the **Prefetchable Memory Limit Upper 32 Bits** register is set to a non-zero value.
- If a PCI Single Address cycle is greater than or equal to the Prefetchable Memory Base address, the transaction is forwarded downstream to the PCI Express interface.
- If a PCI Express Memory transaction is detected with an address below the 4-GB Address Boundary space, and is less than the Prefetchable Memory Base address, the transaction is forwarded upstream to the PCI Bus.
- If a Dual Address PCI transaction is less than or equal to the **Prefetchable Memory Limit** register, it is forwarded downstream to the PCI Express interface.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space is less than or equal to the **Prefetchable Memory Limit** register, it is completed with UR status.
- If a Dual Address PCI transaction is greater than the **Prefetchable Memory Limit** register, the transaction is ignored.
- If a PCI Express Memory transaction above the 4-GB Address Boundary space is greater than the **Prefetchable Memory Limit** register, the transaction is forwarded upstream to the PCI Bus as a Dual Address cycle.

7.4.4 VGA Mode

The **Bridge Control** register *VGA Enable* bit enables VGA Frame Buffer accesses to be forwarded downstream from the primary bus to the secondary bus, independent of the **Prefetchable Memory Base** and **Prefetchable Memory Limit** registers.

The *VGA Enable* bit controls VGA Memory addresses 0A_0000h through 0B_FFFFh.

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Chapter 8 Configuration Transactions

8.1 Introduction

Configuration Requests are initiated only by the Root Complex in a PCI Express-based system, or by the Central Resource function in a PCI-based system. In the *PCI r3.0*, the term *central resource* is used to describe bus support functions supplied by the Host system, typically in a PCI-compliant bridge or standard chipset. (Refer to the *PCI r3.0*, Section 2.4, for further details.)

Devices in a PCI Express or PCI system have a Configuration space that is accessed using Type 0 or Type 1 Configuration transactions:

- Type 0 Configuration transactions are used to access internal PEX 8112 Configuration registers
- Type 1 Configuration transactions are used to access PEX 8112s that reside downstream

The Configuration address is formatted as follows. (Refer to Table 8-1 through Table 8-4.)

Table 8-1. PCI Express

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	***Rsvd***	Extended Register Address	Register Address	***Rsvd***

Table 8-2. PCI Type 0 (at Master)

31 16	15 11	10 8	7 2	1 0
Single bit decoding of Device Number	***Rsvd***	Function Number	Register Number	0 0

Table 8-3. PCI Type 0 (at Target)

31 11	10 8	7 2	1 0
Rsvd	Function Number	Register Number	0 0

Table 8-4. PCI Type 1

31 24	23 16	15 11	10 8	7 2	1 0
Rsvd	Bus Number	Device Number	Function Number	Register Number	0 1

8.2 Type 0 Configuration Transactions

On its primary bus, the PEX 8112 responds only to Type 0 Configuration transactions that address the PEX 8112 Configuration space. A Type 0 Configuration transaction is used to configure the PEX 8112, and is not forwarded downstream to the secondary bus. The PEX 8112 ignores Type 0 Configuration transactions on the secondary bus. Type 0 Configuration transactions always result in the transfer of 1 DWORD.

When Configuration Write data is poisoned, the data is discarded, and a Non-Fatal Error message is generated, when enabled.

8.3 Type 1 Configuration Transactions

Type 1 Configuration transactions are used for device configuration in a hierarchical bus system. The PEX 8112 responds to Type 1 Configuration transactions. Type 1 Configuration transactions are used when the transaction is intended for a device residing on a bus other than the one where the Type 1 request is issued.

The *Bus Number* field in a Configuration transaction request specifies a unique bus in the hierarchy on which transaction Targets reside. The PEX 8112 compares the specified Bus Number with two PEX 8112 Configuration registers – **Secondary Bus Number** and **Subordinate Bus Number** – to determine whether to forward a Type 1 Configuration transaction across the PEX 8112.

When a Type 1 Configuration transaction is received on the primary bus, the following tests are applied, in sequence, to the *Bus Number* field to determine how the transaction must be handled:

- If the *Bus Number* field is equal to the **Secondary Bus Number** register value, and the conditions for converting the transaction into a special cycle transaction are met, the PEX 8112 forwards the Configuration Request to the secondary bus as a special cycle transaction. When the conditions are not met, the PEX 8112 forwards the Configuration Request to the secondary bus as a Type 0 Configuration transaction. (For details, refer to the *PCI r3.0*, Section 3.6.2, “Special Cycles.”)
- If the *Bus Number* field is not equal to the **Secondary Bus Number** register value, but is within the range of the **Secondary Bus Number** and **Subordinate Bus Number** (inclusive) registers, the Type 1 Configuration Request is specifying a bus located behind the PEX 8112. In this case, the PEX 8112 forwards the Configuration Request to the secondary bus as a Type 1 Configuration transaction.
- If the *Bus Number* field does not satisfy the above criteria, the Type 1 Configuration Request is specifying a bus that is not located behind the PEX 8112. In this case, the Configuration Request is invalid:
  - If the primary bus is PCI Express, a Completion with Unsupported Request (UR) status is returned
  - If the primary bus is PCI, the Configuration Request is ignored, resulting in a Master Abort

8.4 Type 1-to-Type 0 Conversion

The PEX 8112 performs a Type 1-to-Type 0 conversion when the Type 1 transaction is generated on the primary bus and is intended for a device directly attached to the secondary bus. The PEX 8112 must convert the Type 1 Configuration transaction to Type 0, thereby allowing the PEX 8112 to respond to it.

Type 1-to-Type 0 conversions are performed only in the downstream direction. The PEX 8112 generates Type 0 Configuration transactions only on the secondary bus, never on the primary bus.

8.4.1 Forward Bridge Mode

The PEX 8112 forwards a Type 1 transaction on the PCI Express interface to a Type 0 transaction on the PCI Bus, when the following are true:

- Type 1 Configuration Request *Bus Number* field is equal to the **Secondary Bus Number** register value.
- Conditions for conversion to a special cycle transaction are not met.

The PEX 8112 then performs the following on the secondary bus:

1. Clears Address bits AD[1:0] to 00b.
2. Derives Address bits AD[7:2] from the Configuration Request *Register Address* field.
3. Derives Address bits AD[10:8] from the Configuration Request *Function Number* field.
4. Clears Address bits AD[15:11] to 0h.
5. Decodes the *Device Number* field, and asserts a single Address bit within the range AD[31:16] during the Address phase.
6. Verifies that the Configuration Request *Extended Register Address* field is zero (0h). When the value is non-zero, the PEX 8112 does not forward the transaction, and treats it as a UR on the PCI Express interface, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

8.4.2 Reverse Bridge Mode

The PEX 8112 forwards a Type 1 transaction on the PCI Bus to a Type 0 transaction on the PCI Express interface, when the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- Type 1 Configuration Request *Bus Number* field (AD[23:16]) is equal to the **Secondary Bus Number** register value.
- Bus command on CBE[3:0]# is a Configuration Read or Write.
- Type 1 Configuration Request *Device Number* field (AD[15:11]) is zero (0h). When the value is non-zero, the transaction is ignored, resulting in a Master Abort.

The PEX 8112 then creates a PCI Express Configuration Request, according to the following:

1. Sets the Request *Type* field to Configuration Type 0.
2. Sets the *Register Address* field [7:2] from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Sets the *Function Number* field [18:16] from the Configuration Request *Function Number* field.
5. Clears the *Device Number* field [23:19] from the Configuration Request *Device Number* field (forced to 0h).
6. Sets the *Bus Number* field [31:24] from the Configuration Request *Bus Number* field.

Type 1-to-Type 0 transactions are performed as Non-Posted (Delayed) transactions.

8.5 Type 1-to-Type 1 Forwarding

Type 1-to-Type 1 transaction forwarding provides a hierarchical configuration mechanism when two or more levels of bridges are used. When the PEX 8112 detects a Type 1 Configuration transaction intended for a PCI Bus downstream from the secondary bus, the PEX 8112 forwards the transaction, unchanged, to the secondary bus.

In this case, the transaction Target does not reside on the PEX 8112's secondary bus; however, is located on a bus segment further downstream. Ultimately, this transaction is converted to a Type 0 or special cycle transaction by a downstream bridge.

8.5.1 Forward Bridge Mode

The PEX 8112 forwards a Type 1 transaction on the PCI Express interface to a Type 1 transaction on the PCI Bus when the following are true:

- Type 1 Configuration transaction is detected on the PCI Express interface.
- Value specified by the *Bus Number* field is within the range of Bus Numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive).

The PEX 8112 then performs the following on the secondary bus:

1. Generates Address bits AD[1:0] as 01b.
2. Generates the PCI Register Number, Function Number, Device Number, and Bus Number from the PCI Express Configuration Request *Register Address*, *Function Number*, *Device Number*, and *Bus Number* fields, respectively.
3. Generates Address bits AD[31:24] as 0h.
4. Verifies that the Configuration Request *Extended Register Address* field is 0h. When the value is non-zero, the PEX 8112 does not forward the transaction, and returns a Completion with UR status on the PCI Express interface, and a Received Master Abort on the PCI Bus.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted transactions.

8.5.2 Reverse Bridge Mode

The PEX 8112 forwards a Type 1 transaction on the PCI Bus to a Type 1 transaction on the PCI Express interface when the following are true during the PCI Address phase:

- Address bits AD[1:0] are 01b.
- Value specified by the *Bus Number* field is within the range of Bus Numbers between the **Secondary Bus Number** (exclusive) and **Subordinate Bus Number** (inclusive).
- Bus command on CBE[3:0]# is a Configuration Read or Write.

The PEX 8112 then creates a PCI Express Configuration Request, according to the following:

1. Sets the Configuration Request *Type* field to Configuration Type 1.
2. Sets the *Register Address* field [7:2] from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Sets the *Function Number* field [18:16] from the Configuration Request *Function Number* field.
5. Sets the *Device Number* field [23:19] from the Configuration Request *Device Number* field.
6. Sets the *Bus Number* field [31:24] from the Configuration Request *Bus Number* field.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted (Delayed) transactions.

8.6 Type 1-to-Special Cycle Forwarding

The Type 1 Configuration mechanism is used to generate special cycle transactions in hierarchical systems. Special cycle transactions are ignored by the PEX 8112 acting as a Target, and are not forwarded across the PEX 8112.

In Forward Bridge mode, special cycle transactions are only generated in the downstream direction (PCI Express-to-PCI).

In Reverse Bridge mode, special cycle transactions are also generated in the downstream direction (PCI-to-PCI Express).

A Type 1 Configuration Write Request on the PCI Express interface is converted to a special cycle on the PCI Bus when the following conditions are met:

- Type 1 Configuration Request *Bus Number* field is equal to the **Secondary Bus Number** register value.
- *Device Number* field is all ones (11111b)
- *Function Number* field is all ones (111b)
- *Register Address* field is all zeros (0h)
- *Extended Register Address* field is all zeros (0h)

When the PEX 8112 initiates the transaction on the PCI Bus, the Bus command is converted from a Configuration Write to a special cycle. The Address and Data fields are forwarded, unchanged, from the PCI Express-to-PCI Bus. Target devices that recognize the special cycle ignore the address, and the message is passed in the Data word. The transaction is performed as a Non-Posted transaction; however, the PCI Target response (always Master Abort in this case) is not returned to the PCI Express interface. After the Master Abort is detected on the PCI Bus, the successful Completion TLP is returned to the PCI Express interface.

8.7 PCI Express Enhanced Configuration Mechanisms

The PCI Express Enhanced Configuration mechanism adds four extra bits to the *Register Address* field, to expand the space to 4,096 bytes. The PEX 8112 forwards Configuration transactions only when the Extended Register Address bits are all zeros (0h). This prevents address aliasing on the PCI Bus, which does not support Extended Register Addressing.

When a Configuration transaction targets the PCI Bus and has a non-zero value in the *Extended Register Address* bits, the PEX 8112 treats the transaction as if it received a Master Abort on the PCI Bus.

The PEX 8112 performs the following:

1. Sets the appropriate status bits for the destination bus, as if the transaction had executed and received a Master Abort.
2. Generates a PCI Express Completion with UR status.
3. Indexed addressing of the Main Control Block registers.

8.7.1 Memory-Mapped Indirect (Reverse Bridge Mode Only)

In Reverse Bridge mode, the PEX 8112 provides the capability for a PCI Host to access the downstream PCI Express Configuration registers of external PCI Express devices, using PCI Memory transactions. The 4-KB region of the Memory range defined by the **PCI Base Address 0** register is used for this mechanism. Memory Reads and Writes to **PCI Base Address 0** register, offsets 2000h to 2FFFh, result in a PCI Express Configuration transaction. The Transaction address is determined by the **Enhanced Configuration Address** register. The format of this Address register is defined in Table 8-5.

After the **Enhanced Configuration Address** register is programmed to point to a particular device, the entire PCI Express endpoint 4-KB Configuration space is directly accessed, using Memory Read and Write transactions. Only single DWORDs are transferred during Enhanced Configuration transactions.

Table 8-5. Enhanced Configuration Address Register Format

31	30 28	27 20	19 15	14 12	11 0
Enhanced Enable	***Rsvd***	Bus Number	Device Number	Function Number	***Rsvd***

8.8 Configuration Retry Mechanism

8.8.1 Forward Bridge Mode

Bridges are required to return a Completion for all Configuration Requests that cross the PEX 8112 from PCI Express-to-PCI, prior to expiration of the Root Complex's Completion Timeout Timer. This requires that bridges take ownership of all Configuration Requests forwarded across the PEX 8112.

When the Configuration Request to the PCI Bus successfully completes prior to the PEX 8112's CRS Timer (**CRS Timer** register, offset 1060h) expiration, the PEX 8112 returns a Completion with Successful status to the PCI Express interface.

When the Configuration Request to the PCI Bus encounters an error condition prior to the CRS Timer expiration, the PEX 8112 returns an appropriate error Completion [non-Configuration Retry Status (CRS)] to the PCI Express interface.

When the Configuration Request to the PCI Bus does not complete successfully or with an error, prior to CRS Timer expiration, the PEX 8112 returns a Completion with CRS.

Although the PEX 8112 returned a Completion with CRS to the PCI Express interface, the PEX 8112 continues to keep the Configuration transaction alive on the PCI Bus. The *PCI r3.0* states that after a PCI Master detects a Target Retry, it must continue to Retry the transaction until at least one DWORD is transferred. The PEX 8112 Retries the transaction until it completes on the PCI Bus, or until the PCI Express-to-PCI Retry Timer expires.

When another PCI Express-to-PCI Configuration transaction is detected while the previous transaction is Retried, a Completion with CRS is immediately returned.

If the first Configuration transaction completes on the PCI Bus after the second Configuration transaction returns with a Completion of CRS status on the PCI Express interface, the PEX 8112 discards the Completion information. Bridges that implement this option are also required to implement bit 15 of the **PCI Express Device Control** register as the *Bridge Configuration Retry Enable* bit. Usually, a Completion TLP is returned to the PCI Express Root Complex after a PCI Express-to-PCI Configuration transaction occurs. For a Write, the Completion information is a status TLP without data. For a Read, the completion information contains status. as well as the Read data.

When the *Bridge Configuration Retry Enable* bit is cleared, the PEX 8112 does not return a Completion with CRS on behalf of Configuration Requests forwarded across the PEX 8112. The lack of a Completion results in eventual Completion Timeout at the Root Complex.

By default, bridges do not return CRS for Configuration Requests to a PCI device behind the PEX 8112, which might result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

8.8.2 Reverse Bridge Mode

In Reverse Bridge mode, the PEX 8112 detects Completion with CRS status from a downstream PCI Express device. The **Device-Specific Control** register *CRS Retry Control* field determines the PEX 8112 response in Reverse Bridge mode when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry status.

Table 8-6. Device-Specific Control Register *CRS Retry Control* Field Values

CRS Retry Control Field	Response
00b	Retry once after 1s. When another CRS is received, Target Abort on the PCI Bus. Typically, a device should be ready to respond within 1s. If the device does not respond within 1s, the PEX 8112 allows the device one more opportunity to respond, before returning a Target Abort to the PCI Host. This default setting is not specified in the *PCI Express-to-PCI/PCI-X Bridge r1.0*, and is up to the designer to select.
01b	Retry eight times, once per second. When another CRS is received, Target Abort on the PCI Bus.
10b	Retry once per second, until successful completion.
11b	***Reserved***

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Chapter 9 Bridge Operation

9.1 Forward Bridge Operation

In Forward Bridge mode, the PEX 8112 presents a Type 1 Configuration Space Header (bridge) on the PCI Express interface. There are no PCI-Compatible Configuration registers available on the PCI Bus. Three sets of Type 1 Configuration Space Header registers define the bridging operation between the PCI Express interface and PCI Bus. (Refer to Table 9-1.)

The PEX 8112 also supports one PCI Base Address register (**PCI Base Address 0**, **BAR0**), which allows a PCI Express or PCI Master to access Internal Configuration registers or shared memory. During bus enumeration, the addresses corresponding to the BAR are excluded from the bridging ranges of the six registers referenced in Table 9-1.

Table 9-1. Type 1 Configuration Space Header Register Sets that Define Bridging Operation between PCI Express Interface and PCI Bus

Register Set	Description
I/O Base and **I/O Limit**	When I/O transactions on the PCI Express interface fall within the range specified by these registers, the transactions are forwarded to the PCI Bus. When I/O transactions on the PCI Bus fall outside the range specified by these registers, the transactions are forwarded to the PCI Express interface.
Memory Base and **Memory Limit**	When Non-Prefetchable Memory transactions on the PCI Express interface fall within the range specified by these registers, the transactions are forwarded to the PCI Bus. When Non-Prefetchable Memory transactions on the PCI Bus fall outside the range specified by these registers, the transactions are forwarded to the PCI Express interface.
Prefetchable Memory Base and **Prefetchable Memory Limit**	When Prefetchable Memory transactions on the PCI Express interface fall within the range specified by these registers, the transactions are forwarded to the PCI Bus. When Prefetchable Memory transactions on the PCI Bus fall outside the range specified by these registers, the transactions are forwarded to the PCI Express interface.

9.1.1 Forward Bridge Flow Control

The PEX 8112 supports the Flow Control mechanism described in the *PCI Express Base r1.0a*, and provides the minimum flow requirements defined in Table 9-2.

The PEX 8112 advertises infinite credits (initial credit value of 0h) for Completion Header and Completion Data. Buffer space is allocated for the resulting Completions. The unit of Flow Control (FC) for data is 16 bytes. For Headers, it is the maximum size Header plus TLP Digest.

Table 9-2. Flow Control Mechanism Minimum Flow Requirements

Credit Type	Minimum Advertisement
PH (Posted Request Headers)	32FC unit – Credit value of 20h
PD (Posted Request Data Payload)	128 FC unit – Credit value of 80h
NPH (Non-Posted Request Header)	16 FC unit – Credit value of 10h
NPD (Non-Posted Request Data Payload)	16 FC unit – Credit value of 10h
CPLH (Completion Headers)	Infinite – Credit value of 00h
CPLD (Completion Data Payload)	Infinite – Credit value of 00h

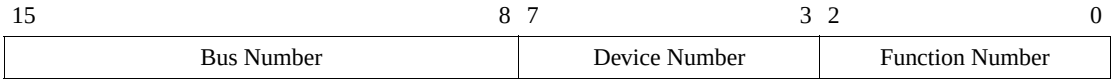
9.1.2 Forward Bridge Buffer Size and Management

The PEX 8112 provides adequate buffers to accept Data transfers from the PCI Express interface, and to deliver a Read Completion.

For upstream requests (PCI-to-PCI Express), the PEX 8112 provides Buffer space for the resultant Completion (Data and/or Header) before the transaction is forwarded to the PCI Express interface.

9.1.3 Forward Bridge Requester ID and Tag Assignment

In certain cases, the PEX 8112 must generate a new Requester ID and Tag combination for transactions forwarded to the PCI Express interface. When the PEX 8112 generates a new Requester ID for a transaction forwarded from the secondary bus to the primary bus, the PEX 8112 assigns the PCI Express Requester ID, using the secondary bus's Bus Number, and clears the *Device Number* and *Function Number* fields to 0. The Requester ID is a 16-bit field formatted as follows, and the *Tag* is a unique 8-bit field.



Outstanding Non-Posted transactions (*such as* transactions requiring a Completion) forwarded to the PCI Express interface must have a unique Transaction ID, regardless of whether multiple PCI Express transactions were generated for a single PCI transaction. When a PCI Non-Posted transaction forwarded to the PCI Express interface crosses a 4-KB Address Boundary space, or a Read Request exceeds the **PCI Express Device Control** register *Maximum Read Request Size* field value, the resulting multiple PCI Express transactions require unique Transaction IDs.

9.1.4 Forward Bridge PCI Express-to-PCI Forwarding (Downstream)

9.1.4.1 Transaction Types

Table 9-3 defines the PCI Express transactions that must be forwarded to the PCI Bus. Table 9-4 defines the PCI transactions that must be performed on the secondary bus.

Table 9-3. Transactions Forwarded to PCI Bus

Primary Bus – PCI Express Command	Secondary Bus – PCI Command
Memory Write Request	Memory Write or Memory Write and Invalidate (refer to Section 9.1.4.2)
Memory Read Request	Memory Read, Memory Read Line, or Memory Read Line Multiple (refer to Section 9.1.4.3)
Memory Read Request – Locked	Memory Read, Memory Read Line, or Memory Read Line Multiple
I/O Write Request	I/O Write
I/O Read Request	I/O Read
Type 1 Configuration Write Request	Type 0 or Type 1 Configuration Write or special cycle (refer to Section 8.3, "Type 1 Configuration Transactions")
Type 1 Configuration Read Request	Type 0 or Type 1 Configuration Read
Message Request – Vendor-Defined	N/A
Message Request with Data Payload – Vendor-Defined	N/A
Completion or Completion with Data	N/A

Table 9-4. Transactions Performed on Secondary Bus

Transaction Type	PEX 8112 Master on Secondary Bus	PEX 8112 Target on Secondary Bus
Interrupt Acknowledge	No	No
Special Cycle	Yes	No
I/O Read	Yes	Yes
I/O Write	Yes	Yes
Memory Read	Yes	Yes
Memory Write	Yes	Yes
Configuration Read	Yes	No
Configuration Write	Yes	No
Memory Read Line Multiple	Yes	Yes
Dual Address Cycle	Yes	Yes
Memory Read Line	Yes	Yes
Memory Write and Invalidate	Yes	Yes

9.1.4.2 Write Transactions

PCI Express-to-PCI Write transactions are Posted or Non-Posted, as defined in Table 9-5. The PEX 8112 accepts Posted transactions without requiring that a Completion be returned to the PCI Express interface. Non-Posted Writes do not generate a Completion until the transaction completes on the secondary (PCI) bus.

Table 9-5. Posted or Non-Posted PCI Express Writes

PCI Express Transaction	Forwarding
Memory Write Request	Posted
I/O Write Request	Non-Posted
Type 0 Configuration Write Request	Not forwarded
Type 1 Configuration Write Request	Non-Posted

Memory Write Request

A PCI Express-to-PCI Memory Write Request is performed as a PCI Memory Write or Memory Write and Invalidate transaction. When the PEX 8112 accepts each PCI Express Memory Write Request TLP, the Posted Write queue issues a Write Request, consisting of the following:

- Address (64 bits)
- Byte Enables for the first and last DWORDs
- TLP total Byte Count (10 bits)
- Sequence Number (6 bits)

The *PCI Express Base r1.0a* states that no TLPs can cross a 4-KB Address Boundary space; therefore, boundary checking does not need be performed when each Write Request is forwarded to the PCI Bus. When a TLP crosses a 4-KB Address Boundary space, it is treated as a malformed TLP. When the TLP Controller's Posted Write Data queue fills to capacity, the PCI Express Master stops sending data.

After transaction ordering requirements on the PCI Bus are met, the PEX 8112 requests the secondary PCI Bus. When the grant is received and the bus is idle, the PEX 8112 drives FRAME#, and the address and command. On the following Clock cycle, the first Data word is driven onto the bus and IRDY# is asserted. Data is transferred to the PCI Target when TRDY# is asserted, and continues transferring until the last word is read from the queue. When a Target Disconnect is detected, the current burst terminates. If there is data remaining in the queue, another Burst Write is initiated with the updated address. This Burst Write continues until the queue is empty, indicating the end of the Write transaction.

When a PCI Express-to-PCI Posted Write terminates with a PCI Target Abort, PCI Master Abort, or PCI Retry Abort, the remaining data is read from the queue and discarded. An ERR_NONFATAL message is sent to the PCI Express Root Complex, if enabled by the **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit.

Translation to Memory Write and Invalidate

The PEX 8112 supports translation of PCI Express Memory Write Requests to PCI Memory Write and Invalidate (MWI) transactions. The **PCI Command** register *Memory Write and Invalidate* bit must be set, and the **PCI Cache Line Size** register must be set to a supported value. The MWI command can be used only when the PCI Express Byte Enables are contiguous. The address, Write Request length, and first and last Byte Enables of each request are used to determine whether an MWI command can be used. The transaction length is loaded into an internal Counter and compared to the Cache Line Size. An MWI transaction is initiated when the following three conditions exist:

- Write Request contains at least the number of bytes indicated by the Cache Line Size
- Write Request starts at a Cache Line boundary
- All Byte Enables are asserted

An internal Counter is decremented as each word is transferred to the PCI Target. At each Cache Line boundary, the Counter is used to determine whether there are at least the number of Cache Line Size bytes remaining. If the necessary number of Cache Line size bytes are present, the MWI burst continues; otherwise, the MWI terminates and a Memory Write command transfers the remaining bytes.

When a Memory Write Request does not begin or end on a Cache Line boundary, the request is segmented into multiple transactions. The bytes up to the first Cache Line boundary are transferred using a Memory Write command. An MWI transaction is then used to transfer the Write data beginning on the aligned Cache Line boundary, including all subsequent complete cache lines up to the final aligned Cache Line boundary contained in the original Memory Write Request. A Memory Write transaction is then used to transfer the remaining bytes of the original Memory Write Request.

I/O and Configuration Writes

PCI Express I/O Writes and Type 1 Configuration Writes are Non-Posted Write transactions. *That is*, the Completion TLP is not returned to the primary (PCI Express) interface until the transaction completes on the secondary (PCI) interface. The forwarding address range of the I/O Writes is determined by the **I/O Base** and **I/O Limit** registers and **Bridge Control** register *ISA Enable* and *VGA Enable* bits.

When the PEX 8112 accepts each PCI Express I/O Write or Type 1 Configuration Write Request TLP, the Non-Posted Transaction queue issues a Write Request, consisting of the following:

- Transaction type
- Address (32 bits)
- Byte Enables for a single DWORD
- TLP total Byte Count (always a value of 1)
- Sequence number (6 bits)

Because all I/O Writes and Type 1 Configuration Writes are 1 DWORD in length, this DWORD is always the first and last DWORD. These Write transactions complete on the PCI Bus, before the Completion TLP is returned to the PCI Express interface.

PCI Express I/O Write Requests are translated into PCI I/O Write transactions. PCI Express Configuration Writes are translated into PCI Configuration transactions. The Configuration Write address can be modified to indicate a Type 0, Type 1, or special cycle. Configuration transaction forwarding is discussed in Chapter 8, "Configuration Transactions."

After the transaction ordering requirements are met, the PEX 8112 requests the secondary (PCI) interface. When the grant is received and the bus is idle, the PEX 8112 drives FRAME#, and the address and command. On the following Clock cycle, the Data word is driven onto the bus and IRDY# is asserted. Data is transferred to the PCI Target when TRDY# is asserted, and the transaction terminates. Only single words are transferred for these transactions. When the transaction successfully completes on the secondary bus, a Completion TLP is transmitted to the PCI Express Master.

When the transaction terminates with a Master Abort, a Completion with Unsupported Request (UR) status is returned to the PCI Express interface and the data is discarded.

When the transaction terminates with a Target Abort, a Completion with Completer Abort status is returned to the PCI Express interface and the data is discarded. An ERR_NONFATAL message is sent to the Root Complex, if enabled by the **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit.

When the transaction terminates with a Retry, the PEX 8112 repeats the transaction until the data transfer is complete or an error condition is detected. When the PEX 8112 is unable to deliver Write data after the number of attempts determined by the **PCI Control** register *PCI Express-to-PCI Retry Count* field, a Completion with Completer Abort status is returned to the PCI Express interface, and the data is discarded. A ERR_NONFATAL message is sent to the Root Complex, if enabled by the **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit.

9.1.4.3 Read Transactions

PCI Express-to-PCI Read transactions are Prefetchable or Non-Prefetchable, as defined in Table 9-6. Because a PCI Express Read Request always specifies the number of bytes to read, the PEX 8112 never reads more data than requested. When translating a PCI Express Memory Read Request into a PCI transaction, the PEX 8112 uses its Prefetchable and Non-Prefetchable Memory windows to determine the proper PCI Read command to use.

Table 9-6. Prefetchable or Non-Prefetchable PCI Express-to-PCI Read Transactions

PCI Express Transaction	Prefetchable
Memory Read Request	Yes, when in Prefetchable space
I/O Read Request	Non-Prefetchable
Type 0 Configuration Read Request	Not forwarded
Type 1 Configuration Read Request	Non-Prefetchable

Non-Prefetchable Memory Read Transactions

When a PCI Express Memory Read falls within Non-Prefetchable Address space, the PEX 8112 uses the PCI Memory Read command to read the number of bytes requested in the PCI Express Memory Read Request. The forwarding address range is determined by the **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers and **Bridge Control** register *VGA Enable* bit.

Prefetchable Memory Read Transactions

When a PCI Express Memory Read falls within Prefetchable Address space, the PEX 8112 uses the PCI Memory Read, Memory Read Line, or Memory Read Line Multiple command. The command type is based upon the starting address and the number of bytes in the request. The PEX 8112 does not extend the length of the burst, but reads the number of bytes requested, as per the *PCI ExpressBridge r1.0*. (*That is*, the PEX 8112 does not prefetch data from the PCI Target, regardless of whether the data is located in Prefetchable Memory space.) (Refer to Table 9-7.)

Memory Read Line transactions are terminated at a Cache Line boundary when there is not at least one cache line of data remaining to read, or if the transaction can be converted to a Memory Read Line Multiple transaction. Any remaining words are read, using a Memory Read command.

Table 9-7. Prefetchable Memory Read Transactions

Command	Status
Memory Read	Used when less than a cache line of data is read.
Memory Read Line	Used when at least one cache line of data is read, and the starting address is not on a Cache Line boundary.
Memory Read Line Multiple	Used when at least one cache line of data is read, and the starting address is on a Cache Line boundary.

Memory Read Request

When the PEX 8112 accepts each PCI Express Memory Read Request, the Non-Posted Transaction queue issues a Read Request, consisting of the following:

- Transaction type (Memory Read)
- Address (64 bits)
- Byte Enables for the first and last DWORD
- TLP total Byte Count of (10 bits)
- Sequence Number (6 bits)

A Memory Read, Memory Read Line, or Memory Read Line Multiple command is performed on the PCI Bus, depending upon the starting address, Byte Enables, and Read Request length. After the transaction ordering requirements are met, the PEX 8112 requests the secondary (PCI) interface. When the grant is received and the bus is idle, the PEX 8112 drives FRAME# and the address and command. On the following Clock cycle, IRDY# is asserted. Read data is transferred to the PEX 8112 when TRDY# is asserted, and continues transferring until the Read Request length is satisfied or the Target disconnects. As the data is read from the PCI Bus, it is written to the Non-Posted Transaction Completion queue.

When the transaction terminates with a Master Abort, a Completion with UR status is returned to the PCI Express interface. When the transaction terminates with a Target Abort, a Completion with Completer Abort status is returned to the PCI Express interface. An ERR_NONFATAL messages is sent to the Root Complex, if enabled by the **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit.

When the transaction terminates with a Retry, the PEX 8112 repeats the transaction until the Data transfer is complete or an error condition is detected. When the PEX 8112 is unable to complete the Read transaction after the number of attempts specified by the **PCI Control** register *PCI-to-PCI Express Retry Count* field, a Completion with Completer Abort status is returned to the PCI Express interface. When a transaction terminates with a PCI Disconnect, the PEX 8112 starts a new Read transaction at the current address, and attempts to complete reading the requested number of bytes. After the transaction is complete, a Completion is transmitted to the PCI Express Master.

The PEX 8112 does not service a new Memory Read Request from the Host (performs Retries on the PCI Bus) until it receives a Completion from the previous Read Request sent by the Host or the PCI-to-PCI Express Retry Count is exceeded.

Memory Read Request Locked

A PCI Express Memory Read Request Locked is similar to a normal Memory Read Request. Refer to Chapter 11, “Exclusive (Locked) Access,” for details.

I/O and Configuration Reads

PCI Express I/O Reads and Type 1 Configuration Reads are Non-Prefetchable Read transactions. *That is*, the Byte Enable information is preserved and no additional bytes are requested. The forwarding address range of the I/O Reads is determined by the **I/O Base** and **I/O Limit** registers and **Bridge Control** register *ISA Enable* and *VGA Enable* bits.

When the PEX 8112 accepts each PCI Express I/O Read or Type 1 Configuration Read Request, the Non-Posted Transaction queue issues a Read Request, consisting of the following:

- Transaction type (I/O or Configuration Type 1 Read)
- Address (32 bits)
- Byte Enables for a single DWORD
- TLP total Byte Count (always a value of 1)
- Sequence Number (6 bits)

An I/O Read or Configuration Read command is performed on the PCI Bus. The Configuration Read address can be modified to indicate a Type 0, Type 1, or special cycle. Configuration transaction forwarding is discussed in Chapter 8, "Configuration Transactions."

After the transaction ordering requirements are met, the PEX 8112 requests the secondary (PCI) interface. When the grant is received and the bus is idle, the PEX 8112 drives FRAME#, and the address and command. On the following Clock cycle, IRDY# is asserted. Read data is transferred to the PEX 8112 when TRDY# is asserted, and the transaction terminates. Only single DWORDs are transferred for these transactions.

When the transaction terminates with a Master Abort, a Completion with UR status is returned to the PCI Express interface. When the transaction terminates with a Target Abort, a Completion with Completer Abort status is returned to the PCI Express interface. An ERR_NONFATAL message is sent to the Root Complex, if enabled by the **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit.

When the transaction terminates with a Retry, the PEX 8112 repeats the transaction until the Data transfer is complete or an error condition is detected. When the PEX 8112 is unable to complete the Read transaction after the number of attempts specified by the **PCI Control** register *PCI-to-PCI Express Retry Count* field, a Completion with Timeout status is returned to the PCI Express interface. After the transaction is complete, a Completion is transmitted to the PCI Express Master.

The PEX 8112 does not service a new I/O Read Request or Type 1 Configuration Read from the Host (performs Retries on the PCI Bus) until it receives a Completion from the previous Read Request sent by the Host or the PCI-to-PCI Express Retry Count is exceeded.

9.1.5 Forward Bridge PCI-to-PCI Express Forwarding (Upstream)

9.1.5.1 Transaction Types

Table 9-8 defines the PCI transactions forwarded upstream to the PCI Express interface.

Table 9-8. PCI Transactions Forwarded Upstream to PCI Express Interface

Secondary Bus – PCI Command	Primary Bus – PCI Express Command
Memory Write or Memory Write and Invalidate	Memory Write Request
Memory Read, Memory Read Line or Memory Read Line Multiple	Memory Read Request
I/O Write	I/O Write Request
I/O Read	I/O Read Request

9.1.5.2 Write Decomposition

PCI Write transactions transfer Byte Enables with every Data phase; however, the PCI Express interface supports Byte Enables only on the first and last DWORDs of a request. Furthermore, non-contiguous Byte Enables are permitted only for requests of 1 or 2 DWORDs in length, and requests with no Byte Enables set must use a length of 1 DWORD. Therefore, in certain cases, the PEX 8112 must break up PCI Write Requests into multiple PCI Express requests. Byte Enables are always set in PCI Memory Write and Invalidate transactions; therefore, these transactions are not broken up into two separate transactions due to non-contiguous Byte Enables.

PCI Express Write transactions cannot cross 4-KB Address boundaries; therefore, PCI Writes are terminated with a Disconnect at 4-KB boundaries. Additionally, PCI Writes are terminated with a Disconnect when the Maximum Payload Size is reached.

9.1.5.3 Read Decomposition

PCI Express Read transactions cannot cross 4-KB Address boundaries; therefore, PCI Reads that cross a 4-KB Address Boundary space are broken up into multiple PCI Express Read transactions. When a PCI Read Request crosses a 4-KB Address Boundary space, the PEX 8112 disconnects at the boundary.

9.1.5.4 PCI Express Header Field Formation Rules

Table 9-9 defines the PCI Express Header Field Formation rules.

Table 9-9. PCI Express Header Field Formation Rules

Header Item	Rule
Fmt[1:0]	Single address PCI cycles (below the 4-GB Address Boundary space) use a 3-DWORD Header. Dual Address cycles (at or above the 4-GB boundary) use a 4-DWORD Header. Write Requests use a request format with data.
Type[4:0]	Populated, based upon the command translations described in Section 9.1.4.1.
TC[3:0]	For requests, this field must be cleared to 0. For Completions, this field must contain the value supplied in the corresponding request.
Attr[1:0]	These bits include the *Relaxed Ordering* and *No Snoop* attributes. Always cleared to 0.
TD	Cleared to 0. The PEX 8112 does ***not support*** End-to-end Cyclic Redundancy Check (ECRC) in the TLP Digest.
EP	Endpoint. Set to 1 when the PEX 8112 is forwarding an Uncorrectable Data error from the PCI Bus.
Length[9:0]	PCI Write or Read Request length, rounded up to nearest DWORD-aligned boundary.
Requester ID[15:0]	Assigned by the PEX 8112, comprised of the Bus Number, Device Number, and Function Number.
Tag[7:0]	Sequentially assigned by the PEX 8112.
First DWORD Byte Enable[3:0] and Last DWORD Byte Enable[3:0]	First and last Byte Enables.
Address[63:2] (4-DWORD Header) or Address[31:2] (3-DWORD Header)	Transaction DWORD starting address. Value is derived from the Byte address of the PCI transaction, by rounding the address down to the nearest DWORD-aligned boundary.

9.1.5.5 Requester ID and Tag

The PEX 8112 uses the Bus Number (from the **Secondary Bus Number** register), Device Number (always a value of 0), and Function Number (always a value of 0) to create the Requester ID. The 8-bit Tag is created by the TLP Controller, and is unique for each transaction.

Requester ID

15 – 8	7 – 3	2 – 0
Bus Number	Device Number	Function Number

Tag

7 – 0
Tag

9.1.5.6 Memory Write or Memory Write and Invalidate

Memory Write or Memory Write and Invalidate transactions are performed as a PCI Express Memory Write Request. The forwarding address range is determined by the **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers and **Bridge Control** register *VGA Enable* bit. Writes cannot cross 4-KB Address boundaries. Write data posting is required for these transactions. The PEX 8112 terminates these transactions with a Retry when the PEX 8112 is locked from the PCI Express interface.

When the PEX 8112 determines that a PCI Write transaction is to be forwarded to the PCI Express interface, DEVSEL# and TRDY# are asserted, assuming that there is sufficient space in the 8-DWORD buffer. When there is insufficient Buffer space, the PEX 8112 responds with a Retry. When there is sufficient space, the PEX 8112 accepts Write data until one of the following occurs:

- PCI Master terminates the transaction by de-asserting FRAME#
- 4-KB Address Boundary space is reached
- Buffer fills and the Secondary Latency Timer (Forward Bridge mode) or PCI Bus Latency Timer (Reverse Bridge mode) times out
- Maximum Payload Size is reached
- No Byte Enables, or Partial Byte Enables, are detected during Memory Write

When one of these events occurs, the PEX 8112 terminates the PCI transaction with a Disconnect. If no Byte Enables, or partial Byte Enables, are asserted during a DWORD transaction, the Write transaction must be broken up into two separate transactions. The data with no Byte Enables, or partial Byte Enables and the corresponding address are written into the Posted Write Data queue as a new transaction.

The TLP Controller prioritizes these transactions. When the Posted Write's Sequence Number is less than that of the Non-Posted transaction, the Posted Write is performed first. When the Posted Write's Sequence Number is greater than that of the Non-Posted transaction, the transactions alternate.

9.1.5.7 Delayed Transactions

Non-Posted PCI transactions (except Memory Write transactions) are performed as Delayed transactions on the PCI Bus. A Delayed transaction occurs when the PEX 8112 responds to a Non-Posted transaction with a Retry, and forwards the request to the PCI Express interface. When the associated Completion returns from the PCI Express Target, the PEX 8112 buffers the Completion until the PCI Master Retries the transaction. The following information is latched from the PCI Bus and stored into the Non-Posted Transaction queue when a new Delayed transaction is detected:

- Address
- Address Parity
- Command
- Byte Enables
- Data for Write transactions
- Data Parity for Write transactions

After latching the above information, the PCI transaction terminates with a Retry. The PEX 8112 then transmits the Delayed transaction request upstream, to the PCI Express interface:

- When the Delayed request is a Read (Memory, I/O, or Configuration), the Read data is read from the PCI Express interface and stored in the TLP Controller
- When the Delayed request is a Write (I/O or Configuration), the Write data is delivered to the PCI Express Target

At the completion of a Delayed Read, the request in the Non-Posted Transaction queue is tagged as *complete*. The request is removed from the Non-Posted Transaction queue when the transaction is Retried and completed on the PCI Bus.

The PEX 8112 differentiates between PCI transactions by comparing the current transaction with the transaction stored in the Non-Posted Transaction queue. When the **Bridge Control** register *Secondary Parity Error Response Enable* bit is cleared to 0, the Address and Data Parity bits are ignored during the comparison. The Byte Enables are ignored when the Read is from the Prefetchable Memory space. When the compare matches a Non-Posted Transaction queue entry, but the transaction is not completed on the PCI Express interface, the transaction is not re-queued, but terminates with a Retry. When the compare matches a Non-Posted Transaction queue entry, and the transaction completed on the PCI Express interface, the transaction completes on the PCI Bus. For a Non-Posted Write, TRDY# is returned, thereby completing the transaction. For a Read transaction, Read data is returned to the PCI Master.

The PEX 8112 can queue up to four delayed transactions. These transactions are performed on the PCI Express interface in the order that they occurred on the PCI Bus. After Non-Posted Writes are completed on the PCI Express interface, they are completed on the PCI Bus in the order that the PCI Master Retries them. Non-Posted Reads are always completed on the PCI Bus in the order they complete on the PCI Express interface.

A bridge is permitted to discard a Delayed request. The PEX 8112 never discards a Delayed request that is not completed on the PCI Express interface. A bridge is allowed to discard a Delayed Completion in the following two cases only:

- If Prefetched data remains in the Delayed Read Data queue when the PCI Master terminates the Read transaction, the data is discarded.
- Each entry in the Non-Posted Transaction queue has an associated Secondary Discard Timer. The timer is activated when a Read or Write transaction completes on the PCI Express interface. If the PCI Master does not Retry the Delayed transaction before the timer times out, the Delayed request and Completion are removed from the Non-Posted Transaction queue. The **Bridge Control** register *Discard Timer Status* bit is set. In addition, the PEX 8112 transmits an Error message to the PCI Express interface, if enabled, by the **Bridge Control** register *Discard Timer SERR# Enable* and **PCI Command** register *SERR# Enable* bits.

9.1.5.8 Memory Read, Memory Read Line, or Memory Read Line Multiple

Memory Read, Memory Read Line, or Memory Read Line Multiple transactions are performed as a PCI Express Memory Read Request. The forwarding address range is determined by the **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers and **Bridge Control** register *VGA Enable* bit. Reads cannot cross 4-KB Address boundaries. This transaction is performed as a Delayed transaction on the PCI Bus.

When the PEX 8112 determines that a PCI Read transaction is to be forwarded to the PCI Express interface, DEVSEL# and STOP# are asserted, indicating a Retry. The Address, Address Parity, Command, and Byte Enables are stored in an entry in the Non-Posted Transaction queue, assuming that there is sufficient space in the queue. If there is insufficient space, the transaction is Retried without entering the transaction into the queue.

After the request reaches the top of the Non-Posted Transaction queue, a Memory Read Request is transmitted to the PCI Express interface. The number of bytes requested from the PCI Express interface is determined by the PCI command, the address space, and the **Device-Specific Control** register *Blind Prefetch Enable* bit. (Refer to Table 9-10.)

When the starting address and Read Request length causes the Read to cross a 4-KB Address Boundary space, the Read Request length is truncated so that the 4-KB Address Boundary space is not crossed. When the Read Request length is greater than the value of the **PCI Express Device Control** register *Maximum Read Request Size* field, the request length is truncated to the specified size. When the Read is to Non-Prefetchable Memory, the Byte Enables are passed from the PCI Bus. When the Read is to Prefetchable memory, all Byte Enables are asserted in the PCI Express request.

When the Memory Read Request does not successfully complete on the PCI Express interface, the Read Request entry in the Non-Posted Transaction queue is appropriately marked. When the transaction is Retried on the PCI Bus, it terminates with a Target Abort response. When the Memory Read Request successfully completes on the PCI Express interface, the Read Request entry in the Non-Posted Transaction queue is marked as *complete*.

When the transaction successfully completes on the PCI Express interface, and all ordering constraints with Posted Write transactions are satisfied, the PEX 8112 transfers data to the PCI Master when the Master Retries the transaction. The PEX 8112 asserts TRDY# and drives data until the final DWORD is transferred from the queue to the PCI Master. When the Master terminates the transaction before all queue data is transferred, the remaining data is read from the queue and discarded.

Table 9-10. Bytes Requested by PCI Express Interface Determined by PCI Command, Address Space, Register, and Bit after Request Reaches Top of Queue

PCI Transaction	Address Space	Blind Prefetch Enable	Number of DWORDs Requested
Memory Read	Non-prefetchable	–	1
	Prefetchable	0	1
	Prefetchable	1	Cache Line Size
Memory Read Line	–	–	Cache Line Size
Memory Read Line Multiple	–	–	2 Cache Line Sizes

Blind Prefetch

When Blind Prefetch mode is enabled (**Device-Specific Control** register *Blind Prefetch Enable* bit is set), the PEX 8112 can prefetch a user-defined data block from the Host when a Memory Read transaction is performed, instead of one DWORD at a time in standard operation. Prefetching can improve Read performance, because the PEX 8112 can burst its Prefetchable data onto the PCI Bus when the Endpoint requests it. The PEX 8112 discards remaining unused data. The Prefetch Size can be programmed from 0 to 4 KB of data, by way of the **PCI Control** register *Programmed Prefetch Size* field.

9.1.5.9 I/O Write

I/O Write transactions are performed as a PCI Express I/O Write Request. The forwarding address range is determined by the **I/O Base** and **I/O Limit** registers and **Bridge Control** register *ISA Enable* and *VGA Enable* bits. This transaction is performed as a Delayed transaction on the PCI Bus. Posting these transactions is not permitted. A Completion must be received from the PCI Express Target before the transaction is completed on the PCI Bus.

When the PEX 8112 determines that a PCI I/O Write transaction is to be forwarded to the PCI Express interface, DEVSEL# and STOP# are asserted, indicating a Retry. The Address, Address Parity, Command, Data, Data Parity, and Byte Enables are stored into an entry in the Non-Posted Transaction queue, assuming that there is sufficient space in the queue. If there is insufficient space, the transaction is Retried without entering the transaction into the queue.

After the request reaches the top of the Non-Posted Transaction queue, an I/O Write Request is transmitted to the PCI Express interface. The Byte Enables are passed through from the PCI Bus, and only 1 DWORD is transferred.

When the Write Request does not successfully complete on the PCI Express interface, the Write Request entry in the Non-Posted Transaction queue is appropriately marked. When the transaction is Retried on the PCI Bus, it terminates with a Target Abort response. When the I/O Write Request successfully completes on the PCI Express interface, the I/O Write Request entry in the Non-Posted Transaction queue is marked as *complete*.

When the transaction successfully completes on the PCI Express interface, the PEX 8112 asserts TRDY# to complete the transaction when the Master Retries the transaction. The I/O Write Request is removed from the Non-Posted Transaction queue when the PCI Master Retries the transaction and the transaction completes (successfully or not) on the PCI Express interface.

9.1.5.10 I/O Read

I/O Read transactions are performed as a PCI Express I/O Read Request. The forwarding address range is determined by the **I/O Base** and **I/O Limit** registers and **Bridge Control** register *ISA Enable* and *VGA Enable* bits. This transaction is performed as a Delayed transaction on the PCI Bus.

When the PEX 8112 determines that a PCI I/O Read transaction is to be forwarded to the PCI Express interface, DEVSEL# and STOP# are asserted, indicating a Retry. The Address, Command, Address Parity, and Byte Enables are stored into an entry in the Non-Posted Transaction queue, assuming that there is sufficient space in the queue. If there is insufficient space, the transaction is Retried without entering the transaction into the queue.

After the request reaches the top of the Non-Posted Transaction queue, an I/O Read Request is transmitted to the PCI Express interface. The Byte Enables are passed through from the PCI Bus, and only 1 DWORD is requested. When all ordering constraints with Posted Write transactions are satisfied, the PEX 8112 transfers data to the PCI Master when the Master Retries the transaction. The PEX 8112 asserts TRDY# and drives a single DWORD of data from the queue to the PCI Master.

If the I/O Read Request does not successfully complete on the PCI Express interface, the Read Request entry in the Non-Posted Transaction queue is appropriately marked. When the transaction is Retried on the PCI Bus, it terminates with a Target Abort response. When the I/O Read Request successfully completes on the PCI Express interface, the Read Request entry in the Non-Posted Transaction queue is marked as *complete*.

9.1.6 Forward Bridge PCI Transaction Terminations

Table 9-11 defines the transaction termination methods used by PCI Masters. Table 9-12 defines the transaction termination methods used by PCI Targets.

Table 9-11. PCI Master Transaction Termination Methods

Termination Methods	Description
Normal Termination	The Master de-asserts FRAME# at the beginning of the last Data phase and de-asserts IRDY# at the end of the last Data phase if the Target asserts TRDY# or STOP#.
Master Abort	If the Master does not detect that DEVSEL# is asserted from the Target within five Clock cycles after asserting FRAME#, the transaction terminates with a Master Abort. If FRAME# remains asserted, the Master de-asserts FRAME# on the next cycle, then de-asserts IRDY# on the following cycle. IRDY# must be asserted in the same cycle in which FRAME# de-asserts. If FRAME# is de-asserted, IRDY# can be de-asserted on the next Clock cycle following detection of the Master Abort condition.

Table 9-12. PCI Target Transaction Termination Methods

Termination Methods	Description
Normal Termination	TRDY# and DEVSEL# are asserted in conjunction with FRAME# de-assertion and IRDY# assertion.
Target Retry	STOP# and DEVSEL# asserted without TRDY# during the first Data phase. No Data transfers occur during the transaction, and the Master must repeat the transaction.
Target Disconnect with Data	STOP# and DEVSEL# asserted with TRDY#, which indicates that this is the last transfer of the transaction. If FRAME# is de-asserted, this is considered a normal termination, although STOP# is asserted.
Target Disconnect without Data	STOP# and DEVSEL# are asserted without TRDY# after previous data transfers occurred, which indicates that no more Data transfers occur during this transaction.
Target Abort	STOP# is asserted without DEVSEL# and TRDY#, which indicates that the Target is never able to complete this transaction. DEVSEL# must be asserted for at least one Clock cycle during the transaction; otherwise, the Master detects a Master Abort.

9.1.6.1 PCI Master Termination Initiated by PEX 8112

The PEX 8112, as a PCI Master, uses normal termination if the Target asserts DEVSEL# within five Clock cycles of FRAME# assertion. As a PCI Master, the PEX 8112 terminates a transaction when any of the following occur:

- During a Delayed Write transaction (I/O or Configuration Write), a single DWORD is delivered
- During a Non-Prefetchable Read (Memory, I/O, or Configuration), a single DWORD is read from the Target
- In the case of a Prefetchable Read transaction, the number of words requested in the PCI Express request are read from the PCI Target
- In the case of a Posted Write transaction, the last word for the transaction is written to the PCI Target
- In the case of a Burst transfer, with the exception of Memory Write and Invalidate transactions, the Master Latency Timer expires and the PCI Bus Grant is de-asserted
- Target terminates the transaction with a Retry, Disconnect, or Target Abort

When a Posted Write or Prefetchable Read transaction terminates because of a latency timeout, another transaction is initiated to complete the transfer.

9.1.6.2 PCI Master Abort Received by PEX 8112

If the PEX 8112, as a PCI Master, does not detect that DEVSEL# is asserted from the Target within five Clock cycles after asserting FRAME#, the PEX 8112 terminates the transaction with a Master Abort. In Forward Bridge mode, the **Secondary Status** register *Secondary Received Master Abort* bit is set. In Reverse Bridge mode, the **PCI Status** register *Received Master Abort* bit is set. Refer to Chapter 10, "Error Handling," and Chapter 11, "Exclusive (Locked) Access," for further details.

9.1.6.3 Delayed Write Target Termination Response

When the PEX 8112 initiates a Delayed Write transaction on the PCI Bus, it responds to certain Target terminations as defined in Table 9-13.

Table 9-13. PEX 8112 Response to Target Terminations upon Delayed Write Transactions

Target Termination	PEX 8112 Response
Normal	Return Completion with Successful Completion status to the PCI Express interface.
Target Retry	Repeat Write transaction for up to 2^{24} attempts.
Target Disconnect	Return Completion with Successful Completion status to the PCI Express interface.
Target Abort	Return Completion with Completer Abort status to the PCI Express interface. Discard Delayed Write Request. **Forward Bridge mode** – Set the **Secondary Status** register *Secondary Received Target Abort* bit. **Reverse Bridge mode** – Set the **PCI Status** register *Received Target Abort* bit.

9.1.6.4 Posted Write Target Termination Response

When the PEX 8112 initiates a Posted Write transaction on the PCI Bus, it responds to certain Target terminations as defined in Table 9-14.

Table 9-14. PEX 8112 Response to Target Terminations upon Posted Write Transactions

Target Termination	PEX 8112 Response
Normal	No action.
Target Retry	Repeat Write transaction for up to 2^{24} attempts.
Target Disconnect	Initiate Write transaction to deliver remaining Posted Write data.
Target Abort	Discard Posted Write data. **Forward Bridge mode** – Set the **Secondary Status** register *Secondary Received Target Abort* bit. **Reverse Bridge mode** – Set the **PCI Status** register *Received Target Abort* bit.

9.1.6.5 Delayed Read Target Termination Response

When the PEX 8112 initiates a Delayed Read transaction on the PCI Bus, it responds to certain Target terminations as defined in Table 9-15.

Table 9-15. PEX 8112 Response to Target Terminations upon Delayed Read Transactions

Target Termination	PEX 8112 Response
Normal	Return Completion with Successful Completion status to the PCI Express interface.
Target Retry	Repeat Read transaction for up to 2^{24} attempts.
Target Disconnect	Initiate Read transaction to obtain remaining Read data.
Target Abort	Return Completion with Completer Abort status to the PCI Express interface. Discard Delayed Read Request. **Forward Bridge mode** – Set the **Secondary Status** register *Secondary Received Target Abort* bit. **Reverse Bridge mode** – Set the Set the **PCI Status** register *Received Target Abort* bit.

9.1.6.6 Target Retry Initiated by PEX 8112

The PEX 8112 returns a Target Retry to a PCI Master when any of the following conditions are met:

- Delayed Write transactions
  - Transaction is entering the Non-Posted Transaction queue
  - Transaction is stored into the Non-Posted Transaction queue; however the transaction is not completed on the PCI Express interface
  - Non-Posted Transaction queue is full, and the transaction cannot be queued
  - Transaction with the same address and bus command is queuing
  - Locked sequence is propagated across the PEX 8112, and the Write transaction is not a Locked transaction
- Delayed Read transactions
  - Transaction is entering the Non-Posted Transaction queue
  - Transaction is stored in the Non-Posted Transaction queue, but the Read data is not yet available
  - Read was received from the PCI Express interface; however, a Posted Write transaction precedes it
  - Non-Posted Transaction queue is full, and the transaction cannot be queued
  - Transaction with the same address and bus command was queued
  - Locked sequence is propagated across the PEX 8112, and the Read transaction is not a Locked transaction
  - PEX 8112 is currently discarding previously prefetched Read data
- Posted Write transactions
  - PCI-to-PCI Express 8-DWORD Write buffer is not empty
  - Locked sequence is propagated across the PEX 8112, and the Write transaction is not a Locked transaction

9.1.6.7 Target Disconnect Initiated by PEX 8112

The PEX 8112 returns a Target Disconnect to a PCI Master when any of the following conditions are met:

- A 4-KB Address Boundary space or Cache Line boundary is reached
- 8-DWORD Posted Write buffer fills and the Secondary Latency Timer (Forward Bridge mode) or PCI Bus Latency Timer (Reverse Bridge mode) times out
- 8-DWORD Read buffer becomes empty and the Secondary Latency Timer (Forward Bridge mode) or PCI Bus Latency Timer (Reverse Bridge mode) times out
- Maximum Payload Size is reached
- Byte Enables not set for Posted Write

9.1.6.8 Target Abort Initiated by PEX 8112

The PEX 8112 returns a Target Abort to a PCI Master when the PEX 8112 is unable to obtain read data from, or write data to, the PCI Express interface. Refer to Chapter 10, "Error Handling," for further details.

9.2 Reverse Bridge Operation

In Reverse Bridge mode, the PEX 8112 presents a Type 1 Configuration Space Header on the PCI Bus. There are no PCI-Compatible Configuration registers available on the PCI Express interface. Three sets of Type 1 Configuration Space Header registers define the bridging operation between the PCI Bus and PCI Express interface. (Refer to Table 9-16.)

The PEX 8112 also supports one PCI Base Address register (BAR), which allows a PCI Express or PCI Master to access internal Configuration registers or shared memory. During bus enumeration, the addresses corresponding to the BAR are excluded from the bridging ranges of the six registers referenced in Table 9-16.

Table 9-16. Type 1 Configuration Space Header Register Sets that Define Bridging Operation between PCI Bus and PCI Express Interface

Register Set	Description
I/O Base and **I/O Limit**	When I/O transactions on the PCI Bus fall within the range specified by these registers, the transactions are forwarded to the PCI Express interface. When I/O transactions on the PCI Express interface fall outside the range specified by these registers, the transactions are forwarded to the PCI Bus.
Memory Base and **Memory Limit**	When Non-Prefetchable Memory transactions on the PCI Bus fall within the range specified by these registers, the transactions are forwarded to the PCI Express interface. When Non-Prefetchable Memory transactions on the PCI Express interface fall outside the range specified by these registers, the transactions are forwarded to the PCI Bus.
Prefetchable Memory Base and **Prefetchable Memory Limit**	When Prefetchable Memory transactions on the PCI Bus fall within the range specified by these registers, the transactions are forwarded to the PCI Express interface. When Prefetchable Memory transactions on the PCI Express interface fall outside the range specified by these registers, the transactions are forwarded to the PCI Bus.

9.2.1 Reverse Bridge PCI-to-PCI Express Forwarding (Downstream)

9.2.1.1 Transaction Types

Table 9-17 defines the PCI transactions forwarded to the PCI Express interface. Table 9-18 defines the PCI transactions performed on the primary bus.

The data paths and control logic for Reverse Bridge mode are the same as those used for Forward Bridge mode, except that address decoding based upon the Configuration registers are located on the PCI Bus. Posted, Non-Posted and Delayed transactions are handled in the same way as for Forward Bridge mode.

Table 9-17. PCI Transactions Forwarded to Secondary Bus (PCI Express)

Primary Bus – PCI Command	Secondary Bus – PCI Express Command
Memory Write or Memory Write and Invalidate	Memory Write Request
Memory Read, Memory Read Line, or Memory Read Line Multiple	Memory Read Request
Memory Read, Memory Read Line, or Memory Read Line Multiple, LOCK# asserted	Memory Read Request – Locked
I/O Write	I/O Write Request
I/O Read	I/O Read Request
Type 1 Configuration Write	Type 0 or Type 1 Configuration Write Request
Type 1 Configuration Read	Type 0 or Type 1 Configuration Read Request

Table 9-18. PCI Transactions Performed on Primary Bus (PCI)

Transaction	PEX 8112 Master on Primary Bus	PEX 8112 Target on Primary Bus
Interrupt Acknowledge	No	No
Special Cycle	No	No
I/O Write	Yes	Yes
I/O Read	Yes	Yes
Memory Write	Yes	Yes
Memory Read	Yes	Yes
Configuration Write	No	Yes
Configuration Read	No	Yes
Memory Write and Invalidate	Yes	Yes
Memory Read Line	Yes	Yes
Memory Read Line Multiple	Yes	Yes
Dual Address Cycle	Yes	Yes

Chapter 10 Error Handling

10.1 Forward Bridge Error Handling

When the PEX 8112 detects errors, it sets the appropriate error status bit [both Conventional PCI error bit(s) and PCI Express error status bit(s)], and optionally generates an error message on the PCI Express interface. Each error condition has a default error severity level, with a corresponding error message generated on the PCI Express interface.

Four Control register bits control Error message generation on the PCI Express interface:

- **PCI Command** register *SERR# Enable* bit
- **PCI Express Device Control** register *Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit
- **PCI Express Device Control** register *Correctable Error Reporting Enable* bit

PCI Express ERR_FATAL messages are enabled for transmission when the *SERR# Enable* or *Fatal Error Reporting Enable* bit is set. ERR_NONFATAL messages are enabled for transmission when either the *SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. ERR_COR messages are enabled for transmission when the *Correctable Error Reporting Enable* bit is set.

The **PCI Express Device Status** register *Fatal Error Detected*, *Non-Fatal Error Detected*, and *Correctable Error Detected* bits are set for the corresponding errors on the PCI Express interface, regardless of the *Error Reporting Enable* bits.

10.1.1 Forward Bridge PCI Express Originating Bus (Primary to Secondary)

This section describes error support for transactions that cross the PEX 8112 when the originating side is the PCI Express interface, and the destination side is the PCI Bus. When a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction must be considered as corrupt. Invert the parity for all data when completing the transaction on the PCI Bus.

Table 10-1 provides the translation the PEX 8112 must perform when the bridge forwards a Non-Posted PCI Express request (Read or Write) to the PCI Bus, and the request is immediately completed on the PCI Bus, either normally or with an error condition.

Table 10-1. Translation Performed when Bridge Forwards a Non-Posted PCI Express Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with Parity error (Reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

10.1.1.1 Received Poisoned TLP

When the PEX 8112 PCI Express interface receives a Write Request or Read Completion with poisoned data, the following occur:

- **PCI Status** register *Detected Parity Error* bit is set
- **PCI Status** register *Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PCI Command** register *Parity Error Response Enable* bit is set
- ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- Parity bit associated with each DWORD of data is inverted
- For a poisoned Write Request, the **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, and the PEX 8112 detects that PERR# is asserted when the PCI Target device detects the inverted parity

10.1.1.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI Bus, and an Uncorrectable PCI error is detected.

Immediate Reads

When the PEX 8112 forwards a Read Request (I/O, Memory, or Configuration) from the PCI Express and detects an Uncorrectable Data error on the secondary bus while receiving an immediate response from the Completer, the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- **Secondary Status** register *Secondary Detected Parity Error* bit is set
- PERR# is asserted on the secondary bus when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8112 continues to fetch data until the Byte Count is satisfied or the Target ends the transaction. When the PEX 8112 creates the PCI Express Completion, it forwards the Completion with Successful Completion status and poisons the TLP.

Posted Writes

When the PEX 8112 detects that PERR# is asserted on the secondary bus (PCI) while forwarding a non-poisoned Posted Write transaction from PCI Express, the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- After the error is detected, the remaining data is forwarded

Non-Posted Writes

When the PEX 8112 detects that PERR# is asserted on the secondary bus (PCI) while forwarding a non-poisoned Non-Posted Write transaction from the primary bus (PCI Express), the following occur:

- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- PCI Express Completion with Unsupported Request (UR) status is generated
- ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

10.1.1.3 PCI Address Errors

When the PEX 8112 forwards transactions from PCI Express-to-PCI, PCI Address errors are reported by SERR# assertion. When the PEX 8112 detects that SERR# is asserted, the following occur:

- **Secondary Status** register *Secondary Received System Error* bit is set
- ERR_FATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **Bridge Control** register *Secondary SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Secondary SERR# Enable* and *SERR# Enable* bits are set

10.1.1.4 PCI Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Secondary Status** register *Secondary Received Master Abort* bit is set
- ERR_NONFATAL message is generated on the PCI Express interface when the following conditions are met:
  - **Bridge Control** register *Master Abort Mode* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Master Abort Mode* and *SERR# Enable* bits are set

10.1.1.5 PCI Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Completion with UR status is returned on the PCI Express interface
- **Secondary Status** register *Secondary Received Master Abort* bit is set

10.1.1.6 PCI Target Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Secondary Status** register *Secondary Received Target Abort* bit is set
- ERR_NONFATAL message is generated on the PCI Express interface when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

10.1.1.7 PCI Target Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Completion with Completer Abort status is returned on the PCI Express
- **Secondary Status** register *Secondary Received Target Abort* bit is set
- **PCI Status** register *Signaled Target Abort* bit is set
- ERR_NONFATAL message is generated on the PCI Express interface when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

10.1.1.8 PCI Retry Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in the maximum number of PCI Retries (selectable in the **PCI Control** register), the following occur:

- Remaining data is discarded
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set

10.1.1.9 PCI Retry Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in the maximum number of PCI Retries (selectable in the **PCI Control** register), the following occur:

- Completion with the Completer Abort status is returned on the PCI Express interface
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set
- **PCI Status** register *Signaled Target Abort* bit is set

  Although a Target Abort has not occurred, the device-specific Retry Abort results in a Completer Abort being sent to the Root Complex. For consistency, the *Signaled Target Abort* bit is also set.

10.1.2 Forward Bridge PCI Originating Bus (Secondary to Primary)

This section describes error support for transactions that cross the PEX 8112 when the originating side is the PCI Bus, and the destination side is PCI Express. The PEX 8112 supports TLP poisoning as a Transmitter to permit proper forwarding of Parity errors that occur on the PCI Bus. Posted Write data received on the PCI Bus with bad parity is forwarded to the PCI Express interface as Poisoned TLPs.

Table 10-2 provides the error forwarding requirements for Uncorrectable Data errors that the PEX 8112 detects when a transaction targets the PCI Express interface.

Table 10-3 describes the PEX 8112's behavior on a PCI Delayed transaction that is forwarded by a bridge to the PCI Express interface as a Memory Read Request or an I/O Read/Write Request, and the PCI Express interface returns a Completion with UR or CA status for the request.

Table 10-2. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with Parity error	Write Request with poisoned TLP
Read Completion with Parity error in Data phase	Read Completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write Completion with Completer Abort Status

Table 10-3. PEX 8112 Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (upon Memory Read or I/O Read)	Target Abort	Normal Completion, return FFFF_FFFFh
Unsupported Request (upon I/O Write)	Target Abort	Normal Completion
Completer Abort	Target Abort	

10.1.2.1 Received PCI Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that it crosses the PEX 8112, and the PEX 8112 detects an Uncorrectable Data error on the secondary bus (PCI), the following occur:

- **Secondary Status** register *Secondary Detected Parity Error* status bit is set.
- If the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set, the transaction is discarded and is not forwarded to the PCI Express interface. The PERR# signal is asserted on the PCI Bus.
- If the **Bridge Control** register *Secondary Parity Error Response Enable* bit is not cleared, the data is forwarded to the PCI Express interface as a poisoned TLP. When the **PCI Command** register *Parity Error Response Enable* bit is set, the **PCI Status** register *Master Data Parity Error* bit is also set. The PERR# signal is not asserted on the PCI Bus.

Uncorrectable Data Error on Posted Write

When the PEX 8112 detects an Uncorrectable Data error on the secondary bus (PCI) for a Posted Write transaction that crosses the PEX 8112, the following occur:

- PCI PERR# signal is asserted when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- **Secondary Status** register *Secondary Detected Parity Error* status bit is set
- Posted Write transaction is forwarded to the PCI Express interface as a poisoned TLP
- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8112 forwards a non-poisoned Read Completion from PCI Express-to-PCI, and detects that PERR# is asserted by the PCI Master, the remainder of the Completion is forwarded.

When the PEX 8112 forwards a poisoned Read Completion from PCI Express-to-PCI, the PEX 8112 proceeds with the above-mentioned actions when it detects that the PERR# is signal asserted by the PCI Master; however, no error message is generated on the PCI Express interface.

Uncorrectable Address Error

When the PEX 8112 detects an Uncorrectable Address error, and Parity error detection is enabled by way of the **Bridge Control** register *Secondary Parity Error Response Enable* bit, the following occur:

- Transaction is terminated with a Target Abort
- **Secondary Status** register *Secondary Detected Parity Error* status bit is set, independent of the setting of the **Bridge Control** register *Secondary Parity Error Response Enable* bit
- **Secondary Status** register *Secondary Signaled Target Abort* bit is set
- ERR_FATAL message is generated on the PCI Express interface when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

10.1.2.2 Unsupported Request Completion Status

The PEX 8112 provides two methods for handling a PCI Express Completion received with UR status in response to a request originated by the PCI Bus. The response is controlled by the **Bridge Control** register *Master Abort Mode* bit. In either case, the **PCI Status** register *Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and a UR is not considered to be an error.

When a Read transaction initiated on the PCI results in the return of a Completion with UR status, the PEX 8112 returns FFFF_FFFFh to the originating Master and terminates the Read transaction on the originating bus normally (by asserting TRDY#).

When a Non-Posted Write transaction results in a Completion with UR status, the PEX 8112 completes the Write transaction on the originating bus normally (by asserting TRDY#) and discards the Write data.

Master Abort Mode Bit Set

When the **Bridge Control** register *Master Abort Mode* bit is set, the PEX 8112 signals a Target Abort to the originating Master of an Upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a Completion with UR status. In addition, the **Secondary Status** register *Secondary Signaled Target Abort* bit is set.

10.1.2.3 Completer Abort Completion Status

When the PEX 8112 receives a Completion with Completer Abort (CA) status on the primary bus (PCI Express) in response to forwarded Non-Posted PCI transactions, the **PCI Status** register *Received Target Abort* bit is set. A CA response can result in a Delayed Transaction Target Abort on the PCI Bus. The PEX 8112 provides data to the requesting PCI agent, up to the point where data was successfully returned from the primary bus (PCI Express), then signals a Target Abort. The **Secondary Status** register *Secondary Signaled Target Abort* bit is set when signaling a Target Abort to a PCI agent.

10.1.3 Forward Bridge Timeout Errors

10.1.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows Requesters to abort a Non-Posted request when a Completion does not arrive within a reasonable length of time. Bridges, when acting as Masters on the PCI Express interface, on behalf of internally generated requests or when forwarding requests from a secondary bus, behave as endpoints for requests of which they take ownership.

When a Completion Timeout is detected and the link is up, the PEX 8112 responds as if a Completion with UR status is received. The following occur:

- ERR_NONFATAL message is generated on the primary bus (PCI Express) when the following conditions are met:
  - **PCI Command** register *SERR# Enable* bit is set –or–
  - **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set

When the link is down, the **PCI Control** register *PCI Express-to-PCI Retry Count* field determines the number of PCI Retries before a Master Abort is returned to the PCI Bus.

10.1.3.2 PCI Delayed Transaction Timeout Errors

The PEX 8112 includes Delayed Transaction Timers for each queued Delayed transaction. When a Delayed transaction timeout is detected, the following occur:

- ERR_NONFATAL message is generated on the PCI Express interface when the following conditions are met:
  - **Bridge Control** register *Discard Timer SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *SERR# Enable* bit is set
- **Bridge Control** register *Discard Timer Status* bit is set

10.1.4 Forward Bridge “Other” Errors

PCI devices assert SERR# when detecting errors that compromise system integrity. When the PEX 8112 detects that SERR# is asserted on the secondary (PCI) bus, the following occur:

- **Secondary Status** register *Secondary Received System Error* bit is set
- ERR_FATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **Bridge Control** register *Secondary SERR# Enable* bit is set
  - **PCI Command** register *SERR# Enable* bit or **PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
- **PCI Status** register *Signaled System Error* bit is set when the *Secondary SERR# Enable* and *SERR# Enable* bits are set

10.2 Reverse Bridge Error Handling

When the PEX 8112 detects errors, it sets the appropriate error status bit [both Conventional PCI error bit(s) and PCI Express error status bit(s)]. PCI Express Error messages are not generated in Reverse Bridge mode.

10.2.1 Reverse Bridge PCI Express Originating Bus (Secondary to Primary)

This section describes error support for transactions that cross the PEX 8112 when the originating side is the PCI Express (secondary) interface, and the destination side is the PCI (primary) interface.

Table 10-4 provides the translation the PEX 8112 performs when it forwards a Non-Posted PCI Express request (Read or Write) to the PCI Bus, and the request is immediately completed on the PCI Bus, either normally or with an error condition.

Table 10-4. PEX 8112 Translation – Non-Posted PCI Request

Immediate PCI Termination	PCI Express Completion Status
Data Transfer with Parity error (Reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Master Abort	Unsupported Request
Target Abort	Completer Abort

10.2.1.1 Received Poisoned TLP

When the PCI Express interface receives a Write Request or Read Completion, and the data is poisoned, the following occur:

- **Secondary Status** register *Secondary Detected Parity Error* bit is set
- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set
- Parity bit associated with each DWORD of data is inverted
- For a poisoned Write Request, the **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set, and the PEX 8112 detects that PERR# is asserted when the PCI Target device detects the inverted parity

10.2.1.2 PCI Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PCI Bus, and an Uncorrectable PCI error is detected.

Immediate Reads

When the PEX 8112 forwards a Read Request (I/O or Memory) from the secondary bus (PCI Express) and detects an Uncorrectable Data error on the primary bus (PCI) while receiving an immediate response from the Completer, the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- **PCI Status** register *Detected Parity Error* bit is set
- PERR# is asserted on the PCI Bus when the **PCI Command** register *Parity Error Response Enable* bit is set

After detecting an Uncorrectable Data error on the destination bus for an immediate Read transaction, the PEX 8112 continues to fetch data until the Byte Count is satisfied or the Target ends the transaction.

When the PEX 8112 creates the PCI Express Completion, it forwards it with Successful Completion status and poisons the TLP.

Non-Posted Writes

When the PEX 8112 detects that PERR# is asserted on the primary bus (PCI) while forwarding a non-poisoned Non-Posted Write transaction from the secondary bus (PCI Express), the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- PCI Express Completion with UR status is returned

Posted Writes

When the PEX 8112 detects that PERR# is asserted on the primary bus (PCI) while forwarding a non-poisoned Posted Write transaction from the secondary bus (PCI Express), the following occur:

- **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
- After the error is detected, the remaining data is forwarded

10.2.1.3 PCI Address Errors

When the PEX 8112 forwards transactions from PCI Express-to-PCI, PCI Address errors are reported by SERR# assertion by the PCI Target. The PEX 8112 ignores the SERR# assertion, and allows the PCI Central Resource Function to service the error.

10.2.1.4 PCI Master Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **PCI Status** register *Received Master Abort* bit is set

10.2.1.5 PCI Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Master Abort on the PCI Bus, the following occur:

- PCI Express Completion with UR status is returned
- **PCI Status** register *Received Master Abort* bit is set

10.2.1.6 PCI Target Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **PCI Status** register *Received Target Abort* bit is set

10.2.1.7 PCI Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Target Abort on the PCI Bus, the following occur:

- PCI Express Completion with Completer Abort status is returned
- **PCI Status** register *Received Target Abort* bit is set

10.2.1.8 PCI Retry Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-PCI results in a Retry Abort on the PCI Bus, the following occur:

- Entire transaction is discarded
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set

10.2.1.9 PCI Retry Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-PCI results in a Retry Abort on the PCI Bus, the following occur:

- PCI Express Completion with Completer Abort status is returned
- **Interrupt Request Status** register *PCI Express-to-PCI Retry Interrupt* bit is set
- **Secondary Status** register *Secondary Signaled Target Abort* bit is set

  Although a Target Abort has not occurred, the device-specific Retry Abort results in a Completer Abort being sent to the Root Complex. For consistency, the *Secondary Signaled Target Abort* bit is also set.

10.2.2 Reverse Bridge PCI Originating Bus (Primary to Secondary)

This section describes error support for transactions that cross the PEX 8112 when the originating side is the PCI Bus, and the destination side is PCI Express. The PEX 8112 supports TLP poisoning as a Transmitter, to permit proper forwarding of Parity errors that occur on the PCI Bus. Posted Write data received on the PCI Bus with bad parity is forwarded to the PCI Express interface as Poisoned TLPs.

Table 10-5 provides the error forwarding requirements for Uncorrectable Data errors that the PEX 8112 detects when a transaction targets the PCI Express interface.

Table 10-6 describes the PEX 8112's behavior on a PCI Delayed transaction that is forwarded to the PCI Express interface as a Memory Read Request or an I/O Read/Write Request, and the PCI Express interface returns a Completion with UR or CA status for the request.

Table 10-5. Error Forwarding Requirements

Received PCI Error	Forwarded PCI Express Error
Write with Parity error	Write Request with poisoned TLP
Read Completion with Parity error in Data phase	Read Completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write Completion with Completer Abort Status

Table 10-6. PEX 8112 Behavior on a PCI Delayed Transaction

PCI Express Completion Status	PCI Immediate Response	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (upon Memory Read or I/O Read)	Target Abort	Normal Completion, return FFFF_FFFFh
Unsupported Request (upon I/O Write)	Target Abort	Normal Completion
Completer Abort	Target Abort	

10.2.2.1 Received PCI Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that it crosses the PEX 8112, and the PEX 8112 detects an Uncorrectable Data error on the PCI Bus, the following occur:

- **PCI Status** register *Detected Parity Error* status bit is set.
- If the **PCI Command** register *Parity Error Response Enable* bit is set, the transaction is discarded and is not forwarded to the PCI Express interface. The PCI PERR# signal is asserted.
- If the **PCI Command** register *Parity Error Response Enable* bit is not cleared, the data is forwarded to the PCI Express interface as a poisoned TLP. The **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set. The PCI PERR# signal is not asserted.

Uncorrectable Data Error on Posted Write

When the PEX 8112 detects an Uncorrectable Data error on the PCI Bus for a Posted Write transaction that crosses the PEX 8112, the following occur:

- PCI PERR# signal is asserted when the **PCI Command** register *Parity Error Response Enable* bit is set
- **PCI Status** register *Detected Parity Error* status bit is set
- Posted Write transaction is forwarded to the PCI Express interface as a poisoned TLP
- **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set

Uncorrectable Data Error on PCI Delayed Read Completions

When the PEX 8112 forwards a non-poisoned or poisoned Read Completion from PCI Express-to-PCI, and PERR# is asserted by the PCI Master, the following occur:

- Remainder of the Completion is forwarded
- PCI Central Resource Function services the PERR# assertion

Uncorrectable Address Error

When the PEX 8112 detects an Uncorrectable Address error, and Parity error detection is enabled by way of the **PCI Command** register *Parity Error Response Enable* bit, the following occur:

- Transaction is terminated with a Target Abort
- **PCI Status** register *Signaled Target Abort* bit is set
- **PCI Status** register *Detected Parity Error* status bit is set, independent of the setting of the **PCI Command** register *Parity Error Response Enable* bit
- SERR# is asserted, when enabled by way of the **PCI Command** register *SERR# Enable* bit
- **PCI Status** register *Signaled System Error* bit is set when SERR# is asserted

10.2.2.2 Unsupported Request Completion Status

The PEX 8112 provides two methods for handling a PCI Express Completion received with Unsupported Request (UR) status in response to a request originated by the PCI Bus. The response is controlled by the **Bridge Control** register *Master Abort Mode* bit. In either case, the **Secondary Status** register *Secondary Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default PCI compatibility mode, and a UR is not considered to be an error. When a Read transaction initiated on the PCI side of the PEX 8112 results in the return of a Completion with UR status, the PEX 8112 returns FFFF_FFFFh to the originating Master and terminates the Read transaction on the originating bus normally (by asserting TRDY#). When a Non-Posted Write transaction results in a Completion with UR status, the PEX 8112 completes the Write transaction on the originating bus normally (by asserting TRDY#) and discards the Write data.

Master Abort Mode Bit Set

When the **Bridge Control** register *Master Abort Mode* bit is set, the PEX 8112 signals a Target Abort to the originating Master of a downstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a Completion with UR status. Moreover, the **PCI Status** register *Signaled Target Abort* bit is set.

10.2.2.3 Completer Abort Completion Status

When the PEX 8112 receives a Completion with Completer Abort (CA) status on the PCI Express interface in response to Forwarded Non-Posted PCI transactions, the **Secondary Status** register *Secondary Received Target Abort* bit is set. A Completion with CA status results in a Delayed Transaction Target Abort on the PCI Bus. The PEX 8112 provides data to the requesting PCI agent, up to the point where data was successfully returned from the PCI Express interface, then signals a Target Abort. The **PCI Status** register *Signaled Target Abort* status bit is set when signaling a Target Abort to a PCI agent.

10.2.3 Reverse Bridge Timeout Errors

10.2.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows Requesters to abort a Non-Posted request when a Completion does not arrive within a reasonable length of time. Bridges, when acting as Masters on the PCI Express interface on behalf of internally generated requests and requests forwarded from a secondary bus (PCI Express), behave as endpoints for requests that they take ownership of. When a Completion Timeout is detected and the link is up, the PEX 8112 responds as when a UR Completion is received.

When the link is down, the **PCI Control** register *PCI-to-PCI Express Retry Count* field determines the number of PCI Retries before a Master Abort is returned to the PCI Bus.

10.2.3.2 PCI Delayed Transaction Timeout Errors

The PEX 8112 includes Delayed Transaction Timers for each queued Delayed transaction. When a Delayed transaction timeout is detected, the following occur:

- **Bridge Control** register *Discard Timer Status* bit is set
- Delayed request is removed from the Non-Posted Transaction queue
- SERR# is asserted when the **PCI Command** register *SERR# Enable* bit is set

10.2.4 Reverse Bridge PCI Express Error Messages

When the PEX 8112 detects an ERR_FATAL, ERR_NONFATAL, or ERR_COR error, or receives an ERR_FATAL, ERR_NONFATAL, or ERR_COR message, the PCI SERR# signal is asserted when the corresponding Reporting Enable bit in the **Root Control** register is set. When an ERR_FATAL or ERR_NONFATAL message is received, the **Secondary Status** register *Secondary Received System Error* bit is set, independent of the Reporting Enable bits in the **Root Control** register.

When the PEX 8112 receives a UR, an **Interrupt Request Status** register interrupt status bit is set. This status bit is enabled to generate an INT*x*# or MSI.

10.2.5 Reverse Bridge “Other” Errors

PCI devices assert SERR# when detecting errors that compromise system integrity. The PEX 8112 never monitors the SERR# ball in Reverse Bridge mode; instead, it allows the PCI Central Resource Function to service the SERR# interrupt.

Chapter 11 Exclusive (Locked) Access

11.1 Forward Bridge Exclusive Accesses

The exclusive access mechanism allows non-exclusive accesses to proceed in the face of exclusive accesses. This allows a Master to hold a hardware lock across several accesses, without interfering with non-exclusive Data transfers. Masters and Targets not involved in the exclusive accesses are allowed to proceed with non-exclusive accesses while another Master retains a bus lock.

Exclusive access support in the PEX 8112 is enabled by the **PCI Control** register *Locked Transaction Enable* bit. When this bit is cleared, PCI Express Memory Read Locked Requests are terminated with a UR status Completion.

11.1.1 Forward Bridge Lock Sequence across PEX 8112

Locked transaction sequences are generated by the Host CPU as one or more Reads, followed by a number of Writes to the same locations. In Forward Bridge mode, the PEX 8112 supports only Locked transactions in the downstream direction (PCI Express-to-PCI). Upstream Locked transactions are not allowed. The initiation of a Locked transaction sequence through the PEX 8112 is as follows:

1. Locked transaction starts with a Memory Read Locked Request.
2. Successive Reads for the Locked transaction also use Memory Read Locked Requests.
3. Successful Memory Read Locked Requests use the CplDLk Completion type, CplD. Unsuccessful Memory Read Locked Requests use the CplLk Completion type. (For further details, refer to the *PCI Express Base r1.0a*, Table 2-3.)
4. When the Locked Completion for the first Locked Read Request is returned, the PEX 8112 does not accept new requests from the PCI Bus.
5. Writes for the locked sequence use Memory Write Requests.
6. PEX 8112 remains locked until it is unlocked by the PCI Express interface. Unlock is then propagated to the PCI Bus by terminating the locked sequence.
7. PCI Express Unlock message is used to indicate the end of a locked sequence. Upon receiving an Unlock message, the PEX 8112 unlocks itself. When the PEX 8112 is not locked, it ignores the Unlock message.

When the Locked Read Request is queued in the PCI Express-to-PCI Non-Posted Transaction queue, subsequent Non-Posted, Non-Locked Requests from the PCI Express interface are completed with Unsupported Request (UR) status. Requests queued before the Locked Read Request are allowed to complete.

11.1.2 Forward Bridge PCI Master Rules for Supporting LOCK#

The PEX 8112 must obey the following rules when performing locked sequences on the PCI Bus:

- Master accesses only a single resource during a Lock operation.
- First transaction of a lock operation must be a Memory Read transaction.
- LOCK# must be asserted during the Clock cycle following the Address phase and remain asserted to maintain control.
- LOCK# must be released when the initial transaction of the Lock Request is terminated with Retry (Lock was not established).
- LOCK# must be released when an access is terminated by Target Abort or Master Abort.
- LOCK# must be de-asserted between consecutive lock operations for a minimum of one Clock cycle while the bus remains in the Idle state.

11.1.3 Forward Bridge Acquiring Exclusive Access across PEX 8112

When a PCI Express Locked Memory Read Request appears at the output of the Non-Posted Request queue, the Locked Request is performed on the PCI Bus. The PEX 8112 monitors the PCI LOCK# ball state when attempting to establish lock. When LOCK# is asserted, the PEX 8112 does not request the PCI Bus to start the transaction.

After LOCK# is de-asserted and the PCI Bus is idle, REQ# is asserted. While waiting for GNT#, the PEX 8112 continues to monitor LOCK#. When LOCK# is busy, the PEX 8112 de-asserts REQ# because another agent gained control of LOCK#.

When the PEX 8112 is granted the bus and LOCK# is not asserted, ownership of LOCK# is obtained. The PEX 8112 is free to perform an exclusive operation when the current transaction completes. LOCK# is de-asserted during the first Address phase, and then is asserted one Clock cycle later. A Locked transaction is not established on the bus until the first Data phase of the first transaction completes (IRDY# and TRDY# asserted).

When the Target terminates the first transaction with Retry, the PEX 8112 terminates the transaction and releases LOCK#. After the first Data phase completes, the PEX 8112 holds LOCK# asserted until the Lock operation completes or a Master Abort or Target Abort causes an early termination.

11.1.4 Forward Bridge Non-Posted Transactions and Lock

The PEX 8112 must consider itself locked when it detects a Locked Memory Read Request on the output of the Non-Posted Request queue, although no data is transferred. This condition is referred to as a *Target-Lock*. While in Target-Lock, the PEX 8112 does not process new requests on the PCI Express interface.

The PEX 8112 locks the PCI Bus when the lock sequence on the PCI Bus completes. A Target-Lock becomes a Full-Lock when the Locked Request completes on the PCI Express interface. At this point, the PCI Express Master established the lock.

11.1.5 Forward Bridge Continuing Exclusive Access

When the PEX 8112 performs another transaction to a locked Target, LOCK# is de-asserted during the Address phase. The locked Target accepts and responds to the request. LOCK# is asserted one Clock cycle after the Address phase to hold the Target in the locked state and allow the PEX 8112 to retain ownership of LOCK# beyond the end of the current transaction.

11.1.6 Forward Bridge Completing Exclusive Access

When the PEX 8112 receives an Unlock message from the PCI Express, it de-asserts LOCK# on the PCI Bus.

11.1.7 Forward Bridge Invalid PCI Express Requests while Locked

When the PEX 8112 is locked, it only accepts PCI Express Memory Read Lock or Memory Write transactions that are being forwarded to the PCI Bus. Other transaction types are terminated with a Completion with UR status, including Non-Posted accesses to internal Configuration registers and shared memory.

11.1.8 Forward Bridge Locked Transaction Originating on PCI Bus

Locked transactions originating on the secondary bus are not allowed to propagate to the primary bus. When a Locked transaction is performed on the PCI Bus and intended for the PEX 8112, the PEX 8112 ignores the transaction.

11.1.9 Forward Bridge PCI Bus Errors while Locked

11.1.9.1 PCI Master Abort during Posted Transaction

When a PCI Master Abort occurs during a PCI Express-to-PCI Locked Write transaction, the PEX 8112 de-asserts LOCK#, thereby releasing the PCI bus from the locked state. Also, the PCI Express interface is released from the locked state, although no Unlock Message is received. Write data is discarded.

Refer to Section 10.1.1.4, "PCI Master Abort on Posted Transaction," for additional details describing the action taken when a Master Abort is detected during a Posted transaction.

11.1.9.2 PCI Master Abort during Non-Posted Transaction

When a PCI Master Abort occurs during a PCI Express-to-PCI Locked Read transaction, the PEX 8112 de-asserts LOCK#, thereby releasing the PCI Bus from the locked state. Also, the PCI Express interface is released from the locked state, although no Unlock Message is received. A CplLk with UR status is returned to the PCI Express interface.

Refer to Section 10.1.1.5, "PCI Master Abort on Non-Posted Transaction," for additional details describing the action taken when a Master Abort is detected during a Non-Posted transaction.

11.1.9.3 PCI Target Abort during Posted Transaction

When a PCI Target Abort occurs during a PCI Express-to-PCI Locked Write transaction, the PEX 8112 de-asserts LOCK#, thereby releasing the PCI bus from the locked state. Also, the PCI Express interface is released from the locked state, although no Unlock message is received. Write data is discarded.

Refer to Section 10.1.1.6, "PCI Target Abort on Posted Transaction," for additional details describing the action taken when a Target Abort is detected during a Posted transaction.

11.1.9.4 PCI Target Abort during Non-Posted Transaction

When a PCI Target Abort occurs during a PCI Express-to-PCI Locked Read transaction, the PEX 8112 de-asserts LOCK#, thereby releasing the PCI Bus from the locked state. Also, the PCI Express interface is released from the locked state, although no Unlock Message is received. A CplLk with Completer Abort status is returned to the PCI Express interface.

Refer to Section 10.1.1.7, "PCI Target Abort on Non-Posted Transaction," for additional details describing the action taken when a Target Abort is detected during a Non-Posted transaction.

11.2 Reverse Bridge Exclusive Accesses

A Reverse bridge is allowed to pass Locked transactions from the primary bus (PCI) to the secondary bus (PCI Express). When a Locked Request (LOCK# asserted) is initiated on the PCI Bus, a Memory Read Locked Request is issued to the PCI Express interface. All subsequent Locked Read transactions targeting the PEX 8112 use the Memory Read Locked Request on the PCI Express interface. All subsequent Locked Write transactions use the Memory Write Request on the PCI Express interface. The PEX 8112 must transmit the Unlock message when PCI Lock sequence is complete.

Exclusive access support in the PEX 8112 is enabled by the **PCI Control** register *Locked Transaction Enable* bit. When this bit is cleared, the PCI LOCK# ball is ignored, and Locked transactions are treated as Unlocked transactions.

11.2.1 Reverse Bridge PCI Target Rules for Supporting LOCK#

The following PCI Target rules apply for supporting LOCK# in Reverse Bridge mode:

- The PEX 8112, acting as a Target of an access, locks itself when LOCK# is de-asserted during the Address phase and is asserted during the following Clock cycle.
- Lock is established when LOCK# is de-asserted during the Address phase, asserted during the following Clock cycle, and data is transferred during the current transaction.
- After lock is established, the PEX 8112 remains locked until both FRAME# and LOCK# are sampled de-asserted, regardless of how the transaction is terminated.
- The PEX 8112 is not allowed to accept new requests (from PCI or PCI Express) while it remains in a locked condition, except from the owner of LOCK#.

11.2.2 Reverse Bridge Acquiring Exclusive Access across PEX 8112

A PCI Master attempts to forward a Locked Memory Read transaction to the PCI Express interface. The PEX 8112 terminates the transaction with a Retry, and the Locked Request is written to the PCI-to-PCI Express Non-Posted Transaction queue. When this Locked Request reaches the top of the queue, the Locked Request is performed on the PCI Express interface as a Memory Read Lock Request. When the PCI Express responds with a Locked Completion, the Locked Request in the queue is marked as completed. When the PCI Master Retries the Locked Memory Read Request, the PEX 8112 responds with TRDY#, thereby completing the lock sequence.

When the PEX 8112 is locked, it only accepts PCI Locked transactions that are being forwarded to the PCI Express interface. Other bus transactions are terminated with a Retry, including accesses to internal Configuration registers and shared memory. All PCI Express requests are terminated with a Completion with UR status.

11.2.3 Reverse Bridge Completing Exclusive Access

When the PEX 8112 detects that LOCK# and FRAME# are de-asserted, it transmits an Unlock message to the PCI Express interface.

11.2.4 Reverse Bridge PCI Express Locked Read Request

When a Locked Read Request is performed on the PCI Express interface, the PEX 8112 responds with a Completion with UR status.

11.2.5 Reverse Bridge Limitations

In systems with multiple PCI Masters that perform exclusive transactions to the PCI Express interface, the **PCI Control** register *Locked Transaction Enable* bit must be set.

Chapter 12 Power Management

12.1 Forward Bridge Power Management

PCI Express defines Link Power Management (PM) states, replacing the Bus PM states defined by the *PCI Power Mgmt. r1.1*. Link states are not visible to *PCI Power Mgmt. r1.1* Conventional PCI-compatible software, and are derived from the Device PM states, or by Active State Power Management (ASPM) protocols.

12.1.1 Forward Bridge Link State PM

12.1.1.1 Link PM States

Table 12-1 defines the Link PM states supported in Forward Bridge mode.

Table 12-1. Supported Link PM States (Forward Bridge Mode)

Link PM State	Description
L0	Active state. All PCI Express operations are enabled.
L0s	A low-resume latency, energy-saving "standby" state.
L1	Higher latency, lower power "standby" state. L1 Link PM state support is required for *PCI Power Mgmt. r1.1*-compatible PM. This state is optional for ASPM. All platform-provided main power supplies and component Reference Clocks must remain active at all times in the L1 Link PM state. The PEX 8112 internal Phase-Locked Loops (PLLs) are turned Off in this state, enabling greater energy savings at a cost of increased exit latency. The L1 Link PM state is entered when all functions of a downstream component on a given PCI Express link are programmed to a Device PM state other than D0, or when the downstream component requests L1 Link PM state entry (ASPM) and receives positive acknowledgement for the request. Exit from the L1 Link PM state is initiated by an upstream-initiated transaction targeting the downstream component, or by the need of the downstream component to initiate a transaction heading upstream. Transition from the L1 to L0 Link PM state is typically a few microseconds. Transaction Layer Packet (TLP) and Data Link Layer Packet (DLLP) communication over a link that remains in the L1 Link PM state is prohibited. The PEX 8112 only requests L1 Link PM state entry for *PCI Power Mgmt. r1.1*-compatible PM. When PMEIN# is asserted, the PEX 8112 requests a transition from the L1 to L0 Link PM state.
L2	***Not supported*** Auxiliary-powered link deep energy-saving state.
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready Link PM state transition protocol support is required. The L2/L3 Ready Link PM state is related to *PCI Power Mgmt. r1.1* Device PM state transitions. L2/L3 Ready is the Link PM state that a given link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready Link PM state transition protocol for that link, the link is then ready for the L2 or L3 Link PM state. Depending upon the implementation choices of the platform with respect to providing a Vaux supply, after main power is removed, the link settles into the L2 Link PM state (*that is*, Vaux is provided), or into a zero power "off" state (refer to L3). The PEX 8112 does ***not support*** the L2 Link PM state in Forward Bridge mode; therefore, it settles into the L3 Link PM state. The L2/L3 Ready Link PM state entry transition process must start as soon as possible, following the PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready Link PM state entry by injecting a PM_Enter_L23 DLLP onto its Transmit port. TLP and DLLP communication over a link that remains in the L2/L3 Ready Link PM state is prohibited. The PEX 8112 exits from the L2/L3 Ready to L0 Link PM state when an upstream-initiated transaction targeting the downstream device occurs before main power is removed and the platform power manager decides not to enter the system sleep state. A link's transition into the L2/L3 Ready Link PM state is one of the final stages involving PCI Express protocol, leading up to the platform entering into in a System Sleep state, wherein main power is turned Off (*such as*, ACPI S3 or S4 sleep state).
L3	Link-off state. Power-off state.

12.1.1.2 Link State Transitions

Figure 12-1 highlights the Link PM state transitions which occur during the course of link operations. The arc indicated in the illustration indicates the case wherein the platform does not provide Vaux. Link PM transitions from an Link PM state to another Link PM state pass through the L0 Link PM state during the transition process, with the exception of the L2/L3 Ready to L3 Link PM state transition. In this case, the link transitions from the L2/L3 Ready Link PM state directly to the L3 Link PM state, when main power to the component is removed. (This follows along with a Device PM state transition from D3, for the corresponding component.)

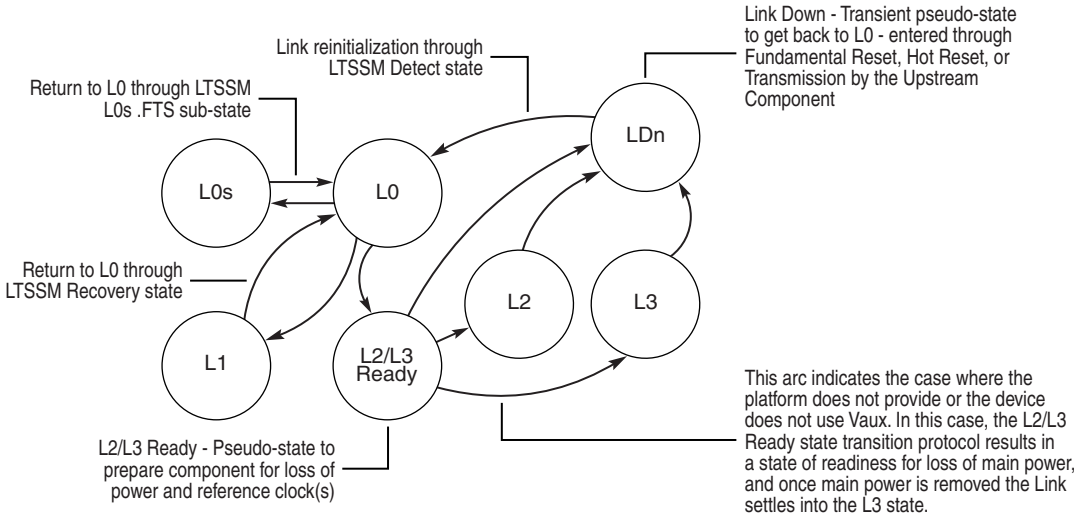
The following sequence, leading up to entering a system sleep state, illustrates the multi-step Link state transition process:

1. System software directs all functions of a downstream component to the D3hot Device PM state.
2. The downstream component then initiates the transition of the link to the L1 Link PM state, as required.
3. System software then causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
4. This message causes the subject link to transition (return) to the L0 Link PM state to transmit it, and enable the downstream component to respond with a PME_TO_Ack message.
5. After the PME_TO_Ack message is transmitted, the downstream component initiates the L2/L3 Ready Link PM state transition protocol.

In summary:

- L0 –> L1 –> L0 –> L2/L3 Ready Link PM state
- L2/L3 Ready Link PM state entry sequence is initiated at the completion of the PME_Turn_Off/ PME_TO_Ack protocol handshake

Figure 12-1. Link PM State Transitions during Link Operations



Note: *In this case, the L2/L3 Ready Link PM state transition protocol results in a state of readiness for loss of main power, and after removal, the link settles into the L3 Link PM state.*

It is also possible to remove power without first placing all devices into the D3hot Device PM state:

1. System software causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
2. The downstream component responds with a PME_TO_Ack message.
3. After the PME_TO_Ack message is transmitted, the downstream component initiates the L2/L3 Ready Link PM state transition protocol.

In summary:

- L0 –> L2/L3 Ready Link PM state

12.1.2 Forward Bridge PM States

The PEX 8112 provides the Configuration registers and support hardware required by the *PCI Power Mgmt. r1.1*. The **PCI Capability Pointer** register points to the Base address of the PM registers (offset 40h).

The PEX 8112 also supports the PCI Express ASPM protocol, as described in Section 12.1.1.

12.1.2.1 Device PM States

Table 12-2 defines the Device PM states supported in Forward Bridge mode, selectable by way of the **Power Management Control/Status** register *Power State* field.

When transitioning from D0 to another Device PM state, the PCI Express link transitions to the L1 Link PM state.

System software must allow a minimum recovery time following a D3hot-to-D0 Device PM state transition of at least 10 ms, prior to accessing the function. *For example*, this recovery time is used by the D3hot-to-D0 Device PM state transitioning component to bootstrap its component interfaces (*such as*, from serial ROM) prior to being accessible. Attempts to target the function during the recovery time (including Configuration Request packets) result in undefined behavior.

The PEX 8112 is able to respond to PCI Express requests immediately after the D3hot-to-D0 Device PM state transition.

Table 12-2. Supported Device PM States (Forward Bridge Mode)

Device PM State	Description
D0_uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0_active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Access Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request (UR). All PCI Express requests generated by the PEX 8112 are disabled except for Power Management Event (PME) messages.
D2	Heavy sleep. Same restrictions as the D1 Device PM state.
D3hot	Function context not maintained. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with a UR. All PCI Express requests generated by the PEX 8112 are disabled except for PME messages.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold to D0_uninitialized Device PM state. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active Device PM state.

12.1.3 Forward Bridge PM Signaling

PCI devices can assert PMEIN# on the PEX 8112, to signal a PME. The PEX 8112 converts the PMEIN# signal, received on the PCI side of the PEX 8112, to PCI Express PME messages. There are no internal events that cause a PME message to transmit upstream.

PM messages are used to support PMEs signaled by devices downstream of the PEX 8112. System software must identify the source of a PCI PME that is reported by a PM_PME message. When the PME is received from an agent on a PCI Bus, the PM_PME Message Requester ID reports the Bus Number from which the PME was collected, and the Device Number and Function Number reported must both be 0.

When the PME message is transmitted to the Host, the **Power Management Control/Status** register *PME Status* bit is set and a 100-ms timer is started. When the status bit is not cleared within 100 ms, another PME message is transmitted.

When the upstream device is powering down the downstream devices, it first places all devices into the D3hot Device PM state. It then transmits a PCI Express PME_Turn_Off message. After the PEX 8112 receives this message, it does not transmit further PME messages upstream. The PEX 8112 then transmits a PME_TO_Ack message to the upstream device and places its link into the L2/L3 Ready Link PM state. It is now ready to be powered-down. When the upstream device returns the PEX 8112 to the D0 Device PM state, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8112, and is not communicated to the PCI devices. The PEX 8112 does not issue a PM_PME message on behalf of a downstream PCI device while its upstream Link remains in the non-communicating L2/L3 Link PM state.

To avoid loss of PCI backplane PME# assertions in the conversion of the level-sensitive PME# signal to the edge-triggered PCI Express PM_PME message, the PEX 8112 polls the PCI PMEIN# ball every 256 ms. A PCI Express PM_PME message is generated when PMEIN# is asserted.

12.1.4 Set Slot Power

The Root Complex transmits a Set Slot Power message when either of the following occurs:

- PCI Express link first comes up
- Root Complex **Slot Capability** register *Slot Power Limit Value* or *Slot Power Limit Scale* field value changes

When the PEX 8112 receives this message, it updates the **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

When the available power indicated by the *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields is greater than or equal to the power requirement indicated in the **Power** register, the PWR_OK signal is asserted.

12.2 Reverse Bridge Power Management

The PEX 8112 supports ASPM in Reverse Bridge mode. By default, the L1 Link PM state is enabled, and the L0s Link PM state is disabled.

12.2.1 Reverse Bridge ASPM

12.2.1.1 ASPM States

Table 12-3 defines the Link PM states supported in Reverse Bridge mode.

Table 12-3. Supported Link PM States (Reverse Bridge Mode)

Link PM State	Description
L0	Active state. All PCI Express operations are enabled.
L0s	A low-resume latency, energy-saving "standby" state. When enabled by the serial EEPROM or external driver, the PEX 8112 Transmitter transitions to the L0s Link PM state after a low-resume latency, energy-saving "standby" state. L0s Link PM state support is required for ASPM. It is not applicable to *PCI Power Mgmt. r1.1*-compatible PM. All main power supplies, component Reference Clocks, and components' internal PLLs must be active at all times during the L0s Link PM state. TLP and DLLP communication over a link that remains in the L0s Link PM state is prohibited. The L0s Link PM state is exclusively used for ASPM. The PCI Express Physical Layer provides mechanisms for quick transitions from this state to the L0 Link PM state. When common (distributed) Reference Clocks are used on both sides of a given link, the transition time from the L0s to L0 Link PM state is typically fewer than 100 symbol times.
L1	Higher-latency, lower-power "standby" state. L1 Link PM state support is required for *PCI Power Mgmt. r1.1*-compatible PM. This state is optional for ASPM. All platform-provided main power supplies and component Reference Clocks must remain active at all times in the L1 Link PM state. A component's internal PLLs are turned Off in this state, enabling greater energy savings at a cost of increased exit latency. The L1 Link PM state is entered when all functions of a downstream component on a given PCI Express link are programmed to a Device PM state other than D0, or when the downstream component requests L1 Link PM state entry (ASPM) and receives positive acknowledgement for the request. Exit from the L1 Link PM state is initiated by an upstream-initiated transaction targeting the downstream component, or by the downstream component's need to initiate a transaction heading upstream. Transition from the L1 to L0 Link PM state is typically a few microseconds. TLP and DLLP communication over a link that remains in the L1 Link PM state is prohibited.
L2	Auxiliary-powered link deep energy-saving state.
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready Link PM state transition protocol support is required. The L2/L3 Ready Link PM state is related to *PCI Power Mgmt. r1.1* Device PM state transitions. L2/L3 Ready is the Link PM state that a given link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready Link PM state transition protocol for that link, the link is then ready for the L2 or L3 Link PM state; the link is not actually in either of those states until main power is removed. If the platform implements a Vaux Supply voltage, after main power is removed, the link settles into the L2 Link PM state; otherwise, it settles into the L3 Link PM state. The PEX 8112 does not have Vaux capability; however, it supports the L2 Link PM state when the system Vaux supply is used as the main power to the PEX 8112. The L2/L3 Ready Link PM state entry transition process must start as soon as possible, following PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready Link PM state entry by injecting a PM_Enter_L23 DLLP onto its Transmit port. TLP and DLLP communication over a link that remains in the L2/L3 Ready Link PM state is prohibited. The PEX 8112 exits from the L2/L3 Ready to L0 Link PM state when an upstream-initiated transaction targeting the downstream device occurs before main power is removed and the platform power manager decides not to enter the system sleep state. A link's transition into the L2/L3 Ready Link PM state is one of the final stages involving PCI Express protocol leading up to the platform entering into in a System Sleep state, wherein main power is turned Off (*for example*, ACPI S3 or S4 sleep state).
L3	Link-off state. Power-off state.

12.2.2 Reverse Bridge PM States

The PEX 8112 provides the Configuration registers and support hardware required by the *PCI Power Mgmt. r1.1*. The **PCI Capability Pointer** register points to the Base address of the PM registers (offset 40h).

12.2.2.1 Device PM States

Table 12-4 defines the Device PM states supported in Reverse Bridge mode, selectable by way of the **Power Management Control/Status** register *Power State* field.

Table 12-4. Supported Device PM States (Reverse Bridge Mode)

Device PM State	Description
D0_uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0_active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Access Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Configuration transactions are accepted. No Master cycles are allowed, and the INT*x*# interrupts are disabled. The PMEOUT# signal is asserted by the PEX 8112 and the PCI clock continues to run in this state.
D2	Heavy sleep. Same as the D1 Device PM state, except that the PCI Host stops the PCI clock.
D3hot	Function context not maintained. Only PCI Configuration transactions are accepted.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold to D0_uninitialized Device PM state. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active Device PM state.

12.2.3 Reverse Bridge Power Down Sequence

During a link power-down, the following sequence occurs:

1. PCI Host places downstream PCI Express device in D3 Device PM state.
2. Downstream device initiates a transition to the L1 Link PM state.
3. PCI Host places PEX 8112 in the D3 Device PM state.
4. PEX 8112 initiates a transition to the L0 Link PM state on the link.
5. PEX 8112 generates a PCI Express PME_Turn_Off message to the PCI Express downstream device.
6. Downstream device responds with a PME_TO_Ack message.
7. Downstream device transmits a DLLP to request transition to the L2/L3 Ready Link PM state (*L2.Idle* Link state).
8. PEX 8112 acknowledges the request, completing the transition to the *L2.Idle* Link state.
9. PMEOUT# signal is asserted to the PCI Host.
10. PCI Host can now remove power from the PEX 8112.

12.2.4 Reverse Bridge PMEOUT# Signal

PME messages from the PCI Express interface are translated to the PCI backplane PMEOUT# signal on the PEX 8112. The **Power Management Control/Status** register *PME Status* bit is set when a PCI Express PME message is received, the WAKEIN# signal is asserted, a beacon is detected, or the link transitions to the L2/L3 Ready Link PM state. PMEOUT# is asserted when the *PME Status* bit is set and PME is enabled.

12.2.5 Reverse Bridge Set Slot Power

The PEX 8112 transmits a Set Slot Power message to the downstream PCI Express device when either of the following occurs:

- PCI Express link first comes up
- PEX 8112 **Slot Capability** register *Slot Power Limit Value* or *Slot Power Limit Scale* field value changes

When the downstream device receives this message, it updates the **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

Chapter 13 PCI Express Messages

13.1 Forward Bridge PCI Express Messages

PCI Express defines a set of messages that are used as a method for in-band communication of events (*such as* interrupts), generally replacing the need for sideband signals. These messages are also used for general-purpose messaging. PCI Express-to-PCI bridge support requirements for these messages are described in the following sections.

PCI Express messages are routed explicitly or implicitly depending upon specific bit field encodings in the Message Request Header. An explicitly routed message is routed based upon a specific address or on an *ID* field located within the Message Header. The destination of an implicitly routed message is inferred from the message *Type* field.

13.1.1 Forward Bridge INT*x*# Interrupt Signaling

INT*x*# Interrupt Signaling messages are used for in-band communication of the state of the PCI line-based interrupts INTA#, INTB#, INTC#, and INTD# for downstream devices. (Refer to Section 5.1, "Forward Bridge PCI Interrupts," for details.)

13.1.2 Forward Bridge Power Management Messages

Power Management (PM) messages are used to support Power Management Events (PMEs) signaled by sources integrated into the PEX 8112 and for downstream devices. (Refer to Section 12.1, "Forward Bridge Power Management," for details.)

13.1.3 Forward Bridge Error Signaling Messages

Error Signaling messages are transmitted by the PEX 8112 on its primary bus (PCI Express), to signal errors for any of the following:

- A particular transaction
- The link interface
- Errors internal to the PEX 8112
- PCI-related errors detected on the secondary bus

The message types include ERR_COR, ERR_FATAL, and ERR_NONFATAL. The relevant Mask bits are located in the **PCI Express Capability** structure. (Refer to Section 10.1, "Forward Bridge Error Handling," for details.)

13.1.4 Forward Bridge Locked Transactions Support

The PCI Express Unlock Message is used to support Locked Transaction sequences in the downstream direction. (Refer to Section 11.1, "Forward Bridge Exclusive Accesses," for details.)

13.1.5 Forward Bridge Slot Power Limit Support

The Set Slot Power Limit message is transmitted to endpoints, including bridges, by the Root Complex or a switch. The PEX 8112 supports and complies with these messages. These messages are particularly relevant to bridges implemented on add-in boards. (Refer to Section 12.1, "Forward Bridge Power Management," for details.)

13.1.6 Forward Bridge Hot Plug Signaling Messages

The PEX 8112 does ***not support*** Hot Plug signaling, and ignores the associated messages.

13.2 Reverse Bridge PCI Express Messages

13.2.1 Reverse Bridge INT*x*# Interrupt Message Support

The PEX 8112 controls the state of the corresponding PCI interrupt balls (INTA#, INTB#, INTC#, and/or INTD#), based upon the Assert_INT*x* and Deassert_INT*x* messages received.

13.2.2 Reverse Bridge Power Management Message Support

The PEX 8112 generates a PME_Turn_Off message when placed into the D3 Device PM state. The PEX 8112 then waits for the PME_TO_Ack message from the downstream device before proceeding with the power-down sequence.

13.2.2.1 Power Management Event Handling Requirements

The PEX 8112 translates Power Management Event (PME) messages from the PCI Express interface to the PCI backplane PME# signal. The PEX 8112 converts the edge-triggered PMEs on the PCI Express interface to the level-triggered PME# signal on the PCI Bus. The PEX 8112 signals PMEOUT# on the PCI Bus for the following:

- PCI Express WAKEIN# signal is asserted while the link is in the L2 state
- PCI Express beacon is received while the link is in the L2 state
- PCI Express PM_PME message is received

For compatibility with existing software, the PEX 8112 does not signal PMEOUT# unless the PME signaling is enabled by the **Power Management Control/Status** register *PME Enable* bit. The PEX 8112 sets the **Power Management Control/Status** register *PME Status* bit when PMEOUT# is signaled and de-asserts PMEOUT# when the *PME Enable* or *PME Status* bit is cleared. All PME messages received while the *PME Enable* bit is cleared are ignored and the *PME Status* bit is not set during this time.

13.2.3 Reverse Bridge Error Signaling Message Support

The PEX 8112 converts all ERR_COR, ERR_FATAL, and ERR_NONFATAL messages to SERR# on the PCI Bus.

13.2.4 Reverse Bridge Locked Transaction Support

The PEX 8112 is allowed to pass Locked transactions from the primary bus to the secondary bus. The PEX 8112 uses the Memory Read Locked Request to initiate a locked sequence when a Locked Request is transmitted on the PCI Bus. All subsequent Locked Read transactions targeting the PEX 8112 use the Memory Read Locked Request on the PCI Express interface. All subsequent Locked Write transactions use the Memory Write Request on the PCI Express interface. The PEX 8112 transmits the Unlock message when the PCI Lock sequence is complete. (Refer to Section 11.2, “Reverse Bridge Exclusive Accesses,” for details.)

13.2.5 Reverse Bridge Slot Power Limit Support

The Set Slot Power Limit message is transmitted to endpoints, including bridges, by the Root Complex or a Switch. The PEX 8112 supports and complies with these messages. These messages are particularly relevant to bridges implemented on add-in boards. (Refer to Section 12.2, “Reverse Bridge Power Management,” for details.)

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Chapter 14 PCI Arbiter

14.1 Overview

A PCI system using the PEX 8112 uses an External Bus Arbiter, or the PEX 8112 Internal PCI Arbiter. The Internal PCI Arbiter accepts bus requests from up to four external PCI Masters. The PCI Express-to-PCI Bridge Controller logic also requests control of the PCI Bus.

14.2 Internal Arbiter Mode

When the EXTARB signal is de-asserted, the PEX 8112 accepts and arbitrates PCI requests from up to four external devices. The PEX 8112 supports single and multi-level Arbiter modes, selected by the **PCI Control** register *PCI Multi-Level Arbiter* bit.

14.2.1 Single-Level Mode

The four external requests and the PCI Express-to-PCI Bridge Controller request are placed into a single-level Arbiter. After a device is granted the bus, it becomes the lowest level Requester. All devices have the same priority. *For example*, when all internal and external agents are requesting the bus, the order of the agents that are granted the bus is as follows:

- PEX 8112 PCI Master
- External Requester 0
- External Requester 1
- External Requester 2
- External Requester 3
- Bridge

and so forth.

14.2.2 Multi-Level Mode

The four external requests are placed into a two-level Round Robin Arbiter with the PCI Express-to-PCI Bridge Controller. Level 0 alternates between the PCI Express-to-PCI Bridge Controller and Level 1, guaranteeing that the PCI Express-to-PCI Bridge is granted up to 50% of the accesses. Level 1 consists of the four external PCI Requesters.

For example, when all internal and external agents are requesting the bus, the order of the agents that are granted the bus is as follows:

- PEX 8112 PCI Master
- External Requester 0
- PEX 8112 PCI Master
- External Requester 1
- PEX 8112 PCI Master
- External Requester 2
- PEX 8112 PCI Master
- External Requester 3

and so forth.

14.3 External Arbiter Mode

When the EXTARB signal is asserted, the PEX 8112 PCI request inputs to the Internal PCI Arbiter are disabled. The PEX 8112 generates a PCI Request (REQ0#) to an External Arbiter when the PEX 8112 must use the PCI Bus. The PCI Grant input (GNT0#) to the PEX 8112 allows the PEX 8112 to become the PCI Master.

14.4 Arbitration Parking

The PCI Bus is not allowed to float for more than eight Clock cycles. When there are no requests for the bus, the Arbiter selects a device to drive the bus to a known state, by driving its GNT# ball active. When the EXTARB signal is de-asserted (Internal Arbiter mode), the PEX 8112 selects a PCI Master to be parked on the bus during idle periods. The **PCI Control** register *PCI Arbiter Park Select* field determines which Master is parked on the bus. When parked (GNT# driven during idle bus), the PEX 8112 drives AD[31:0], CBE[3:0]#, and PAR to a known state. The PEX 8112 drives AD[31:0], CBE[3:0]#, and PAR with the previous output value.

In Forward Bridge mode, the PEX 8112 parks on the PCI Bus during reset, independent of the EXTARB signal, and drives AD[31:0], CBE[3:0]#, and PAR Low.

Chapter 15 Forward Bridge Mode Configuration Registers

15.1 Register Description

This chapter describes the PEX 8112 Configuration registers specific to Forward Bridge mode. Registers specific to Reverse Bridge mode are discussed in Chapter 16.

The PCI-Compatible Forward Bridge Mode Configuration registers are accessed by the PCI Express Root Complex, using the PCI Configuration Address space. All Configuration registers are accessed from the PCI Express interface or PCI Bus, using the 64-KB memory space defined by the **PCI Base Address 0** register. Registers that are written by the Serial EEPROM Controller are also written using Memory Writes through the **PCI Base Address 0** register.

When the Configuration registers are accessed using Memory transactions to the **PCI Base Address 0** register, the register map defined in Table 15-1 is used.

The Serial EEPROM Controller writes to Configuration registers. An upper Address bit is used to select one of two register spaces, as defined in Table 15-2.

Each register is 32 bits wide, and is accessed one byte, word, or DWORD at a time. These registers use Little Endian byte ordering, which is consistent with the *PCI r3.0*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8112 is powered up or reset, the registers are set to their default values. Writes to unused registers are ignored. Reads from unused registers return a value of 0.

Table 15-1. Forward Bridge Mode PCI Base Address 0 Register Map

Address Offset	Register Space
0000h – 0FFFh	PCI-Compatible Configuration registers
1000h – 1FFFh	Main Configuration registers
2000h – 2FFFh	–
8000h – 9FFFh	8-KB internal shared memory

Table 15-2. Selecting Register Space

AD12	Register Space
0	PCI-Compatible Configuration registers
1	Main Configuration registers

15.1.1 Indexed Addressing

In addition to Memory-Mapped accesses, the PEX 8112 **Main Configuration** registers can be accessed using the **Main Control Register Index** and **Main Control Register Data** registers. This method allows all Main Configuration registers to be accessed using Configuration transactions, rather than Memory transactions. First, the **Main Configuration** register offset is written to the **Main Control Register Index** register (offset 84h). Then, the **Main Configuration** register is written or read by accessing the **Main Control Register Data** register (offset 88h).

The **Main Control Register Index** and **Main Control Register Data** registers are used only to access the **Main Control** registers, because there is a built-in offset of 1000h. *For example*, if the **Main Control Register Index** register is set to 20h, the **Main Control Register Data** register stores the contents of the **General-Purpose I/O Control** register during a Memory Read.

15.2 Configuration Access Types

Table 15-3 defines configuration access types referenced by the registers in this chapter.

Table 15-3. Configuration Access Types

Access Type	Description
CFG	Initiated by PCI Configuration transactions on the primary bus.
MM	Initiated by PCI Memory transactions on the primary or secondary bus, using the Address range defined by the **PCI Base Address 0** register.
EE	Initiated by the Serial EEPROM Controller during initialization.

15.3 Register Attributes

Table 15-4 defines the register attributes used to indicate access types provided by each register bit/field.

Table 15-4. Access Provided by Register Bits

Register Attribute	Description
HwInit	**Hardware-Initialized** Register bits are initialized by firmware or hardware mechanisms *such a*s ball strapping (on the BAR0ENB#, EXTARB, and FORWARD balls) or serial EEPROM. Bits are Read-Only after initialization and reset only with a Fundamental Reset.
RO	**Read-Only Register** Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8112 Hardware-Initialization mechanism or PEX 8112 Serial EEPROM register Initialization feature.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve the value read, for writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write Register** Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	**Read-Only Status, Write 1 to Clear Status Register** Register bits indicate status when read; a set bit that is indicating a status event, is cleared by writing 1. Writing 0 to RW1C bits has no effect.
WO	**Write-Only** Used to indicate that a register is written by the Serial EEPROM Controller.

15.4 Register Configuration and Map

Table 15-5 lists the register configuration and map for Forward Bridge mode.

Table 15-5. Forward Bridge Mode Register Configuration and Map

Register Group	PCI Space	Offset Address Range
PCI-Compatible Configuration (Type 1) Registers	PCI Express Configuration	00h – 3Ch
	Memory-Mapped, **BAR0**	
PCI-Compatible Extended Capability Registers for PCI Express Interface	PCI Express Configuration	40h – FFh
	Memory-Mapped, **BAR0**	
PCI Express Extended Capability Registers	PCI Express Configuration	100h – FFFh
	Memory-Mapped, **BAR0**	
Main Control Registers	Memory-Mapped, **BAR0**	1000h – FFFFh
PCI Express Configuration Registers Using Enhanced Configuration Access	Memory-Mapped, **BAR0**	2000h – 2FFFh
8-KB Shared Memory instead of General Purpose Memory	Memory-Mapped, **BAR0**	8000h – 9FFFh

15.5 PCI-Compatible Configuration (Type 1) Registers

This section details the PEX 8112 Forward Bridge mode PCI-Compatible Configuration (Type 1) registers. Table 15-6 defines the register map.

Table 15-6. Forward Bridge Mode PCI-Compatible Configuration (Type 1) Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
00h	PCI Device ID		PCI Vendor ID	
04h	PCI Status		PCI Command	
08h	PCI Class Code			PCI Device Revision ID
0Ch	PCI Built-In Self-Test ***(Not Supported)***	PCI Header Type	PCI Bus Latency Timer	PCI Cache Line Size
10h	PCI Base Address 0			
14h	PCI Base Address 1			
18h	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Memory Base Upper 32 Bits			
2Ch	Prefetchable Memory Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	***Reserved***			PCI Capability Pointer
38h	PCI Base Address for Expansion ROM ***(Not Supported)***			
3Ch	Bridge Control		PCI Interrupt Pin	PCI Interrupt Line

Register 15-1. (Offset 00h; PCIVENDID) PCI Vendor ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID** Identifies the device manufacturer. The PEX 8112 returns the PLX PCI-SIG-assigned Vendor ID, 10B5h.	RO	RW	WO	10B5h

Register 15-2. (Offset 02h; PCIDEVID) PCI Device ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Device ID** Identifies the particular device, as specified by the vendor. The PEX 8112 returns the PLX-assigned Device ID, 8112h.	RO	RW	WO	8112h

Register 15-3. (Offset 04h; PCICMD) PCI Command

Bit(s)	Description	CFG	MM	EE	Default
0	**I/O Access Enable** Enables the PEX 8112 to respond to I/O Space accesses on the primary bus (PCI Express). These accesses must be directed to a Target on the PCI Bus, because the PEX 8112 does not have internal I/O-Mapped resources. 0 = PEX 8112 responds to all I/O requests on its primary bus with an Unsupported Request Completion	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8112 to respond to Memory Space accesses on the primary bus (PCI Express). These accesses are directed to a Target on the PCI Bus, or to internal Memory-Mapped registers. 0 = PEX 8112 responds to all Memory requests on the primary bus with an Unsupported Request Completion	RW	RW	WO	0
2	**Bus Master Enable** Enables the PEX 8112 to issue Memory and I/O Read/Write Requests on the primary bus (PCI Express). Requests other than Memory or I/O Requests are not controlled by this bit. 0 = PEX 8112 does not respond (issue a Target Abort) to Memory nor I/O transactions on the secondary bus (PCI). No Memory or I/O transactions are forwarded to the primary bus (PCI Express).	RW	RW	WO	0
3	**Special Cycle Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** 0 = Enables the PEX 8112 PCI Master logic to use the Memory Write command 1 = Enables the PEX 8112 PCI Master logic to use the Memory Write and Invalidate command	RW	RW	WO	0
5	**VGA Palette Snoop** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	**Parity Error Response Enable** Controls the PEX 8112's response to Data Parity errors forwarded from the primary bus (*such as*, a poisoned Transaction Layer Packet (TLP)). 0 = PEX 8112 must ignore (but records status, *such as* by setting the **PCI Status** register *Detected Parity Error* bit) Data Parity errors detected and continue standard operation 1 = PEX 8112 must take its standard action when a Data Parity error is detected (refer to Section 10.1.1.1, "Received Poisoned TLP")	RW	RW	WO	0
7	**Address Stepping Enable** The PEX 8112 performs Address Stepping for PCI Configuration Requests; therefore this bit is Read/Write, with an initial value of 1.	RW	RW	WO	1

Register 15-3. (Offset 04h; PCICMD) PCI Command *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
8	**SERR# Enable** Enables reporting of Fatal and Non-Fatal errors to the Root Complex. ***Note:*** *Errors are reported when enabled through this bit or through the* ***PCI Express Device Control*** *register PCI Express-specific bits.*	RW	RW	WO	0
9	**Fast Back-to-Back Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** 1 = PEX 8112 is prevented from generating INT*x*# Interrupt messages on behalf of functions integrated into the PEX 8112. INT*x*# emulation interrupts previously asserted must be de-asserted. There is no effect on INT*x*# messages generated on behalf of INT*x*# inputs associated with the secondary bus (PCI).	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-4. (Offset 06h; PCISTAT) PCI Status

Bit(s)	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** 1 = Indicates that an INT*x*# Interrupt message is pending on behalf of functions integrated into the PEX 8112 Does not reflect the status of INT*x*# inputs associated with the secondary bus.	RO	RO	–	0
4	**Capabilities List** Indicates whether the **PCI Capability Pointer** at offset 34h is valid. Because all PCI Express devices are required to implement the **PCI Express Capability** structure, this bit is hardwired to 1.	RO	RO	–	1
5	**66 MHz Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Used to report Data Parity error detection by the PEX 8112. Set when the **PCI Command** register *Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a Completion marked poisoned on the primary bus • Bridge poisons a Write Request or Read Completion on the primary bus Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	00b
11	**Signaled Target Abort** Set when the PEX 8112 completes a request as a transaction Target on its primary bus, using Completer Abort Completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Received Target Abort** Set when the PEX 8112 receives a Completion with Completer Abort Completion status on its primary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the PEX 8112 receives a Completion with Unsupported Request Completion status on its primary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the PEX 8112 transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the **PCI Command** register *SERR# Enable* bit is set. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set when the PEX 8112 receives a poisoned TLP on the primary bus, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 15-5. (Offset 08h; PCIDEVREV) PCI Device Revision ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Device Revision ID** Identifies the PEX 8112 Silicon Revision. Bits [3:0] represent the minor Revision Number and bits [7:4] represent the major Revision Number.	RO	RO	–	AAh

Register 15-6. (Offset 09h; PCICLASS) PCI Class Code

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Programming Interface**	RO	RW	WO	00h
15:8	**Sub-Class Code**	RO	RW	WO	04h
23:16	**Base Class Code**	RO	RW	WO	06h

Register 15-7. (Offset 0Ch; PCICACHESIZE) PCI Cache Line Size

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size** Specifies the System Cache Line Size (in units of DWORDs). The value in this register is used by PCI Master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands for accessing memory. 0h = 0 DWords 2h = 2 DWords 4h = 4 DWords 8h = 8 DWords 10h = 16 DWords 20h = 32 DWords Writes of values other than these result in a Cache Line Size of 0; however, the value written is returned when this register is read.	RW	RW	WO	0h

Register 15-8. (Offset 0Dh; PCILATENCY) PCI Bus Latency Timer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Bus Latency Timer** Also referred to as *Primary Latency Timer* for Type 1 Configuration Space Header devices. The Primary/Master Latency Timer does not apply to PCI Express.	RO	RO	–	0h

Register 15-9. (Offset 0Eh; PCIHEADER) PCI Header Type

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Header Type** Specifies the format of the second part of the pre-defined Configuration Header, starting at offset 10h. For PCI bridges, this field is forced to 1h.	RO	RO	–	1h

Register 15-10. (Offset 0Fh; PCIBIST) PCI Built-In Self-Test

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self-Test** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h

Register 15-11. (Offset 10h; PCIBASE0) PCI Base Address 0 (BAR0)

Bit(s)	Description	CFG	MM	EE	Default
0	**Space Type** When Low, this space is accessed as memory. When High, this space is accessed as I/O. ***Note:*** *Hardwired to 0.*	RO	RO	–	0
2:1	**Address Type** Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = ***Reserved***	RO	RW	WO	10b
3	**Prefetch Enable** 1 = Indicates that prefetching has no side effects on Reads	RO	RW	WO	1
15:4	**Base Address** This section of the Base address is ignored for a 64-KB space. ***Note:*** *Hardwired to 0.*	RO	RO	–	0h
31:16	**Base Address** Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the PEX 8112 Configuration registers and shared memory.	RW	RW	WO	0h

Register 15-12. (Offset 14h; PCIBASE1) PCI Base Address 1 (BAR1)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Base Address 1** Determines the upper 32 bits of the address when **PCI Base Address 0** is configured for 64-bit addressing.	RW	RW	WO	0h

Register 15-13. (Offset 18h; PRIMBUSNUM) Primary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the PEX 8112's primary bus is connected.	RW	RW	WO	0h

Register 15-14. (Offset 19h; SECBUSNUM) Secondary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the PEX 8112's secondary bus is connected.	RW	RW	WO	0h

Register 15-15. (Offset 1Ah; SUBBUSNUM) Subordinate Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number** Used to record the Bus Number of the highest-numbered PCI Bus segment behind (or subordinate to) the PEX 8112.	RW	RW	WO	0h

Register 15-16. (Offset 1Bh; SECLATTIMER) Secondary Latency Timer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Secondary Latency Timer** Specifies (in PCI clock units) the Latency Timer value during secondary bus (PCI) Master bursts. When the Latency Timer expires, the PEX 8112 must terminate its tenure on the bus.	RW	RW	WO	0h

Register 15-17. (Offset 1Ch; IOBASE) I/O Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are ***reserved***.	RO	RW	WO	0000b
7:4	**I/O Base** Determines the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the PEX 8112 assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are 000h. Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB Address Boundary space, and the top is one less than a 4-KB Address Boundary space.	RW	RW	WO	0h

Register 15-18. (Offset 1Dh; IOLIMIT) I/O Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are ***reserved***. The value returned in this field is derived from the **I/O Base** register *I/O Base Address Capability* field.	RO	RO	–	0000b
7:4	**I/O Limit** Determines the I/O Space range forwarded from the primary bus to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the PEX 8112 assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary side of the PEX 8112, the *I/O Limit* field is programmed to a value smaller than the **I/O Base** register *I/O Base* field. In this case, the PEX 8112 does not forward I/O transactions from the primary bus to the secondary bus; however, the PEX 8112 does forward all I/O transactions from the secondary bus to the primary bus.	RW	RW	WO	0h

Register 15-19. (Offset 1Eh; SECSTAT) Secondary Status

Bit(s)	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable** Indicates whether the PEX 8112's secondary bus is capable of operating at 66 MHz.	RO	RW	WO	1
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Indicates whether the PEX 8112's secondary bus is capable of decoding Fast Back-to-Back transactions when the transactions are from the same Master but to different Targets. (A bridge is required to support Fast Back-to-Back transactions from the same Master.) The PEX 8112 does ***not support*** Fast Back-to-Back decoding.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Reports Data Parity error detection by the PEX 8112, when the bridge is the transaction Master on the secondary bus. Set when the following three conditions are true: • Bridge is the PCI Master of the transaction on the secondary bus • Bridge asserted PERR# (Read transaction) or detected that PERR# is asserted (Write transaction) • **Bridge Control** register *Secondary Parity Error Response Enable* bit is set Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Encodes the secondary bus DEVSEL# timing. The encoding must indicate the slowest response time that the PEX 8112 uses to assert DEVSEL# on its secondary bus when responding as a Target to a transaction other than a Configuration Read or Write. 01b = Indicates medium DEVSEL# timing ***Note:*** *Hardwired to 01b.*	RO	RO	–	01b
11	**Secondary Signaled Target Abort** Reports Target Abort termination signaling by the PEX 8112 when the bridge responds as the transaction Target on its secondary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 15-19. (Offset 1Eh; SECSTAT) Secondary Status *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
12	**Secondary Received Target Abort** Reports Target Abort termination detection by the PEX 8112 when the bridge is the transaction Master on its secondary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Reports Master Abort termination detection by the PEX 8112 when the bridge is the transaction Master on its secondary bus. Also set for a PCI Express-to-PCI Configuration transaction with an extended address not equal to 0. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Reports SERR# assertion detection on the PEX 8112's secondary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Reports Address or Data Parity error detection by the PEX 8112 on its secondary bus. Set when any of the following three conditions are true: • Bridge detects an Address Parity error as a potential Target • Bridge detects a Data Parity error when the PEX 8112 is a Write transaction Target • Bridge detects a Data Parity error when the PEX 8112 is a Read transaction Master Set irrespective of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 15-20. (Offset 20h; MEMBASE) Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Base** Determines the starting address at which Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are 0_0000h. The bottom of the defined Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.	RW	RW	WO	–

Register 15-21. (Offset 22h; MEMLIMIT) Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Limit** Determines the Memory Space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are F_FFFFh. When there are no Memory-Mapped I/O addresses on the secondary side of the PEX 8112, the *Memory Limit* field must be programmed to a value smaller than the **Memory Base** register *Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the PEX 8112, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 15-22. (Offset 24h; PREBASE) Prefetchable Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other encodings are ***reserved***.	RO	RW	WO	0000b
15:4	**Prefetchable Memory Base** Determines the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are 0_0000h. The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.	RW	RW	WO	–

Register 15-23. (Offset 26h; PRELIMIT) Prefetchable Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other encodings are ***reserved***. The value returned in this field is derived from the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field.	RO	RO	–	0000b
15:4	**Prefetchable Memory Limit** Determines the Prefetchable Memory space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are F_FFFFh. When there is no prefetchable memory on the secondary side of the PEX 8112, the *Prefetchable Memory Limit* field must be programmed to a value smaller than the **Prefetchable Memory Base** register *Prefetchable Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the PEX 8112, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 15-24. (Offset 28h; PREBASEUPPER) Prefetchable Memory Base Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits** When the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus.	RW	RW	WO	0h

Register 15-25. (Offset 2Ch; PRELIMITUPPER) Prefetchable Memory Limit Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits** When the **Prefetchable Memory Limit** register *Prefetchable Limit Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Limit Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the Prefetchable Memory range forwarded from the primary bus to the secondary bus.	RW	RW	WO	0h

Register 15-26. (Offset 30h; IOBASEUPPER) I/O Base Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits** When the **I/O Base** register *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus.	RW	RW	WO	–

Register 15-27. (Offset 32h; IOLIMITUPPER) I/O Limit Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits** When the **I/O Limit** register *I/O Limit Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Limit Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the I/O range forwarded from the primary bus to the secondary bus.	RW	RW	WO	–

Register 15-28. (Offset 34h; PCICAPPTR) PCI Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Capability Pointer** Provides the offset location of the first New Capabilities register (offset 40h, **Power Management Capability** structure).	RO	RW	WO	40h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-29. (Offset 3Ch; PCIINTLINE) PCI Interrupt Line

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Line** Indicates to which System Interrupt Controller input the PEX 8112 Interrupt ball is connected. Device drivers and operating systems use this field.	RW	RW	WO	0h

Register 15-30. (Offset 3Dh; PCIINTPIN) PCI Interrupt Pin

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt message(s) used by the PEX 8112. Valid values are 1, 2, 3, and 4, which map to Conventional PCI Interrupt messages for INTA#, INTB#, INTC#, and INTD#, respectively. 0h = Indicates that the PEX 8112 does not use Conventional PCI Interrupt messages	RO	RW	WO	1h

Register 15-31. (Offset 3Eh; BRIDGECTL) Bridge Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the PEX 8112's response to Address and Data Parity errors on the secondary bus (PCI). 0 = PEX 8112 must ignore detected Parity errors and continue standard operation. A bridge must generate parity, regardless of whether Parity error reporting is disabled. Also, the PEX 8112 must always forward Posted Write data with poisoning, from PCI-to-PCI Express on a PCI Data Parity error, regardless of this bit's setting. 1 = PEX 8112 must take its standard action when a Parity error is detected. (Refer to Section 10.1.1.2, "PCI Uncorrectable Data Errors" and Section 10.1.1.3, "PCI Address Errors.")	RW	RW	WO	0
1	**Secondary SERR# Enable** Controls forwarding of secondary bus (PCI) SERR# assertions to the primary bus (PCI Express). The PEX 8112 transmits an ERR_FATAL message on the primary bus when all of the following are true: • SERR# is asserted on the secondary bus • This bit is set • **PCI Command** register *SERR# Enable* bit is set or **PCI Express Device Control** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set	RW	RW	WO	0

Register 15-31. (Offset 3Eh; BRIDGECTL) Bridge Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
2	**ISA Enable** Modifies the PEX 8112's response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. 1 = PEX 8112 blocks forwarding from the primary bus to the secondary bus of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the PEX 8112's response to VGA-compatible addresses. When set to 1, the PEX 8112 positively decodes and forwards the following accesses on the primary bus to the secondary bus (and, conversely, blocks the forwarding of these addresses from the secondary bus to the primary bus): • Memory accesses within the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is within the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When set to 1, VGA address forwarding is independent of the: • Bit 2 (*ISA Enable)* setting • Memory and I/O Address ranges defined by the **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers VGA address forwarding is qualified by the **PCI Command** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Does not forward VGA-compatible Memory and I/O addresses from the primary bus to the secondary bus (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forwards VGA-compatible Memory and I/O addresses (addresses defined above) from the primary bus to the secondary bus (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 15-31. (Offset 3Eh; BRIDGECTL) Bridge Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the PEX 8112 to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable*) is also set to 1, enabling VGA I/O decoding and bridge forwarding. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary bus to the secondary bus, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls the PEX 8112's behavior when it receives a Master Abort termination on the PCI Bus or an Unsupported Request on the PCI Express interface. 0 = Do not report Master Aborts • When a PCI Express UR is received: – Return FFFF_FFFFh to the PCI Bus for Reads – Complete Non-Posted Write normally on the PCI Bus (assert TRDY#) and discard the Write data – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI 1 = Report Master Aborts • When a PCI Express UR is received: – Complete Reads and Non-Posted Writes with a PCI Target Abort – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**Secondary Bus Reset** 1 = Forces PCIRST# to be asserted on the secondary bus. Additionally, the PEX 8112 secondary bus, and buffers between the two buses (primary and secondary), must be initialized to their default state. The primary bus and Configuration Space registers must not be affected by setting this bit. Because PCIRST# is asserted while this bit is set, software must observe proper PCI Reset timing requirements.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported*** Controls the PEX 8112's ability to generate Fast Back-to-Back transactions to various secondary bus devices.	RO	RO	–	0

Register 15-31. (Offset 3Eh; BRIDGECTL) Bridge Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** In Forward Bridge mode, this bit does not apply and is forced to 0.	RO	RO	–	0
9	**Secondary Discard Timer** Selects the number of PCI clocks that the PEX 8112 waits for a Master on the secondary bus to repeat a Delayed Transaction request. The Counter starts after the Completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the PEX 8112 downstream queue (*that is*, all ordering requirements are satisfied and the PEX 8112 is ready to complete the Delayed Transaction with the originating Master on the secondary bus). When the originating Master does not repeat the transaction before the Counter expires, the PEX 8112 deletes the Delayed Transaction from its queue and sets bit 10 (*Discard Timer Status*). 0 = Secondary Discard Timer counts 2^{15} PCI clock periods 1 = Secondary Discard Timer counts 2^{10} PCI clock periods	RW	RW	WO	0
10	**Discard Timer Status** Set to 1 when the *Secondary Discard Timer* expires and a Delayed Completion is discarded from a queue within the PEX 8112. Writing 1 clears this bit.	RW1C	RW1C	WO	0
11	**Discard Timer SERR# Enable** When set to 1, enables the PEX 8112 to generate an ERR_NONFATAL message on the primary bus when the *Secondary Discard Timer* expires and a Delayed Transaction is discarded from a queue within the PEX 8112. 0 = Does not generate ERR_NONFATAL message on the primary bus as a result of the *Secondary Discard Timer* expiration 1 = Generates ERR_NONFATAL message on the primary bus when the *Secondary Discard Timer* expires and a Delayed Transaction is discarded from a queue within the PEX 8112	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	–	0h

15.6 PCI-Compatible Extended Capability Registers for PCI Express Interface

This section details the PEX 8112 Forward Bridge mode PCI-Compatible Extended Capability registers for the PCI Express interface. Table 15-7 defines the register map.

Table 15-7. Forward Bridge Mode PCI-Compatible Extended Capability for PCI Express Interface Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
40h	Power Management Capability		Power Management Next Capability Pointer	Power Management Capability ID
44h	Power Management Data	Power Management Bridge Support	Power Management Control/Status	
48h	Device-Specific Control			
4Ch	***Reserved***			
50h	MSI Control		MSI Next Capability Pointer	MSI Capability ID
54h	MSI Address			
58h	MSI Upper Address			
5Ch	***Reserved***		MSI Data	
60h	PCI Express Capability		PCI Express Next Capability Pointer	PCI Express Capability ID
64h	Device Capability			
68h	PCI Express Device Status		PCI Express Device Control	
6Ch	Link Capability			
70h	Link Status		***Reserved***	Link Control
74h	Slot Capability			
78h	Slot Status		Slot Control	
7Ch – 80h	***Reserved***			
84h	Main Control Register Index			
88h	Main Control Register Data			
8Ch – FFh	***Reserved***			

Register 15-32. (Offset 40h; PWRMNGID) Power Management Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID** Specifies the Power Management Capability ID.	RO	RO	–	01h

Register 15-33. (Offset 41h; PWRMNGNEXT) Power Management Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List (offset 50h, **MSI Capability** structure).	RO	RW	WO	50h

Register 15-34. (Offset 42h; PWRMNGCAP) Power Management Capability

Bit(s)	Description	CFG	MM	EE	Default
2:0	**PM Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1*.	RO	RW	WO	010b
3	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express; therefore, must always be a value of 0.	RO	RO	–	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the PEX 8112 requires special initialization following a transition to the D0_uninitialized Device PM state, before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PCI backplane PMEOUT# generation from the D3cold Device PM state is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Indicates whether the PEX 8112 supports the D1 Device PM state.	RO	RW	WO	1
10	**D2 Support** Indicates whether the PEX 8112 supports the D2 Device PM state. By default, D2 is ***not supported***; however, with additional circuitry, the PEX 8112 can support D2.	RO	RW	WO	0
15:11	**PME Support** Default 0101_1b indicates that the corresponding PEX 8112 port forwards PME messages in the D0, D3hot, and D3cold Device PM states. XXXX_1b = Assertable from D0 XXX1_Xb = Assertable from D1 XX1X_Xb = Assertable from D2 X1XX_Xb = Assertable from D3hot 1XXX_Xb = Assertable from D3cold	RO	RW	WO	0101_1b

Register 15-35. (Offset 44h; PWRMNGCSR) Power Management Control/Status

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine the current Device PM state of the port, and to set the port into a new Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3hot In the D1 and D2 Device PM states, when the corresponding *D1 Support* and *D2 Support* bits are set, PCI Memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration Requests are allowed. In the D3hot Device PM state, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables a PME message to transmit upstream.	RW	RW	WO	0
12:9	**Data Select** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** Indicates that a PME message was transmitted upstream. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 15-36. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support

Bit(s)	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** ***Not supported*** in Forward Bridge mode; therefore, forced to 0.	RO	RO	–	0
7	**Bus Power/Clock Control Enable** ***Not supported*** in Forward Bridge mode; therefore, forced to 0.	RO	RO	–	0

Register 15-37. (Offset 47h; PWRMNGDATA) Power Management Data

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Data** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h

Register 15-38. (Offset 48h; DEVSPECCTL) Device-Specific Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable** 0 = Memory Read command on the PCI Bus that targets the PCI Express Memory space causes only 1 word to be read from the PCI Express interface. 1 = Memory Read command on the PCI Bus that targets the PCI Express Memory space causes at least one Cache Line to be read from the PCI Express interface. Additional Dwords can be read by setting the **PCI Control** register *Programmed Prefetch Size* field.	RW	RW	WO	0
1	**PCI Base Address 0 Enable** 1 = Enables the **PCI Base Address 0** (**BAR0**) space for Memory-Mapped access to the Configuration registers and shared memory. **BAR0** is also enabled when the BAR0ENB# ball is Low.	RW	RW	WO	0
2	**L2 Enable** Does not apply to Forward Bridge mode.	RW	RW	WO	0
3	**PM Power Off** 1 = Link transitioned to the L2/L3 Ready Link PM state, and is ready to power down	RO	RO	–	0
7:4	**PM Link State** Indicates the Link PM state. 0001b = L0 0010b = L0s 0100b = L1 1000b = L2 All other encodings are ***reserved***.	RO	RO	–	–
9:8	**CRS Retry Control** Does not apply to Forward Bridge mode.	RW	RW	WO	00b
10	**WAKE Out Enable** 1 = WAKEOUT# signal is asserted when PMEIN# is asserted and the link remains in the L2 Link PM state	RW	RW	WO	0
11	**Beacon Generate Enable** 1 = Beacon is generated when PMEIN# is asserted and the link remains in the L2 Link PM state	RW	RW	WO	0
12	**Beacon Detect Enable** Does not apply to Forward Bridge mode.	RW	RW	WO	0
13	**PLL Locked** High when internal Phase-Locked Loop (PLL) is locked.	RO	RO	–	–
15:14	***Reserved***	RsvdP	RsvdP	–	00b
20:16	**Link Training and Status State Machine** ***Factory Test Only***	RO	RO	–	–
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-39. (Offset 50h; MSIID) MSI Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID** Specifies the Message Signaled Interrupt (MSI) Capability ID.	RO	RO	–	5h

Register 15-40. (Offset 51h; MSINEXT) MSI Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List (offset 60h, **PCI Express Capability** structure).	RO	RW	WO	60h

Register 15-41. (Offset 52h; MSICTL) MSI Control

Bit(s)	Description	CFG	MM	EE	Default
0	**MSI Enable** 1 = Enables the PEX 8112 to use MSI to request service. Virtual interrupt support for internal interrupt sources are disabled.	RW	RW	WO	0
3:1	**Multiple Message Capable** System software reads this field, to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four). 000b = 1 message requested 001b = 2 messages requested 010b = 4 messages requested 011b = 8 messages requested 100b = 16 messages requested 101b = 32 messages requested 110b, 111b = ***Reserved***	RO	RO	–	000b
6:4	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. 000b = 1 message allocated 001b = 2 messages allocated 010b = 4 messages allocated 011b = 8 messages allocated 100b = 16 messages allocated 101b = 32 messages allocated 110b, 111b = ***Reserved***	RW	RW	WO	000b
7	**MSI 64-Bit Address Capable** 1 = PEX 8112 is capable of generating a 64-bit Message address	RO	RW	WO	1
8	**Per Vector Masking Capable** ***Not supported*** Forced to 0.	RO	RO	–	0
15:9	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-42. (Offset 54h; MSIADDR) MSI Address

Bit(s)	Description	CFG	MM	EE	Default
1:0	***Reserved***	RsvdP	RsvdP	–	00b
31:2	**MSI Address** When the **MSI Control** register *MSI Enable* bit is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits [1:0] are driven to zero (00b) during the Address phase. ***Note:*** *Refer to register offset 58h for MSI Upper Address.*	RW	RW	WO	0h

Register 15-43. (Offset 58h; MSIUPPERADDR) MSI Upper Address

Bit(s)	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address** Valid/used only when the PEX 8112 supports a 64-bit Message address (**MSI Control** register *MSI 64-Bit Address Capable* bit is set to 1). When the **MSI Control** register *MSI Enable* bit is set, the register contents specify the upper 32 bits of a 64-bit message. When the register contents are zero (0h), the PEX 8112 uses the 32-bit address specified by the **MSI Address** register. ***Note:*** *Refer to register offset 54h for MSI Address.*	RW	RW	WO	0h

Register 15-44. (Offset 5Ch; MSIDATA) MSI Data

Bit(s)	Description	CFG	MM	EE	Default
15:0	**MSI Data** When the **MSI Control** register *MSI Enable* bit is set, the Message data is driven onto the lower word of the AD Bus (AD[15:0]) of the Memory Write Transaction Data phase. The upper word (AD[31:16]) is always cleared to 0h.	RW	RW	WO	0h
31:16	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-45. (Offset 60h; PCIEXID) PCI Express Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID** Specifies the PCI Express Capability ID.	RO	RW	–	10h

Register 15-46. (Offset 61h; PCIEXNEXT) PCI Express Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Capability Pointer** 0h = Last capability in the New Capabilities Linked List	RO	RW	WO	0h

Register 15-47. (Offset 62h; PCIEXCAP) PCI Express Capability

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Capability Version** Indicates the **PCI Express Capability** structure Version Number.	RO	RW	WO	1h
7:4	**Device/Port Type** Indicates the type of PCI Express logical device. 0000b = PCI Express Endpoint device 0001b = Conventional PCI Express Endpoint device 0100b = Root Port of PCI Express Root Complex 0101b = Upstream port of PCI Express switch 0110b = Downstream port of PCI Express switch 0111b = PCI Express-to-PCI/PCI-X bridge 1000b = PCI/PCI-X-to-PCI Express bridge All other encodings are ***reserved***.	RO	RW	WO	0111b
8	**Slot Implemented** 1 = Indicates that the PCI Express link associated with this port is connected to a slot	RO	RW	WO	0
13:9	**Interrupt Message Number** When this function is allocated more than one MSI number, this field must contain the offset between the Base Message data and the MSI message generated when **Slot Status** register bits of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the PEX 8112 changes.	RO	RO	–	0h
15:14	***Reserved***	RsvdP	RsvdP	–	00b

Register 15-48. (Offset 64h; DEVCAP) Device Capability

Bit(s)	Description	CFG	MM	EE	Default
2:0	**Maximum Payload Size Supported** Indicates the Maximum Payload Size that the PEX 8112 supports for TLPs. 000b = 128 bytes All other encodings are ***reserved***. *Because the* PEX 8112 *supports a Maximum Payload Size of only 128 bytes, this field is hardwired to 000b.*	RO	RO	–	000b
4:3	**Phantom Functions Supported** ***Not supported*** Hardwired to 00b. Indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called *Phantom Functions*) with the Tag identifier.	RO	RO	–	00b
5	**Extended Tag Field Supported** Indicates the maximum supported *Tag* field size. 0 = 5-bit *Tag* field is supported 1 = 8-bit *Tag* field is supported ***Note:*** *8-bit Tag field support must be enabled by the corresponding Control field in the* ***PCI Express Device Control*** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L0s to L0 Link PM state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Link PM state Acceptable Latency number to compare against the L0s Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L0s Link PM state entry is used with no performance loss. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	000b

Register 15-48. (Offset 64h; DEVCAP) Device Capability *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
11:9	**Endpoint L1 Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L1 to L0 Link PM state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Link PM state Acceptable Latency number to compare against the L1 Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L1 Link PM state entry is used with no performance loss. 000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs	RO	RW	WO	000b
12	**Attention Button Present** ***Not supported*** Forced to 0.	RO	RO	–	0
13	**Attention Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
14	**Power Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
17:15	***Reserved***	RsvdP	RsvdP	–	000b
25:18	**Captured Slot Power Limit Value** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Value is set by the Set Slot Power Limit message.	RO	RW	WO	0h
27:26	**Captured Slot Power Limit Scale** Specifies the scale used for the *Slot Power Limit Value.* Value is set by the Set Slot Power Limit message. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
31:28	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-49. (Offset 68h; DEVCTL) PCI Express Device Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable** Controls Correctable error reporting. When a Correctable error is detected in Forward Bridge mode and this bit is set, an ERR_COR message is transmitted to the Root Complex.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable** Controls Non-Fatal error reporting. When a Non-Fatal error is detected in Forward Bridge mode and this bit is set, an ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
2	**Fatal Error Reporting Enable** Controls Fatal error reporting. When a Fatal error is detected in Forward Bridge mode and this bit is set, an ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable** Controls Unsupported Request reporting. When an Unsupported Request response is received from the PCI Express in Forward Bridge mode and this bit is set, a ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
4	**Enable Relaxed Ordering** ***Not supported*** Forced to 0.	RO	RO	–	0
7:5	**Maximum Payload Size** Sets the maximum TLP Payload Size for the PEX 8112. As a Receiver, the PEX 8112 must handle TLPs as large as the set value; as Transmitter, the PEX 8112 must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the **Device Capability** register *Maximum Payload Size Supported* field. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = ***Reserved***	RW	RW	WO	000b

Register 15-49. (Offset 68h; DEVCTL) PCI Express Device Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable** 0 = PEX 8112 is restricted to a 5-bit *Tag* field 1 = Enables PEX 8112 to use an 8-bit *Tag* field as a Requester Forced to 0 when the **Device Capability** register *Extended Tag Field Supported* bit is cleared.	RW	RW	WO	0
9	**Phantom Function Enable** ***Not supported*** Hardwired to 0.	RO	RO	–	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported*** Hardwired to 0.	RO	RO	–	0
11	**Enable No Snoop** ***Not supported*** Hardwired to 0.	RO	RO	–	0
14:12	**Maximum Read Request Size** The value specified in this register is the upper boundary of the **PCI Control** register *Programmed Prefetch Size* field if the **Device-Specific Control** register *Blind Prefetch Enable* bit is set. Sets the Maximum Read Request Size for the PEX 8112 as a Requester. The PEX 8112 must not generate Read Requests with a size that exceeds the set value. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = ***Reserved***	RW	RW	WO	010b
15	**Bridge Configuration Retry Enable** 0 = PEX 8112 does not generate Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. 1 = PEX 8112 generates Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. Occurs after a delay determined by the **CRS Timer** register.	RW	RW	WO	0

Register 15-50. (Offset 6Ah; DEVSTAT) PCI Express Device Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Detected** Indicates Correctable errors detected status. Errors are logged in this register, regardless of whether Error Reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
1	**Non-Fatal Error Detected** Indicates Non-Fatal errors detected status. Errors are logged in this register, regardless of whether Error Reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
2	**Fatal Error Detected** Indicates Fatal errors detected status. Errors are logged in this register, regardless of whether Error Reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
3	**Unsupported Request Detected** Indicates that the PEX 8112 received an Unsupported Request. Errors are logged in this register, regardless of whether Error Reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
4	**AUX Power Detected** Devices that require AUX power report this bit as set when the PEX 8112 detects AUX power.	RO	RO	–	0
5	**Transactions Pending** Because the PEX 8112 does not internally generate Non-Posted transactions, this bit is forced to 0.	RO	RO	–	0
15:6	***Reserved***	RsvdZ	RsvdZ	–	0h

Register 15-51. (Offset 6Ch; LINKCAP) Link Capability

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed** Indicates the maximum link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are ***reserved***.	RO	RO	–	0001b
9:4	**Maximum Link Width** Indicates the maximum width of the given PCI Express link. By default, the PEX 8112 has a x1 link; therefore, this field is hardwired to 00_0001b. All other encodings are ***not supported***.	RO	RO	–	00_0001b
11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported on the given PCI Express link. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported 00b, 10b = ***Reserved***	RO	RW	WO	11b
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L0s to L0 Link PM state. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	100b
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L1 to L0 Link PM state. 000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs	RO	RW	WO	100b
23:18	***Reserved***	RsvdP	RsvdP	–	0h
31:24	**Port Number** Indicates the PCI Express Port Number for the given PCI Express link.	RO	RW	WO	0h

Register 15-52. (Offset 70h; LINKCTL) Link Control

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Active State Power Management (ASPM) Control** Controls the level of ASPM supported on the given PCI Express link. 00b = Disabled 01b = L0s Link PM state entry is supported 10b = ***Reserved*** 11b = L0s and L1 Link PM state entry is supported ***Note:*** *"L0s Entry Enabled" indicates the Transmitter entering the L0s Link PM state.*	RW	RW	WO	00b
2	***Reserved***	RsvdP	RsvdP	–	0
3	**Read Completion Boundary (RCB) Control** 0 = Read Completion boundary is 64 bytes 1 = Read Completion boundary is 128 bytes	RW	RW	WO	0
4	**Link Disable** Does not apply to Forward Bridge mode.	RO	RO	–	0
5	**Retrain Link** Does not apply to Forward Bridge mode.	RO	RO	–	0
6	**Common Clock Configuration** 0 = Indicates that the PEX 8112 and the component at the opposite end of the link are operating with **asynchronous** Reference Clock. Components use this common clock configuration information to report the correct L0s and L1 Link PM state Exit Latencies. 1 = Indicates that the PEX 8112 and the component at the opposite end of the link are operating with a **distributed** common Reference Clock.	RW	RW	WO	0
7	**Extended Sync** 1 = Forces extended transmission of FTS Ordered-Sets in FTS and extra TS2 at exit from the L1 Link PM state prior to entering the L0 Link PM state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters the L0 Link PM state and resumes communication.	RW	RW	WO	0
15:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-53. (Offset 72h; LINKSTAT) Link Status

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Link Speed** Indicates the negotiated link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are ***reserved***.	RO	RO	–	0001b
9:4	**Negotiated Link Width** Indicates the negotiated width of the given PCI Express link. By default, the PEX 8112 has a x1 link; therefore, this field is hardwired to 00_0001b. All other encodings are ***not supported***.	RO	RO	–	00_0001b
10	**Link Training Error** Does not apply to Forward Bridge mode.	RO	RO	–	0
11	**Link Training** Does not apply to Forward Bridge mode.	RO	RO	–	0
12	**Slot Clock Configuration** Indicates that the PEX 8112 uses the same physical Reference Clock that the platform provides on the connector. When the PEX 8112 uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	HwInit	RW	WO	0
15:13	***Reserved***	RsvdZ	RsvdZ	–	000b

Register 15-54. (Offset 74h; SLOTCAP) Slot Capability

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Present** ***Not supported*** Forced to 0.	RO	RO	–	0
1	**Power Controller Present** ***Not supported*** Forced to 0.	RO	RO	–	0
2	**MRL Sensor Present** ***Not supported*** Forced to 0.	RO	RO	–	0
3	**Attention Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
4	**Power Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
5	**Hot Plug Surprise** ***Not supported*** Forced to 0.	RO	RO	–	0
6	**Hot Plug Capable** ***Not supported*** The PEX 8112 does ***not support*** Hot Plug operations; therefore, this bit is forced to 0.	RO	RO	–	0
14:7	**Slot Power Limit Value** Does not apply to Forward Bridge mode.	RO	RW	WO	25d
16:15	**Slot Power Limit Scale** Does not apply to Forward Bridge mode.	RO	RW	WO	00b
18:17	***Reserved***	RsvdP	RsvdP	–	00b
31:19	**Physical Slot Number** ***Not supported*** Forced to 0h.	RO	RO	–	0h

Register 15-55. (Offset 78h; SLOTCTL) Slot Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
1	**Power Fault Detected Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
2	**MRL Sensor Changed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
3	**Presence Detect Changed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
4	**Command Completed Interrupt Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
7:6	**Attention Indicator Control** ***Not supported*** Forced to 00b.	RW	RW	WO	00b
9:8	**Power Indicator Control** ***Not supported*** Forced to 00b.	RW	RW	WO	00b
10	**Power Controller Control** ***Not supported*** Forced to 0.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-56. (Offset 7Ah; SLOTSTAT) Slot Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed** ***Not supported*** Forced to 0.	RO	RO	–	0
1	**Power Fault Detected** ***Not supported*** Forced to 0.	RO	RO	–	0
2	**MRL Sensor Changed** ***Not supported*** Forced to 0.	RO	RO	–	0
3	**Presence Detect Changed** ***Not supported*** Forced to 0.	RO	RO	–	0
4	**Command Completed** ***Not supported*** Forced to 0.	RO	RO	–	0
5	**MRL Sensor State** ***Not supported*** Forced to 0.	RO	RO	–	0
6	**Presence Detect State** ***Not supported*** Forced to 1.	RO	RO	–	1
15:7	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-57. (Offset 84h; MAININDEX) Main Control Register Index

Bit(s)	Description	CFG	MM	EE	Default
11:0	**Main Control Register Index** Selects a **Main Control** register, that is accessed by way of the **Main Control Register Data** register.	RW	RW	WO	0h
31:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-58. (Offset 88h; MAINDATA) Main Control Register Data

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Main Control Register Data** Writes to and reads from this register are mapped to a **Main Control** register, selected by the **Main Control Register Index** register.	RW	RW	WO	0h

15.7 PCI Express Extended Capability Registers

This section details the PEX 8112 Forward Bridge mode PCI Express Extended Capability registers – Power Budget Capability and Device Serial Number. Table 15-8 defines the register map.

Table 15-8. Forward Bridge Mode Power Budget Capability and Device Serial Number Register Map

PCI Express Configuration Register Offset	31 20	19 16	15 8	7 0
100h	Power Budget Next Capability Offset	Power Budget Capability Version	Power Budget PCI Express Extended Capability ID	
104h	***Reserved***			Power Budget Data Select
108h	Power Budget Data			
10Ch	Power Budget Capability			
110h	Serial Number Next Capability Offset	Serial Number Capability Version	Serial Number PCI Express Extended Capability ID	
114h	Serial Number Low (Lower DWORD)			
118h	Serial Number Hi (Upper DWORD)			
11Ch – FFFh	***Reserved***			

15.7.1 PCI Express Power Budget Registers

Register 15-59. (Offset 100h; PWRCAPHDR) Power Budget Enhanced Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability.	RO	RW	WO	4h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present.	RO	RW	WO	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List. Set to 110h when Serial Number Capability must be enabled.	RO	RW	WO	000h

Register 15-60. (Offset 104h; PWRDATASEL) Power Budget Data Select

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Data Select** Indexes the Power Budget Data reported through the **Power Budget Data** register. Selects the DWORD of Power Budget Data that is to appear in the **Power Budget Data** register. The PEX 8112 supports values from 0 to 31 for this field. For values greater than 31, a value of 0h is returned when the **Power Budget Data** register is read.	RW	RW	WO	0h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-61. (Offset 108h; PWRDATA) Power Budget Data

Bit(s)	Description	CFG	MM	EE	Default
Note: *This register returns the DWORD of Power Budget Data selected by the* ***Power Budget Data Select*** *register. When the* ***Power Budget Data Select*** *register has a value greater than or equal to the number of operating conditions for which the PEX 8112 provides power information, this register returns all zeros (0). The PEX 8112 supports 32 operating conditions.*					
7:0	**Base Power** Specifies (in Watts) the base power value in the given operating condition. This value must be multiplied by the Data Scale, to produce the actual power consumption value.	RO	RW	WO	0h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The PEX 8112 power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
12:10	**PM Sub-State** Specifies the power management sub-state of the operating condition being described. 000b = Default Sub-State All other values = Device-Specific Sub-State	RO	RW	WO	000b
14:13	**PM State** Specifies the Device PM state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in the *PM Type* field to specify the D3cold Device PM state. An encoding of 11b, along with any other *PM Type* field value, specifies the D3hot Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3	RO	RW	WO	00b
17:15	**PM Type** Specifies the type of operating condition being described. 000b = PME Aux 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	RO	RW	WO	000b
20:18	**Power Rail** Specifies the power rail of the operating condition being described. 000b = Power (12V) 001b = Power (3.3V) 010b = Power (1.8V) 111b = Thermal All other encodings are ***reserved***.	RO	RW	WO	000b
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 15-62. (Offset 10Ch; PWRBUDCAP) Power Budget Capability

Bit(s)	Description	CFG	MM	EE	Default
0	**System Allocated** 1 = Indicates that the PEX 8112 power budget is included within the system power budget, and software is to ignore Reported Power Budget data for power budgeting decisions	RO	RW	WO	0
31:1	***Reserved***	RsvdP	RsvdP	–	0h

15.7.2 PCI Express Serial Number Registers

Register 15-63. (Offset 110h; SERCAPHDR) Serial Number Enhanced Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	3h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present. Forced to 0h when Serial Number Capability is disabled.	RO	RO	–	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List.	RO	RO	–	000h

Register 15-64. (Offset 114h; SERNUMLOW) Serial Number Low (Lower DWORD)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the lower DWORD of the IEEE-defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0h when Serial Number Capability is disabled.	RO	RW	WO	0h

Register 15-65. (Offset 118h; SERNUMHI) Serial Number Hi (Upper DWORD)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the upper DWORD of the IEEE defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0h when Serial Number Capability is disabled.	RO	RW	WO	0h

15.8 Main Control Registers

This section details the PEX 8112 Forward Bridge mode Main Control registers. Table 15-9 defines the register map.

Table 15-9. Forward Bridge Mode Main Control Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
1000h	Device Initialization			
1004h	Serial EEPROM Control			
1008h	Serial EEPROM Clock Frequency			
100Ch	PCI Control			
1010h	PCI Express Interrupt Request Enable			
1014h	***Reserved***			
1018h	Interrupt Request Status			
101Ch	Power			
1020h	General-Purpose I/O Control			
1024h	General-Purpose I/O Status			
1030h	Mailbox 0			
1034h	Mailbox 1			
1038h	Mailbox 2			
103Ch	Mailbox 3			
1040h	***Reserved***		Chip Silicon Revision	
1044h	Diagnostic Control ***(Factory Test Only)***			
1048h	***Reserved***	TLP Controller Configuration 0		
104Ch	TLP Controller Configuration 1			
1050h	TLP Controller Configuration 2			
1054h	***Reserved***	TLP Controller Tag		
1058h	TLP Controller Time Limit 0			
105Ch	TLP Controller Time Limit 1			
1060h	***Reserved***		CRS Timer	
1064h	Enhanced Configuration Address			
1068h – 1FFFh	***Reserved***			

Register 15-66. (Offset 1000h; DEVINIT) Device Initialization

Bit(s)	Description	CFG	MM
3:0	**PCLKO Clock Frequency** Controls the PCLKO ball frequency as follows, when PCLKO62SEL# is strapped High or left disconnected. When cleared to 0000b, the clock is stopped and remains at a logic Low (0V) DC value. Non-zero values represent divisors of the 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. The default value is 0011b, representing a frequency of 33, 62.5, or 66 MHz. When PCLKO62SEL# is pulled Low and M66EN is High, the PCLKO frequency is 62.5 MHz, with a 50% Duty cycle. 0000b = 0 0001b = 100 0010b = 50 0011b = 33.3/66/62.5, depending upon M66EN and PCLKO62SEL# values 0100b = 25 0101b = 20 0110b = 16.7 0111b = 14.3 1000b = 12.5 1001b = 11.1 1010b = 10 1011b = 9.1 1100b = 8.3 1101b = 7.7 1110b = 7.1 1111b = 6.7	RW	0011b
4	**PCI Express Enable** 0 = All Configuration accesses to the PEX 8112, configured in Forward Bridge mode, result in a Completion status of Configuration Request Retry Status. 1 = PEX 8112 responds normally to PCI Express Configuration accesses. Automatically set when a valid serial EEPROM is not detected.	RW	0
5	**PCI Enable** 0 = All PCI accesses to the PEX 8112 result in a Target Retry response 1 = PEX 8112 responds normally to PCI accesses Automatically set when a valid serial EEPROM is not detected.	RW	0
31:6	***Reserved***	RsvdP	0h

Register 15-67. (Offset 1004h; EECTL) Serial EEPROM Control

Bit(s)	Description	CFG	MM
7:0	**Serial EEPROM Write Data** Determines the byte written to the serial EEPROM when the *Serial EEPROM Byte Write Start* bit is set. Represents an opcode, address, or data being written to the serial EEPROM.	RW	0h
15:8	**Serial EEPROM Read Data** Determines the byte read from the serial EEPROM when the *Serial EEPROM Byte Read Start* bit is set.	RO	–
16	**Serial EEPROM Byte Write Start** 1 = Value in the *Serial EEPROM Write Data* field is written to the serial EEPROM Automatically cleared when the Write operation is complete.	RW	0
17	**Serial EEPROM Byte Read Start** 1 = A byte is read from the serial EEPROM, and accessed using the *Serial EEPROM Read Data* field Automatically cleared when the Read operation is complete.	RW	0
18	**Serial EEPROM Chip Select Enable** 1 = Serial EEPROM Chip Select is enabled	RW	0
19	**Serial EEPROM Busy** 1 = Serial EEPROM Controller is busy performing a Byte Read or Write operation An interrupt is generated when this bit goes false.	RO	0
20	**Serial EEPROM Valid** 1 = Serial EEPROM with 5Ah in the first byte is detected	RO	–
21	**Serial EEPROM Present** Set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the PEX 8112.	RO	–
22	**Serial EEPROM Chip Select Active** Set when the EECS# ball to the serial EEPROM is active. The Chip Select can be active across multiple byte operations.	RO	–
24:23	**Serial EEPROM Address Width** Reports the installed serial EEPROM's addressing width. When the addressing width cannot be determined, 00b is returned. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	RO	–
30:25	***Reserved***	RsvdP	0h
31	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the serial EEPROM. Reading this bit returns 0 while initialization is in progress, and 1 when initialization is complete.	RW	0

Register 15-68. (Offset 1008h; EECLKFREQ) Serial EEPROM Clock Frequency

Bit(s)	Description	Access	Default
2:0	**Serial EEPROM Clock Frequency** Controls the EECLK ball frequency. 000b = 2 MHz 001b = 5 MHz 010b = 8.3 MHz 011b = 10 MHz 100b = 12.5 MHz 101b = 16.7 MHz 110b = 25 MHz 111b = ***Reserved***	RW	000b
31:3	***Reserved***	RsvdP	0h

Register 15-69. (Offset 100Ch; PCICTL) PCI Control

Bit(s)	Description	Access	Default
0	**PCI Multi-Level Arbiter** 0 = All PCI Requesters are placed into a single-level Round-Robin Arbiter, each with equal access to the PCI Bus 1 = Two-level Arbiter is selected	RW	0
3:1	**PCI Arbiter Park Select** Determines which PCI Master Controller is granted the PCI Bus when there are no pending requests. 000b = Last grantee 001b = PCI Express interface 010b, 011b = ***Reserved*** 100b = External Requester 0 101b = External Requester 1 110b = External Requester 2 111b = External Requester 3	RW	000b
4	**Bridge Mode** Reflects the FORWARD ball status. When Low, the PEX 8112 operates as a Reverse Bridge (PCI-to-PCI Express). When High, the PEX 8112 operates as a Forward Bridge (PCI Express-to-PCI).	RO	–
5	**PCI External Arbiter** Reflects the EXTARB ball state. When Low, the PEX 8112 enables its Internal PCI Arbiter. The PEX 8112 then expects external requests on REQ[3:0]# and issues bus grants on GNT[3:0]#. When High, the PEX 8112 asserts REQ0# and expects GNT0# from an External Arbiter.	RO	–
6	**Locked Transaction Enable** 0 = PCI Express Memory Read Lock Requests are completed with UR status, and the PCI LOCK# ball is not driven	RW	0
7	**M66EN** Reflects the M66EN ball state. When Low, the PEX 8112 PCI Bus is operating at 33 MHz. When High, the PEX 8112 PCI Bus is operating at 66 MHz.	RO	0

Register 15-69. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bit(s)	Description	Access	Default
15:8	**PCI-to-PCI Express Retry Count** Does not apply to Forward Bridge mode.	RW	80h
23:16	**PCI Express-to-PCI Retry Count** Determines the number of times to Retry a PCI Express-to-PCI transaction before aborting the transfer (in units of 2^4 Retries). Values 1 to 254 select multiples of 2^4. Values 0 and 255 are special cases (0 = Retry forever, 255 = 2^{24} Retries) 0 = Indicates that the transaction is Retried forever 1 = Selects a Retry Count of 2^4 254 = Selects a Retry Count of 254 * (2^4) 255 = Selects a Retry Count of 2^{24} (special case)	RW	0h
24	**Memory Read Line Enable** 0 = PEX 8112 issues a Memory Read command for transactions that do not start on a Cache boundary. 1 = Memory Read Line command is issued when a transaction is not aligned to a Cache boundary in Prefetchable Address space, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst is stopped at the Cache Line boundary when the Burst Transfer Size is less than one Cache Line of data or when a Memory Read Multiple command is started.	RW	1
25	**Memory Read Multiple Enable** 0 = PEX 8112 issues a Memory Read command for transactions that start on a Cache boundary. 1 = Memory Read Multiple command is issued when a transaction is aligned to a Cache boundary in Prefetchable Address space, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst continues when the Burst Transfer Size remains greater than or equal to one cache line of data.	RW	1
26	**Early Byte Enables Expected** 0 = PEX 8112 expects the PCI Bytes Enables to be valid after IRDY# is asserted 1 = PEX 8112 expects the PCI Byte Enables to be valid in the clock tick following the Address phase For maximum compatibility with non-compliant PCI devices, clear this bit to 0. For maximum performance, set this bit to 1.	RW	0

Register 15-69. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bit(s)	Description	Access	Default
29:27	**Programmed Prefetch Size** Valid only for Memory Read Line and Memory Read Multiple transactions, or Memory Read transactions accessing Prefetchable Memory space with the **Device-Specific Control** register *Blind Prefetch Enable* bit set. Determines the number of bytes requested from the PCI Express interface as a result of a PCI-to-PCI Express Read. If a Prefetch Size is specified, the Cache Line boundary requirements of the Memory Read Line and Memory Read Multiple commands are disabled and the number of bytes requested will match the Prefetch Size. Enable this feature only when the PCI Master reads all requested data without disconnecting. Otherwise, performance is impacted. The Prefetch Size is limited by the **PCI Express Device Control** register *Maximum Read Request Size* field. 000b = Disabled 001b = 64 bytes 010b = 128 bytes 011b = 256 bytes 100b = 512 bytes 101b = 1,024 bytes 110b = 2,048 bytes 111b = 4,096 bytes (4 KB; refer to Note) ***Note:*** *If the Programmed Prefetch Size is 4 KB, the **TLP Controller Configuration 0** register Limit Completion Flow Control Credit bit must be set.*	RW	000b
30	**Short Discard Timer Timeout Select** Specifies the length of time that data returned from the PCI Express device, in response to a PCI Read Request, is held before it is discarded. 0 = Data is discarded after 32,767 or 1,024 PCI Clock cycles, as selected by the **Bridge Control** register *Primary Discard Timer* bit (bit 8) 1 = Data is discarded after only 64 PCI Clock cycles	RW	0
31	**PE2P Rdline Override** PCI Express-to-PCI Memory Read Line Override. In Forward Bridge mode, PCI Express-to-PCI Read Requests in Memory-Mapped I/O (Non-Prefetchable) space usually result in PCI Memory Read commands, as per the *PCI-to-PCI Bridge r1.1*. For certain applications, however, it might be necessary to issue PCI Memory Read Line or Memory Read Multiple commands. Although the request is to Non-Prefetchable space, setting this bit enables these PCI Cache commands, as long as all other requirements are met.	RW	0

Register 15-70. (Offset 1010h; PCIEIRQENB) PCI Express Interrupt Request Enable

Bit(s)	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when a Serial EEPROM Read or Write transaction completes ***Note:*** *Refer to Section 5.1, "Forward Bridge PCI Interrupts," for further details.*	RW	0
1	**GPIO Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when an interrupt is active from one of the GPIO balls	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when the PCI Express-to-PCI Retry Count is reached	RW	0
4	**Mailbox 0 Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when Mailbox 0 is written	RW	0
5	**Mailbox 1 Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when Mailbox 1 is written	RW	0
6	**Mailbox 2 Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when Mailbox 2 is written	RW	0
7	**Mailbox 3 Interrupt Enable** 1 = Enables a PCI Express interrupt to generate when Mailbox 3 is written	RW	0
8	**Unsupported Request Interrupt Enable** 1 = Enables a PCI interrupt to be generated when an Unsupported Request Completion response is received from the PCI Express interface	RW	0
30:9	***Reserved***	RsvdP	0h
31	**PCI Express Internal Interrupt Enable** 1 = Enables a PCI Express interrupt to be generated as a result of an internal PEX 8112 interrupt source. The internal interrupt is serviced as a Message Signaled interrupt (MSI) or Virtual Wire interrupt. ***Note:*** *Refer to Section 5.1, "Forward Bridge PCI Interrupts," for further details.*	RW	1

Register 15-71. (Offset 1018h; IRQSTAT) Interrupt Request Status

Bit(s)	Description	Access	Default
0	**Serial EEPROM Done Interrupt** Set when a Serial EEPROM Read or Write transaction completes. Writing 1 clears this status bit.	RW1C	0
1	**GPIO Interrupt** Conveys the interrupt status for the four GPIO balls. Set independently of the *GPIO Interrupt Enable* bits. This bit is an OR of the four individual GPIO status bits. 1 = **General-Purpose I/O Status** register is read to determine the cause of the interrupt	RO	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt** Set when the PCI Express-to-PCI Retry count is reached. Writing 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt** Set when Mailbox 0 is written. Writing 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt** Set when Mailbox 1 is written. Writing 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt** Set when Mailbox 2 is written. Writing 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt** Set when Mailbox 3 is written. Writing 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt** Set when an Unsupported Request Completion is received from the PCI Express interface, provided that the **PCI Express Interrupt Request Enable** register *Unsupported Request Interrupt Enable* bit is set.	RW1C	0
31:9	***Reserved***	RsvdZ	0h

Register 15-72. (Offset 101Ch; POWER) Power

Bit(s)	Description	Access	Default
7:0	**Power Compare 0** Specifies the power required for this device and downstream PCI devices. It is compared with the **Device Capability** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capability** register *Captured Slot Power Limit Scale* field is 00b (scale = 1.0x).	RW	0h
15:8	**Power Compare 1** Specifies the power required for this device and downstream PCI devices. It is compared with the **Device Capability** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capability** register *Captured Slot Power Limit Scale* field is 01b (scale = 0.1x).	RW	0h
23:16	**Power Compare 2** Specifies the power required for this device and downstream PCI devices. It is compared with the **Device Capability** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capability** register *Captured Slot Power Limit Scale* field is 10b (scale = 0.01x).	RW	0h
31:24	**Power Compare 3** Specifies the power required for this device and downstream PCI devices. It is compared with the **Device Capability** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the **Device Capability** register *Captured Slot Power Limit Scale* field is 11b (scale = 0.001x).	RW	0h

Register 15-73. (Offset 1020h; GPIOCTL) General-Purpose I/O Control

Bit(s)	Description	Access	Default
0	**GPIO0 Data** When programmed as an output, values written to this bit appear on the GPIO0 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 ball.	RW	0
1	**GPIO1 Data** When programmed as an output, values written to this bit appear on the GPIO1 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 ball.	RW	0
2	**GPIO2 Data** When programmed as an output, values written to this bit appear on the GPIO2 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 ball.	RW	0
3	**GPIO3 Data** When programmed as an output, values written to this bit appear on the GPIO3 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 ball.	RW	0
4	**GPIO0 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO0 ball is an input 1 = GPIO0 ball is an output	RW	1
5	**GPIO1 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO1 ball is an input 1 = GPIO1 ball is an output	RW	0
6	**GPIO2 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO2 ball is an input 1 = GPIO2 ball is an output	RW	0
7	**GPIO3 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO3 ball is an input 1 = GPIO3 ball is an output	RW	0
8	**GPIO0 Interrupt Enable** 1 = Changes on the GPIO0 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
9	**GPIO1 Interrupt Enable** 1 = Changes on the GPIO1 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
10	**GPIO2 Interrupt Enable** 1 = Changes on the GPIO2 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
11	**GPIO3 Interrupt Enable** 1 = Changes on the GPIO3 ball (when programmed as an input) are enabled to generate an interrupt	RW	0

Register 15-73. (Offset 1020h; GPIOCTL) General-Purpose I/O Control *(Cont.)*

Bit(s)	Description	Access	Default
13:12	**GPIO Diagnostic Select** Selects diagnostic signals that are output on the GPIO balls. 00b = Normal GPIO operation 01b = GPIO0 driven High when the link is up. GPIO[3:1] operate according to the configuration specified by bits [7:5] of this register 10b = GPIO[3:0] driven with lower four bits of the Link Training and Status State Machine (LTSSM) for 2s, alternating with GPIO[1:0] driven with the upper two bits of the LTSSM for 1s 11b = GPIO[3:0] driven with PM Link state (L2, L1, L0s, and L0 Link PM states) **LTSSM Codes** 00h – L3_L2 (Fundamental Reset) 01h – Detect 02h – Polling.Active 03h – Polling.Configuration 04h – Polling.Compliance 05h – ***Reserved*** 06h – ***Reserved*** 07h – ***Reserved*** 08h – ***Reserved*** 09h – Configuration.Linkwidth.Start 0Ah – Configuration.Linkwidth.Accept 0Bh – Configuration.Lanenum.Wait & Accept 0Ch – Configuration.Complete 0Dh – Configuration.Idle 0Eh – L0 0Fh – L0 (Transmit E.I.Ordered-Set) 10h – L0 (Wait E.I.Ordered-Set) 12h – L1.Idle 14h – L2.Idle 15h – Recovery.Rcvrlock (Extended Sync enabled) 16h – Recovery.Rcvrlock 17h – Recovery.RcvrCfg 18h – Recovery.Idle 19h – Disabled (Transmit TS1) 1Ah – Disabled (Transmit E.I.Ordered-Set) 1Dh – Disabled (Wait Electrical Idle) 1Eh – Disabled (Disable) 1Fh – Loopback.Entry 20h – Loopback.Active 21h – Loopback.Exit 22h – ***Reserved*** 23h – Hot Reset (Reset Active) 24h – Loopback.Actice (Transmit E.I.Ordered-Set) 25h – Loopback.Active (Wait Electrical Idle)	RW	01b
31:14	***Reserved***	RsvdP	0h

Register 15-74. (Offset 1024h; GPIOSTAT) General-Purpose I/O Status

Bit(s)	Description	Access	Default
0	**GPIO0 Interrupt** Set when the GPIO0 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt** Set when the GPIO1 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt** Set when the GPIO2 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt** Set when the GPIO3 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
31:4	***Reserved***	RsvdZ	0h

Register 15-75. (Offset 1030h; MAILBOX0) Mailbox 0

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	FEED_FACEh

Register 15-76. (Offset 1034h; MAILBOX1) Mailbox 1

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 15-77. (Offset 1038h; MAILBOX2) Mailbox 2

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 15-78. (Offset 103Ch; MAILBOX3) Mailbox 3

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 15-79. (Offset 1040h; CHIPREV) Chip Silicon Revision

Bit(s)	Description	Access	Default
15:0	**Chip Revision** Returns the PEX 8112 current Silicon Revision number. ***Note: CHIPREV** is the Silicon Revision, encoded as a 4-digit BCD value. The **CHIPREV** value for the first release of the chip (Rev. AA) is 0A0Ah. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*	RO	Current Revision
31:16	***Reserved***	RsvdP	0h

Register 15-80. (Offset 1044h; DIAGCTL) Diagnostic Control *(Factory Test Only)*

Bit(s)	Description	Access	Default
0	**Fast Times** ***Factory Test Only***	RW	0
1	**Force PCI Interrupt** ***Factory Test Only*** 1 = Forces the PCI INT*x*# Interrupt signal to assert. The **PCI Interrupt Pin** register determines which INT*x*# signal is asserted. Effective only when the **PCI Command** register *Interrupt Disable* bit is Low.	RW	0
2	**Force PCI SERR** ***Factory Test Only*** 1 = Forces the PCI SERR# Interrupt signal to assert when the **Bridge Control** register *Secondary SERR# Enable* bit is set	RW	0
3	**Force PCI Express Interrupt** ***Factory Test Only*** 1 = Forces an interrupt to the PCI Express Root Complex, using Message Signaled interrupts or virtual INT*x*# interrupts	RW	0
31:4	***Reserved***	RsvdP	0h

Register 15-81. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0

Bit(s)	Description	Access	Default
7:0	**CFG_NUM_FTS** Forced NUM_FTS signal. NUM_FTS represents the number of Fast Training sequence (0 to 255). Refer to the *PCI Express r1.0a*, Section 4.2.4.3, for further details.	RW	20h
8	**CFG_ACK_FMODE** PCI Express interface ACK_DLLP transmitting interval mode. 0 = PCI Express interface uses own interval value 1 = PCI Express interface uses *CFG_ACK_COUNT* as interval value	RW	0
9	**CFG_TO_FMODE** PCI Express interface Timeout Detection mode for the Replay Timer. 0 = PCI Express interface uses own timer value 1 = PCI Express interface uses *CFG_TO_COUNT* as timer value	RW	1
10	**CFG_PORT_DISABLE** 1 = Serializer/De-Serializer (SerDes) in the PCI Express interface is disabled. This allows the endpoint to disable the PCI Express connection when powered up or before configuration is complete.	RW	0
11	**CFG_RCV_DETECT** Set when the PCI Express interface establishes the PCI Express connection.	RO	0
12	**CFG_LPB_MODE** Link Loop-Back mode. 1 = PEX 8112 changes its LTSSM state to the Loop-Back state, becomes the Loop-Back Master, and starts transmitting packets of pseudo-random numbers	RW	0
13	**CFG_PORT_MODE** 0 = Link PCI Express interface is configured as an upstream port (Endpoint) 1 = Link PCI Express interface is configured as a downstream port (Root Complex)	RW	0
14	***Reserved***	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE** The PEX 8112 does ***not support*** End-to-end Cyclic Redundancy Check (ECRC); therefore, this bit is cleared to 0.	RW	0

Register 15-81. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0 *(Cont.)*

Bit(s)	Description	Access	Default
16	**TLP_CPLD_NOSUCCESS_MALFORM_ENABLE** 0 = Received Completion is retained 1 = Completion received when Completion timeout expired is treated as a malformed TLP and discarded	RW	1
17	**Scrambler Disable** 0 = Data scrambling is enabled. 1 = Data scrambling is disabled. Set only when testing and debugging.	RW	0
18	**Delay Link Training** 0 = Link training is allowed to commence immediately after PERST# is de-asserted 1 = Link training is delayed for 12 ms after PERST# is de-asserted	RW	1
19	**Decode Primary Bus Number** 0 = PEX 8112 ignores the Primary Bus Number in a PCI Express Type 0 Configuration Request. 1 = PEX 8112 compares the Primary Bus Number in a PCI Express Type 0 Configuration Request with the **Primary Bus Number** register. When they match, the request is accepted. Otherwise, an Unsupported Request is returned. This comparison occurs only after the first Type 0 Configuration Write occurs.	RW	0
20	**Ignore Function Number** 0 = PEX 8112 only responds to Function Number 0 during a Type 0 Configuration transaction. Accesses to other Function Numbers result in an Unsupported Request (PCI Express) or Master Abort (PCI). 1 = PEX 8112 ignores the Function Number in a PCI or PCI Express Type 0 Configuration Request, and responds to all eight functions.	RW	0
21	**Check RCB Boundary** 0 = PEX 8112 ignores Read Completion Boundary (RCB) violations. 1 = PEX 8112 checks for RCB violations. When detected, the PEX 8112 treats an RCB violation as a malformed TLP (packet is dropped and a Fatal Error message is transmitted).	RW	0
22	**Limit Completion Flow Control Credit** Must be set when the **PCI Control** register *Programmed Prefetch Size* field is set to 4 KB. When GPIO2 is Low at the trailing edge of PERST#, this bit is automatically set. Because this bit is used during link training, it must be set by driving GPIO2 Low during PERST# assertion. 0 = PEX 8112 advertises infinite Flow Control credits for Completions 1 = PEX 8112 advertises Completion Flow Control credits, based upon available buffer storage	RW	0
23	**L2 Secondary Bus Reset** Does not apply to Forward Bridge mode.	RW	1
31:24	***Reserved***	RsvdP	0h

Register 15-82. (Offset 104Ch; TLPCFG1) TLP Controller Configuration 1

Bit(s)	Description	Access	Default
20:0	**CFG_TO_COUNT** PCI Express interface Replay Timer timeout value when *CFG_TO_FMODE* is set to 1.	RW	D4h
30:21	**CFG_ACK_COUNT** PCI Express interface ACK_DLLP transmitting interval value when *CFG_ACK_FMODE* is set to 1.	RW	0h
31	***Reserved***	RsvdP	0

Register 15-83. (Offset 1050h; TLPCFG2) TLP Controller Configuration 2

Bit(s)	Description		Access	Default
2:0	**Function Number**	**CFG_COMPLETER_ID0** The Bus Number, Device Number, and Function Number of a Configuration transaction to the PEX 8112 are latched in this register. The latched values are then used when generating the Completion.	RW	0h
7:3	**Device Number**			
15:8	**Bus Number**			
26:16	**Update Credit FC** Controls a Counter that determines the gap between UpdateFC DLLPs (in units of 62.5 MHz clocks = 16 ns = 4 symbol times). When Data or Headers are read from the TLP Controller, the Credit Allocation Manager transmits a set of UpdateFC DLLPs; Posted, Non-Posted, and Completion when the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. While transmitting the set of DLLPs, the Credit Allocation Manager uses the Counter value to insert gaps between the DLLPs. The Bus Number, Device Number, and Function Number of a Configuration transaction to the PEX 8112 are latched in this register. The latched values are then used when generating the Completion.		RW	1h
31:27	***Reserved***		RsvdP	0h

Register 15-84. (Offset 1054h; TLPTAG) TLP Controller Tag

Bit(s)	Description	Access	Default
7:0	**TAG BME1** Message Request *Tag* field.	RW	0h
15:8	**TAG ERM** Error Manager *Tag* field.	RW	0h
23:16	**TAG PME** Power Manager *Tag* field.	RW	0h
31:24	***Reserved***	RsvdP	0h

Register 15-85. (Offset 1058h; TLPTIMELIMIT0) TLP Controller Time Limit 0

Bit(s)	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT** Bus Master engine Completion timeout (in PCI Clock units). The default value produces a 10-ms timeout.	RW	51615h (M66EN Low) A2C2Ah (M66EN High)
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT** Determines length of time before power is removed after entering the L2/L3 Ready Link PM state. Value must be at least 100 ns. Contains PCI clock units.	RW	4h (M66EN Low) 8h (M66EN High)
31:28	***Reserved***	RsvdP	0h

Register 15-86. (Offset 105Ch; TLPTIMELIMIT1) TLP Controller Time Limit 1

Bit(s)	Description	Access	Default
10:0	**ASPM_LI_DLLP_INTERVAL_TIME_LIMIT** Determines time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions. The default is 10 µs for both 14Dh and 29Ah. Allow at least 10 µs spent in the LTSSM L0 and L0s Link PM states before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP is transmitted. Refer to the *PCI Express r1.0a Errata*, page 19, for further details. Contains PCI clock units.	RW	14Dh (M66EN Low) 29Ah (M66EN High)
31:11	***Reserved***	RsvdP	0h

Register 15-87. (Offset 1060h; CRSTIMER) CRS Timer

Bit(s)	Description	Access	Default
15:0	**CRS Timer** Valid only when the **PCI Express Device Control** register *Bridge Configuration Retry Enable* bit is set. Determines the number of microseconds to wait before returning a Completion with CRS status in response to a PCI Express-to-PCI Configuration transaction. When the timer times out and the Completion with CRS status is returned, the transaction is discarded from the Non-Posted Transaction queue.	RW	25d
31:16	***Reserved***	RsvdP	0h

Register 15-88. (Offset 1064h; ECFGADDR) Enhanced Configuration Address

Bit(s)	Description	Access	Default
11:0	***Reserved***	RsvdP	0h
14:12	**Configuration Function Number** Provides the Function Number for an enhanced Configuration transaction.	RW	000b
19:15	**Configuration Device Number** Provides the Device Number for an enhanced Configuration transaction.	RW	0h
27:20	**Configuration Bus Number** Provides the Bus Number for an enhanced Configuration transaction.	RW	0h
30:28	***Reserved***	RsvdP	000b
31	**Enhanced Configuration Enable** Does not apply to Forward Bridge mode.	RW	0

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Chapter 16 Reverse Bridge Mode Configuration Registers

16.1 Register Description

This chapter describes the PEX 8112 Configuration registers specific to Reverse Bridge mode. Registers specific to Forward Bridge mode are discussed in Chapter 15.

The PCI-Compatible Reverse Bridge mode Configuration registers are accessed by the PCI Host, using the PCI Configuration Address space. All Configuration registers are accessed from the PCI Express interface or PCI Bus, using the 64-KB memory space defined by the **PCI Base Address 0** register. Registers that are written by the Serial EEPROM Controller are also written using Memory Writes through the **PCI Base Address 0** register.

In Reverse Bridge mode, a PCI Master cannot access the PCI Express Extended Capability registers by way of PCI Configuration transactions.

When the Configuration registers are accessed using Memory transactions to the **PCI Base Address 0** register, the address mapping defined in Table 16-1 is used.

The Serial EEPROM Controller writes to Configuration registers. An upper Address bit is used to select one of two register spaces, as defined in Table 16-2.

Each register is 32 bits wide, and is accessed one byte, word, or DWORD at a time. These registers use Little Endian byte ordering, which is consistent with the *PCI r3.0*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8112 is powered up or reset, the registers are set to their default values. Writes to unused registers are ignored. Reads from unused registers return a value of 0.

Table 16-1. Reverse Bridge Mode PCI Base Address 0 Register Map

Address Offset	Register Space
0000h – 0FFFh	PCI-Compatible Configuration registers
1000h – 1FFFh	Main Configuration registers
2000h – 2FFFh	Memory-Mapped indirect access to downstream PCI Express Endpoint registers
8000h – 9FFFh	8-KB internal shared memory

Table 16-2. Selecting Register Space

AD12	Register Space
0	PCI-Compatible Configuration registers
1	Main Configuration registers

16.1.1 Indexed Addressing

In addition to Memory-Mapped accesses, the PEX 8112 **Main Configuration** registers can be accessed using the **Main Control Register Index** and **Main Control Register Data** registers. This method allows all Main Configuration registers to be accessed using Configuration transactions, rather than Memory transactions. First, the **Main Configuration** register offset is written to the **Main Control Register Index** register (offset 84h). Then, the **Main Configuration** register is written or read by accessing the **Main Control Register Data** register (offset 88h).

The **Main Control Register Index** and **Main Control Register Data** registers are used only to access the **Main Control** registers, because there is a built-in offset of 1000h. *For example*, if the **Main Control Register Index** register is set to 20h, the **Main Control Register Data** register stores the contents of the **General-Purpose I/O Control** register during a Memory Read.

16.2 Configuration Access Types

Table 16-3 defines configuration access types referenced by the registers in this chapter.

Table 16-3. Configuration Access Types

Access Type	Description
CFG	Initiated by PCI Configuration transactions on the primary bus.
MM	Initiated by PCI Memory transactions on the primary or secondary bus, using the Address range defined by the **PCI Base Address 0** register.
EE	Initiated by the Serial EEPROM Controller during initialization.

16.3 Register Attributes

Table 16-4 defines the register attributes used to indicate access types provided by each register bit.

Table 16-4. Access Provided by Register Bits

Register Attribute	Description
HwInit	**Hardware-Initialized** Register bits are initialized by firmware or hardware mechanisms *such a*s ball strapping (on the BAR0ENB#, EXTARB, and FORWARD balls) or serial EEPROM. Bits are Read-Only after initialization and reset only with “Fundamental Reset.”
RO	**Read-Only Register** Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8112 Hardware-Initialization mechanism or PEX 8112 Serial EEPROM register Initialization feature.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve the value read, for writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write Register** Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	**Read-Only Status, Write 1 to Clear Status Register** Register bits indicate status when read; a set bit that is indicating a status event, is cleared by writing 1. Writing 0 to RW1C bits has no effect.
WO	**Write-Only** Used to indicate that a register is written by the Serial EEPROM Controller.

16.4 Register Summary

Table 16-5 lists the register configuration and map for Reverse Bridge mode.

Table 16-5. Reverse Bridge Mode Register Configuration and Map

Register Group	PCI Space	Offset Address Range
PCI-Compatible Configuration Registers (Type 1)	PCI Configuration	00h – 3Ch
	Memory-Mapped, **BAR0**	
PCI-Compatible Extended Capability Registers for PCI Express Interface	PCI Configuration	40h – FFh
	Memory-Mapped, **BAR0**	
PCI Express Extended Capability Registers	Memory-Mapped, **BAR0**	100h – FFFh
Main Control Registers	Memory-Mapped, **BAR0**	1000h – 1FFFh
PCI Express Configuration Registers Using Enhanced Configuration Access	Memory-Mapped, **BAR0**	2000h – 2FFFh
8-KB Shared Memory instead of General Purpose Memory	Memory-Mapped, **BAR0**	8000h – 9FFFh

16.5 PCI-Compatible Configuration Registers (Type 1)

This section details the PEX 8112 Reverse Bridge mode PCI-Compatible Configuration (Type 1) registers. Table 16-6 defines the register map.

Table 16-6. Reverse Bridge Mode PCI-Compatible Configuration (Type 1) Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
00h	PCI Device ID		PCI Vendor ID	
04h	PCI Status		PCI Command	
08h	PCI Class Code			PCI Device Revision ID
0Ch	PCI Built-In Self-Test ***(Not Supported)***	PCI Header Type	PCI Bus Latency Timer	PCI Cache Line Size
10h	PCI Base Address 0			
14h	PCI Base Address 1			
18h	***Reserved***	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Memory Base Upper 32 Bits			
2Ch	Prefetchable Memory Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	***Reserved***			PCI Capability Pointer
38h	PCI Base Address for Expansion ROM ***(Not Supported)***			
3Ch	Bridge Control		PCI Interrupt Pin	PCI Interrupt Line

Register 16-1. (Offset 00h; PCIVENDID) PCI Vendor ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID** Identifies the device manufacturer. The PEX 8112 returns the PLX PCI-SIG-assigned Vendor ID, 10B5h.	RO	RW	WO	10B5h

Register 16-2. (Offset 02h; PCIDEVID) PCI Device ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Device ID** Identifies the particular device, as specified by the vendor. The PEX 8112 returns the PLX-assigned Device ID, 8112h.	RO	RW	WO	8112h

Register 16-3. (Offset 04h; PCICMD) PCI Command

Bit(s)	Description	CFG	MM	EE	Default
0	**I/O Access Enable** Enables the PEX 8112 to respond to I/O Space accesses on the primary bus (PCI). These accesses are directed to a Target on the PCI Express interface, because the PEX 8112 does not have internal I/O-Mapped devices. 0 = PCI I/O accesses to the PEX 8112 result in a Master Abort	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8112 to respond to Memory Space accesses on the primary bus (PCI). These accesses are directed to a Target on the PCI Express interface, or to internal Memory-Mapped registers. 0 = PCI Memory accesses to the PEX 8112 result in a Master Abort	RW	RW	WO	0
2	**Bus Master Enable** 0 = PEX 8112 must disable response as a Target to all Memory or I/O transactions on the secondary bus (PCI Express) [they cannot be forwarded to the primary bus (PCI)]. In this case, all Memory and I/O requests are terminated with an Unsupported Request Completion. 1 = Enables the PEX 8112 to perform Memory or I/O transactions on the primary bus (PCI). Configuration transactions are forwarded from the secondary bus (PCI Express) and performed on the primary bus, independent of this bit.	RW	RW	WO	0
3	**Special Cycle Enable** Bridges do not respond to special cycle transactions; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** 0 = Enables the PEX 8112 PCI Master logic to use the Memory Write command 1 = Enables the PEX 8112 PCI Master logic to use the Memory Write and Invalidate command	RW	RW	WO	0
5	**VGA Palette Snoop** 1 = I/O writes in the first 64 KB of the I/O Address space with Address bits [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA aliases – AD[15:10] are not decoded and are of any value) must be positively decoded on the PCI Bus and forwarded to the secondary bus (PCI Express)	RW	RW	WO	0
6	**Parity Error Response Enable** Controls the PEX 8112's response to Data Parity errors on the PCI Bus. 0 = PEX 8112 ignores PCI Data Parity errors 1 = PEX 8112 takes standard action when a PCI Data Parity error occurs (refer to Section 10.2.1.2, "PCI Uncorrectable Data Errors" and Section 10.2.2.1, "Received PCI Errors")	RW	RW	WO	0
7	***Reserved***	RsvdP	RsvdP	–	0

Register 16-3. (Offset 04h; PCICMD) PCI Command *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
8	**SERR# Enable** 1 = Enables the SERR# signal to assert	RW	RW	WO	0
9	**Fast Back-to-Back Enable** The PEX 8112 PCI Master does not perform Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** 1 = PEX 8112 is prevented from asserting INT*x*# signals on behalf of functions integrated into the PEX 8112 There is no effect on INT*x*# signals asserted on behalf of INT*x*# messages associated with the secondary bus (PCI Express).	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-4. (Offset 06h; PCISTAT) PCI Status

Bit(s)	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** Reflects the PEX 8112 internal PCI interrupt status state. One of the INT*x*# signals is asserted when this bit is High, the **PCI Command** register *Interrupt Disable* bit is Low, and the Device PM state is D0.	RO	RO	–	0
4	**Capabilities List** Indicates when the **PCI Capability Pointer** at offset 34h is valid.	RO	RW	WO	1
5	**66 MHz Capable** Indicates whether the PEX 8112 is capable of running at 66 MHz. 0 = Indicates 33 MHz 1 = Indicates PEX 8112 is 66-MHz capable	RO	RW	WO	1
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** The PEX 8112 does not accept Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** 1 = Indicates that a data parity error occurred when this device was the PCI Master. The **PCI Command** register *Parity Error Response Enable* bit must be set for this bit to be set. Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Determines how quickly this device responds to a transaction with DEVSEL#. 01b = Indicates a medium response	RO	RO	–	01b
11	**Signaled Target Abort** Reports Target Abort termination signaling by the PEX 8112 when the bridge responds as the transaction Target on its primary bus. This does not occur on the PEX 8112; therefore, this bit always returns 0.	RsvdZ	RsvdZ	–	0
12	**Received Target Abort** Reports Target Abort termination detection by the PEX 8112 when the bridge is the transaction Master on its primary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Reports Master Abort termination detection by the PEX 8112 when the bridge is the transaction Master on its primary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the PEX 8112 asserts the SERR# signal. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set when the PEX 8112 detects a Parity error on incoming addresses or data from the PCI Bus, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 16-5. (Offset 08h; PCIDEVREV) PCI Device Revision ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Device Revision ID** Identifies the PEX 8112 Silicon Revision. Bits [3:0] represent the minor Revision Number and bits [7:4] represent the major Revision Number.	RO	RO	–	AAh

Register 16-6. (Offset 09h; PCICLASS) PCI Class Code

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Programming Interface**	RO	RW	WO	00h
15:8	**Sub-Class Code**	RO	RW	WO	04h
23:16	**Base Class Code**	RO	RW	WO	06h

Register 16-7. (Offset 0Ch; PCICACHESIZE) PCI Cache Line Size

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size** Specifies the System Cache Line Size (in units of DWORDs). The value in this register is used by PCI Master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands for accessing memory. 0h = 0 DWords 2h = 2 DWords 4h = 4 DWords 8h = 8 DWords 10h = 16 DWords 20h = 32 DWords Writes of values other than these result in a Cache Line Size of 0; however, the value written is returned when this register is read.	RW	RW	WO	0h

Register 16-8. (Offset 0Dh; PCILATENCY) PCI Bus Latency Timer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Bus Latency Timer** Also referred to as *Primary Latency Timer* for Type 1 Configuration Space Header devices. Specifies (in PCI Clock units) the value of the Latency Timer during PCI Master bursts. When the Latency Timer expires, the PEX 8112 must terminate its tenure on the bus.	RW	RW	WO	0h

Register 16-9. (Offset 0Eh; PCIHEADER) PCI Header Type

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Header Type** Specifies the format of the second part of the pre-defined Configuration Header, starting at offset 10h. For PCI bridges, this field is forced to 1h.	RO	RO	–	1h

Register 16-10. (Offset 0Fh; PCIBIST) PCI Built-In Self-Test

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self-Test** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h

Register 16-11. (Offset 10h; PCIBASE0) PCI Base Address 0 (BAR0)

Bit(s)	Description	CFG	MM	EE	Default
0	**Space Type** When Low, this space is accessed as memory. When High, this space is accessed as I/O. ***Note:*** *Hardwired to 0.*	RO	RO	–	0
2:1	**Address Type** Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = ***Reserved***	RO	RW	WO	10b
3	**Prefetch Enable** 1 = Indicates that prefetching has no side effects on Reads	RO	RW	WO	1
15:4	**Base Address** This section of the Base address is ignored for a 64-KB space. ***Note:*** *Hardwired to 0.*	RO	RO	–	0h
31:16	**Base Address** Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the PEX 8112 Configuration registers and shared memory.	RW	RW	WO	0h

Register 16-12. (Offset 14h; PCIBASE1) PCI Base Address 1 (BAR1)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Base Address 1** Determines the upper 32 bits of the address when **PCI Base Address 0** is configured for 64-bit addressing.	RW	RW	WO	0h

Register 16-13. (Offset 18h; PRIMBUSNUM) Primary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the PEX 8112's primary bus is connected.	RW	RW	WO	0h

Register 16-14. (Offset 19h; SECBUSNUM) Secondary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number** Used to record the Bus Number of the PCI Bus segment to which the PEX 8112's secondary bus is connected.	RW	RW	WO	0h

Register 16-15. (Offset 1Ah; SUBBUSNUM) Subordinate Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number** Used to record the Bus Number of the highest-numbered PCI Bus segment behind (or subordinate to) the PEX 8112.	RW	RW	WO	0h

Register 16-16. (Offset 1Ch; IOBASE) I/O Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are ***reserved***.	RO	RW	WO	0000b
7:4	**I/O Base** Determines the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the PEX 8112 assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are 000h. Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB Address Boundary space, and the top is one less than a 4-KB Address Boundary space.	RW	RW	WO	0h

Register 16-17. (Offset 1Dh; IOLIMIT) I/O Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other encodings are ***reserved***. The value returned in this field is derived from the **I/O Base** register *I/O Base Address Capability* field.	RO	RO	–	0000b
7:4	**I/O Limit** Determines the I/O Space range forwarded from the primary bus to the secondary bus. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the PEX 8112 assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary side of the PEX 8112, the *I/O Limit* field is programmed to a value smaller than the **I/O Base** register *I/O Base* field. In this case, the PEX 8112 does not forward I/O transactions from the primary bus to the secondary bus; however, the PEX 8112 does forward all I/O transactions from the secondary bus to the primary bus.	RW	RW	WO	0h

Register 16-18. (Offset 1Eh; SECSTAT) Secondary Status

Bit(s)	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable** Not valid for PCI Express. Indicates whether the PEX 8112 secondary bus is capable of operating at 66 MHz. Forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Not valid for PCI Express. Indicates whether the PEX 8112's secondary bus is capable of decoding Fast Back-to-Back transactions when the transactions are from the same Master, but to different Targets. Forced to 0.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Used to report Data Parity error detection by the PEX 8112. Set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a Completion marked poisoned on the secondary bus • Bridge poisons a Write Request or Read Completion on the secondary bus Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Not valid for PCI Express. Encodes the secondary bus DEVSEL# timing. Forced to 00b.	RO	RO	–	00b
11	**Secondary Signaled Target Abort** Set when the PEX 8112 completes a request as a transaction Target on its secondary bus, using Completer Abort Completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Set when the PEX 8112 receives a Completion with Completer Abort Completion status on its secondary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Set when the PEX 8112 receives a Completion with Unsupported Request Completion status on its secondary bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Set when the PEX 8112 receives an ERR_FATAL or ERR_NONFATAL message from the downstream PCI Express device. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Set by the PEX 8112 when it receives a poisoned Transaction Layer Packet (TLP) on the secondary bus, regardless of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 16-19. (Offset 20h; MEMBASE) Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Base** Determines the starting address at which Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are 0_0000h. The bottom of the defined Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.	RW	RW	WO	–

Register 16-20. (Offset 22h; MEMLIMIT) Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Limit** Determines the Memory Space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are F_FFFFh. When there are no Memory-Mapped I/O addresses on the secondary side of the PEX 8112, the *Memory Limit* field must be programmed to a value smaller than the **Memory Base** register *Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the PEX 8112, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 16-21. (Offset 24h; PREBASE) Prefetchable Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other encodings are ***reserved***.	RO	RW	WO	0000b
15:4	**Prefetchable Memory Base** Determines the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are 0_0000h. The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space.	RW	RW	WO	–

Register 16-22. (Offset 26h; PRELIMIT) Prefetchable Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other encodings are ***reserved***. The value returned in this field is derived from the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field.	RO	RO	–	0000b
15:4	**Prefetchable Memory Limit** Determines the Prefetchable Memory space range forwarded from the primary bus to the secondary bus. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the PEX 8112 assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are F_FFFFh. When there is no Prefetchable memory on the secondary side of the PEX 8112, the *Prefetchable Memory Limit* field must be programmed to a value smaller than the **Prefetchable Memory Base** register *Prefetchable Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary side of the PEX 8112, the bridge does not forward Memory transactions from the primary bus to the secondary bus; however, it does forward all Memory transactions from the secondary bus to the primary bus.	RW	RW	WO	–

Register 16-23. (Offset 28h; PREBASEUPPER) Prefetchable Memory Base Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits** When the **Prefetchable Memory Base** register *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary bus are forwarded to the secondary bus.	RW	RW	WO	0h

Register 16-24. (Offset 2Ch; PRELIMITUPPER) Prefetchable Memory Limit Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits** When the **Prefetchable Memory Limit** register *Prefetchable Limit Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Limit Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the Prefetchable Memory range forwarded from the primary bus to the secondary bus.	RW	RW	WO	0h

Register 16-25. (Offset 30h; IOBASEUPPER) I/O Base Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits** When the **I/O Base** register *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary bus are forwarded to the secondary bus.	RW	RW	WO	–

Register 16-26. (Offset 32h; IOLIMITUPPER) I/O Limit Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits** When the **I/O Limit** register *I/O Limit Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0h. When the *I/O Limit Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the I/O range forwarded from the primary bus to the secondary bus.	RW	RW	WO	–

Register 16-27. (Offset 34h; PCICAPPTR) PCI Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Capability Pointer** Provides the offset location of the first New Capabilities register (offset 40h, **Power Management Capability** structure).	RO	RW	WO	40h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-28. (Offset 3Ch; PCIINTLINE) PCI Interrupt Line

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Line** Indicates to which System Interrupt Controller input the PEX 8112 Interrupt ball is connected. Device drivers and operating systems use this field.	RW	RW	WO	0h

Register 16-29. (Offset 3Dh; PCIINTPIN) PCI Interrupt Pin

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Interrupt Pin** Selects the Interrupt ball to be used by the PEX 8112. 1h = INTA#	RO	RW	WO	1h

Register 16-30. (Offset 3Eh; BRIDGECTL) Bridge Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the PEX 8112's response to Data Parity errors forwarded from the primary bus (*such as*, a poisoned TLP). 0 = PEX 8112 must ignore Data Parity errors detected and continue standard operation 1 = PEX 8112 must take its standard action when a Data Parity error is detected (refer to Section 10.2.1.1, "Received Poisoned TLP" and Section 10.2.2.1, "Received PCI Errors")	RW	RW	WO	0
1	**Secondary SERR# Enable** No effect in Reverse Bridge mode. Secondary bus error reporting using SERR# is controlled by the **Root Control** register.	RW	RW	WO	0
2	**ISA Enable** Modifies the PEX 8112's response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. 1 = PEX 8112 blocks forwarding from the primary bus to the secondary bus, of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the PEX 8112's response to VGA-compatible addresses. When set to 1, the PEX 8112 positively decodes and forwards the following accesses on the primary bus to the secondary bus (and, conversely, blocks the forwarding of these addresses from the secondary bus to the primary bus): • Memory accesses within the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is within the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When set to 1, VGA address forwarding is independent of the: • Bit 2 (*ISA Enable)* setting • Memory and I/O Address ranges defined by the **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers VGA address forwarding is qualified by the **PCI Command** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Does not forward VGA-compatible Memory and I/O addresses from the primary bus to the secondary bus (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forwards VGA-compatible Memory and I/O addresses (addresses defined above) from the primary bus to the secondary bus (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 16-30. (Offset 3Eh; BRIDGECTL) Bridge Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the PEX 8112 to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable*) is also set to 1, enabling VGA I/O decoding and forwarding by the PEX 8112. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary bus to the secondary bus, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls the PEX 8112's behavior when it receives a Master Abort termination on the PCI Bus or an Unsupported Request on the PCI Express interface. 0 = Do not report Master Aborts • When a PCI Express UR is received: – Return FFFF_FFFFh to the PCI Bus for Reads – Complete Non-Posted Write normally on the PCI Bus (assert TRDY#) and discard the Write data – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI 1 = Report Master Aborts • When a PCI Express UR is received: – Complete Reads and Non-Posted Writes with a PCI Target Abort – Discard Posted PCI-to-PCI Express Write data • When a PCI transaction terminates with a Master Abort: – Complete Non-Posted transaction with an Unsupported Request – Discard Posted Write data from PCI Express-to-PCI – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**Secondary Bus Reset** 1 = Causes a Hot Reset to be communicated on the secondary bus. Additionally, the PEX 8112 secondary bus, and buffers between the two buses (primary and secondary), must be initialized to their default state. The primary bus and Configuration Space registers are not affected by setting this bit.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported*** Controls the PEX 8112's ability to generate Fast Back-to-Back transactions to different devices on the secondary bus.	RO	RO	–	0

Register 16-30. (Offset 3Eh; BRIDGECTL) Bridge Control *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>CFG</th><th>MM</th><th>EE</th><th>Default</th></tr>
<tr><td>8</td><td>Primary Discard Timer
Selects the number of PCI clocks that the PEX 8112 waits for a Master on the primary bus, to repeat a Delayed Transaction request. The Counter starts after the Completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the PEX 8112 downstream queue (that is, all ordering requirements are satisfied and the PEX 8112 is ready to complete the Delayed Transaction with the originating Master on the primary bus).
When the originating Master does not repeat the transaction before the Counter expires, the PEX 8112 flushes the Delayed Transaction from its queue and sets bit 10 (Discard Timer Status). Usually, this bit selects either 2^{15} or 2^{10} PCI clocks. When using the PEX 8112 Blind Prefetch feature, these long discard delays could result in significant performance degradation. The PEX 8112 includes an additional Control bit (PCI Control register Short Discard Timer Timeout Select bit) that can provide a short timeout of 2^6 clocks.
<table>
<tr><th>PCI Control Register Short Discard Timer Timeout Select Bit (Bit 30) Value</th><th>Primary Discard Timer Bit Value</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Transaction data is flushed in 2^{15} PCI clock periods</td></tr>
<tr><td>0</td><td>1</td><td>Transaction data is flushed in 2^{10} PCI clock periods</td></tr>
<tr><td>1</td><td>X</td><td>Transaction data is flushed in 2^6 PCI clock periods</td></tr>
</table>
Note: “X” is “Don’t Care.”</td><td>RW</td><td>RW</td><td>WO</td><td>0</td></tr>
<tr><td>9</td><td>Secondary Discard Timer
In Reverse Bridge mode, this bit does not apply and is forced to 0.</td><td>RO</td><td>RO</td><td>–</td><td>0</td></tr>
<tr><td>10</td><td>Discard Timer Status
Set to 1 when the Primary Discard Timer expires and a Delayed Completion is discarded from a queue within the PEX 8112.</td><td>RW1C</td><td>RW1C</td><td>–</td><td>0</td></tr>
<tr><td>11</td><td>Discard Timer SERR# Enable
When set to 1, enables the PEX 8112 to assert SERR# on the primary bus when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the PEX 8112.
0 = Does not assert SERR# on the primary bus as a result of the Primary Discard Timer expiration
1 = Generates SERR# on the primary bus when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the PEX 8112</td><td>RW</td><td>RW</td><td>WO</td><td>0</td></tr>
<tr><td>15:12</td><td>Reserved</td><td>RsvdP</td><td>RsvdP</td><td>–</td><td>0h</td></tr>
</table>

16.6 PCI-Compatible Extended Capability Registers for PCI Express Interface

This section details the PEX 8112 Reverse Bridge mode PCI-Compatible Extended Capability registers for the PCI Express interface. Table 16-7 defines the register map.

Table 16-7. Reverse Bridge Mode PCI-Compatible Extended Capability for PCI Express Interface Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
40h	Power Management Capability		Power Management Next Capability Pointer	Power Management Capability ID
44h	Power Management Data	Power Management Bridge Support	Power Management Control/Status	
48h	Device-Specific Control			
4Ch	***Reserved***			
50h	MSI Control		MSI Next Capability Pointer	MSI Capability ID
54h	MSI Address			
58h	MSI Upper Address			
5Ch	***Reserved***		MSI Data	
60h	PCI Express Capability		PCI Express Next Capability Pointer	PCI Express Capability ID
64h	Device Capability			
68h	PCI Express Device Status		PCI Express Device Control	
6Ch	Link Capability			
70h	Link Status		***Reserved***	Link Control
74h	Slot Capability			
78h	Slot Status		Slot Control	
7Ch	***Reserved***		Root Control	
80h	Root Status			
84h	Main Control Register Index			
88h	Main Control Register Data			
8Ch – FFh	***Reserved***			

Register 16-31. (Offset 40h; PWRMNGID) Power Management Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID** Specifies the Power Management Capability ID.	RO	RO	–	01h

Register 16-32. (Offset 41h; PWRMNGNEXT) Power Management Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, (offset 50h, **MSI Capability** structure).	RO	RW	WO	50h

Register 16-33. (Offset 42h; PWRMNGCAP) Power Management Capability

Bit(s)	Description	CFG	MM	EE	Default
2:0	**PM Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1*.	RO	RW	WO	010b
3	**PME Clock** Power Management Event (PME) clock. When Low, indicates that no PCI clock is required to generate PMEOUT#. When High, indicates that a PCI clock is required to generate PMEOUT#.	RO	RW	WO	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the PEX 8112 requires special initialization following a transition to the D0_uninitialized Device PM state, before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PMEOUT# generation from the D3cold Device PM state is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Indicates whether the PEX 8112 supports the D1 Device PM state.	RO	RW	WO	1
10	**D2 Support** Indicates whether the PEX 8112 supports the D2 Device PM state.	RO	RW	WO	0
15:11	**PME Support** Default 0101_1b indicates that the corresponding PEX 8112 port forwards PME messages in the D0, D3hot, and D3cold Device PM states. XXXX_1b = Assertable from D0 XXX1_Xb = Assertable from D1 XX1X_Xb = Assertable from D2 X1XX_Xb = Assertable from D3hot 1XXX_Xb = Assertable from D3cold	RO	RW	WO	0101_1b

Register 16-34. (Offset 44h; PWRMNGCSR) Power Management Control/Status

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine the current Device PM state of the port, and to set the port into a new Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3hot In the D1 and D2 Device PM states, when the corresponding *D1 Support* and *D2 Support* bits are set, PCI Memory and I/O accesses are disabled, as well as the PCI interrupt; however, Configuration Requests are allowed. In the D3hot Device PM state, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables the PMEOUT# signal to assert.	RW	RW	WO	0
12:9	**Data Select** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** When bit 8 (*PME Enable*) is set High, indicates that PMEOUT# is being driven. Writing 1 from the PCI Bus clears this bit.	RW1C	RW1C	–	0

Register 16-35. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support

Bit(s)	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** 0 = Indicates that, when the PEX 8112 function is programmed to the D3hot Device PM state, power is removed (B3) from its secondary bus. Useful only when bit 7 (*Bus Power/Clock Control Enable*) is set. 1 = Indicates that, when the PEX 8112 function is programmed to the D3hot Device PM state, its secondary bus PCI clock is stopped (B2).	RO	RW	WO	0
7	**Bus Power/Clock Control Enable** 1 = Indicates that the bus power/clock control mechanism (as defined in the *PCI-to-PCI Bridge r1.1*, Section 4.7.1) is enabled	RO	RW	WO	0

Register 16-36. (Offset 47h; PWRMNGDATA) Power Management Data

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Data** ***Not supported*** Always returns a value of 0h.	RO	RO	–	0h

Register 16-37. (Offset 48h; DEVSPECCTL) Device-Specific Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable** 0 = Memory Read command on the PCI Bus that targets the PCI Express Memory space causes only 1 word to be read from the PCI Express interface. 1 = Memory Read command on the PCI Bus that targets the PCI Express Memory space causes at least one Cache Line to be read from the PCI Express interface. Additional Dwords can be read by setting the **PCI Control** register *Programmed Prefetch Size* field.	RW	RW	WO	0
1	**PCI Base Address 0 Enable** 1 = Enables the **PCI Base Address 0** space for Memory-Mapped access to the Configuration registers and shared memory. **PCI Base Address 0** is also enabled when the BAR0ENB# ball is Low.	RW	RW	WO	0
2	**L2 Enable** 0 = Power state change to the D3 Device PM state does not cause the PEX 8112 to change the Link PM state to L2 1 = Power state change to the D3 Device PM state causes the PEX 8112 to change the Link PM state to L2	RW	RW	WO	0
3	**PM Power Off** 1 = Link transitioned to the L2/L3 Ready Link PM state, and is ready to power down	RO	RO	–	0
7:4	**PM Link State** Indicates the Link PM state. 0001b = L0 0010b = L0s 0100b = L1 1000b = L2 All other encodings are ***reserved***.	RO	RO	–	–

Register 16-37. (Offset 48h; DEVSPECCTL) Device-Specific Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
9:8	**CRS Retry Control** Determines the PEX 8112 response when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry status. 00b = Retry once after 1s. When another CRS is received, Target Abort on the PCI Bus. 01b = Retry eight times, once per second. When another CRS is received, Target Abort on the PCI Bus. 10b = Retry once per second, until successful completion. 11b = ***Reserved***	RW	RW	WO	00b
10	**WAKE Out Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
11	**Beacon Generate Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
12	**Beacon Detect Enable** 1 = Beacon detected while the link is in the L2 Link PM state causes the **Power Management Control/Status** register *PME Status* bit to be set	RW	RW	WO	0
13	**PLL Locked** High when the internal Phase-Locked Loop (PLL) is locked.	RO	RO	–	–
15:14	***Reserved***	RsvdP	RsvdP	–	00b
20:16	**Link Training and Status State Machine** ***Factory Test Only***	RO	RO	–	–
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-38. (Offset 50h; MSIID) MSI Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID** Specifies the Message Signaled Interrupt (MSI) Capability ID.	RO	RO	–	5h

Register 16-39. (Offset 51h; MSINEXT) MSI Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List (offset 60h, **PCI Express Capability** structure).	RO	RW	WO	60h

Register 16-40. (Offset 52h; MSICTL) MSI Control

Bit(s)	Description	CFG	MM	EE	Default
0	**MSI Enable** 1 = Enables the PEX 8112 to use MSI to request service. INT*x*# outputs are disabled.	RW	RW	WO	0
3:1	**Multiple Message Capable** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four). 000b = 1 message requested 001b = 2 messages requested 010b = 4 messages requested 011b = 8 messages requested 100b = 16 messages requested 101b = 32 messages requested 110b, 111b = ***Reserved***	RO	RO	–	000b
6:4	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. 000b = 1 message allocated 001b = 2 messages allocated 010b = 4 messages allocated 011b = 8 messages allocated 100b = 16 messages allocated 101b = 32 messages allocated 110b, 111b = ***Reserved***	RW	RW	WO	000b
7	**MSI 64-Bit Address Capable** 1 = PEX 8112 is capable of generating a 64-bit Message address	RO	RW	WO	0
8	**Per Vector Masking Capable** ***Not supported*** Forced to 0.	RO	RO	–	0
15:9	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-41. (Offset 54h; MSIADDR) MSI Address

Bit(s)	Description	CFG	MM	EE	Default
1:0	***Reserved***	RsvdP	RsvdP	–	00b
31:2	**MSI Address** When the **MSI Control** register *MSI Enable* bit is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits [1:0] are driven to zero (00b) during the Address phase. ***Note:*** *Refer to register offset 58h for MSI Upper Address.*	RW	RW	WO	0h

Register 16-42. (Offset 58h; MSIUPPERADDR) MSI Upper Address

Bit(s)	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address** Valid/used only when the PEX 8112 supports a 64-bit Message address (**MSI Control** register *MSI 64-Bit Address Capable* bit is set to 1). When the **MSI Control** register *MSI Enable* bit is set, the register contents specify the upper 32 bits of a 64-bit message. When the register contents are zero (0h), the PEX 8112 uses the 32-bit address specified by the **MSI Address** register. ***Note:*** *Refer to register offset 54h for MSI Address.*	RW	RW	WO	0h

Register 16-43. (Offset 5Ch; MSIDATA) MSI Data

Bit(s)	Description	CFG	MM	EE	Default
15:0	**MSI Data** When the **MSI Control** register *MSI Enable* bit is set, the Message data is driven onto the lower word of the AD Bus (AD[15:0]) of the Memory Write Transaction Data phase. The upper word (AD[31:16]) is always cleared to 0h.	RW	RW	WO	0h
31:16	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-44. (Offset 60h; PCIEXID) PCI Express Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID** Specifies the PCI Express Capability ID.	RO	RW	–	10h

Register 16-45. (Offset 61h; PCIEXNEXT) PCI Express Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Capability Pointer** 0h = Last capability in the New Capabilities Linked List	RO	RW	WO	0h

Register 16-46. (Offset 62h; PCIEXCAP) PCI Express Capability

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Capability Version** Indicates the **PCI Express Capability** structure Version Number.	RO	RW	WO	1h
7:4	**Device/Port Type** Indicates the type of PCI Express logical device. 0000b = PCI Express Endpoint Device 0001b = Conventional PCI Express Endpoint Device 0100b = Root Port of PCI Express Root Complex 0101b = Upstream Port of PCI Express Switch 0110b = Downstream Port of PCI Express Switch 0111b = PCI Express-to-PCI/PCI-X Bridge 1000b = PCI/PCI-X-to-PCI Express Bridge All other encodings are ***reserved***.	RO	RW	WO	1000b
8	**Slot Implemented** 1 = Indicates that the PCI Express link associated with this port is connected to a slot	RO	RW	WO	0
13:9	**Interrupt Message Number** When this function is allocated more than one MSI number, this field must contain the offset between the Base Message data and MSI message generated when the **Slot Status** or **Root Status** register bits of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the PEX 8112 changes.	RO	RO	–	0h
15:14	***Reserved***	RsvdP	RsvdP	–	00b

Register 16-47. (Offset 64h; DEVCAP) Device Capability

Bit(s)	Description	CFG	MM	EE	Default
2:0	**Maximum Payload Size Supported** Indicates the Maximum Payload Size that the PEX 8112 supports for TLPs. 000b = 128 bytes All other encodings are ***reserved***. ***Note:*** *Because the PEX 8112 supports a Maximum Payload Size of only 128 bytes, this field is hardwired to 000b.*	RO	RO	–	000b
4:3	**Phantom Functions Supported** ***Not supported*** Hardwired to 00b. Indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called *Phantom Functions*) with the Tag identifier.	RO	RO	–	00b
5	**Extended Tag Field Supported** Indicates the maximum supported *Tag* field size 0 = 5-bit *Tag* field is supported 1 = 8-bit *Tag* field is supported ***Note:*** *8-bit Tag field support must be enabled by the corresponding Control field in the* ***PCI Express Device Control*** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L0s to L0 Link PM state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Link PM state Acceptable Latency number to compare against the L0s Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L0s Link PM state entry is used with no performance loss. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	000b

Register 16-47. (Offset 64h; DEVCAP) Device Capability *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
11:9	**Endpoint L1 Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L1 to L0 Link PM state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Link PM state Acceptable Latency number to compare against the L1 Link PM state exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether ASPM L1 Link PM state entry is used with performance loss. 000b = Less than 1 µs 001b = 1 µs to less than 2 µs 010b = 2 µs to less than 4 µs 011b = 4 µs to less than 8 µs 100b = 8 µs to less than 16 µs 101b = 16 µs to less than 32 µs 110b = 32 to 64 µs 111b = More than 64 µs	RO	RW	WO	000b
12	**Attention Button Present** ***Not supported*** Forced to 0.	RO	RO	–	0
13	**Attention Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
14	**Power Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
17:15	***Reserved***	RsvdP	RsvdP	–	000b
25:18	**Captured Slot Power Limit Value** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Value is set by the Set Slot Power Limit message.	RO	RW	WO	0h
27:26	**Captured Slot Power Limit Scale** Specifies the scale used for the *Slot Power Limit Value.* Value is set by the Set Slot Power Limit message. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
31:28	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-48. (Offset 68h; DEVCTL) PCI Express Device Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
2	**Fatal Error Reporting Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable** Does not apply to Reverse Bridge mode.	RW	RW	WO	0
4	**Enable Relaxed Ordering** ***Not supported*** Forced to 0.	RO	RO	–	0
7:5	**Maximum Payload Size** Sets the maximum TLP Payload Size for the PEX 8112. As a Receiver, the PEX 8112 must handle TLPs as large as the set value; as Transmitter, the PEX 8112 must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the **Device Capability** register *Maximum Payload Size Supported* field. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = ***Reserved***	RW	RW	WO	000b

Register 16-48. (Offset 68h; DEVCTL) PCI Express Device Control *(Cont.)*

Bit(s)	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable** 0 = PEX 8112 is restricted to a 5-bit *Tag* field 1 = Enables PEX 8112 to use an 8-bit *Tag* field as a Requester Forced to 0 when the **Device Capability** register *Extended Tag Field Supported* bit is cleared.	RW	RW	WO	0
9	**Phantom Function Enable** ***Not supported*** Hardwired to 0.	RO	RO	–	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported*** Hardwired to 0.	RO	RO	–	0
11	**Enable No Snoop** ***Not supported*** Hardwired to 0.	RO	RO	–	0
14:12	**Maximum Read Request Size** The value specified in this register is the upper boundary of the **PCI Control** register *Programmed Prefetch Size* field if the **Device-Specific Control** register *Blind Prefetch Enable* bit is set. Sets the Maximum Read Request Size for the PEX 8112 as a Requester. The PEX 8112 must not generate Read Requests with a size that exceeds the set value. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = ***Reserved***	RW	RW	WO	010b
15	**Bridge Configuration Retry Enable** 0 = PEX 8112 does not generate Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions 1 = PEX 8112 generates Completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions	RW	RW	WO	0

Register 16-49. (Offset 6Ah; DEVSTAT) PCI Express Device Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Detected** Does not apply to Reverse Bridge mode.	RW1C	RW1C	–	0
1	**Non-Fatal Error Detected** Does not apply to Reverse Bridge mode.	RW1C	RW1C	–	0
2	**Fatal Error Detected** Does not apply to Reverse Bridge mode.	RW1C	RW1C	–	0
3	**Unsupported Request Detected** Does not apply to Reverse Bridge mode.	RW1C	RW1C	–	0
4	**AUX Power Detected** Devices that require AUX power report this bit as set when the PEX 8112 detects AUX power.	RO	RO	–	0
5	**Transactions Pending** Because the PEX 8112 does not internally generate Non-Posted transactions, this bit is forced to 0.	RO	RO	–	0
15:6	***Reserved***	RsvdZ	RsvdZ	–	0h

Register 16-50. (Offset 6Ch; LINKCAP) Link Capability

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed** Indicates the maximum link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are ***reserved***.	RO	RO	–	0001b
9:4	**Maximum Link Width** Indicates the maximum width of the given PCI Express link. By default, the PEX 8112 has a x1 link; therefore, this field is hardwired to 00_0001b. All other encodings are ***not supported***.	RO	RO	–	00_0001b
11:10	**Active State Power Management (ASPM) Support** Indicates the level of ASPM supported on the given PCI Express link. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported 00b, 10b = ***Reserved***	RO	RW	WO	11b
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L0s to L0 Link PM state. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	100b
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from the L1 to L0 Link PM state. 000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs	RO	RW	WO	100b
23:18	***Reserved***	RsvdP	RsvdP	–	0h
31:24	**Port Number** Indicates the PCI Express Port Number for the given PCI Express link.	RO	RW	WO	0h

Register 16-51. (Offset 70h; LINKCTL) Link Control

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Active State Power Management (ASPM) Control** Controls the level of ASPM supported on the given PCI Express link. 00b = Disabled 01b = L0s Link PM state entry is supported 10b = ***Reserved*** 11b = L0s and L1 Link PM state entry is supported ***Note:*** *"L0s Entry Enabled" indicates the Transmitter entering the L0s Link PM state.*	RW	RW	WO	00b
2	***Reserved***	RsvdP	RsvdP	–	0
3	**Read Completion Boundary (RCB) Control** 0 = Read Completion boundary is 64 bytes 1 = Read Completion boundary is 128 bytes	RO	RW	WO	0
4	**Link Disable** Disables the link when set to 1. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RW	RW	WO	0
5	**Retrain Link** 1 = Initiates link retraining Always returns 0 when read.	RW	RW	WO	0
6	**Common Clock Configuration** 0 = Indicates that the PEX 8112 and the component at the opposite end of the link are operating with **asynchronous** Reference Clock. Components use this common clock configuration information to report the correct L0s and L1 Link PM state Exit Latencies. 1 = Indicates that the PEX 8112 and the component at the opposite end of the link are operating with a **distributed** common Reference Clock.	RW	RW	WO	0
7	**Extended Sync** 1 = Forces extended transmission of FTS Ordered-Sets in FTS and extra TS2 at exit from the L1 Link PM state prior to entering the L0 Link PM state. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters the L0 Link PM state and resumes communication.	RW	RW	WO	0
15:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-52. (Offset 72h; LINKSTAT) Link Status

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Link Speed** Indicates the negotiated link speed of the given PCI Express link. Set to 0001b for 2.5 Gbps. All other encodings are ***reserved***.	RO	RO	–	0001b
9:4	**Negotiated Link Width** Indicates the negotiated width of the given PCI Express link. By default, the PEX 8112 has a x1 link; therefore, this field is hardwired to 00_0001b. All other encodings are ***not supported***.	RO	RO	–	00_0001b
10	**Link Training Error** Indicates that a Link Training error occurred. Cleared by hardware upon successful training of the link to the L0 Link PM state.	RO	RO	–	0
11	**Link Training** Indicates that link training is in progress; hardware clears this bit after link training is complete.	RO	RO	–	0
12	**Slot Clock Configuration** Indicates that the PEX 8112 uses the same physical Reference Clock that the platform provides on the connector. When the PEX 8112 uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	HwInit	RW	WO	0
15:13	***Reserved***	RsvdZ	RsvdZ	–	000b

Register 16-53. (Offset 74h; SLOTCAP) Slot Capability

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Present** ***Not supported*** Forced to 0.	RO	RO	–	0
1	**Power Controller Present** ***Not supported*** Forced to 0.	RO	RO	–	0
2	**MRL Sensor Present** ***Not supported*** Forced to 0.	RO	RO	–	0
3	**Attention Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
4	**Power Indicator Present** ***Not supported*** Forced to 0.	RO	RO	–	0
5	**Hot Plug Surprise** ***Not supported*** Forced to 0.	RO	RO	–	0
6	**Hot Plug Capable** ***Not supported*** The PEX 8112 does ***not support*** Hot Plug operations; therefore, this bit is forced to 0.	RO	RO	–	0
14:7	**Slot Power Limit Value** In combination with the field [16:15] (*Slot Power Limit Scale*) value, specifies the upper limit on power supplied by the slot. The Power Limit (in Watts) is calculated by multiplying the value in this field by the *Slot Power Limit Scale* field value. Writes to this register cause the PEX 8112 to transmit the Set Slot Power Limit message downstream.	RO	RW	WO	25d
16:15	**Slot Power Limit Scale** Specifies the scale used for field [14:7] (*Slot Power Limit Value*). Writes to this register cause the PEX 8112 to transmit the Set Slot Power Limit message downstream. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
18:17	***Reserved***	RsvdP	RsvdP	–	00b
31:19	**Physical Slot Number** ***Not supported*** Forced to 0h.	RO	RO	–	0h

Register 16-54. (Offset 78h; SLOTCTL) Slot Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
1	**Power Fault Detected Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
2	**MRL Sensor Changed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
3	**Presence Detect Changed Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
4	**Command Completed Interrupt Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable** ***Not supported*** Forced to 0.	RW	RW	WO	0
7:6	**Attention Indicator Control** ***Not supported*** Forced to 00b.	RW	RW	WO	00b
9:8	**Power Indicator Control** ***Not supported*** Forced to 00b.	RW	RW	WO	00b
10	**Power Controller Control** ***Not supported*** Forced to 0.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-55. (Offset 7Ah; SLOTSTAT) Slot Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed** ***Not supported*** Forced to 0.	RO	RO	–	0
1	**Power Fault Detected** ***Not supported*** Forced to 0.	RO	RO	–	0
2	**MRL Sensor Changed** ***Not supported*** Forced to 0.	RO	RO	–	0
3	**Presence Detect Changed** ***Not supported*** Forced to 0.	RO	RO	–	0
4	**Command Completed** ***Not supported*** Forced to 0.	RO	RO	–	0
5	**MRL Sensor State** ***Not supported*** Forced to 0.	RO	RO	–	0
6	**Presence Detect State** ***Not supported*** Forced to 1.	RO	RO	–	1
15:7	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-56. (Offset 7Ch; ROOTCTL) Root Control

Bit(s)	Description	CFG	MM	EE	Default
0	**System Error on Correctable Error Enable** 1 = System error (SERR#) is generated when an ERR_COR is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
1	**System Error on Non-Fatal Error Enable** 1 = System error (SERR#) is generated when an ERR_NONFATAL is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
2	**System Error on Fatal Error Enable** 1 = System error (SERR#) is generated when an ERR_FATAL is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
3	**PME Interrupt Enable** 1 = Enables PME interrupt generation upon PME message receipt as reflected in the **Root Status** register *PME Status* bit. A PME interrupt is also generated when the *PME Status* bit is set when this bit is set from a cleared state.	RW	RW	WO	0
31:4	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-57. (Offset 80h; ROOTSTAT) Root Status

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PME Requester ID** Indicates the PCI Requester ID of the last PME Requester.	RO	RO	–	–
16	**PME Status** Indicates that PME was asserted by the Requester ID indicated in the *PME Requester ID* field. Subsequent PMEs remain pending until this bit is cleared by software, by writing 1.	RW1C	RW1C	–	0
17	**PME Pending** Indicates that another PME is pending when the *PME Status* bit is set. When the *PME Status* bit is cleared by software, the PME is delivered by hardware by setting the *PME Status* bit again and updating the Requester ID appropriately. Cleared by hardware when no other PMEs are pending.	RO	RO	–	–
31:18	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-58. (Offset 84h; MAININDEX) Main Control Register Index

Bit(s)	Description	CFG	MM	EE	Default
11:0	**Main Control Register Index** Selects a **Main Control** register, that is accessed by way of the **Main Control Register Data** register.	RW	RW	WO	0h
31:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-59. (Offset 88h; MAINDATA) Main Control Register Data

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Main Control Register Data** Writes to and Reads from this register are mapped to a **Main Control** register, selected by the **Main Control Register Index** register.	RW	RW	WO	0h

16.7 PCI Express Extended Capability Registers

This section details the PEX 8112 Reverse Bridge mode PCI Express Extended Capability registers – Power Budget Capability and Device Serial Number. Table 16-8 defines the register map.

Table 16-8. Reverse Bridge Mode Power Budget Capability and Device Serial Number Register Map

PCI Express Configuration Register Offset	31 20	19 16	15 8	7 0
100h	Power Budget Next Capability Offset	Power Budget Capability Version	Power Budget PCI Express Extended Capability ID	
104h	***Reserved***			Power Budget Data Select
108h	Power Budget Data			
10Ch	Power Budget Capability			
110h	Serial Number Next Capability Offset	Serial Number Capability Version	Serial Number PCI Express Extended Capability ID	
114h	Serial Number Low (Lower DWORD)			
118h	Serial Number Hi (Upper DWORD)			
11Ch – FFFh	***Reserved***			

16.7.1 PCI Express Power Budget Registers

Register 16-60. (Offset 100h; PWRCAPHDR) Power Budget Enhanced Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability.	RO	RW	WO	4h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present.	RO	RW	WO	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List. Set to 110h when Serial Number Capability must be enabled.	RO	RW	WO	000h

Register 16-61. (Offset 104h; PWRDATASEL) Power Budget Data Select

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Data Select** Indexes the Power Budget Data reported through the **Power Budget Data** register. Selects the DWORD of Power Budget Data that is to appear in the **Power Budget Data** register. The PEX 8112 supports values from 0 to 31 for this field. For values greater than 31, a value of 0h is returned when the **Power Budget Data** register is read.	RW	RW	WO	0h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-62. (Offset 108h; PWRDATA) Power Budget Data

Bit(s)	Description	CFG	MM	EE	Default
*Note: This register returns the DWORD of Power Budget Data selected by the **Power Budget Data Select** register. When the **Power Budget Data Select** register has a value greater than or equal to the number of operating conditions for which the PEX 8112 provides power information, this register returns all zeros (0). The PEX 8112 supports 32 operating conditions.*					
7:0	**Base Power** Specifies (in Watts) the base power value in the given operating condition. This value must be multiplied by the Data Scale, to produce the actual power consumption value.	RO	RW	WO	0h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The PEX 8112 power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
12:10	**PM Sub-State** Specifies the power management sub-state of the operating condition being described. 000b = Default Sub-State All other values = Device-Specific Sub-State	RO	RW	WO	000b
14:13	**PM State** Specifies the Device PM state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in the *PM Type* field to specify the D3cold Device PM state. An encoding of 11b, along with any other *PM Type* field value, specifies the D3hot Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3	RO	RW	WO	00b
17:15	**PM Type** Specifies the type of operating condition being described. 000b = PME Aux 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	RO	RW	WO	000b
20:18	**Power Rail** Specifies the power rail of the operating condition being described. 000b = Power (12V) 001b = Power (3.3V) 010b = Power (1.8V) 111b = Thermal All other encodings are ***reserved***.	RO	RW	WO	000b
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 16-63. (Offset 10Ch; PWRBUDCAP) Power Budget Capability

Bit(s)	Description	CFG	MM	EE	Default
0	**System Allocated** 1 = Indicates that the PEX 8112 power budget is included within the system power budget, and software is to ignore Reported Power Budget data for power budgeting decisions	RO	RW	WO	0
31:1	***Reserved***	RsvdP	RsvdP	–	0h

16.7.2 PCI Express Serial Number Registers

Register 16-64. (Offset 110h; SERCAPHDR) Serial Number Enhanced Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	3h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present. Forced to 0h when Serial Number Capability is disabled.	RO	RO	–	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List.	RO	RO	–	000h

Register 16-65. (Offset 114h; SERNUMLOW) Serial Number Low (Lower DWORD)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the lower DWORD of the IEEE-defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0h when Serial Number Capability is disabled.	RO	RW	WO	0h

Register 16-66. (Offset 118h; SERNUMHI) Serial Number Hi (Upper DWORD)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the upper DWORD of the IEEE defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0h when Serial Number Capability is disabled.	RO	RW	WO	0h

16.8 Main Control Registers

This section details the PEX 8112 Reverse Bridge mode Main Control registers. Table 16-9 defines the register map.

Table 16-9. Reverse Bridge Mode Main Control Register Map

PCI Configuration Register Offset	31 24	23 16	15 8	7 0
1000h	Device Initialization			
1004h	Serial EEPROM Control			
1008h	Serial EEPROM Clock Frequency			
100Ch	PCI Control			
1010h	***Reserved***			
1014h	PCI Interrupt Request Enable			
1018h	Interrupt Request Status			
101Ch	***Reserved***			
1020h	General-Purpose I/O Control			
1024h	General-Purpose I/O Status			
1030h	Mailbox 0			
1034h	Mailbox 1			
1038h	Mailbox 2			
103Ch	Mailbox 3			
1040h	***Reserved***		Chip Silicon Revision	
1044h	Diagnostic Control ***(Factory Test Only)***			
1048h	***Reserved***	TLP Controller Configuration 0		
104Ch	TLP Controller Configuration 1			
1050h	TLP Controller Configuration 2			
1054h	***Reserved***	TLP Controller Tag		
1058h	TLP Controller Time Limit 0			
105Ch	TLP Controller Time Limit 1			
1060h	***Reserved***			
1064h	Enhanced Configuration Address			
1068h – 1FFFh	***Reserved***			

Register 16-67. (Offset 1000h; DEVINIT) Device Initialization

Bit(s)	Description	CFG	MM
3:0	**PCLKO Clock Frequency** Controls the PCLKO ball frequency as follows, when PCLKO62SEL# is strapped High or left disconnected. When cleared to 0000b, the clock is stopped and remains at a logic Low (0V) DC value. Non-zero values represent divisors of the 100-MHz Fixed-Frequency or Spread-Spectrum Reference Clock. The default value is 0011b, representing a frequency of 33, 62.5, or 66 MHz. When PCLKO62SEL# is pulled Low and M66EN is High, the PCLKO frequency is 62.5 MHz, with a 50% Duty cycle. 0000b = 0 0001b = 100 0010b = 50 0011b = 33.3/66/62.5, depending upon M66EN and PCLKO62SEL# values 0100b = 25 0101b = 20 0110b = 16.7 0111b = 14.3 1000b = 12.5 1001b = 11.1 1010b = 10 1011b = 9.1 1100b = 8.3 1101b = 7.7 1110b = 7.1 1111b = 6.7	RW	0011b
4	**PCI Express Enable** Does not apply to Reverse Bridge mode.	RW	0
5	**PCI Enable** 0 = All PCI accesses to the PEX 8112 result in a Target Retry response 1 = PEX 8112 responds normally to PCI accesses Automatically set when a valid serial EEPROM is not detected.	RW	0
31:6	***Reserved***	RsvdP	0h

Register 16-68. (Offset 1004h; EECTL) Serial EEPROM Control

Bit(s)	Description	CFG	MM
7:0	**Serial EEPROM Write Data** Determines the byte written to the serial EEPROM when the *Serial EEPROM Byte Write Start* bit is set. Represents an opcode, address, or data being written to the serial EEPROM.	RW	0h
15:8	**Serial EEPROM Read Data** Determines the byte read from the serial EEPROM when the *Serial EEPROM Byte Read Start* bit is set.	RO	–
16	**Serial EEPROM Byte Write Start** 1 = Value in the *Serial EEPROM Write Data* field is written to the serial EEPROM Automatically cleared when the Write operation is complete.	RW	0
17	**Serial EEPROM Byte Read Start** 1 = A byte is read from the serial EEPROM, and accessed using the *Serial EEPROM Read Data* field Automatically cleared when the Read operation is complete.	RW	0
18	**Serial EEPROM Chip Select Enable** 1 = Serial EEPROM Chip Select is enabled	RW	0
19	**Serial EEPROM Busy** 1 = Serial EEPROM Controller is busy performing a Byte Read or Write operation An interrupt is generated when this bit goes false.	RO	0
20	**Serial EEPROM Valid** 1 = Serial EEPROM with 5Ah in the first byte is detected	RO	–
21	**Serial EEPROM Present** Set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the PEX 8112.	RO	–
22	**Serial EEPROM Chip Select Active** Set when the EECS# ball to the serial EEPROM is active. The Chip Select can be active across multiple byte operations.	RO	–
24:23	**Serial EEPROM Address Width** Reports the installed serial EEPROM's addressing width. When the addressing width cannot be determined, 00b is returned. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	RO	–
30:25	***Reserved***	RsvdP	0h
31	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the serial EEPROM. Reading this bit returns 0 while initialization is in progress, and 1 when initialization is complete.	RW	0

Register 16-69. (Offset 1008h; EECLKFREQ) Serial EEPROM Clock Frequency

Bit(s)	Description	Access	Default
2:0	**Serial EEPROM Clock Frequency** Controls the EECLK ball frequency. 000b = 2 MHz 001b = 5 MHz 010b = 8.3 MHz 011b = 10 MHz 100b = 12.5 MHz 101b = 16.7 MHz 110b = 25 MHz 111b = ***Reserved***	RW	000b
31:3	***Reserved***	RsvdP	0h

Register 16-70. (Offset 100Ch; PCICTL) PCI Control

Bit(s)	Description	Access	Default
0	**PCI Multi-Level Arbiter** 0 = All PCI Requesters are placed into a single-level Round-Robin Arbiter, each with equal access to the PCI Bus 1 = Two-level Arbiter is selected	RW	0
3:1	**PCI Arbiter Park Select** Determines which PCI Master Controller is granted the PCI Bus when there are no pending requests. 000b = Last grantee 001b = PCI Express interface 010b, 011b = ***Reserved*** 100b = External Requester 0 101b = External Requester 1 110b = External Requester 2 111b = External Requester 3	RW	000b
4	**Bridge Mode** Reflects the FORWARD ball status. When Low, the PEX 8112 operates as a Reverse Bridge (PCI-to-PCI Express). When High, the PEX 8112 operates as a Forward Bridge (PCI Express-to-PCI).	RO	–
5	**PCI External Arbiter** Reflects the EXTARB ball state. When Low, the PEX 8112 enables its Internal PCI Arbiter. The PEX 8112 then expects external requests on REQ[3:0]# and issues bus grants on GNT[3:0]#. When High, the PEX 8112 asserts REQ0# and expects GNT0# from an External Arbiter.	RO	–
6	**Locked Transaction Enable** The PCI LOCK# ball is ignored. 1 = Locked transactions are propagated through the PEX 8112, from the primary bus to the secondary bus	RW	0
7	**M66EN** Reflects the M66EN ball state. When Low, the PEX 8112 PCI Bus is operating at 33 MHz. When High, the PEX 8112 PCI Bus is operating at 66 MHz.	RO	0

Register 16-70. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bit(s)	Description	Access	Default
15:8	**PCI-to-PCI Express Retry Count** Valid only when the PCI Express link is down. Determines the number of times to Retry a PCI Type 1 Configuration transaction to the PCI Express interface before aborting the transfer (in units of 2^{14} Retries). When the timer times out, the PEX 8112 holds DEVSEL# de-asserted, to signal the PCI Initiator to perform a Master Abort on the PCI Bus. Values 1 to 254 select multiples of 2^4. Values 0 and 255 are special cases (0 = Retry forever, 255 = 2^{24} Retries) 0 = Indicates that the transaction is Retried forever 1 = Selects a Retry Count of 2^{14} 254 = Selects a Retry Count of 254 * (2^{14}) 255 = Selects a Retry Count of 2^{24} (special case)	RW	80h
23:16	**PCI Express-to-PCI Retry Count** Determines the number of times to Retry a PCI Express-to-PCI transaction before aborting the transfer (in units of 2^4 Retries). Values 1 to 254 select multiples of 2^4. Values 0 and 255 are special cases (0 = Retry forever, 255 = 2^{24} Retries) 0 = Indicates that the transaction is Retried forever 1 = Selects a Retry Count of 2^4 254 = Selects a Retry Count of 254 * (2^4) 255 = Selects a Retry Count of 2^{24} (special case)	RW	0h
24	**Memory Read Line Enable** In Reverse Bridge mode, this bit enables Memory Read Line commands for PCI Express-to-PCI Reads that occur outside Memory or Prefetchable space. Memory Read Line commands occur only for PCI Express-to-PCI Reads above the 4-GB Address Boundary space, unless bit 31 (*PE2P Rdline Override*) is set. 0 = PEX 8112 issues a Memory Read command for transactions that could have otherwise been started with a Memory Read Line command. 1 = Memory Read Line command is issued when a transaction is not aligned to a Cache boundary, is above the 4-GB Address Boundary space or bit 31 (*PE2P Rdline Override*) is set, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst is stopped at the Cache Line boundary when the Burst Transfer Size is less than one Cache Line of data or when a Memory Read Multiple command is started.	RW	1
25	**Memory Read Multiple Enable** In Reverse Bridge mode, this bit enables Memory Read Multiple commands for PCI Express-to-PCI Reads that occur outside Memory or Prefetchable space. Memory Read Multiple commands occur only for PCI Express-to-PCI Reads above the 4-GB Address Boundary space, unless bit 31 (*PE2P Rdline Override*) is set. 0 = PEX 8112 issues a Memory Read command for transactions that could have otherwise been started with a Memory Read Multiple command. 1 = Memory Read Multiple command is issued when a transaction is aligned to a Cache boundary, is above the 4-GB Address Boundary space or bit 31 (*PE2P Rdline Override*) is set, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst continues when the Burst Transfer Size remains greater than or equal to one Cache Line of data.	RW	1
26	**Early Byte Enables Expected** 0 = PEX 8112 expects PCI Bytes Enables to be valid after IRDY# is asserted 1 = PEX 8112 expects the PCI Byte Enables to be valid in the clock tick following the Address phase For maximum compatibility with non-compliant PCI devices, clear this bit to 0. For maximum performance, set this bit to 1.	RW	0

Register 16-70. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bit(s)	Description	Access	Default
29:27	**Programmed Prefetch Size** Valid only for Memory Read Line and Memory Read Multiple transactions, or Memory Read transactions accessing Prefetchable Memory space with the **Device-Specific Control** register *Blind Prefetch Enable* bit set. Determines the number of bytes requested from the PCI Express interface as a result of a PCI-to-PCI Express Read. If a Prefetch Size is specified, the Cache Line boundary requirements of the Memory Read Line and Memory Read Multiple commands are disabled and the number of bytes requested will match the Prefetch Size. Enable this feature only when the PCI Master reads all requested data without disconnecting. Otherwise, performance is impacted. The Prefetch Size is limited by the **PCI Express Device Control** register *Maximum Read Request Size* field. 000b = Disabled 001b = 64 bytes 010b = 128 bytes 011b = 256 bytes 100b = 512 bytes 101b = 1,024 bytes 110b = 2,048 bytes 111b = 4,096 bytes (4 KB; refer to Note) ***Note:*** *If the Programmed Prefetch Size is 4 KB, the **TLP Controller Configuration 0** register Limit Completion Flow Control Credit bit must be set.*	RW	000b
30	**Short Discard Timer Timeout Select** Specifies the length of time that data returned from the PCI Express device, in response to a PCI Read Request, is held before it is discarded. 0 = Data is discarded after 32,767 or 1,024 PCI Clock cycles, as selected by the **Bridge Control** register *Primary Discard Timer* bit (bit 8) 1 = Data is discarded after only 64 PCI Clock cycles	RW	0
31	**PE2P Rdline Override** PCI Express-to-PCI Memory Read Line override. In Reverse Bridge mode, a PCI Express-to-PCI Read Request that is outside both Memory-Mapped I/O and Prefetchable space is forwarded upstream, to the PCI Bus: • Addresses below the 4-GB Address Boundary space usually result in PCI Memory Read commands • Addresses above the 4-GB Address Boundary space usually result in PCI Memory Read Line or Memory Read Multiple commands For certain applications, it might be necessary to issue PCI Memory Read Line or Memory Read Multiple commands for addresses below the 4-GB Address Boundary space. Although the address is below the 4-GB Address Boundary space, setting this bit enables these PCI Cache commands, as long as all other requirements are met.	RW	1

Register 16-71. (Offset 1014h; PCIIRQENB) PCI Interrupt Request Enable

Bit(s)	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** 1 = Enables a PCI interrupt to be generated when a Serial EEPROM Read or Write transaction completes ***Note:*** *Refer to Section 5.2, "Reverse Bridge PCI Interrupts," for further details.*	RW	0
1	**GPIO Interrupt Enable** 1 = Enables a PCI interrupt to be generated when an interrupt is active from one of the GPIO balls	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** 1 = Enables a PCI interrupt to be generated when the PCI Express-to-PCI Retry count is reached	RW	0
4	**Mailbox 0 Interrupt Enable** 1 = Enables a PCI interrupt to be generated when Mailbox 0 is written	RW	0
5	**Mailbox 1 Interrupt Enable** 1 = Enables a PCI interrupt to be generated when Mailbox 1 is written	RW	0
6	**Mailbox 2 Interrupt Enable** 1 = Enables a PCI interrupt to be generated when Mailbox 2 is written	RW	0
7	**Mailbox 3 Interrupt Enable** 1 = Enables a PCI interrupt to be generated when Mailbox 3 is written	RW	0
8	**Unsupported Request Interrupt Enable** 1 = Enables a PCI interrupt to be generated when an Unsupported Request Completion response is received from the PCI Express	RW	0
30:9	***Reserved***	RsvdP	0h
31	**PCI Internal Interrupt Enable** 1 = Enables a PCI interrupt to be generated as a result of an internal PEX 8112 interrupt source ***Note:*** *Refer to Section 5.2, "Reverse Bridge PCI Interrupts," for further details.*	RW	1

Register 16-72. (Offset 1018h; IRQSTAT) Interrupt Request Status

Bit(s)	Description	Access	Default
0	**Serial EEPROM Done Interrupt** Set when a Serial EEPROM Read or Write transaction completes. Writing 1 clears this status bit.	RW1C	0
1	**GPIO Interrupt** Conveys the interrupt status for the four GPIO balls. Set independently of the *GPIO Interrupt Enable* bits. This bit is an OR of the four individual GPIO status bits. 1 = **General-Purpose I/O Status** register is read to determine the cause of the interrupt	RO	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt** Set when the PCI Express-to-PCI Retry count is reached. Writing 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt** Set when Mailbox 0 is written. Writing 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt** Set when Mailbox 1 is written. Writing 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt** Set when Mailbox 2 is written. Writing 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt** Set when Mailbox 3 is written. Writing 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt** Set when an Unsupported Request Completion is received from the PCI Express interface, provided that the **PCI Interrupt Request Enable** register *Unsupported Request Interrupt Enable* bit is set.	RW1C	0
31:9	***Reserved***	RsvdZ	0h

Register 16-73. (Offset 1020h; GPIOCTL) General-Purpose I/O Control

Bit(s)	Description	Access	Default
0	**GPIO0 Data** When programmed as an output, values written to this bit appear on the GPIO0 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 ball.	RW	0
1	**GPIO1 Data** When programmed as an output, values written to this bit appear on the GPIO1 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 ball.	RW	0
2	**GPIO2 Data** When programmed as an output, values written to this bit appear on the GPIO2 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 ball.	RW	0
3	**GPIO3 Data** When programmed as an output, values written to this bit appear on the GPIO3 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 ball.	RW	0
4	**GPIO0 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO0 ball is an input 1 = GPIO0 ball is an output	RW	1
5	**GPIO1 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO1 ball is an input 1 = GPIO1 ball is an output	RW	0
6	**GPIO2 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO2 ball is an input 1 = GPIO2 ball is an output	RW	0
7	**GPIO3 Output Enable** The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected. 0 = GPIO3 ball is an input 1 = GPIO3 ball is an output	RW	0
8	**GPIO0 Interrupt Enable** 1 = Changes on the GPIO0 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
9	**GPIO1 Interrupt Enable** 1 = Changes on the GPIO1 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
10	**GPIO2 Interrupt Enable** 1 = Changes on the GPIO2 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
11	**GPIO3 Interrupt Enable** 1 = Changes on the GPIO3 ball (when programmed as an input) are enabled to generate an interrupt	RW	0

Register 16-73. (Offset 1020h; GPIOCTL) General-Purpose I/O Control *(Cont.)*

Bit(s)	Description	Access	Default
13:12	**GPIO Diagnostic Select** Selects diagnostic signals that are output on the GPIO balls. 00b = Normal GPIO operation 01b = GPIO0 driven High when the link is up. GPIO[3:1] operate according to the configuration specified by bits [7:5] of this register 10b = GPIO[3:0] driven with lower four bits of the Link Training and Status State Machine (LTSSM) for 2s, alternating with GPIO[1:0] driven with the upper two bits of the LTSSM for 1s 11b = GPIO[3:0] driven with PM Link state (L2, L1, L0s, and L0 Link PM states) **LTSSM Codes** 00h – L3_L2 (Fundamental Reset) 01h – Detect 02h – Polling.Active 03h – Polling.Configuration 04h – Polling.Compliance 05h – Configuration.Linkwidth.Start & Accept 06h – Configuration.Lanenum.Wait & Accept 07h – Configuration.Complete 08h – Configuration.Idle 09h – ***Reserved*** 0Ah – ***Reserved*** 0Bh – ***Reserved*** 0Ch – ***Reserved*** 0Dh – ***Reserved*** 0Eh – L0 0Fh – L0 (Transmit E.I.Ordered-Set) 10h – L0 (Wait E.I.Ordered-Set) 12h – L1.Idle 14h – L2.Idle 15h – Recovery.Rcvrlock (Extended Sync enabled) 16h – Recovery.Rcvrlock 17h – Recovery.RcvrCfg 18h – Recovery.Idle 19h – Disabled (Transmit TS1) 1Ah – Disabled (Transmit E.I.Ordered-Set) 1Dh – Disabled (Wait Electrical Idle) 1Eh – Disabled (Disable) 1Fh – Loopback.Entry 20h – Loopback.Active 21h – Loopback.Exit 22h – Hot Reset (Wait TS1 with Hot Reset) 23h – Hot Reset (Reset Active) 24h – Loopback.Actice (Transmit E.I.Ordered-Set) 25h – Loopback.Active (Wait Electrical Idle)	RW	01b
31:14	***Reserved***	RsvdP	0h

Register 16-74. (Offset 1024h; GPIOSTAT) General-Purpose I/O Status

Bit(s)	Description	Access	Default
0	**GPIO0 Interrupt** Set when the GPIO0 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt** Set when the GPIO1 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt** Set when the GPIO2 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt** Set when the GPIO3 ball state changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
31:4	***Reserved***	RsvdZ	0h

Register 16-75. (Offset 1030h; MAILBOX0) Mailbox 0

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	FEED_FACEh

Register 16-76. (Offset 1034h; MAILBOX1) Mailbox 1

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 16-77. (Offset 1038h; MAILBOX2) Mailbox 2

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 16-78. (Offset 103Ch; MAILBOX3) Mailbox 3

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or PCI Bus. Interrupts are generated to the PCI Express interface or PCI Bus when this register is written.	RW	0h

Register 16-79. (Offset 1040h; CHIPREV) Chip Silicon Revision

Bit(s)	Description	Access	Default
15:0	**Chip Revision** Returns the PEX 8112 current Silicon Revision number. ***Note: CHIPREV** is the Silicon Revision, encoded as a 4-digit BCD value. The **CHIPREV** value for the first release of the chip (Rev. AA) is 0A0Ah. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*	RO	Current Revision
31:16	***Reserved***	RsvdP	0h

Register 16-80. (Offset 1044h; DIAGCTL) Diagnostic Control *(Factory Test Only)*

Bit(s)	Description	Access	Default
0	**Fast Times** ***Factory Test Only***	RW	0
1	**Force PCI Interrupt** ***Factory Test Only*** 1 = Forces the PCI INT*x*# Interrupt signal to assert. The **PCI Interrupt Pin** register determines which INT*x*# signal is asserted. Effective only when the **PCI Command** register *Interrupt Disable* bit is Low.	RW	0
2	**Force PCI SERR** ***Factory Test Only*** 1 = Forces the PCI SERR# Interrupt signal to assert when the **PCI Command** register *SERR# Enable* bit is set	RW	0
3	**Force PCI Express Interrupt** ***Factory Test Only*** 1 = Forces an interrupt to the PCI Express Root Complex, using Message Signaled interrupts or virtual INT*x*# interrupts	RW	0
31:4	***Reserved***	RsvdP	0h

Register 16-81. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0

Bit(s)	Description	Access	Default
7:0	**CFG_NUM_FTS** Forced NUM_FTS signal. NUM_FTS represents the number of Fast Training sequence (0 to 255). Refer to the *PCI Express r1.0a*, Section 4.2.4.3, for further details.	RW	20h
8	**CFG_ACK_FMODE** PCI Express interface ACK_DLLP transmitting interval mode. 0 = PCI Express interface uses own interval value 1 = PCI Express interface uses *CFG_ACK_COUNT* as interval value	RW	0
9	**CFG_TO_FMODE** PCI Express interface Timeout Detection mode for the Replay Timer. 0 = PCI Express interface uses own timer value 1 = PCI Express interface uses *CFG_TO_COUNT* as timer value	RW	1
10	**CFG_PORT_DISABLE** 1 = Serializer/De-Serializer (SerDes) in the PCI Express interface is disabled. This allows the endpoint to disable the PCI Express connection when powered up or before configuration is complete.	RW	0
11	**CFG_RCV_DETECT** Set when the PCI Express interface establishes the PCI Express connection.	RO	0
12	**CFG_LPB_MODE** Link Loop-Back mode. 1 = PEX 8112 changes its LTSSM state to the Loop-Back state, becomes the Loop-Back Master, and starts transmitting packets of pseudo-random numbers	RW	0
13	**CFG_PORT_MODE** 0 = Link PCI Express interface is configured as an upstream port (Endpoint) 1 = Link PCI Express interface is configured as a downstream port (Root Complex)	RW	1
14	***Reserved***	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE** The PEX 8112 does ***not support*** End-to-end Cyclic Redundancy Check (ECRC); therefore, this bit is cleared to 0.	RW	0

Register 16-81. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0 *(Cont.)*

Bit(s)	Description	Access	Default
16	**TLP_CPLD_NOSUCCESS_MALFORM_ENABLE** 0 = Received Completion is retained 1 = Completion received when Completion timeout expired is treated as a malformed TLP and discarded	RW	1
17	**Scrambler Disable** 0 = Data scrambling is enabled. 1 = Data scrambling is disabled. Set only when testing and debugging.	RW	0
18	**Delay Link Training** 0 = Link training is allowed to commence immediately after PCIRST# is de-asserted 1 = Link training is delayed for 12 ms after PCIRST# is de-asserted	RW	1
19	**Decode Primary Bus Number** 0 = PEX 8112 ignores the Primary Bus Number in a PCI Express Type 0 Configuration Request. 1 = PEX 8112 compares the Primary Bus Number in a PCI Express Type 0 Configuration Request with the **Primary Bus Number** register. When they match, the request is accepted. Otherwise, an Unsupported Request is returned. This comparison occurs only after the first Type 0 Configuration Write occurs.	RW	0
20	**Ignore Function Number** 0 = PEX 8112 only responds to Function Number 0 during a Type 0 Configuration transaction. Accesses to other Function Numbers result in an Unsupported Request (PCI Express) or Master Abort (PCI). 1 = PEX 8112 ignores the Function Number in a PCI or PCI Express Type 0 Configuration Request, and responds to all eight functions.	RW	0
21	**Check RCB Boundary** 0 = PEX 8112 ignores Read Completion Boundary (RCB) violations. 1 = PEX 8112 checks for RCB violations. When detected, the PEX 8112 treats an RCB violation as a malformed TLP (packet is dropped and a Fatal Error message is transmitted).	RW	0
22	**Limit Completion Flow Control Credit** Must be set when the **PCI Control** register *Programmed Prefetch Size* field is set to 4 KB. When GPIO2 is Low at the trailing edge of PCIRST#, this bit is automatically set. Because this bit is used during link training, it must be set by driving GPIO2 Low during PCIRST# assertion. 0 = PEX 8112 advertises infinite Flow Control credits for Completions 1 = PEX 8112 advertises Completion Flow Control credits, based upon available buffer storage	RW	0
23	**L2 Secondary Bus Reset** When clear and the PEX 8112 remains in the L2/L3 Ready Link PM state, PCI-to-PCI Express Configuration transactions are Retried until the **PCI Control** register *PCI-to-PCI Express Retry Count* expires. The PEX 8112 responds with a Master Abort. When set, and the PEX 8112 remains in the L2/L3 Ready Link PM state, PCI-to-PCI Express Configuration transactions result in a Secondary Bus Reset. After the link training completes, the PCI-to-PCI Express Configuration transaction completes normally.	RW	1
31:24	***Reserved***	RsvdP	0h

Register 16-82. (Offset 104Ch; TLPCFG1) TLP Controller Configuration 1

Bit(s)	Description	Access	Default
20:0	**CFG_TO_COUNT** PCI Express interface Replay Timer timeout value when *CFG_TO_FMODE* is set to 1.	RW	D4h
30:21	**CFG_ACK_COUNT** PCI Express interface ACK_DLLP transmitting interval value when *CFG_ACK_FMODE* is set to 1.	RW	0h
31	***Reserved***	RsvdP	0

Register 16-83. (Offset 1050h; TLPCFG2) TLP Controller Configuration 2

Bit(s)	Description		Access	Default
2:0	**Function Number**	**CFG_COMPLETER_ID0** The Bus Number, Device Number, and Function Number of a Configuration transaction to the PEX 8112 are latched in this register. The latched values are then used when generating the Completion.	RW	0h
7:3	**Device Number**			
15:8	**Bus Number**			
26:16	**Update Credit FC** Controls a Counter that determines the gap between UpdateFC DLLPs (in units of 62.5 MHz clocks = 16 ns = 4 symbol times). When Data or Headers are read from the TLP Controller, the Credit Allocation Manager transmits a set of UpdateFC DLLPs; Posted, Non-Posted, and Completion when the **TLP Controller Configuration 0** register *Limit Completion Flow Control Credit* bit is set. While transmitting the set of DLLPs, the Credit Allocation Manager uses the Counter value to insert gaps between the DLLPs. The Bus Number, Device Number, and Function Number of a Configuration transaction to the PEX 8112 are latched in this register. The latched values are then used when generating the Completion.		RW	1h
31:27	***Reserved***		RsvdP	0h

Register 16-84. (Offset 1054h; TLPTAG) TLP Controller Tag

Bit(s)	Description	Access	Default
7:0	**TAG BME1** Message Request *Tag* field.	RW	0h
15:8	**TAG ERM** Error Manager *Tag* field.	RW	0h
23:16	**TAG PME** Power Manager *Tag* field.	RW	0h
31:24	***Reserved***	RsvdP	0h

Register 16-85. (Offset 1058h; TLPTIMELIMIT0) TLP Controller Time Limit 0

Bit(s)	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT** Bus Master engine Completion timeout (in PCI Clock units). The default value produces a 10-ms timeout.	RW	51615h (M66EN Low) A2C2Ah (M66EN High)
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT** Determines length of time before power is removed after entering the L2 Link PM state. Value must be at least 100 ns. Contains PCI clock units.	RW	4h (M66EN Low) 8h (M66EN High)
31:28	***Reserved***	RsvdP	0h

Register 16-86. (Offset 105Ch; TLPTIMELIMIT1) TLP Controller Time Limit 1

Bit(s)	Description	Access	Default
10:0	**ASPM_LI_DLLP_INTERVAL_TIME_LIMIT** Determines time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions. The default is 10 µs for both 14Dh and 29Ah. Allow at least 10 µs spent in the LTSSM L0 and L0s Link PM states before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP is transmitted. Refer to the *PCI Express r1.0a Errata*, page 19, for further details. Contains PCI clock units.	RW	14Dh (M66EN Low) 29Ah (M66EN High)
31:11	***Reserved***	RsvdP	0h

Register 16-87. (Offset 1064h; ECFGADDR) Enhanced Configuration Address

Bit(s)	Description	Access	Default
11:0	***Reserved***	RsvdP	0h
14:12	**Configuration Function Number** Provides the Function Number for an enhanced Configuration transaction.	RW	000b
19:15	**Configuration Device Number** Provides the Device Number for an enhanced Configuration transaction.	RW	0h
27:20	**Configuration Bus Number** Provides the Bus Number for an enhanced Configuration transaction.	RW	0h
30:28	***Reserved***	RsvdP	000b
31	**Enhanced Configuration Enable** 0 = Accesses to the **PCI Base Address 0** register (**BAR0**), offset 2000h, are not responded to by the PEX 8112 1 = Accesses to the **PCI Base Address 0** register (**BAR0**), offset 2000h, are forwarded to the PCI Express interface as a Configuration Request	RW	0

Chapter 17 Shared Memory

17.1 Overview

The PEX 8112 contains a 2 KB x 32-bit (8-KB) memory block that is accessed from the serial EEPROM, PCI Express interface, or PCI Bus.

17.2 Serial EEPROM Accesses

When the *Shared Memory Load* bit in the Serial EEPROM Format byte is set, the shared memory is loaded from the serial EEPROM starting at location REG_BYTE_COUNT + 6. The number of bytes to load is determined by the value in serial EEPROM locations REG_BYTE_COUNT + 4 and REG_BYTE_COUNT + 5. The serial EEPROM data is always loaded into the shared memory starting at Address 0. Data is transferred from the serial EEPROM to the shared memory (in units of DWORDs). (Refer to Chapter 6, "Serial EEPROM Controller," for details.)

17.3 PCI Express Accesses

The shared memory is accessed using the 64-KB Address space defined by the **PCI Base Address 0** register (**BAR0**). The shared memory is located at offset 8000h in this space. PCI Express Posted Writes are used to write data to the shared memory. Single or Burst Writes are accepted, and PCI Express first and last Byte Enables are supported. When shared Memory Write data is poisoned, the data is discarded and an ERR_NONFATAL message is generated (when enabled). PCI Express Non-Posted Reads are used to read data from the shared memory. Single or Burst Reads are accepted. When the 8-KB Address Boundary space of the shared memory is reached during a Burst Write or Read, the address wraps around to the start of memory.

17.4 PCI Accesses

The shared memory is accessed using the 64-KB Address space defined by the **PCI Base Address 0** register (**BAR0**). The shared memory is located at Address offset 8000h in this space. PCI Single or Burst Writes are used to write data to the shared memory. PCI Byte Enables are supported for each DWORD transferred. PCI Single or Burst Reads are used to read data from the shared memory. When the 8-KB Address Boundary space of the shared memory is reached during a Burst Write or Read, a PCI Disconnect is generated.

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Chapter 18 Testability and Debug

18.1 JTAG Interface

The PEX 8112 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball.

18.1.1 *IEEE Standard 1149.1* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*. This standard describes a method for accessing internal PEX 8112 facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG Debug Port implements the four required JTAG signals (TCK, TDI, TDO, TMS) and the optional TRST# signal
- JTAG Clock Requirements – TCK signal frequency range from DC to 10 MHz
- JTAG Reset Requirements – Refer to Section 18.1.4

18.1.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE instructions, provided by the JTAG Debug Port, and their input codes. ***PRIVATE instructions are for PLX USE ONLY.*** Invalid instructions behave as BYPASS instructions. Table 18-1 lists the JTAG instructions, along with their input codes.

Table 18-2 defines the JTAG IDCODE values returned by the PEX 8112.

Table 18-1. EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE Instructions

Instruction	Input Code	Comments
EXTEST	0_0000b	*IEEE Standard 1149.1-1990*
IDCODE	0_0001b	
SAMPLE/PRELOAD	0_0011b	
BYPASS	1_1111b	
PRIVATE[a]	0_0011b	
	0_0100b	
	0_0101b	
	0_0110b	
	0_0111b	
	0_1000b	
	0_1001b	
	0_1010b	

a. Warning: Non-PLX use of PRIVATE instructions can cause the PEX 8112 to operate in a hazardous manner.

Table 18-2. JTAG IDCODE Values

Unit of Measure	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0000b	1000_0001_1101_0011b	000_0001_0000b	1
Hex	0h	81D3h	10h	1h
Decimal	0	33235	16	1

18.1.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to the *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture. BSDL*, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, which allows a rigorous description of testability features in components that comply with the standard. It is used by automated test pattern generation tools for package interconnect tests, and Electronic Design Automation (EDA) tools for synthesized test logic and verification. *BSDL* supports robust extensions that are used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of *BSDL* include the logical port description, physical ball map, instruction set, and **Boundary** register description.

The logical port description assigns symbolic names to the PEX 8112 balls. Each ball contains a logical type of In, Out, In Out, Buffer, or Linkage that defines the logical direction of signal flow.

The physical ball map correlates the PEX 8112 logical ports to the physical balls of a specific package. A *BSDL* description has several physical ball maps; each map is assigned a unique name.

Instruction Set statements describe the bit patterns that must be shifted into the **Instruction** register to place the PEX 8112 in the various test modes defined by the standard. Instruction Set statements also support descriptions of instructions that are unique to the PEX 8112.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell contains a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

18.1.4 JTAG Reset Input TRST#

The TRST# Input ball is the asynchronous JTAG logic reset. When TRST# is asserted, it causes the PEX 8112 JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8112 normal logic path (PCI Express interface-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  - TRST# input signal uses a Low-to-High transition one time during the PEX 8112 boot-up, along with the PERST# (Forward Bridge mode) or PCIRST# (Reverse Bridge mode) signal
  - Hold the PEX 8112 TMS ball High while transitioning the PEX 8112 TCK ball five times
- If JTAG functionality is not required, the TRST# signal must be directly connected to ground
- If the PEX 8112's JTAG TAP Controller is not intended to be used by the design, it is recommended that a 1.5KΩ pull-down resistor be connected to the TRST# ball, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation

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Chapter 19 Electrical Specifications

19.1 Power Requirements

19.1.1 Power Consumption

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-1. Power Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDD1.5}$	VDD1.5 Supply Current	VDD1.5 = 1.5V		180	207	mA
$I_{VDDSERDES}$	VDD_P, VDD_R, VDD_T, AVDD Supply Currents	VDD_P, VDD_R, VDD_T, AVDD = 1.5V				
$I_{VDD3.3}$	VDD3.3 Supply Current	VDD3.3 = 3.3V		19	22	mA
I_{VDDQ}	VDDQ Supply Current	VDDQ = 3.3V				
I_{VDD5}	VDD5 Supply Current	VDD5 = 5.0V		.003	.004	mA

Notes:

1. *$I_{VDD1.5}$ + $I_{VDDSERDES}$ = 207 mA @ 33 MHz.*
2. *$I_{VDD3.3}$ + I_{VDDQ} = 22 mA @ 33 MHz.*
3. *$I_{VDD1.5}$ + $I_{VDDSERDES}$ = 280 mA @ 66 MHz.*
4. *$I_{VDD3.3}$ + I_{VDDQ} = 40 mA @ 66 MHz.*

19.1.2 Power Sequence

The power supply for the PEX 8112 I/O buffers are 3.3V (VDD3.3 and VDDQ) and core is 1.5V (VDD1.5, VDD_P, VDD_R, VDD_T, and AVDD). To fully comply with the *PCI r2.2* or *PCI r3.0*, a third power supply for VIO (VDD5) is also supported. VIO connects to a cathode of the High clamp diode in the PCI buffers. In a 5V system, set VIO to 5V, and in a 3.3V system, set to 3.3V.

The following sections describe the power sequencing rules for all designs, and those that power VIO and VDDQ/VDD3.3 separately. It is required that all power supplies ramp and decay linearly and monotonically.

19.1.2.1 Power Sequence Rule for All Designs

The ideal power supply design powers up and powers down all supply rails within 10 ms of one another, in any order.

Applying power to the I/O supply balls (VDDQ, VDD3.3) with the VIO or core power balls at 0V for greater than 10 ms is not recommended. The resulting high current can cause immediate device failure, or cause undetectable damage that will shorten the operating life of the PEX 8112.

If this timing constraint is satisfied, the PEX 8112 can be powered by using simple regulators connected in any manner (parallel, cascade, or a combination), without additional load switching or power-sequencing hardware.

19.1.2.2 Power Sequence Rules for Separate Power Supplies

If VIO and VDDQ/VDD3.3 are powered from separate (independent) power supplies, the following power sequence rules apply.

- VIO ***must always*** be greater than VDDQ/VDD3.3, when voltage is present on VDD3.3 or any PCI I/O ball. Otherwise, the PCI clamping diodes could become forward biased creating a low-resistance path between supplies. If this design criteria is met, current-limiting resistors in series with the VIO balls are not required, but are recommended as an added measure of protection.
- For designs that ***do not*** satisfy the rule above, current-limiting resistors must be placed in series with the VIO balls to prevent high current from damaging the PEX 8112 when the over-voltage clamping diodes on the PCI I/O balls are forward biased.

Table 19-2 specifies the recommended PEX 8112 power-on and power-down sequences if the 10-ms rule cannot be met. Table 19-2 does not imply that one voltage must fully ramp or decay before the next supply ramps or decays, but it shows the order in which the supplies should be sequenced.

Table 19-2. Power Sequence

Power-On Sequence	Power-Down Sequence
1. VDD5	**1.** 1.5V
2. 3.3V	**2.** 3.3V
3. 1.5V	**3.** VDD5

19.1.3 VIO

If the VIO voltage source is not powered and it presents a low-impedance path to ground, the PEX 8112's VIO balls can source High current, which could immediately damage the PEX 8112 or cause it undue long-term electrical stress. The amount of current each PCI ball/pad sources is dependent upon the device that is driving the signal/pad, or the value of the pull-up resistor when the signal is not driven.

For designs and add-in boards that have an independent voltage source for VIO, for which proper power sequencing cannot be guaranteed, a resistor is strongly recommended between the VIO voltage source and PEX 8112 VIO balls (VDD5) to limit the current and protect the devices from damage or long-term undue stress. Use the following guidelines to determine the value of this required resistance:

- **3.3V Signaling Environments** – 40Ω to 200Ω resistance between the VIO voltage source and the PEX 8112 VIO balls is recommended if VIO is a maximum of 3.6V
- **3.3 or 5V Signaling Environments** – 40Ω to 70Ω resistance is recommended

A single resistor can be used if the VIO balls are bused, or multiple parallel resistors can be used between the VIO voltage source and VIO balls. The resistor power dissipation rating depends upon the resistance size and signaling environment. *For example*, if a single 50Ω resistor is used in a 5V-signaling environment, the worst-case power dissipation can result in 480 mW, calculated as follows:

$$480\ \text{mW} = \frac{(V * V)/R\ (5.5V\ (\text{Maximum Signal Amplitude, Plus 10\%}) - 0.6V\ (1\ \text{Diode Drop}))^2}{50\Omega}$$

If four, 200Ω resistors are used in parallel, each must dissipate 120 mW.

Any resistance value within the recommended ranges prevents damage to the PEX 8112, while providing sufficient clamping action to hold the Input Voltage (VIN) below its maximum rating. A resistance value at the lower end of the range is recommended to provide preferable clamping action, and a sufficient VIN margin.

19.2 Absolute Maximum Ratings

Caution: ***Conditions that exceed the Absolute Maximum limits can destroy the PEX 8112.***

Table 19-3. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Power Supply Voltages	With respect to Ground	-0.5	+1.8	V
VDD3.3, VDDQ	3.3V Power Supply Voltages	With respect to Ground	-0.5	+4.6	V
VDD5	5V Power Supply Voltage	With respect to Ground	-0.5	+6.6	V
V_I	DC Input Voltage	3.3V buffer	-0.5	+4.6	V
		5V tolerant buffer (PCI)	-0.5	+6.6	V
I_{OUT}	DC Output Current, per ball	3 mA buffer	-10	+10	mA
		6 mA buffer	-20	+20	mA
		12 mA buffer	-40	+40	mA
		24 mA buffer (PCI)	-70	+70	mA
T_{STG}	Storage Temperature	No bias	-65	+150	°C
V_{ESD}	ESD Rating	R = 1.5KΩ, C = 100 pF	–	2	KV

19.3 Recommended Operating Conditions

Caution: ***Conditions that exceed the Operating limits can cause the PEX 8112 to malfunction.***

Table 19-4. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Power Supply Voltages		1.35	1.65	V
VDD3.3, VDDQ	3.3V Power Supply Voltages		3.0	3.6	V
VDD5	5V Power Supply Voltage	Note 1	4.75	5.25	V
V_N	Negative Trigger Voltage	3.3V buffer	0.8	1.7	V
		5V tolerant buffer (PCI)	0.8	1.7	V
V_P	Positive Trigger Voltage	3.3V buffer	1.3	2.4	V
		5V tolerant buffer (PCI)	1.3	2.4	V
V_{IL}	Low Level Input Voltage	3.3V buffer	0	0.7	V
		5V tolerant buffer (PCI)	0	0.8	V
V_{IH}	High Level Input Voltage	3.3V buffer	1.7	VDD3.3	V
		5V tolerant buffer (PCI)	2.0	VDD5 + 0.5	V
I_{OL}	Low Level Output Current	3 mA buffer (V_{OL} = 0.4)		3	mA
		6 mA buffer (V_{OL} = 0.4)		6	mA
		12 mA buffer (V_{OL} = 0.4)		12	mA
		24 mA buffer (V_{OL} = 0.4) (PCI)		24	mA
I_{OH}	High Level Output Current	3 mA buffer (V_{OH} = 2.4)		-3	mA
		6 mA buffer (V_{OH} = 2.4)		-6	mA
		12 mA buffer (V_{OH} = 2.4)		-12	mA
		24 mA buffer (V_{OH} = 2.4) (PCI)		-24	mA
T_A	Operating Temperature (Industrial)		-40	+85	°C
t_R	Input Rise Times	Normal input	0	200	ns
t_F	Input Fall Time		0	200	ns
t_R	Input Rise Times	Schmitt input	0	10	ms
t_F	Input Fall Time		0	10	ms

Notes:

1. *In a 3.3V-only system, the VDD5 balls can be connected to the 3.3V power supply (3.0 to 3.6V).*
2. *V_{IL} and V_{IH} for non-PCI buffered inputs, such as JTAG, GPIO, and serial EEPROM signals and Strapping signals (EXTARB, FORWARD, and so forth), are 3.3V LVTTL inputs (CMOS) V_{IL} = 0.8V maximum and V_{IH} = 2V minimum.*

19.4 PCI Express Specifications

19.4.1 SerDes Interface AC/DC Specifications

Table 19-5. PCI Express AC and DC Electrical Characteristics

Item	Conditions	Min	Typ	Max	Unit
Tx I/O Characteristics					
Differential Output Amplitude		0.8	1.01	1.2	V
Emphasis Levels		3.25	3.61	3.76	dB
Tx Eye Width		0.85	0.92	0.96	UI[a]
Maximum time between the jitter median and deviation from the median		0.02	0.03	0.07	UI
Tx rise time and fall time		0.19	0.27	0.40	UI
RMS AC common mode voltage		9.2	12.8	18.2	mV
Absolute delta of DC common mode voltage during the L0 Link PM state and Electrical Idle		0.5	25	97	mV
Absolute delta of DC common mode voltage between D+ and D-		0.7	8.8	16.9	mV
Electrical Idle differential peak output voltage		2.35	4.81	9.0	mV
The amount of voltage change allowed during Receiver detection		401	460	484	mV
Tx DC common mode voltage		0.60	0.84	0.97	V
Tx short current		43.1	52.2	67.4	mA
Maximum time to transition to a valid Electrical Idle after transmitting an Electrical Idle Ordered-Set		4.4	5.2	6.4	UI
Maximum time to transition to a valid Tx specification after leaving an Electrical Idle condition		2.1	2.9	3.5	UI
Differential return loss		11.4	14.1	16.4	dB
Common mode return loss		6.5	10.2	12.3	dB
DC differential Tx impedance		95.2	107.6	116.9	Ω
Lane-to-Lane Output Skew		115	167	215	ps

Table 19-5. PCI Express AC and DC Electrical Characteristics *(Cont.)*

Item	Conditions	Min	Typ	Max	Unit
Rx I/O Characteristics					
Differential input amplitude		0.175	–	3.3	V
Jitter tolerance	Rx data input amplitude = 175 mV	Sinusoidal jitter – 0.256 UI Backplane length – 76.2 cm (30 in.)			
Rx differential return loss		15.6	19.1	21.8	dB
Rx common mode return loss		7.7	12.4	14.0	dB
DC differential input impedance		92.7	107.0	115.8	Ω
DC input impedance		45.0	53.2	57.5	Ω
Power down input impedance		361	3380	–	Ω
Electrical Idle detect threshold		61	–	173	mV

a. UI is Unit Interval. Given a data stream of a repeating pattern of alternating 1 and 0 values, the Unit Interval is the value measured by averaging the time interval between voltage transitions, over a sufficient interval of time, to make all intentional frequency modulations of the source clock negligible.

b. 150 nF AC-coupling capacitors are required only on the PEX 8112 Tx PETn0 and PETp0 balls, if standard CML Reference Clocks are used.

Figure 19-1. SIG-TEST Results

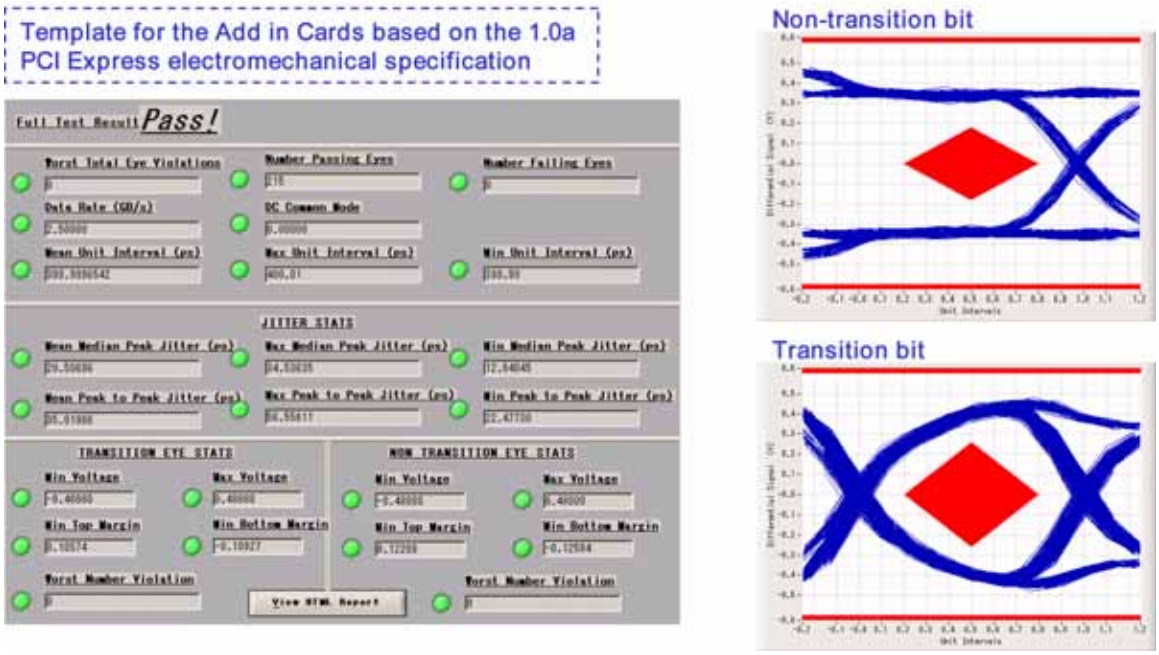
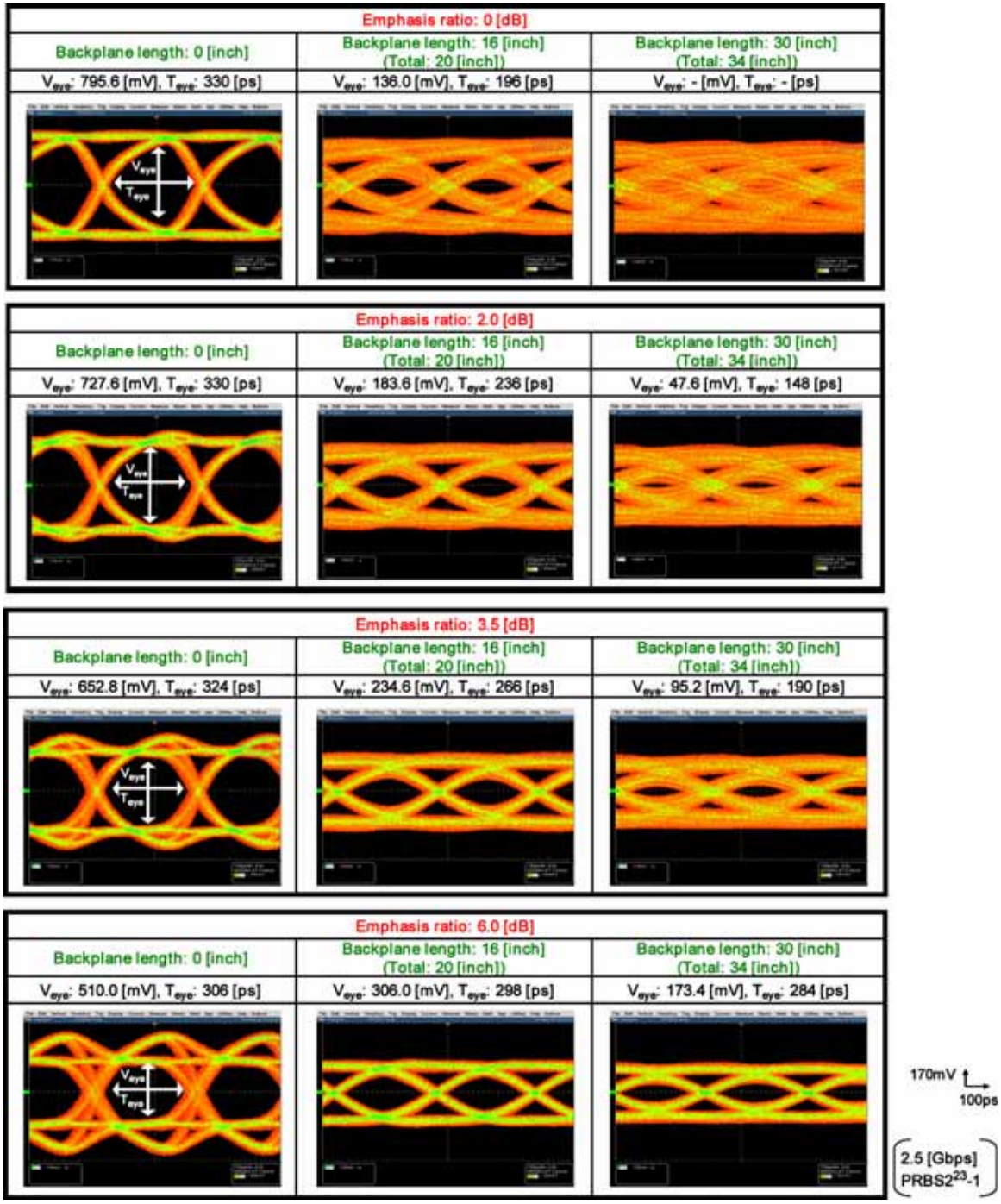


Figure 19-2. Near-End/Far-End Eye Diagram



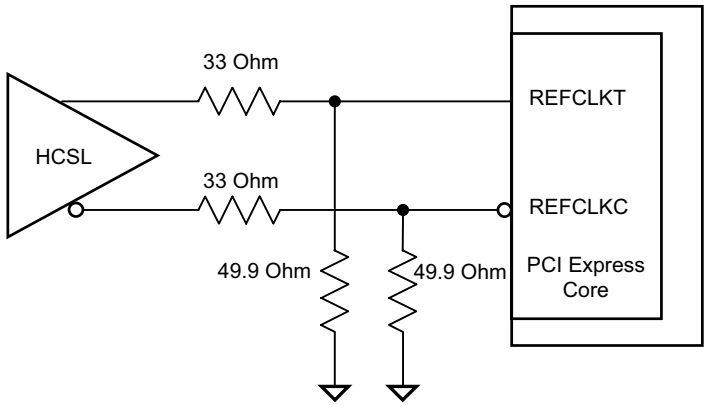
19.4.2 PCI Express REFCLK DC Specifications

Differential clock pair input (REFCLKT/C) accepts a low-jitter 100-MHz Reference Clock, which is compliant with Table 2-1, "REFCLCK DC Specifications and AC Timing Requirements," in the *PCI ExpressCard r1.0a*. (Refer to Table 19-6 and Figure 19-3.)

Table 19-6. PCI Express Reference Input DC Clock Specification

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Differential Input High Voltage		+150		mV
V_{IL}	Differential Input Low Voltage			-150	mV
V_{cross}	Absolute Crossing Point Voltage		250	+550	mV
V_{MAX}	Absolute Maximum Input Voltage			1.15	V
V_{MIN}	Absolute Minimum Input Voltage		-0.3		V
Z_{c-dc}	Clock Source DC Impedance		40	60	Ω

Figure 19-3. PCI Express Reference Clock Input Reference Diagram



When using an LVPECL or LVDS clock source, Reference Clock input must be AC-coupled. The Reference Clock Receiver has an internal biasing circuit and integrated differential termination. The Reference Clock Receiver also accepts LVPECL/LVDS clock input with AC-coupling. The recommended value for AC-coupling capacitors is 0.01 µF. (Refer to Figure 19-4 and Figure 19-5.)

When using AC-coupled Reference Clock input, the differential voltage swing must be greater than 250 mV and less than 2V.

Figure 19-4. LVPECL Clock Input Reference Diagram

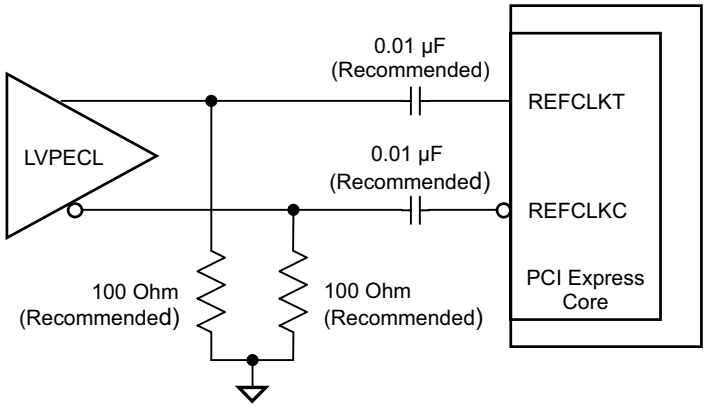
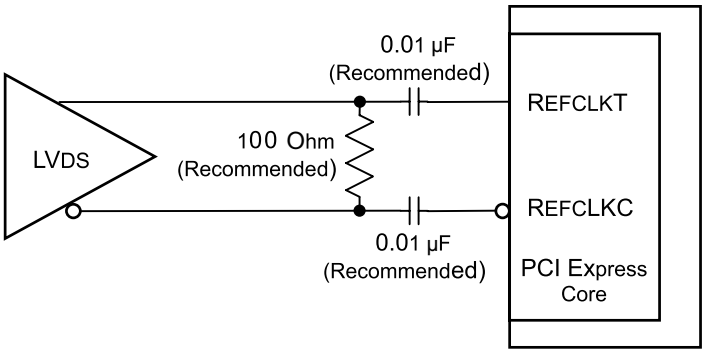


Figure 19-5. LVDS Clock Input Reference Diagram



19.4.3 PCI Express REFCLK AC Specifications

Table 19-7. PCI Express REFCLK AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PEX_REFCLK	100-MHz Differential Reference Clock Input			100		MHz
$ClkIn_{DC}$	Input Clock Duty Cycle		40	50	60	%
T_R/T_F	Input Clock Rise/Fall Times				0.2	RCUI[a]
V_{SW}	Differential Input Voltage Swing		0.6		1.6	V
R_{TERM}	Reference Clock Differential Termination			110		Ω

a. RCUI refers to the Reference Clock period (10 ns typical).

19.5 PCI Bus Specifications

19.5.1 PCI Bus DC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-8. PCI Bus DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHd}	PCI 3.3V Input High Voltage		0.5 * VDD3.3		VDD3.3	V
V_{ILd}	PCI 3.3V Input Low Voltage		0		0.7	V
V_{IH}	PCI 5.0V Input High Voltage		2.0		5.5	V
V_{IL}	PCI 5.0V Input Low Voltage		0		0.8	V
I_{IL}	Input Leakage	0V < V_{IN} < VDD5	-10		+10	µA
I_{OZ}	Hi-Z State Data Line Leakage				10	µA
V_{OH3}	PCI 3.3V Output High Voltage	I_{OUT} = -500 µA	0.9 * VDD3.3			V
V_{OL3}	PCI 3.3V Output Low Voltage	I_{OUT} = 1500 µA			0.1 * VDD3.3	V
V_{OH}	PCI 5.0V Output High Voltage	I_{OUT} = -12 mA	2.4			V
V_{OL}	PCI 5.0V Output Low Voltage	I_{OUT} = 12 mA			0.4	V
C_{IN}	Input Capacitance	Ball to GND			10	pF
C_{CLK}	CLK Ball Capacitance		5		12	pF
C_{IDSEL}	IDSEL Ball Capacitance				8	pF

19.5.2 PCI Bus 33-MHz AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-9. PCI Bus 33-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		30	∞	ns	
T_{VAL}	CLK to Signal Valid Delay – Bused Signals		2	11	ns	2, 3
T_{VAL}(ptp)	CLK to Signal Valid Delay – Point-to-Point		2	12	ns	2, 3
T_{ON}	Float to Active Delay		2		ns	7
T_{OFF}	Active to Float Delay			28	ns	7
T_{SU}	Input Setup to CLK – Bused Signals		6		ns	3, 8
T_{SU}(ptp)	Input Setup to CLK – Point-to-Point		10,12		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset Active Time after Power Stable		1		ms	5
$T_{RST-CLK}$	Reset Active Time after CLK Stable		100		µs	5
$T_{RST-OFF}$	Reset Active to Output Float Delay			40	ns	5, 6, 7
T_{RHFA}	RST# High to First Configuration Access		2^{25}		clocks	9
T_{RHFF}	RST# High to First FRAME# Assertion		5		clocks	

Notes:

2. For parts compliant to the 5V signaling environment:

Minimum times are evaluated with 0 pF equivalent load; maximum times are evaluated with 50 pF equivalent load. Actual test capacitance varies; however, results must be correlated to these specifications.

Faster buffers can exhibit ring back when attached to a 50 pF lump load but should be of no consequence when the output buffers are in full compliance with slew rate and V/I curve specifications.

For parts compliant to the 3.3V signaling environment:

Minimum times are evaluated with the same load used for slew rate measurement; maximum times are evaluated with a parallel RC load of 25Ω and 10 pF.

3. REQ# and GNT# are point-to-point signals and have different output valid delay and input setup times than bused signals. The setup for REQ# is 12. The setup for GNT# is 10. All other signals are bused.

5. CLK is stable when it meets the PCI CLK specifications. RST# is asserted and de-asserted asynchronously with respect to CLK.

6. All output drivers must be asynchronously floated when RST# is active.

7. For Active/Float timing measurement purposes, the Hi-Z or "off" state is defined as "total current delivered through the PEX 8112 ball is less than or equal to the leakage current specification."

8. Setup time applies only when the device is not driving the ball. Devices cannot drive and receive signals at the same time.

9. At 33 MHz, the PEX 8112 must be ready to accept a Configuration access within 1s after RST# is High.

19.5.3 PCI Bus 66-MHz AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-10. PCI Bus 66-MHz AC Specifications

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
T_{CYC}	PCI CLK Cycle Time		15	∞	ns	
T_{VAL}	CLK to Signal Valid Delay – Bused Signals		2	6	ns	3, 8
T_{VAL}(ptp)	CLK to Signal Valid Delay – Point-to-Point		2	6	ns	3, 8
T_{ON}	Float to Active Delay		2		ns	8, 9
T_{OFF}	Active to Float Delay			14	ns	9
T_{SU}	Input Setup to CLK – Bused Signals		3		ns	3, 10
T_{SU}(ptp)	Input Setup to CLK – Point-to-Point		5		ns	3
T_H	Input Hold from CLK		0		ns	
T_{RST}	Reset Active Time after Power Stable		1		ms	5
$T_{RST-CLK}$	Reset Active Time after CLK Stable		100		µs	5
$T_{RST-OFF}$	Reset Active to Output Float Delay			40	ns	5, 6
T_{RHFA}	RST# High to First Configuration Access		2^{25}		clocks	9
T_{RHFF}	RST# High to First FRAME# Assertion		5		clocks	

Notes:

3. REQ# and GNT# are point-to-point signals and have different input setup times than bused signals. The setup for REQ# and GNT# is 5 ns at 66 MHz. All other signals are bused.

5. When M66EN is asserted, CLK is stable when it meets the PCI r3.0, Section 7.6.4.1, requirements. RST# is asserted and de-asserted asynchronously with respect to CLK. Refer to the PCI r3.0, Section 4.3.2, for further details.

6. All output drivers must be floated when RST# is active.

8. When M66EN is asserted, the minimum specification for Tval(min), Tval(ptp)(min), and Ton are reduced to 1 ns when a mechanism is provided to guarantee a minimum value of 2 ns when M66EN is de-asserted.

9. For Active/Float timing measurement purposes, the Hi-Z or "off" state is defined as "total current delivered through the PEX 8112 ball is less than or equal to the leakage current specification."

10. Setup time applies only when the device is not driving the signal. Devices cannot drive and receive signals at the same time. Refer to the PCI r3.0, Section 3.10, item 9, for further details.

19.6 Serial EEPROM Specifications

19.6.1 Serial EEPROM DC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-11. Serial EEPROM DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		2.0		VDD3.3	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 0 mA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = 0 mA	VDD3.3 -0.1			V
I_{IL}	Input Leakage[a]	0V < V_{IN} < VDD3.3	-10		+10	µA
I_{OZ}	Hi-Z State Leakage[a]	V_{OUT} = VDD3.3 or GND			±10	µA
I_{OL}	Output Current, Low[a]	V_{OL} = 0.4V		+3.0		mA
I_{OH}	Output Current, High[a]	V_{OH} = 2.4V		-3.0	11.0[b]	mA
C_{IN}	Input Capacitance[c]	Ball to GND	2.9		4.9	pF

a. The (+) sign indicates current flowing into the device, and the (-) sign indicates current flowing out of the device.

b. Absolute maximum drive strength value for EECLK, EECS#, and EEWRDATA. Damage may occur if the absolute maximum rating is exceeded, even momentarily. Operating conditions must ensure that the absolute maximum drive strength is not exceeded.

c. VDD3.3 = 0V, T_J = 25°C, f = 1 MHz

19.6.2 Serial EEPROM AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

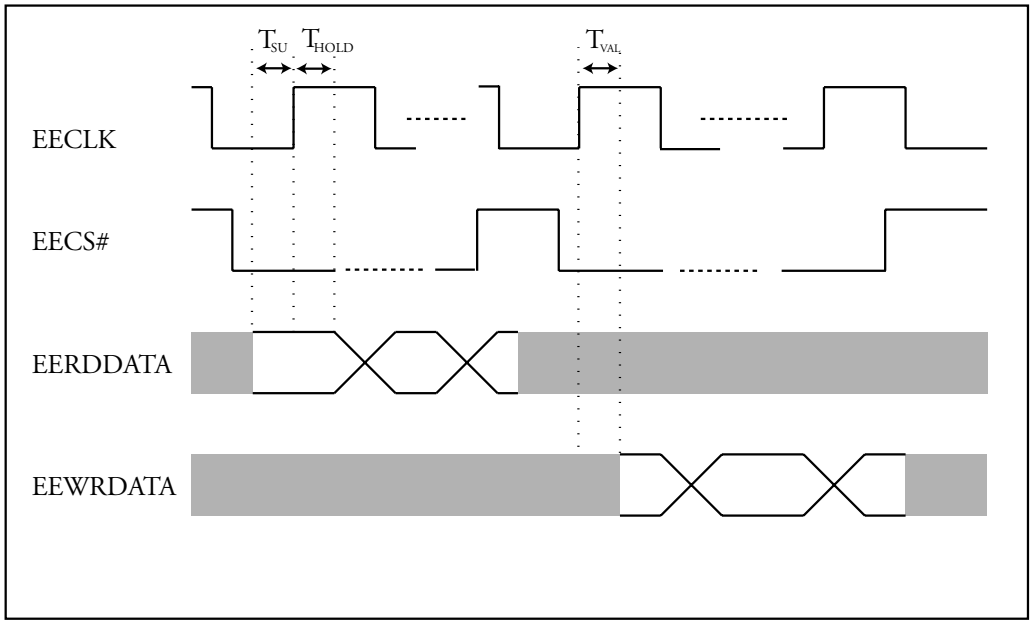
Figure 19-6 illustrates the timing relationship between EECLK, EECS#, EERDDATA, and EEWRDATA. Table 19-12 provides specific timing values relative to Figure 19-6.

Table 19-12. Serial EEPROM AC Specifications

Symbol	Parameter	Min	Max	Unit	Comment
T_{CYC}	EECLK Cycle Time	40		ns	25 MHz maximum
T_{VAL}	EECLK to Output Signal Valid	9.9	10.0	ns	Applies to EEWRDATA
T_{SU}	Input Setup to EECLK	7.7		ns	Applies to EERDDATA
T_{HOLD}	Hold Time of Input after EECLK		8.3	ns	Applies to EERDDATA

Note: *EECS# is asynchronous to EECLK, and must be asserted before accesses to the serial EEPROM are allowed.*

Figure 19-6. Serial EEPROM Timing Diagram



19.7 GPIO Specifications

19.7.1 GPIO DC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

Table 19-13. GPIO DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		2.0		VDD3.3	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 0 mA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = 0 mA	VDD3.3 -0.1			V
I_{IL}	Input Leakage	0V < V_{IN} < VDD3.3	-10		+10	µA
I_{OZ}	Hi-Z State Leakage	V_{OUT} = VDD3.3 or GND			±10	µA
I_{OL}	Output Current, Low[a]	V_{OL} = 0.4V		+12.0		mA
I_{OH}	Output Current, High[a]	V_{OH} = 2.4V		-12.0	-45[b]	mA
C_{IN}	Input Capacitance[c]	Ball to GND	2.9		4.9	pF

a. The (+) sign indicates current flowing into the device, and the (-) sign indicates current flowing out of the device.

b. Absolute maximum drive strength value for GPIO outputs. Damage can occur if the absolute maximum rating is exceeded, even momentarily. Operating conditions must ensure that the absolute maximum drive strength is not exceeded.

c. VDD3.3 = 0V, T_J = 25°C, f = 1 MHz

19.7.2 GPIO AC Specifications

Operating Conditions – VDD1.5 = 1.5V ±0.1V, VDD3.3 = 3.3V ±0.3V, T_A = -40 to +85°C

Typical Values – VDD1.5 = 1.5V, VDD3.3 = 3.3V, T_A = 25°C

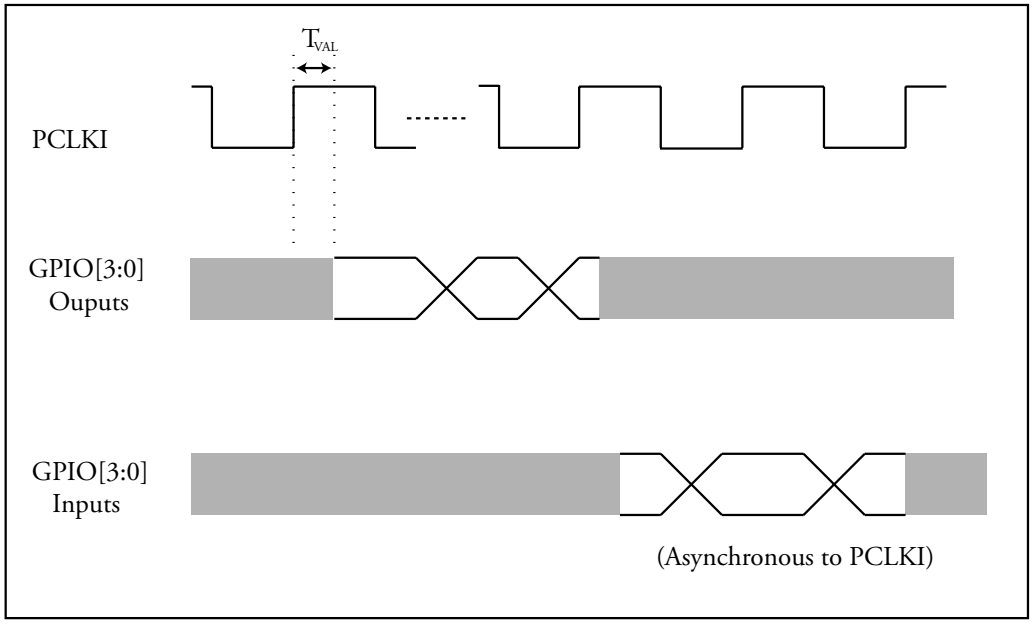
Figure 19-7 illustrates the timing relationship between PCLKI and GPIO[3:0]. Table 19-14 provides specific timing values relative to Figure 19-7.

Table 19-14. GPIO AC Specifications

Symbol	Parameter	Signal	Min	Max	Unit
T_{VAL}	PCLKI to Output Signal Valid	GPIO0	2.4	6.8	ns
		GPIO1	2.5	6.9	ns
		GPIO2	2.6	7.6	ns
		GPIO3	2.5	7.1	ns

Note: *Timing values relative to PCLKI. However, GPIO input can be asynchronous to PCLKI. To guarantee functionality, GPIO input must be asserted for at least one PCLKI period.*

Figure 19-7. GPIO Timing Diagram



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Chapter 20 Thermal and Mechanical Specifications

20.1 Introduction

The PEX 8112 is offered in two package types:

- 144-ball, 13 x 13 mm^2 PBGA (Plastic BGA) package
- 161-ball, 10 x 10 mm^2 FBGA (Fine-Pitch BGA) package

20.2 Thermal Characteristics

Maximum Junction Temperature – 125°C

Table 20-1. Thermal Resistance

Package	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)			
	0 m/s	0 m/s	1 m/s	2 m/s	3 m/s
144-Ball PBGA	11.06	33.07	28.45	26.94	25.90
161-Ball FBGA	11.05	45.71	39.35	36.67	34.78

20.3 Mechanical Specifications

20.3.1 144-Ball PBGA

20.3.1.1 General 144-Ball PBGA Specifications

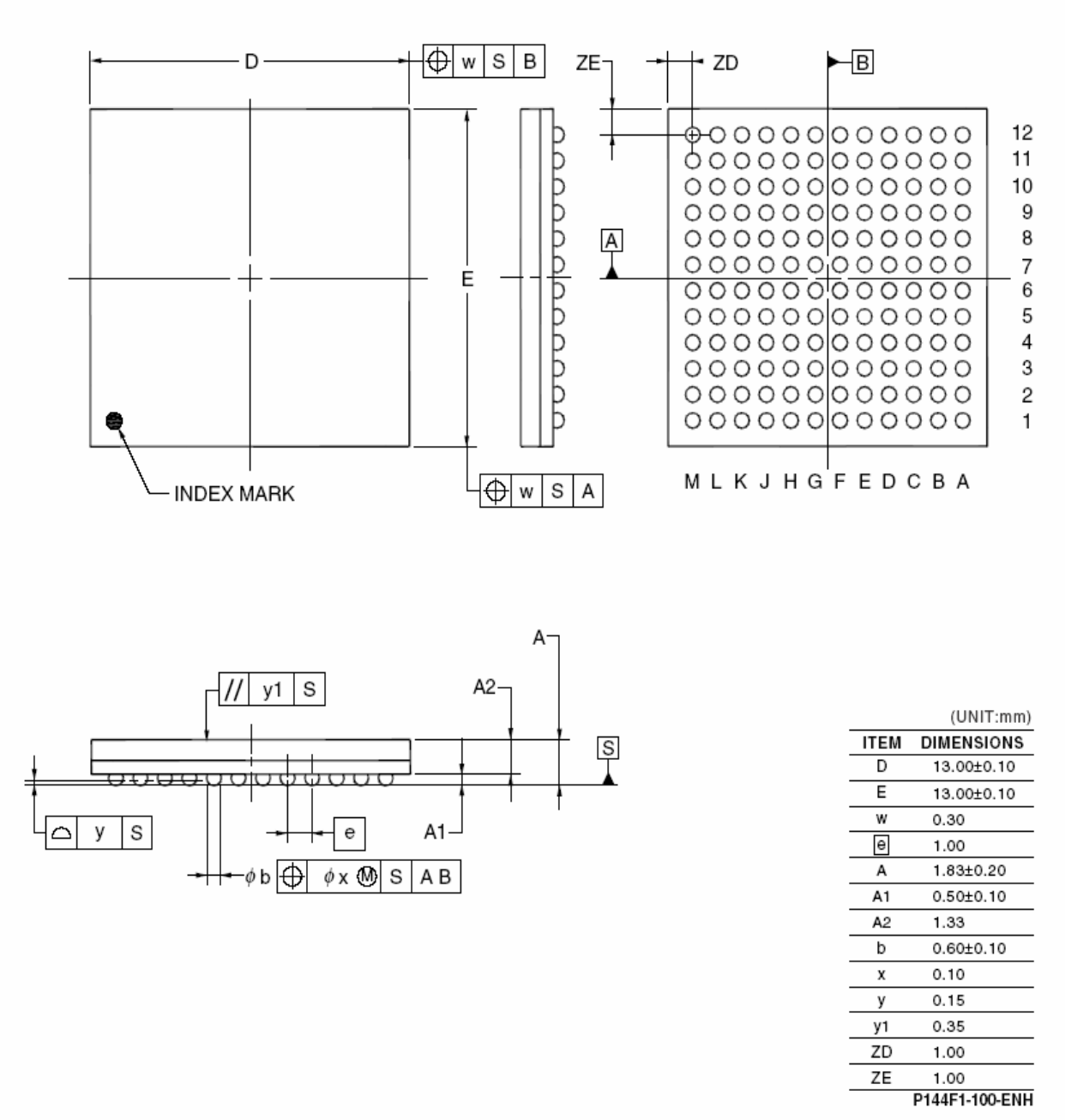
Table 20-2 lists general package specifications. For a more complete list, refer to Figure 20-1.

Table 20-2. General PBGA Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Number of Balls	144
Package Dimensions	13 x 13 mm^2 (approximately 1.83-mm high)
Ball matrix pattern	12 x 12
Ball pitch	1.00 mm
Ball diameter	0.60 ±0.10 mm
Ball spacing	0.40 mm

20.3.1.2 144-Ball PBGA Mechanical Dimensions

Figure 20-1. 144-Ball PBGA Mechanical Dimensions



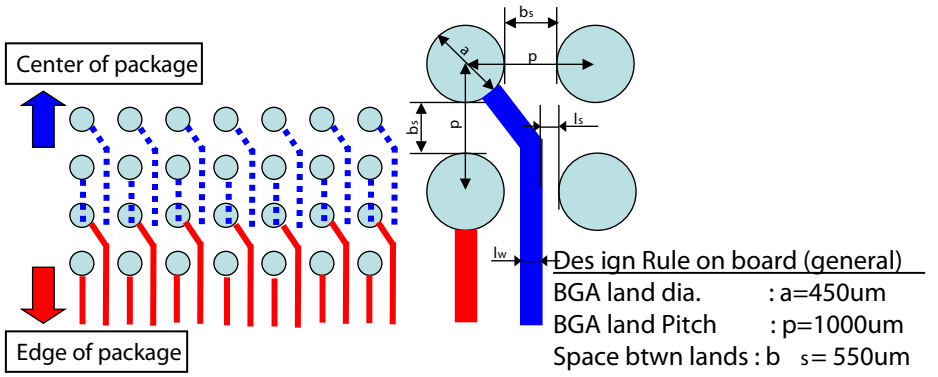
(UNIT:mm)

ITEM	DIMENSIONS
D	13.00±0.10
E	13.00±0.10
w	0.30
e	1.00
A	1.83±0.20
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P144F1-100-ENH

20.3.1.3 144-Ball PBGA PCB Layout

Figure 20-2. 144-Ball PBGA PCB Layout



Red : traces on an upper signal layer for the PCB
Blue : traces on a lower signal layer for PCB

2 signal layers are required due to routing only one trace between BGA lands.

Note: *Refer to the PLX PEX 8112 AA Schematic Design Checklist Application Note for the trace lengths and a detailed description of the PCI Express layout considerations.*

20.3.2 161-Ball FBGA

20.3.2.1 General 161-Ball FBGA Specifications

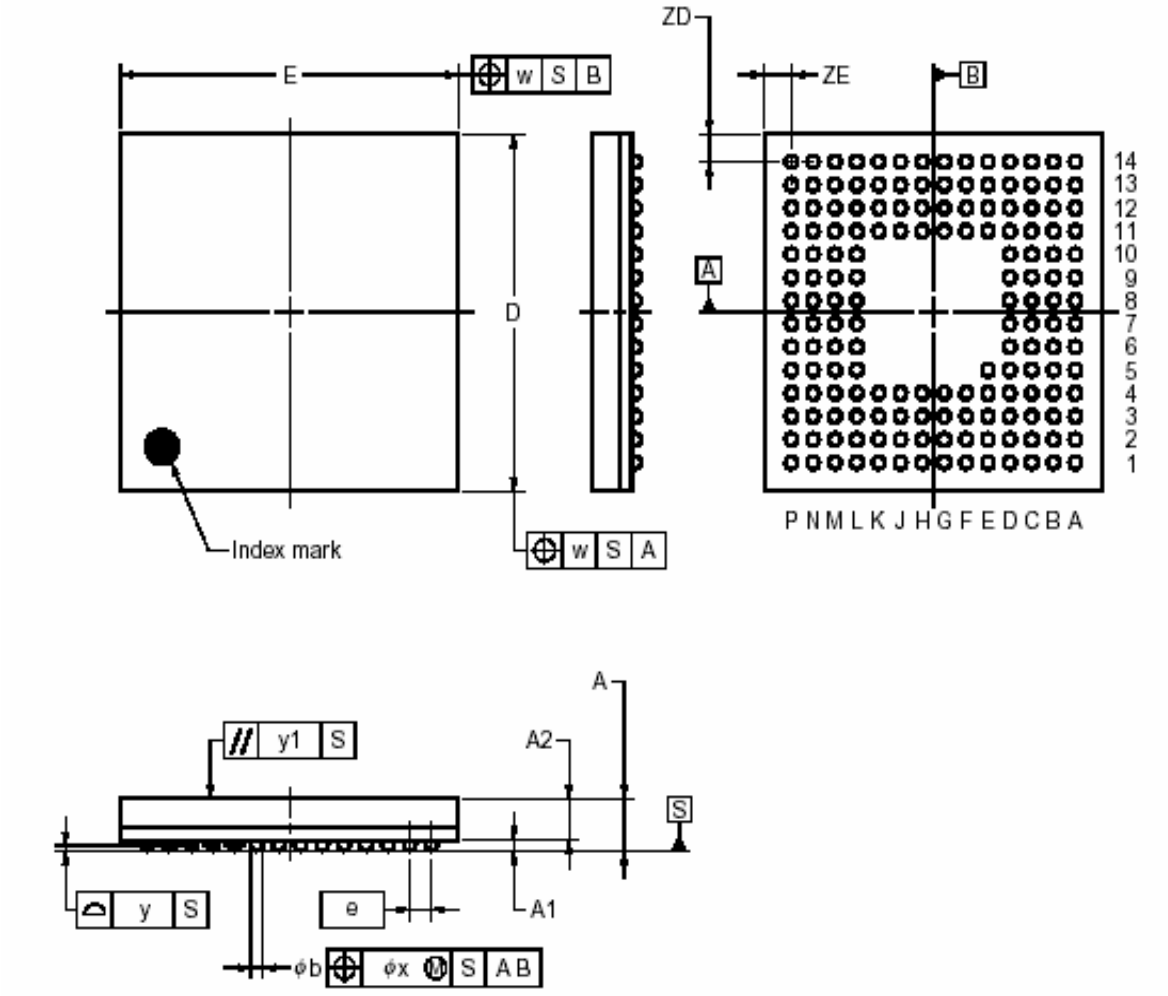
Table 20-3 lists general package specifications. For a more complete list, refer to Figure 20-3.

Table 20-3. General FBGA Specifications

Parameter	Specification
Package Type	Fine-Pitch Ball Grid Array (FBGA)
Number of Balls	161
Package Dimensions	10 x 10 mm^2 (approximately 1.43-mm high)
Ball matrix pattern	9 x 9
Ball pitch	0.65 mm
Ball diameter	0.40 ±0.05 mm
Ball spacing	0.25 mm

20.3.2.2 161-Ball FBGA Mechanical Dimensions

Figure 20-3. 161-Ball FBGA Mechanical Dimensions

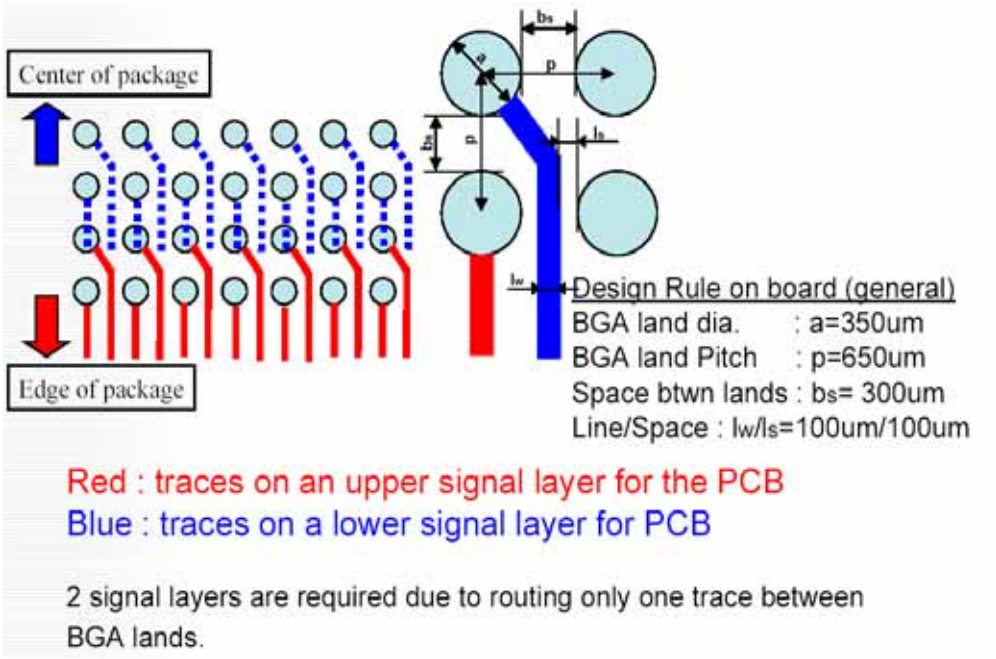


ITEM	MILLIMETERS
D	10.00±0.10
E	10.00±0.10
w	0.20
A	1.43±0.10
A1	0.30±0.05
A2	1.13
e	0.65
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.775
ZE	0.775

P161F1-65-DA1

20.3.2.3 161-Ball FBGA PCB Layout

Figure 20-4. 161-Ball FBGA PCB Layout



Note: *Refer to the PLX PEX 8112 AA Schematic Design Checklist Application Note for the trace lengths and a detailed description of the PCI Express layout considerations.*

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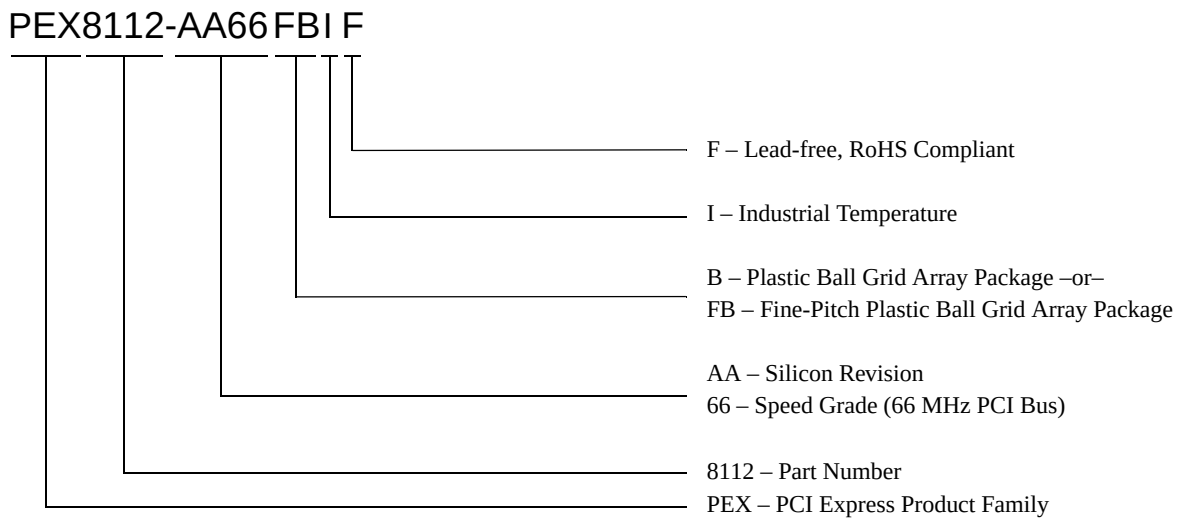
Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1. Product Ordering Information

Part Number	Description
PEX8112-AA66BI	PEX 8112 PCI Express-to-PCI Bridge, Standard BGA (144-Ball, 13 x 13 mm^2) Leaded Package
PEX8112-AA66BI F	PEX 8112 PCI Express-to-PCI Bridge, Standard BGA (144-Ball, 13 x 13 mm^2) Lead Free Package
PEX8112-AA66FBI F	PEX 8112 PCI Express-to-PCI Bridge, Fine-Pitch BGA (161-Ball, 10 x 10 mm^2) Lead Free Package
PEX 8112-AA RDK-F	PEX 8112 Forward Bridge Rapid Development Kit
PEX 8112-AA RDK-R	PEX 8112 Reverse Bridge Rapid Development Kit



A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support, or call 800 759-3735 (domestic only) or 408 774-9060.