AFCT-57V6NSZ

Small Form Factor Pluggable (SFP) LC Optical Transceiver for 1.25GBd Ethernet at Extended Link Lengths (Up to 40km)

AVAGO TECHNOLOGIES

Data Sheet

Description

The AFCT-57V6NSZ transceiver is a specially customised low-cost and hot-pluggable SFP MSA-compliant optical interconnect module for Gigabit Ethernet applications at transmission distances up to 40km [1, 2].

The AFCT-57V6NSZ implements the serial portion of the physical layer, and supports the features shown below The AFCT-57V6NSZ features differential serial I/O interface lines that are AC-coupled signals. Avago's design of the long wavelength SFP module uses a 1550 nm distributed feedback (DFB) laser diode (LD) and takes advantage of an integrated preamplifier/photo-detector. The AFCT-57V6NSZ also contains transmitter, receiver and control electronics.

Singlemode optical fiber, with LC connectors, is recommended as the communication media. The AFCT-57V6NSZ has a digital diagnostic monitoring (DDM) function in accordance with SFF-8472 [3] which allows monitoring operating temperature, supply voltage, laser bias current, transmitter optical output power and optical received power in real time via a serial-ID interface.

On the following page, Table1 lists the general specifications for the AFCT-57V6NSZ SFP.

Figure 1 shows a simplified block diagram of the AFCT-57V6NSZ electronics.

Related Products

- AFBR-5715Z family:
  850 nm 1.25 GBd 3.3 V multimode SFP Gigabit Ethernet transceivers with DMI
- AFCT-5715Z:
  1.25 GBd Ethernet (1000Base-LX) SFP with DMI

Features

- Gigabit Ethernet transceiver
- RoHS Compliant
- IEEE 802.3z, 1000BASE-ZX
- Extended transmission distance up to 40 km
- Compliant with SFP Multi Source Agreement (MSA)
- Duplex-LC optical interface
- 1550 nm DFB-LD
- Serial ID
- Digital Diagnostic Monitoring interface
- Bail delatch for easy removal from cage
- Available in industrial temperature range (-40 to +85°C)
- Immune to ESD, RF fields, and Vcc noise
- Designed for very low RF emissions
- Class 1 laser safety
- AC-coupled differential serial I/O interface
- Single +3.3 Volt supply operation
- Low power dissipation

Applications

- Ethernet switches
- Multi-service switches and routers
- Broadband aggregation and wireless infrastructure
- Switched backplane applications
- High Speed Interface for server farms
- Metro access switch GbE connections

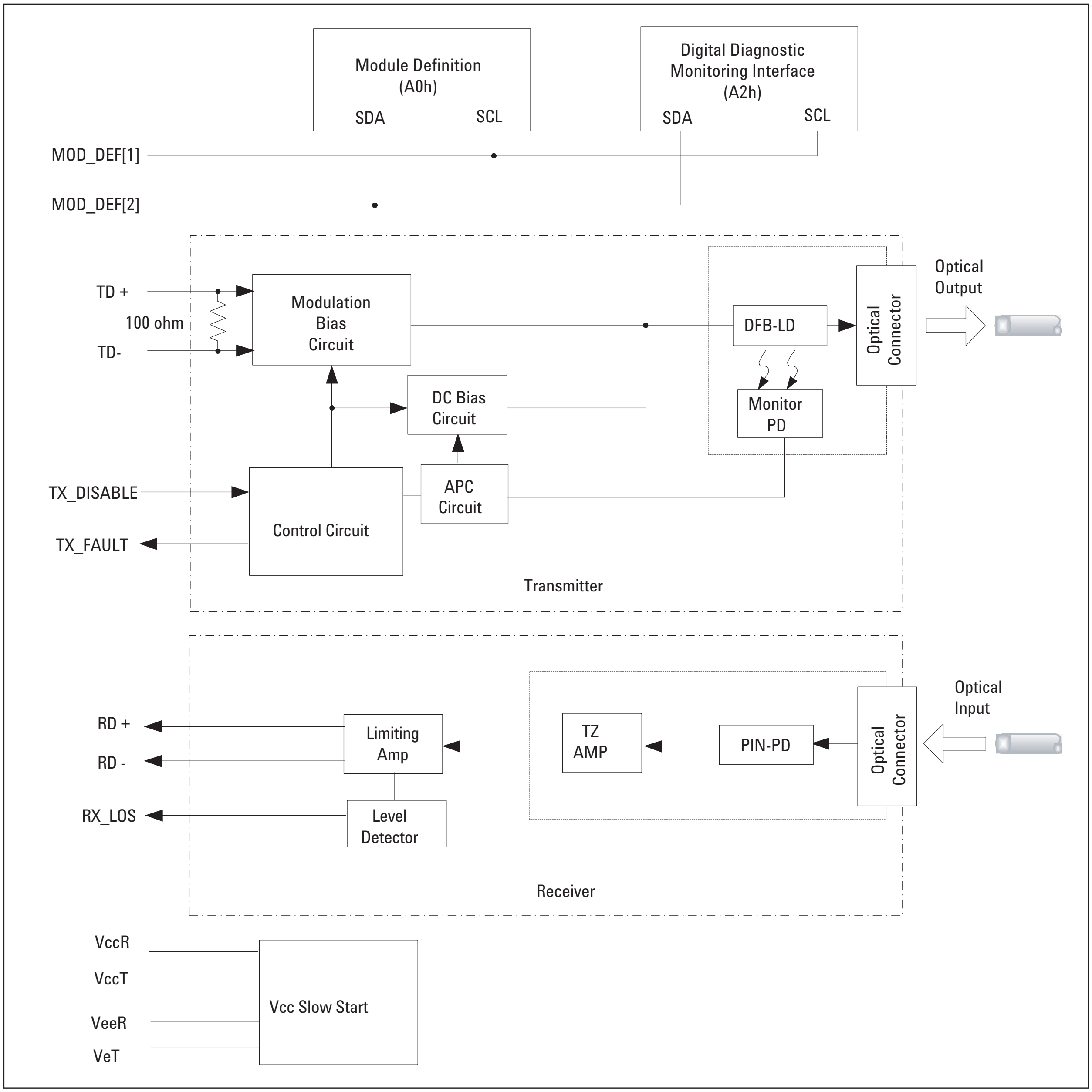


Figure 1. AFCT-57V6NSZ Simplified Block Diagram

Table 1. General AFCT-57V6NSZ Specifications

Parameter	1000BASE-ZX*	unit
Nominal Bit Rate	1.25	Gbps
Link Loss Budget	17	dB
Minimum Required Link Loss	0	dB
Bit Error Ratio(BER)	$<10^{-12}$	-
Fiber Core Diameter	9	μm
Operating Range(max)	40	km

† Optical specifications are modified to realize 40 km transmission in singlemode fiber.

Absolute Maximum Ratings

Operation of the AFCT-57V6NSZ beyond the Absolute Maximum Ratings listed in Table 2 can degrade or damage the product. With the exception of laser safety, it is not implied that the product will function above the Recommended Operating Conditions. It is possible to reduce the reliability and lifetime of the device if the Recommended Operating Conditions are exceeded (see Table 3).

Recommended Operating Conditions

Table 3 lists the conditions under which the AFCT-57V6NSZ is tested and should be operated. It is possible to reduce the reliability and lifetime of the device if these ratings are exceeded for extended periods. Functional operation should be restricted to these Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	4.0	V
Relative Humidity *	RH	5	85	%
TX_DISABLE Input Voltage	VIN	-0.5	Vcc+0.5	V
Storage Temperature	Ts	-40	+85	°C

† No condensation

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Ripple And Noise	-	-	-	100	mVp-p
Operating Case Temperature					
AFCT-57V6NSZ	T_C	-5	-	70	°C
AFCT-57V6ANSZ	T_C	-40	-	85	

† Measured with a sinusoidal signal from 100 Hz to 2 MHz at the input of the recommended power supply filter shown in Figure 13.

Handling Precautions

Avago advises that precautions be taken to avoid electrostatic discharge (ESD) during handling, assembly, and testing of the AFCT-57V6NSZ. Degradation or damage can occur if proper guidelines for handling ESD sensitive devices are not followed. This could result in an inoperable device or unsafe operation as described above.

In particular, avoid getting particulate or solvent contamination onto the optical surfaces of the laser and photodetector assemblies. It is also strongly recommended that the LC connector receptacle be covered when not in use. Excessive force when installing and extracting the AFCT-57V6NSZ should be avoided. Refer to the SFP Application Note [6] for additional handling information.

Optical Description

Table 4 describes the performance of the transmitter portion of the AFCT-57V6NSZ over the operating conditions. Table 5 describes the performance of the receiver portion of the AFCT-57V6NSZ over the operating conditions.

The optical pulse characteristics of the transmitter are specified in the form of an eye pattern. When measured in accordance with [2], the mask shown in Figure 2 evaluates rise time, fall time, overshoot and undershoot.

Table 4. Transmitter Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Spectral Center Wavelength	λ_C	1500	1550	1580	nm
-20dB Spectral Width	$\Delta\lambda_{20}$	-	-	0.5	nm
Side Mode Suppression Ratio	SMSR	30	-	-	dB
Optical Output Power, Average*	P_O	-4	-	0	dBm
Extinction Ratio	ER	9	-	-	dB
Rise/Fall Time**	Tr/Tf	-	-	260	ps
Total Jitter (TJ)	TJ	-	-	0.28	UI
Optical Waveform	-	Compliant with IEEE 802.3z eye mask (Refer to Figure 2)			-
Disable Optical Output Power	-	-	-	-35	dBm

† SMF 9/125
†† 20 % - 80 % edge rate without filter

Table 5. Receiver Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Spectral Center Wavelength	λ_C	1270	-	1600	nm
Receiver Saturation	Pmax	0	-	.	dBm
Minimum Receiver Sensitivity	Pmin	.	-	-21	dBm
RX_LOS Assert Level	LOS_A	-35	-	.	dBm
RX_LOS De-assert Level	LOS_D	.	-	-24.5	dBm
RX_LOS Hysteresis	LOS_{HYS}	0.5	2	.	dB
Return Loss	RL	12	-	.	dB

† Receiver sensitivity is measured at the center of the eye for BER=1x10-12 using PRBS 2^7-1

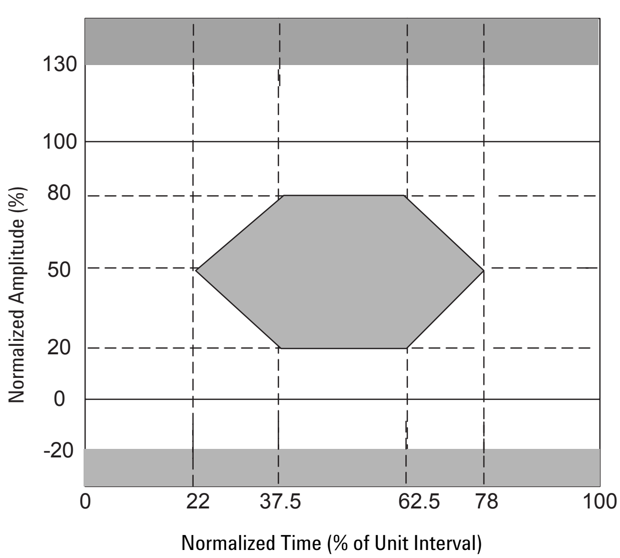


Figure 2. Transmitter Eye Mask

Electrical Description

The supply current of the AFCT-57V6NSZ is described in Table 6 below. The inrush current is defined as the additional inrush due to hot plugging.

The characteristics for the control and status signals are shown in Table 7. Output status signals, TX_FAULT and RX_LOS, are all open-collector/drain, and the levels indicated assuming 4.7k-10k ohm pull-up resistor to Host_Vcc is present. The levels of MOD_DEF[1] and MOD_DEF[2] are also indicated assuming that they are pulled up with a 4.7k-10k ohm resistor to +3.3 V on host board. Table 8 indicates the voltage levels required to be delivered by the host to the transmitter differential serial data input TD+/-. Table 9 indicates the voltage level output from the receiver differential serial data output RD+/-.

Table 6. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	-	-	300	mA
Inrush Current*	Linrush	-	-	30	mA

† greater than the steady state value

Table 7. Control/Status Signal Characteristics

Parameter	Symbol	Min	Max	Unit
TX_DISABLE Input Voltage - High	V_{IH}	2.0	VccT	V
TX_DISABLE Input Voltage - Low	V_{IL}	0	0.8	V
TX_FAULT Output Voltage - High	V_{OH}	Host_Vcc-0.5	Host_Vcc	V
TX_FAULT Output Voltage - Low	V_{OL}	0	0.4	V
RX_LOS Output Voltage – High	V_{OH}	Host_Vcc-0.5	Host_Vcc	V
RX_LOS Output Voltage – Low	V_{OL}	0	0.4	V
MOD_DEF[2] (SDA) Output Voltage – Low	V_{OL}	.	0.4	V
MOD_DEF[1] (SCL) Input Voltage – High	V_{IH}	VccT, (VccR) x 0.7	.	V
MOD_DEF[1] (SCL) Input Voltage – Low	V_{IL}	-	VccT(VccR) x 0.3	V

Table 8. TD+/- Input Signal Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Input Amplitude, Differential	V_I	200	.	2400	mV p-p
Input Impedance, Differential	R_I	.	100	.	Ω
Deterministic Jitter	DJ	.	.	0.10	UI
Total Jitter ††	TJ	.	.	0.24	UI
Mark Ratio	.	.	50	.	%

† AC-coupled.
†† TJ = RJ + DJ. At BER = 10-12

Table 9. RD+/- Output Signal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Output Amplitude, Differential*	V_O	600	-	1200	mVp-p
Output Impedance, Differential	R_O	-	100	-	Ω

† AC-coupled.

Pin Description

A brief description of all of the electrical connector pins follows. The connector has staged contacts, so that hot-plugging can be performed. See Table 10.

Table 10. Pinout

Pin No.	Sequence	Description
1	1	VeeT
2	3	TX_FAULT
3	3	TX_DISABLE
4	3	MOD_DEF[2]
5	3	MOD_DEF[1]
6	3	MOD_DEF[0]
7	3	RATE_SELECT
8	3	RX_LOS
9	1	VeeR
10	1	VeeR

Pin No	Sequence	Description
11	1	VeeR
12	3	RD-
13	3	RD+
14	1	VeeR
15	2	VccR
16	2	VccT
17	1	VeeT
18	3	TD+
19	3	TD-
20	1	VeeT

Hot-Plugging Sequence

The ground, VCC and other pins designated as the sequence (1) pins engage first during hot-plugging. The sequence (2) pins connect second during hot-plugging followed by the sequence (3) pins. Conversely, when the module is unplugged from the host system, the sequence (3) pins disengages before the sequence (2) pins disengages and then followed by the sequence (1) pins. Inserting or removing the AFCT-57V6NSZ will disrupt data transmission. This disruption occurs when the downstream receiver (e.g. deserializer phase-lock-loop) resynchronizes to a different bitstream signal. When this occurs, the downstream system will recognize the associated error (e.g. comma detect, loss-of-light, disparity, CRC, and frame errors).

It is the responsibility of the system integrator to assure that no thermal, energy, or voltage hazard exists during the hot-plug-unplug sequence. It is also the responsibility of the system integrator and end-user to minimize static electricity and the probability of ESD events by careful design.

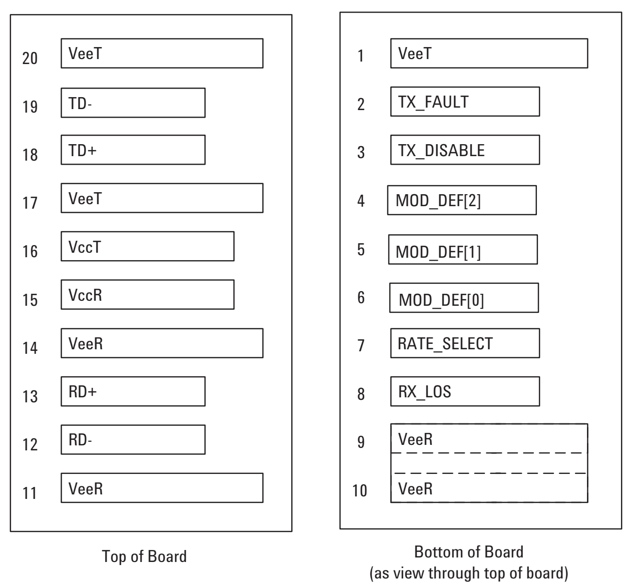


Figure 3. SFP Transceiver Electrical Pad Layout

Pin Definitions

TD+/TD- Transmit Data In and Inverted Transmit Data In are differential input to the transmitter. They are internally AC-coupled into an equivalent load of RI differential, as shown in Figure 13.

TX_DISABLE Active high TTL input, with internal 10kΩ pull-up resistor to Vcc.

Asserting the transmitter disable will deactivate the laser within the assert time. The truth table shown describes the state of the module, and Table 11 indicates the timing of TX_DISABLE.

RD+/RD- Received Data Out and Inverted Received Data Out are differential serial output from the receiver. These are AC-coupled 100 ohm differential lines which should be terminated with a 100 ohm (differential) at the user SERDES, as shown in Figure 13. AC coupling is done inside the module and is thus not required on the host board.

RX_LOS Active high open collector/drain output which indicates a loss-of-signal condition (LOS). When the average optical power received by the module is below the Assert Level, RX_LOS is indicated according to the truth table below, and Table 11 indicates the timing of RX_LOS. RX_LOS requires a 4.7k-10k ohm pull-up resistor external to the module, i.e., in the host system Host_Vcc, as shown in Figure 13. The pull-up voltage is between 2.0 V and VccR(VccT) + 0.3 V.

RATE_SELECT Not Connected.

TX_FAULT Active high open collector/drain output which indicates a fault in the module.

This can be (1) failure of the laser driver or (2) end-of-life of the laser. Under these conditions, the laser will be deactivated within the assert time. TX_FAULT also requires a 4.7k-10k ohm pull-up resistor external to the module, i.e. in the host system Host_Vcc, as shown in Figure 13. The pull-up voltage is between 2.0 V and VccT(VccR) + 0.3 V. Conditions (1) and (2) are latched, and for diagnostic purposes only, may be reset by toggling TX_DISABLE high for at least t_reset. See Table 11 and Figure 8.

MOD_DEF[0:2] The AFCT-57V6NSZ has a serial ID function which provides information about the transceiver's capabilities, standard interfaces, manufacturer and other information, and has a digital diagnostic monitoring function, per SFF-8472 [3], which allows monitoring operating temperature, supply voltage, laser bias current, transmitter optical output power and optical received power in real time. These functions are provided via a two wire serial EEPROM interface.

MOD_DEF[0] is connected to ground inside the module. MOD_DEF[1] is the serial clock signal input. MOD_DEF[2] is the data output/input.

Timing Characteristics of Control and Status I/O

The timing characteristics of the control and status line are listed in Table 11 and Figure 4 to 10.

Table 11. Timing Characteristics of Control and Status I/O

Parameter	Symbol	Min	Max	Unit	Condition
TX_DISABLE Assert Time	t_off	-	10	µs	Time from rising edge of TX_DISABLE to when the optical output falls below 10 % of nominal
TX_DISABLE Negate Time	t_on	-	1	ms	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal
Time to Initialize, including reset of TX_FAULT	t_init	-	300	ms	From power on or negation of TX_FAULT using TX_DISABLE
TX_FAULT Assert Time	T_fault	-	100	µs	Time from fault to TX_FAULT on
TX_DISABLE to Reset	T_reset	10	-	µs	Time TX_DISABLE must be held high to reset TX_FAULT
RX_LOS Assert Time	t_losson	-	100	µs	Time from LOS state to RX_LOS Assert
RX_LOS Negate Time	t_lossoff	-	100	µs	Time from non-LOS state to RX_LOS deassert
Serial ID Clock Rate	F_clock	-	100	kHz	-

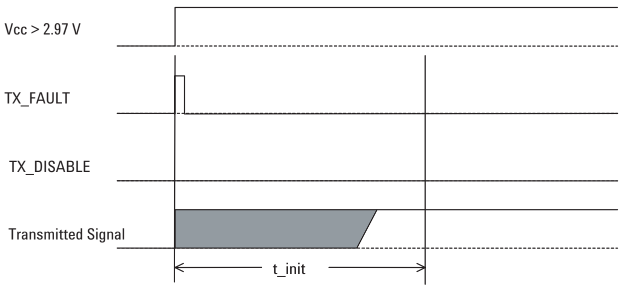


Figure 4. Power on initialization of SFP transceiver, TX_DISABLE negated

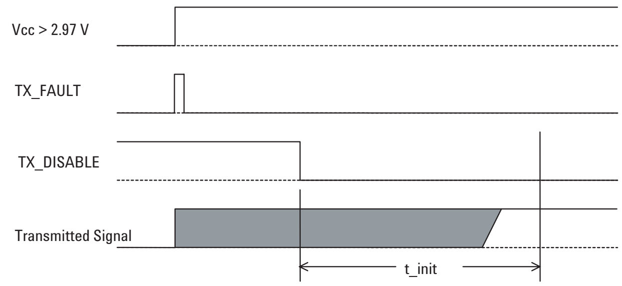


Figure 5. Power on initialization of SFP transceiver, TX_DISABLE asserted

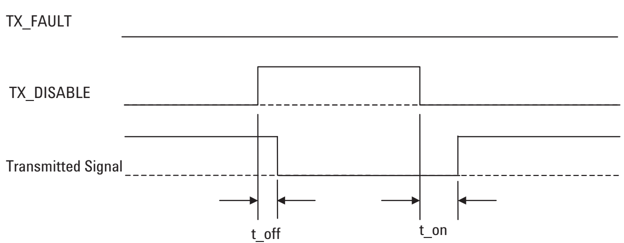


Figure 6. SFP TX_DISABLE timing during normal operation

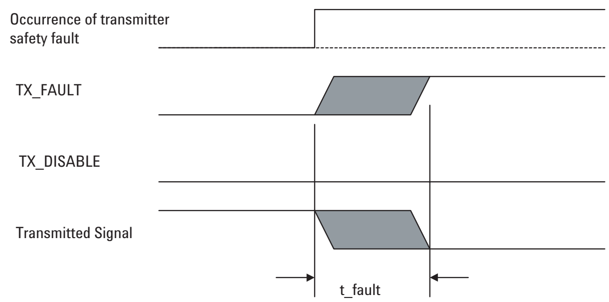


Figure 7. Detection of transmitter safety fault condition

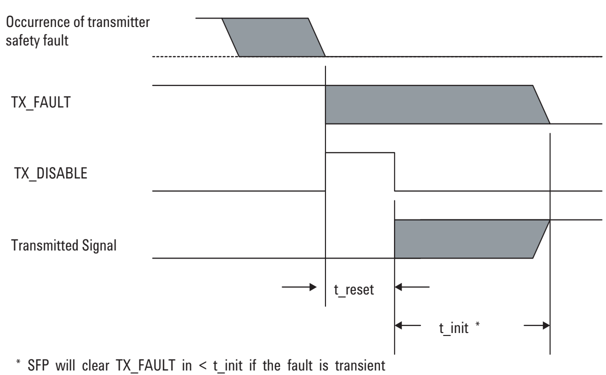


Figure 8. Successful recovery from transient safety fault condition

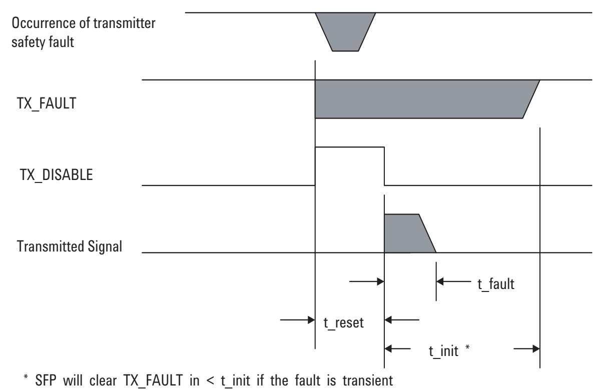


Figure 9. Unsuccessful recovery from safety fault condition

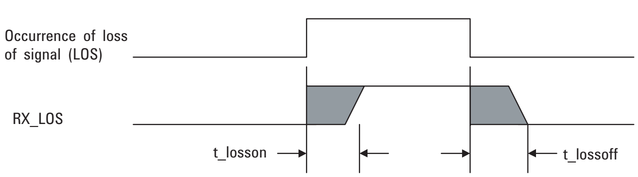


Figure 10. Timing of RX_LOS detection

Serial Identification

The serial identification (ID) at 2 wire serial bus address 1010000X (A0h) provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information. The serial interface uses the 2-wire serial CMOS E2PROM protocol defined for the ATMEL AT24C01A/02/04 family of components or equivalent components. The information obtained from the AFCT-57V6NSZ via the serial ID is shown in Table 12.

Table 12. Serial ID: Data Fields - 2-Wire Address A0h

BASE ID FIELDS				
Data Address	**Field Size (Byte)**	**Name of field**	**Description of Field**	**Context (Hex)**
0	1	Identifier	SFP	03h
1	1	Ext. Identifier	SFP	04h
2	1	Connector	LC	07h
3	8	Transceiver	——————	00h
4			——————	00h
5			——————	00h
6			1000BASE-LX	02h
7			——————	00h
8			——————	00h
9			——————	00h
10			——————	00h
11	1	Encoding	8B/10B	01h
12	1	BR, Nominal	x 100 Mbits/sec	0Ch
13	1	Reserved	——————	00h
14	1	Length (9μm) - km	40 x 1 km	28h
15	1	Length (9μm)	Longer than 25.4 km	FFh
16	1	Length (50μm)	Not Supported -	00h
17	1	Length (62.5μm)	Not Supported -	00h
18	1	Length (Copper)	Not Supported -	00h
19	1	Reserved	——————	00h
20	16	Vendor name	A	41
21			V	56
22			A	41
23			G	47
24			O	4F
25			——————	20h
26			——————	20h
27			——————	20h
28			——————	20h
29			——————	20h
30			——————	20h
31			——————	20h
32			——————	20h
33			——————	20h
34			——————	20h
35			——————	20h

Table 12. Serial ID: Data Fields - 2-Wire Address A0h (Continued)

BASE ID FIELDS				
Data Address	**Field Size (Byte)**	**Name of field**	**Description of Field**	**Context (Hex)**
36	1	Reserved	———————	00h
37	3	Vendor OUI	00-17-6A	00h
38				17h
39				6Ah
40	16	Vendor PN	A	41
41			F	46
42			C	43
43			T	54
44			-	2D
45			5	35
46			7	37
47			V	56
48			5	35
49			N	4E
50			S	53
51			Z	5A
52			———————	20h
53			———————	20h
54			———————	20h
55			———————	20h
56	4	Vendor Rev.	———————	Note 1
57			———————	Note 1
58			———————	Note 1
59			———————	Note 1
60	2	Laser Wavelength	1550 nm	06h
61				0Eh
62	1	Reserved	———————	00h
63	1	CC BASE	Check Code	Note 2

Notes:
1. These addresses are reserved for Vendor Revision.
2. Data Address 63 is the Check Sum for byte 0 to byte 62 (BASE ID FIELDS).

Table 12.- Serial ID: Data Fields - 2-Wire Address A0h (Continued)

EXTENDED ID FIELDS				
Data Address	**Field Size (Byte)**	**Name of field**	**Description of Field**	**Context (Hex)**
64	2	Function	—————	00h
65			TX_DISABLE, TX_FAULT, RX_LOS	1Ah
66	1	BR, max.	Unspecified	00h
67	1	BR, min.	Unspecified	00h
68	16	Vendor S/N		Note 3
69				Note 3
70				Note 3
71				Note 3
72				Note 3
73				Note 3
74				Note 3
75				Note 3
76				Note 3
77				Note 3
78				Note 3
79				Note 3
80				Note 3
81				Note 3
82				Note 3
83				Note 3
84	8	Data Code	Year (ASCII code)	Note 4
85				Note 4
86			Digits of Month (ASCII code)	Note 4
87				Note 4
88			Day of Month (ASCII code)	Note 4
89				Note 4
90			Vendor Specific Lot Code (ASCII code)	Note 4
91				Note 4
92	1	Diagnostic Monitoring Type	-Digital Diagnositic Monitoring-Internally Calibrated-Average power	68h
93	1	Enchanced Option	-Alarm/Warning Flags Implemented-Soft TX_FAULT and RX_LOS Monitoring	F0h
94	1	SFF-8472 Compliance	Includes Functionality Described in Rev 9.3 SFF8472	01h
95	1	CC_EXT	Check code for Extended ID Fields	Note 5
VENDOR SPECIFIC ID FIELDS				
96-255	160			00h

Notes:
3. These addresses are reserved for Vendor SN (serial number).
4. These addresses are reserved for date code information
5. Data Address 95 is the Check Sum for byte 64 to byte 94 (EXTENDED ID FIELDS).

Digital Diagnostic Monitoring

2 wire serial bus address 1010001X (A2h) is used to access measurement of transceiver temperature, internally measured supply voltage, TX bias current, TX optical output power and RX optical input power which are shown in Table 13. Each diagnostic parameter has a corresponding high alarm, low alarm, high warning and low warning threshold which are shown in Table 14. Alarm flags indicate conditions likely to be associated with an inoperational link and cause for immediate action. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. It is recommended that detection of an asserted flag bit should be verified by a second read of the flag at least 100 msec later. The detail contents of the 2 wire address A2h are shown in Table 15 to 21.

Table 13. Diagnostic Parameters

Diagnostic Parameter	Range		LSB	Accuracy	Address	Note
	Min.	Max.				
Transceiver Temperature(Temp)	-15 [ºC]	+105 [ºC]	1/256 [ºC]	±3 [ºC]	96-97	A 16 bit signed twos complement value
Supply Voltage (Voltage)	+2.97 [V]	+3.63 [V]	100 [µV]	±3 [%]	98-99	A 16 bit unsigned integer
TX Bias Current (Bias)	0 [mA]	+95 [mA]	2.0 [µA]	±10 [%]	100-101	A 16 bit unsigned integer
TX Optical Output Power (TX Power)	-6 [dBm]	+2 [dBm]	0.1 [µW]	±3 [dB]	102-103	A 16 bit unsigned integer
RX Optical Input Power (RX Power)	-25 [dBm]	+3 [dBm]	0.1 [µW]	±3 [dB]	104-105	A 16 bit unsigned integer

Table 14. Alarm and Warning Thresholds

Parameter	Unit	Warning		Alarm	
		Low	High	Low	High
Transceiver Temperature	ºC	-5	+70	-10	+75
Supply Voltage	V	+3.1	+3.5	+3	+3.6
TX Bias Current	mA	5	80	3	90
TX Optical Output Power	dBm	-4	0	-7	+3
RX Optical Input Power	dBm	-21	0	-22	+1

Table 15. Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at low address
02-03	2	Temp Low Alarm	MSB at low address
04-05	2	Temp High Warning	MSB at low address
06-07	2	Temp Low Warning	MSB at low address
08-09	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address
40-55	16	Reserved	Reserved for future monitored quantities

Table 16. Calibration constants for External Calibration Option (2-Wire Address A2h)

Address	# Bytes	Name	Description	Content
56-59	4	Rx_PWR(4)	Single precision floating point calibration data -Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB.	0
60-63	4	Rx_PWR(3)	Single precision floating point calibration data -Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB.	0
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB.	0
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB.	1
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB.	0
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB.	1
78-79	2	Tx_I(Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB.	0
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB.	1
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB.	0
84-85	2	T(Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB.	1
86-87	2	T(Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB.	0
88-89	2	V(Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB.	1
90-91	2	V(Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB.	0
92-94	3	Reserved	Reserved	———
95	1	Checksum	Byte 95 contains the low order 8 bits of the sumof bytes 0-94.	———

Table 17. A/D Values and Status Bits (2 Wire Address A2h)

Byte	Bit	Name	Description
Converted analog values. Calibrated 16 bit data			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX_DISABLE Input Pin.
110	6	Soft TX Disable	Read/write bit that allows software disable of laser.
110	5	Reserved	
110	4	RX Rate Select State	Digital state of the SFP RX Rate Select Input Pin.Not supported.
110	3	Soft RX Rate Select	Read/write bit that allows software RX rate select.Not supported.
110	2	TX Fault	Digital state of the TX_FAULT Output Pin.
110	1	LOS	Digital state of the RX_LOS Output Pin.
110	0	Data Ready Bar	Indicates transceiver has achieved power up and dataBit remains high until data is ready to be read at whichdevice sets the bit low.
111	7-0	Reserved	Reserved.

Table 18. Alarm and Warning Flag Bits (2-Wire Address A2h)

Byte	Bit	Name	Description
Reserved Optional Alarm and Warning Flag Bits			
112	7	Temp High Alarm	Set and latch when internal temperature exceeds high alarm level †
112	6	Temp Low Alarm	Set and latch when internal temperature is below low alarm level †
112	5	Vcc High Alarm	Set and latch when internal supply voltage exceeds high alarm level †
112	4	Vcc Low Alarm	Set and latch when internal supply voltage is below low alarm level †
112	3	TX Bias High Alarm	Set and latch when TX Bias current exceeds high alarm level †
112	2	TX Bias Low Alarm	Set and latch when TX Bias current is below low alarm level †
112	1	TX Power High Alarm	Set and latch when TX output power exceeds high alarm level †
112	0	TX Power Low Alarm	Set and latch when TX output power is below low alarm level †
113	7	RX Power High Alarm	Set and latch when Received Power exceeds high alarm level †
113	6	RX Power Low Alarm	Set and latch when Received Power is below low alarm level †
113	5	Reserved Alarm	
113	4	Reserved Alarm	
113	3	Reserved Alarm	
113	2	Reserved Alarm	
113	1	Reserved Alarm	
113	0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set and latch when internal temperature exceeds high warning level †
116	6	Temp Low Warning	Set and latch when internal temperature is below low warning level †
116	5	Vcc High Warning	Set and latch when internal supply voltage exceeds high warning level †
116	4	Vcc Low Warning	Set and latch when internal supply voltage is below low warning level †
116	3	TX Bias High Warning	Set and latch when TX Bias current exceeds high warning level †
116	2	TX Bias Low Warning	Set and latch when TX Bias current is below low warning level †
116	1	TX Power High Warning	Set and latch when TX output power exceeds high warning level †
116	0	TX Power Low Warning	Set and latch when TX output power is below low warning level †
117	7	RX Power High Warning	Set and latch when Received Power exceeds high warning level †
117	6	RX Power Low Warning	Set and latch when Received Power is below low warning level †
117	5	Reserved Warning	
117	4	Reserved Warning	
117	3	Reserved Warning	
117	2	Reserved Warning	
117	1	Reserved Warning	
117	0	Reserved Warning	
118	All	Reserved	
119	All	Reserved	

† Latch state cleared on read, power cycle or the host toggles TX_DISABLE.

Table 19. Vendor Specific Memory Address and User EEPROM (2-Wire Address A2h)

Byte	# Byte	Name	Description
120-127	8	Vendor Specific	00h.
128-247	120	User EEPROM	User Writable EEPROM
248-255	8	——————	00h

Table 20. Bit weights (°C) for Temperature Reporting Registers

Most Significant Byte (Byte 96)								Least Significant Byte (Byte 97)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
SIGN	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table 21. Digital Temperature Format

Temputer		BINARY		HEXADECIMAL	
DECIMAL	FRACTION	HIGH BYTE	LOW BYTE	HIGH BYTE	LOW BYTE
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+0.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000000	E7	00
-40.000	-40	11011000	00000000	D8	00
-127.996	-127 255/256	10000000	00000001	80	01
-128.000	-128	10000000	00000000	80	00

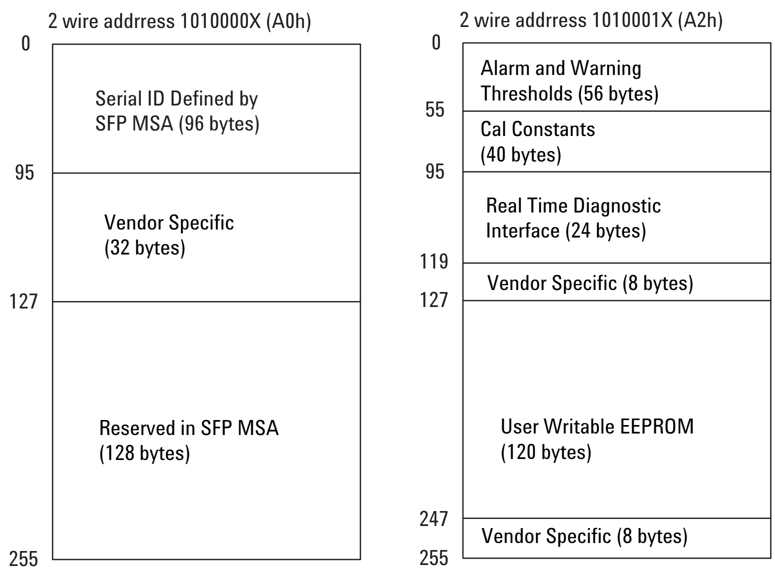


Figure 11. Serial ID and Digital Diagnostic Memory Map

Timing Characteristics of Serial ID/DDM

The timing characteristics of the serial ID /DDM are listed in Table 22 and Figure 12.

Table 22. Timing Characteristics of Serial ID / DDM

Parameter	Symbol	Min	Max	Unit
SCL Clock Rate	f_clock	.	100	kHz
BUS Free Time between STOP and START Condition	t_{BUF}	4.7	.	µs
START Condition Hold Time	$t_{HD:STA}$	4.0	.	µs
START Condition Setup Time	$t_{SU:STA}$	4.7	.	µs
Low Period of SCL Clock	t_{LOW}	4.7	.	µs
High Period of SCL Clock	t_{HIGH}	4.0	.	µs
Data Hold Time	$t_{HD:DAT}$	0	.	ns
Data Setup Time	$t_{SU:DAT}$	250	.	ns
Rise Time	t_R	.	1.0	µs

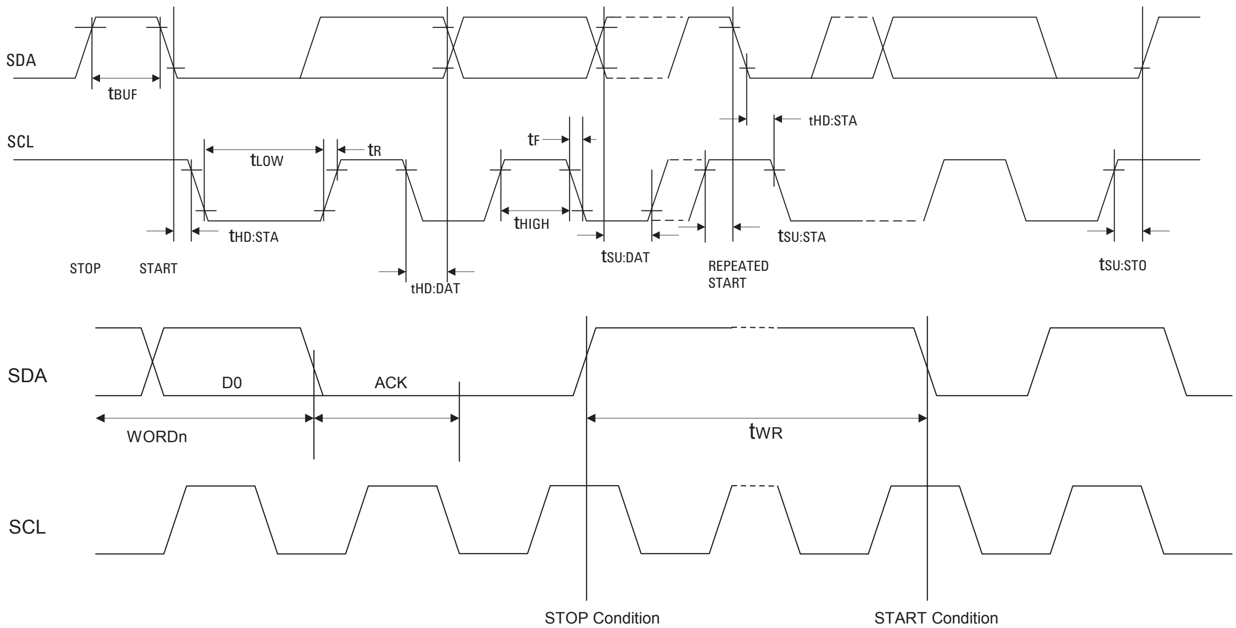
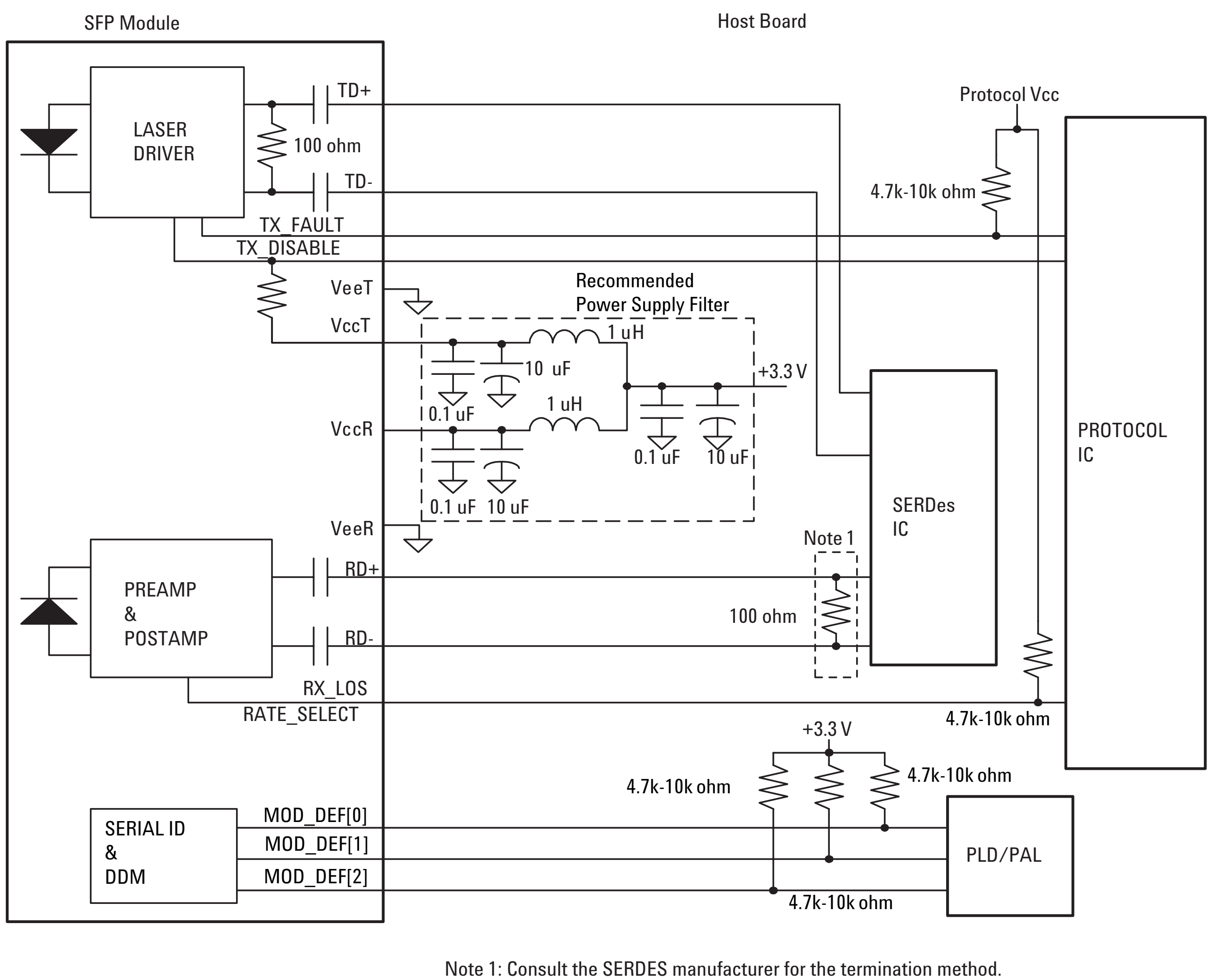


Figure 12. Serial ID and DDM Timing



Note 1: Consult the SERDES manufacturer for the termination method.

Figure 13. Recommended Power Supply Filter and Example of SFP Host Board Schematic

Connectors and Cables

The optical interface of the AFCT-57V6NSZ is a duplex LC connector which is described in TIA/EIA FOCIS document [5]. PC-polished ferrules are recommended in mating cables for the AFCT-57V6NSZ.

The electrical connection is provided by a card edge connector which mates with a corresponding socket [1]. In addition the transceiver fits a cage assembly [1] which also functions as an EMI shield. Contact an Avago sales office for cable, electrical connector, cage and accessory ordering information.

Physical Description

Figure 14 shows the mechanical outline of the Avago AFCT-57V6NSZ SFP. For a complete description of the footprint standards, refer to the MSA specification [1].

Laser Eye Safety

The Avago Technologies AFCT-57V6NSZ module is a Class 1 laser product under the requirements of IEC 60825-1:1993+A1:1997+A2:2001 and U. S. 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001, when used as specified by Avago. Class 1 products are considered to be safe.

Caution -Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure. Any modification, adjustment, or use of the AFCT-57V6NSZ module not specified by Avago may void the certification of the product and constitute an act of new manufacturing of a laser product under 21 CFR Subchapter J, and as such will require recertification by the new manufacturer. This includes operation beyond the Absolute Maximum Ratings listed in Table 2.

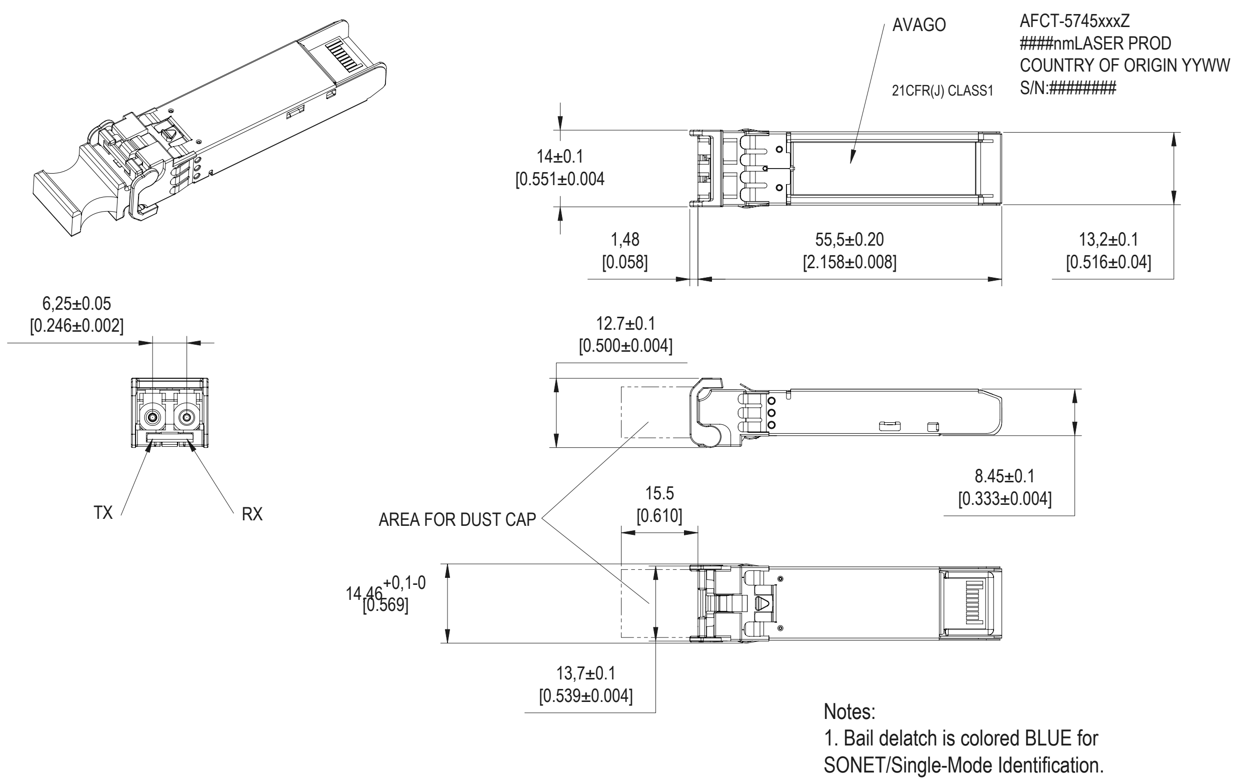


Figure 14. AFCT-57V6NSZ Mechanical Outline Drawing

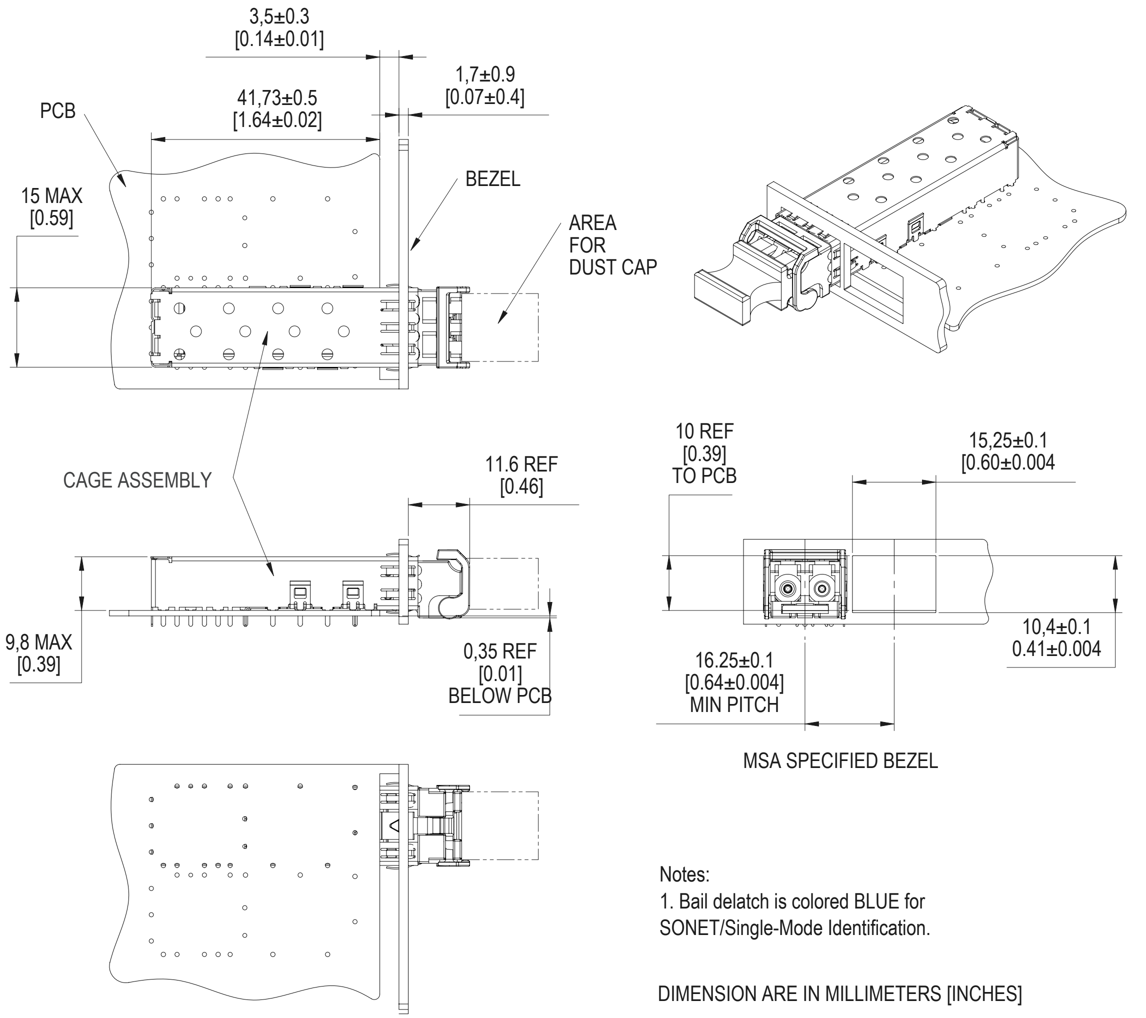


Figure 15. Mounting drawing

Regulatory Information

This product is under testing with respect to American and European product safety and electromagnetic compatibility regulations. For further information regarding regulatory certification, refer to the SFP Regulatory Specification [7] and SFP Application Note [6], or contact the Avago sales office.

References

[1] Small Form-factor Pluggable (SFP) Transceiver Multi Source Agreement, September 14, 2000

[2] IEEE 802.3z Media Access Control (MAC) Parameters, Physical Layer, Repeater and Management Parameters for 1000Mb/s Operation.

[3] SFF-8472, Digital Diagnostic Monitoring Interface for Optical Transceivers, Draft Revision 9.3, August 1, 2002

[4] A. Widmer & P. Franaszek, "A DC-balanced, partitioned-block, 8B/10B transmission code "IBM Journal of Research & Development", Vol. 27, No. 5, Pg. 440-451, (Sept. 1983).

[5] TIA/EIA-604-10, "FOCIS 10, Fiber Optic Connector Intermateability Standard", 1999

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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