ACPM-5005-TR1

Multimode PA - UMTS Band5 and CDMA Cellular (815-849MHz) 3x3mm Power Amplifier Module with Coupler

Data Sheet

Description

The ACPM-5005-TR1 is a fully matched 10-pin surface mount module developed to support multimode applications including UMTS Band5 and CDMA BC0(cellular) and BC10. The ACPM-5005-TR1 meets stringent linearity requirements up to 28.25dBm output power for UMTS Rel.99 and 27.75dBm for CDMA. The 3mmx3mm form factor package is self contained, incorporating 50ohm input and output matching networks. The PA also contains internal DC blocking capacitors for RF input and output ports.

The ACPM-5005-TR1 features 5th generation of CoolPAM (CoolPAM5) circuit technology which supports 3 power modes – active bypass, mid power and high power modes. The CoolPAM is stage bypass technology enhancing PAE (power added efficiency) at low and medium power range. The active bypass feature is added to CoolPAM5 to enhance the PAE further at low output range and it enables the PA to have exceptionally low quiescent current. It dramatically saves the average power consumption and accordingly extends the talk time of mobiles and prolongs a battery life.

A directional coupler is integrated into the module and both coupling and isolation ports are available externally, supporting daisy chain. The integrated coupler has excellent coupler directivity, which minimizes the coupled output power variation or delivered power variation caused by the load mismatch from the antenna. The coupler directivity, or the output power variation into the mismatched load, is critical to the TRP and SAR performance of the mobile phones in real field operations as well as compliance tests for the system specifications.

The ACPM-5005 has integrated on-chip Vref and on-module bias switch as the one of the key features of the CoolPAM-5, so an external constant voltage source is not required, eliminating the external LDO regulators and switches from circuit boards of mobile devices. It also makes the PA fully digital-controllable by the Ven pin that simply turns the PA on and off from the digital control logic input from

Features

- Thin Package (0.9mm typ)
- Excellent Linearity
- 3-mode power control with Vbp and Vmode
  - Bypass / Mid Power Mode / High Power Mode
- High Efficiency at max output power
- 10-pin surface mounting package
- Internal 50ohm matching networks for both RF input and output
- Integrated coupler
  - Coupler and Isolation ports for daisy chain
- Lead-free, RoHS compliant, Green

Applications

- UMTS (WCDMA, HSDPA, HSUPA, HSPA+)
- LTE
- CDMA

Ordering Information

Part Number	Number of Devices	Container
ACPM-5005-TR1	1000	178mm (7”) Tape/Reel
ACPM-5005-BLK	100	Bulk

Description (Cont.)

baseband chipsets. All of the digital control input pins such as the Ven, Vmode and Vbp are fully CMOS compatible and can operate down to the 1.35V logic. The current consumption by digital control pins is negligible.

The power amplifier is manufactured on an advanced InGaP HBT (hetero-junction Bipolar Transistor) MMIC (microwave monolithic integrated circuit) technology offering state-of-the-art reliability, temperature stability and ruggedness.

Absolute Maximum Ratings

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.

Operation of any single parameter outside these conditions with the remaining parameters set at or below nominal values may result in permanent damage.

Description	Min.	Typ.	Max.	Unit
RF Input Power (Pin)		0	10	dBm
DC Supply Voltage (Vcc1, Vcc2)	0	3.4	5.0	V
Enable Voltage (Ven)	0	2.6	3.3	V
Mode Control Voltage (Vmode)	0	2.6	3.3	V
Bypass Control (Vbp)	0	2.6	3.3	V
Storage Temperature (Tstg)	-55	25	+125	°C

Recommended Operating Condition

Description		Min.	Typ.	Max.	Unit
DC Supply Voltage (Vcc1, Vcc2)		3.2	3.4	4.2	V
Enable Voltage (Ven)					
	Low	0	0	0.5	V
	High	1.35	2.6	3.1	V
Mode Control Voltage (Vmode)					
	Low	0	0	0.5	V
	High	1.35	2.6	3.1	V
Bypass Control Voltage (Vbp)					
	Low	0	0	0.5	V
	High	1.35	2.6	3.1	V
Operating Frequency (fo)		815		849	MHz
Ambient Temperature (Ta)					
	UMTS	-20	25	85	°C
	CDMA	-30	25	85	°C

Operating Logic Table

Power Mode	Ven	Vmode	Vbp	Pout (Rel99)	Pout (HSDPA, HSUPA MPR=0dB)
High Power Mode	High	Low	X	~ 28.25 dBm	~ 27.25 dBm
Mid Power Mode	High	High	Low	~ 17 dBm	~ 16 dBm
Bypass Mode	High	High	High	~ 7 dBm	~ 6 dBm
Shut Down Mode	Low	Low	Low	–	–

Electrical Characteristics for WCDMA Mode

– Conditions: Vcc = 3.4V, Ven = 2.6V, Ta = 25°C, Zin/Zout = 50ohm
– Signal Configuration: 3GPP (DPCCH + 1DPDCH) Up-Link unless specified otherwise.

Characteristics	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range		815	–	849	MHz
Maximum Output Power (High Power Mode)	Rel99	28.25			dBm
	HSDPA, HSUPA MPR=0dB	27.25			dBm
	CDMA2000 RC1	27.75			dBm
Gain	High Power Mode, Pout=28.25dBm	24.5	28		dB
	Mid Power Mode, Pout=17dBm	15	19		dB
	Bypass Mode, Pout=7dBm	9	13.5		dB
Power Added Efficiency	High Power Mode, Pout=28.25dBm	36	40.1		%
	Mid Power Mode, Pout=17dBm	15.7	20.8		%
	Bypass Mode, Pout=7dBm	7	12.8		%
Total Supply Current	High Power Mode, Pout=28.25dBm		490	545	mA
	Mid Power Mode, Pout=17dBm		70	93	mA
	Mid Power Mode, Pout=13.5dBm		50		mA
	Bypass Mode, Pout=7dBm		11	20	mA
	Bypass Mode, Pout=3.5dBm		8.5		mA
Quiescent Current	High Power Mode	90	123	155	mA
	Mid Power Mode	10	19	30	mA
	Bypass Mode	1	3.1	5	mA
Enable Current	High Power Mode		5		µA
	Mid Power Mode		5		µA
	Bypass Mode		5		µA
Mode Control Current	Mid Power Mode		5		µA
	Bypass Mode		5		µA
Bypass Control Current	Bypass		5		µA
Total Current in Power-down mode	Ven=0V, Vmode=0V, Vbp=0V			5	µA
UMTS Adjacent Channel Leakage Ratio (ACLR) 5 MHz offset	Pout ≤ (max power – MPR)		-44	-36	dBc
10 MHz offset			-58	-46	dBc
LTE ACLR	LTE to LTE, E-UTRA$_{ACLR}$ Pout ≤ (maximum power – MPR)			-33	dBc
	UTRA$_{ACLR1}$ Pout ≤ (maximum power – MPR)			-36	dBc
	UTRA$_{ACLR2}$ Pout ≤ (maximum power – MPR)			-39	dBc
Adjacent Channel Power Ratio (ACPR) ±885kHz offset	Pout ≤ max power		-49	-44	dBc
±1.98 MHz offset			-60	-56	dBc
Harmonic Suppression Second	High Power Mode, Pout=28.25dBm		-40	-35	dBc
Third			-66	-42	dBc
Input VSWR				2.5:1	
Stability (Spurious Output)	VSWR 5:1, All phase			-60	dBc
Rx Band Noise Power (Vcc=4.2V)	High Power Mode, Pout=28.25dBm		-137		dBm/Hz
GPS Band Noise Power (Vcc=4.2V)	High Power Mode, Pout=28.25dBm		-154		dBm/Hz
ISM Band Noise Power (Vcc=4.2V)	High Power Mode, Pout=28.25dBm		-158		dBm/Hz
Rx Band Gain (869-894MHz)	Where G is gain in Tx band		G-0.5		dB
GPS Band Gain (1574-1577MHz)	Where G is gain in Tx band		G-31		dB
GLONASS Band Gain (1597-1607MHz)	Where G is gain in Tx band		G-31		dB
ISM Band Gain (2400-2483.5MHz)	Where G is gain in Tx band		G-65		dB
Media Band Gain (716-728MHz)	Where G is gain in Tx band		G		dB

Continued on next page...

Electrical Characteristics for WCDMA Mode (Cont.)

Phase Discontinuity	low power mode↔mid power mode, at Pout=7dBm mid power mode↔high power mode, at Pout=17dBm	20 30		deg deg
Ruggedness	Pout<28.25dBm, Pin<10dBm, All phase High Power Mode		10:1	VSWR
Coupling factor	RF Out to CPL port	21		dB
Daisy Chain Insertion Loss	ISO port to CPL port, Ven=Low	0.25		dB

HSDPA Signal configuration used:

3GPP TS 34.121-1
Annex C (normative e): Measurement channels
C.10.1 UL reference measurement channel for HSDPA tests
Table C.10.1.4: β values for transmitter characteristics tests with HS-DPCCH
Sub-test 2 (CM=1.0, MPR=0.0)

HSUPA signal configuration used:

3GPP TS 34.121-1
Annex C (normative): Measurement channels
C.11.1 UL reference measurement channel for E-DCH tests
Table C.11.1.3: β values for transmitter characteristics tests with HS-DPCCH and E-DCH Sub-test 1 (CM=1.0, MPR=0.0)

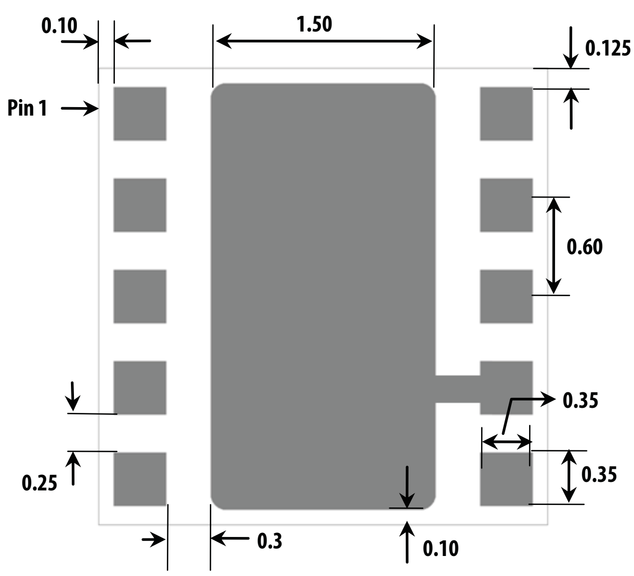
CDMA signal configuration used:

CDMA2000 RC1: R-FCH(9600bps)

At 3.2V operation, 0.5dB backoff is allowed for maximum power output.

Footprint

All dimensions are in millimeter



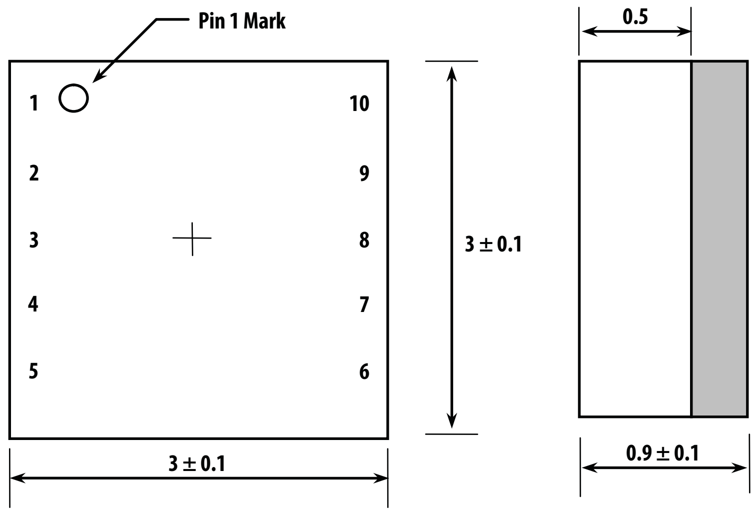
X-Ray Top View

PIN Description

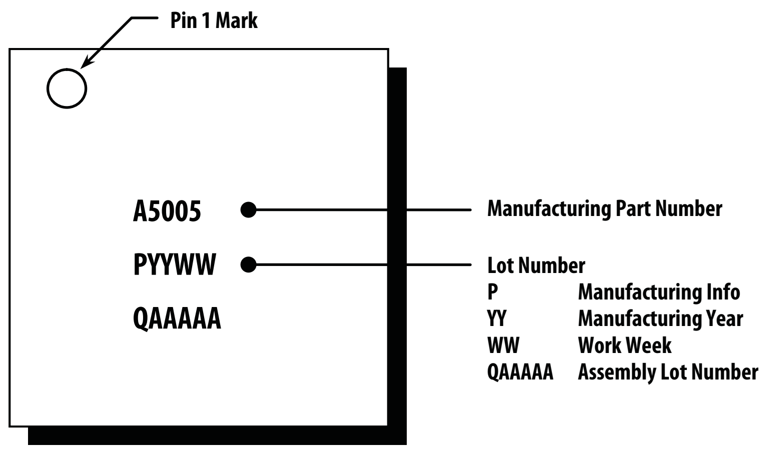
Pin #	Name	Description
1	Vcc1	DC Supply Voltage
2	RFin	RF Input
3	Vbp	Bypass Control
4	Vmode	Mode Control
5	Ven	PA Enable
6	CPL	Coupling port of Coupler
7	GND	Ground
8	ISO	Isolation port of Coupler
9	RFOut	RF Out
10	Vcc2	DC Supply Voltage

Package Dimensions

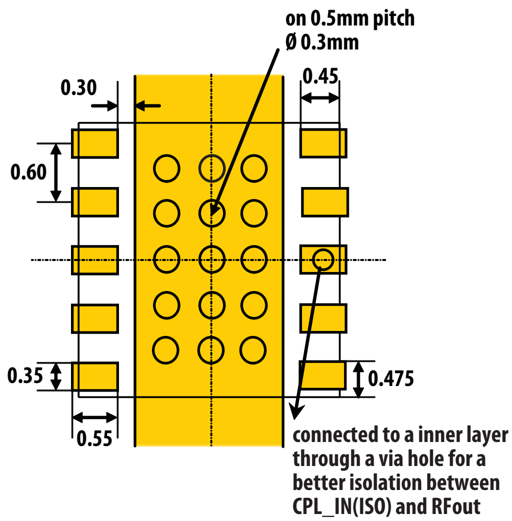
All dimensions ae in millimeter



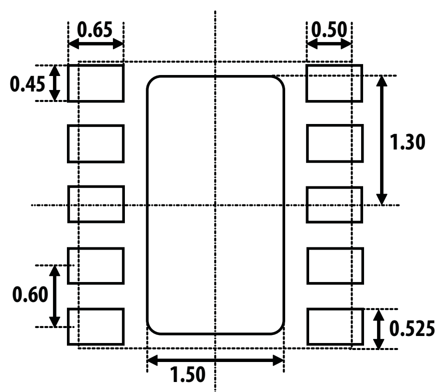
Marking Specification



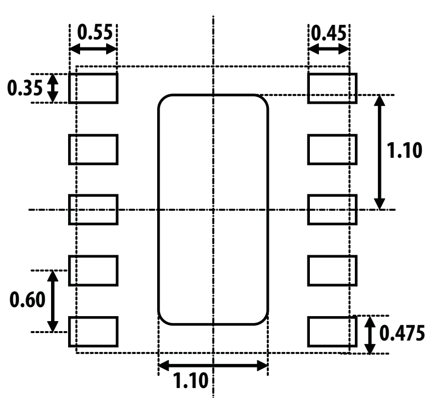
Metallization



Solder Mask Opening



Solder Paste Stencil Aperture



PCB Design Guidelines

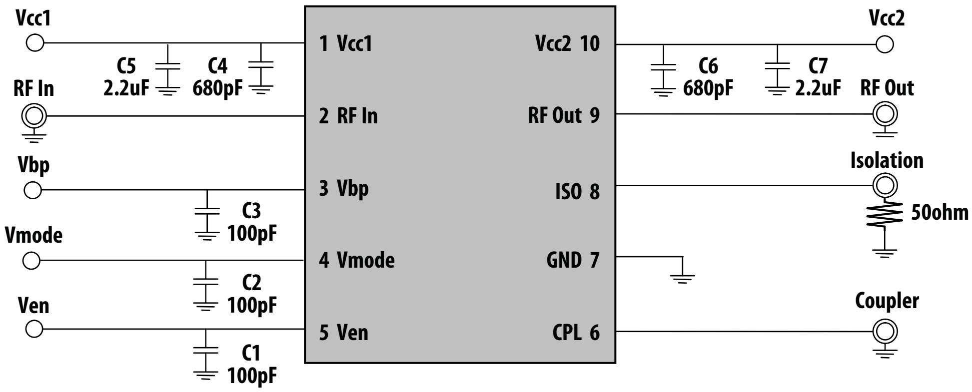
The recommended PCB land pattern is shown in figures on the left side. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

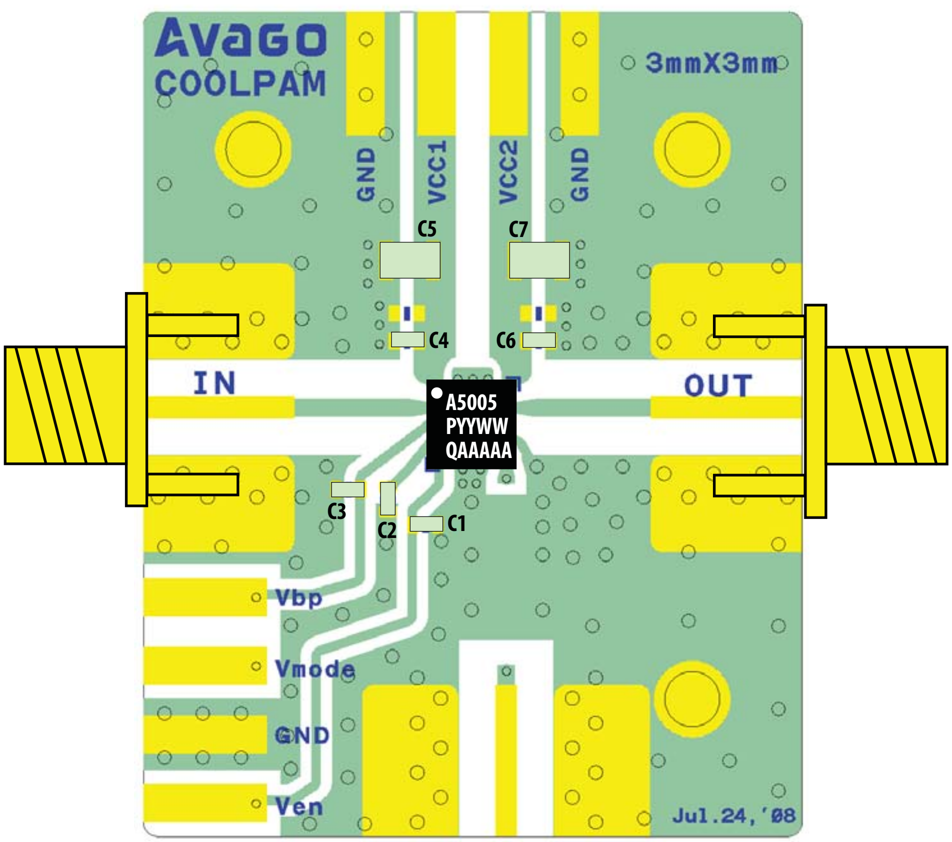
A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown here. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm(4mils) or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

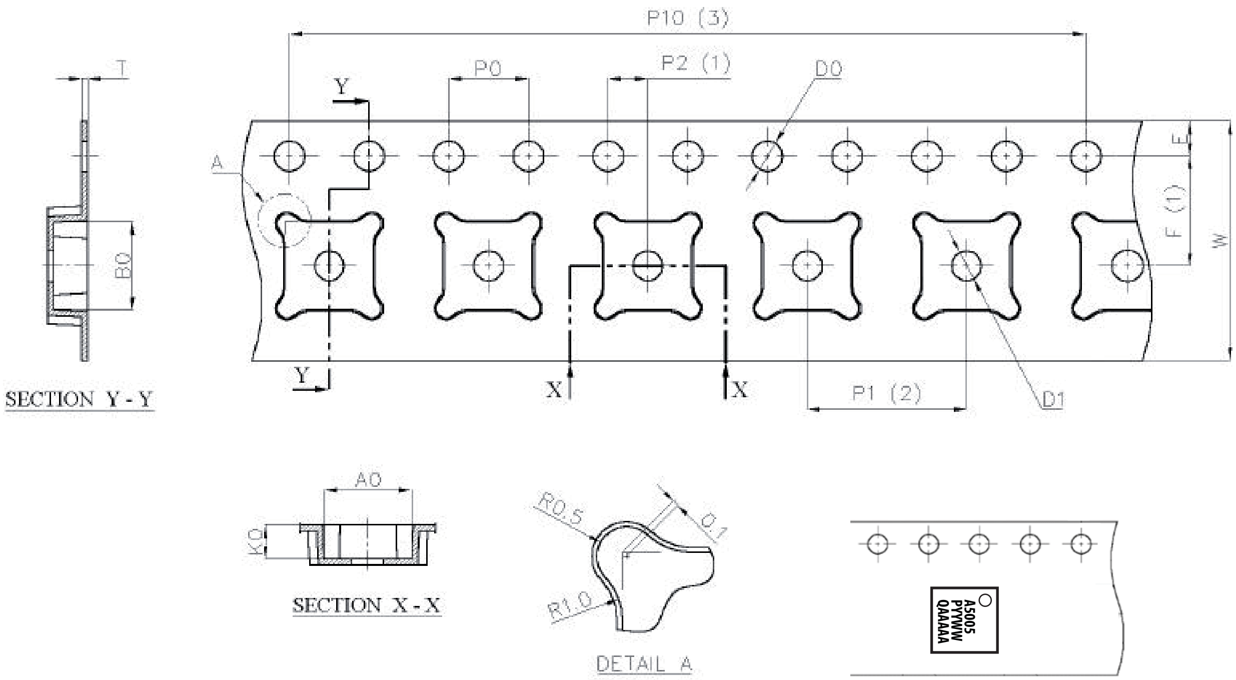
Evaluation Board Schematic



Evaluation Board Description



Tape and Reel Information



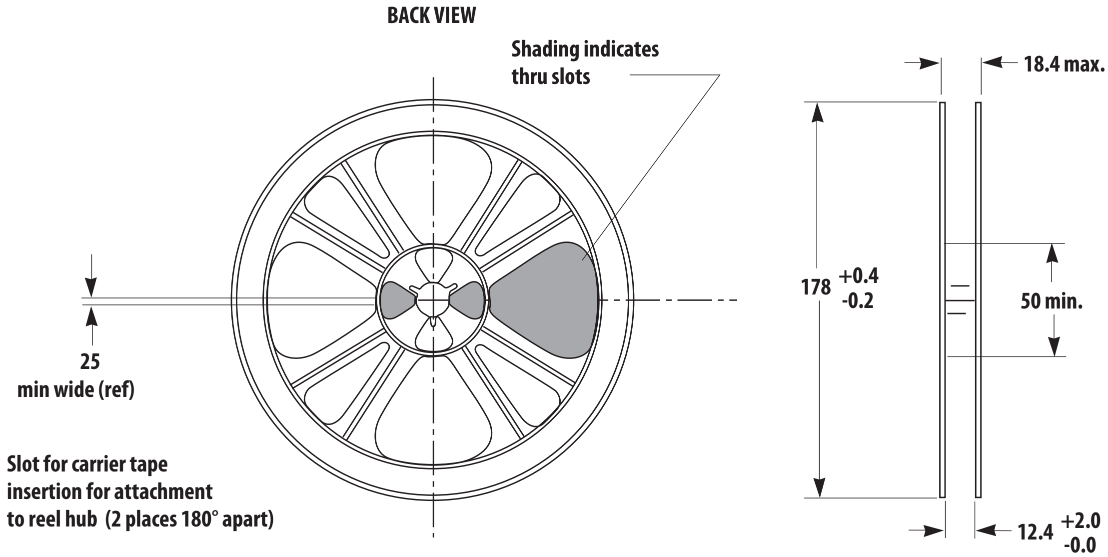
Dimension List

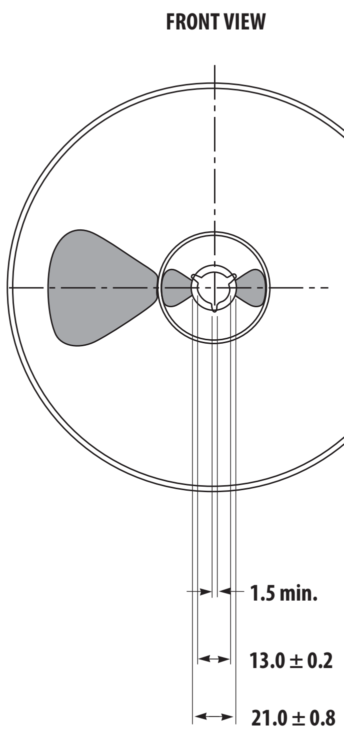
Annote	Millimeter
A0	3.40±0.10
B0	3.40±0.10
K0	1.35±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10
P1	8.00±0.10

Annote	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Tape and Reel Format – 3 mm x 3 mm

Reel Drawing





NOTES:
1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

ACPM-5005-TR1 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-5005-TR1 is targeted at 260°C +0/-5°C. Figure and table on next page show typical SMT profile for maximum temperature of 260 +0/-5°C.

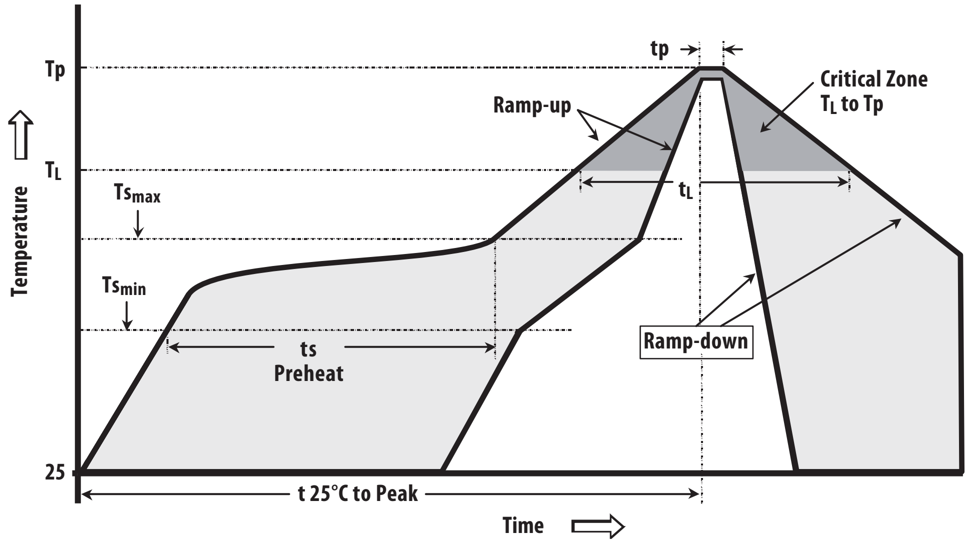
Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :

1. The MSL Level is marked on the MSL Label on each shipping bag.

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-120 sec
Tsmax to TL – Ramp-up Rate		 3°C/sec max
Time maintained above: – Temperature (TL) – Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework
Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in next table. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table on next page lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

Table on next page is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C, 35°C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified) Maximum Percent Relative Humidity

Maximum Percent Relative Humidity												
Package Type and Body Thickness	**Moisture Sensitivity Level**	**5%**	**10%**	**20%**	**30%**	**40%**	**50%**	**60%**	**70%**	**80%**	**90%**	
Body Thickness ≥3.1 mm	Level 2a	∞	∞	94	44	32	26	16	7	5	4	35°C
Including		∞	∞	124	60	41	33	28	10	7	6	30°C
PQFPs >84 pin,		∞	∞	167	78	53	42	36	14	10	8	25°C
PLCCs (square)		∞	∞	231	103	69	57	47	19	13	10	20°C
All MQFPs	Level 3	∞	∞	8	7	6	6	6	4	3	3	35°C
or		∞	∞	10	9	8	7	7	5	4	4	30°C
All BGAs ≥1 mm		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	3	3	3	2	2	2	2	1	1	35°C
		∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	2	2	2	2	1	1	1	1	1	35°C
		∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	1	1	1	1	1	1	1	1	1	35°C
		∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm	Level 2a	∞	∞	∞	∞	58	30	22	3	2	1	35°C
≤ Thickness		∞	∞	∞	∞	86	39	28	4	3	2	30°C
<3.1 mm including		∞	∞	∞	∞	148	51	37	6	4	3	25°C
PLCCs (rectangular)		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
18-32 pin	Level 3	∞	∞	12	9	7	6	5	2	2	1	35°C
SOICs (wide body)		∞	∞	19	12	9	8	7	3	2	2	30°C
SOICs ≥20 pins,		∞	∞	25	15	12	10	9	5	3	3	25°C
PQFPs ≤80 pins		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	5	4	3	3	2	2	1	1	1	35°C
		∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	3	2	2	2	2	1	1	1	1	35°C
		∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	1	1	1	1	1	1	1	0.5	0.5	35°C
		∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm	Level 2a	∞	∞	∞	∞	∞	∞	17	1	0.5	0.5	35°C
including		∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
SOICs <18 pin		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
All TQFPs, TSOPs		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
or	Level 3	∞	∞	∞	∞	∞	8	5	1	0.5	0.5	35°C
All BGAs <1 mm body		∞	∞	∞	∞	∞	11	7	1	1	1	30°C
thickness		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	7	4	3	2	1	0.5	0.5	35°C
		∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	7	3	2	2	1	1	0.5	0.5	35°C
		∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	7	2	1	1	1	1	1	0.5	0.5	35°C
		∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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