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ATP A4G04QA8BLPBSE

4GB DDR4-2133 UNBUFFERED NON-ECC SODIMM

DESCRIPTION

The ATP A4G04QA8BLPBSE is a high performance 4GB DDR4-2133 Unbuffered NON-ECC SDRAM memory module. It is organized as 512M x 64 in a 260-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes eight 512Mx8 DDR4 SDRAMs in FBGA package. The module consists of a 512-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 4GB (512M x 64)
- DIMM Rank: 1 Rank
- Cycle Time: 0.93ns (1067MHz)
- CAS Latency: 15
- Power supply: V_{DD}=1.2V ± 0.06V
  V_{PP}=2.5V± 0.125V
  V_{DDSPD}=2.2V~3.6V
- Nominal and dynamic on-die termination(ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion(DBI) for data bus
- 16 internal banks(x8); 4 groups of 4 banks each
- Internal self calibration through ZQ
- Temperature controlled refresh (TCR)
- Asynchronous Reset
- 7.8 μs refresh interval at lower than T_{CASE}85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Support address and command signals parity function
- Selectable BC4 or BL8 on-the fly(OTF)
- Dynamic On Die Termination
- Fly-by topology
- Full module heat spreader
- PCB Height: 1.18 inches(30mm)
- Minimum Thickness of Golden Finger: 30 Micro-inch
- RoHS compliant

Part No.	Max Freq	Interface
A4G04QA8BLPBSE	1067MHz (0.93ns@CL=15) x2	POD12

Your Ultimate Memory Solution!

PIN DESCRIPTION

Pin Name	Description
A0~A16	Address Inputs
A10/AP	Address Input/Auto precharge
A12/BC_n	Address Input/Burst chop
BA0,BA1	SDRAM Bank Address
BG0,BG1	Bank group address inputs
RAS_n	Row address strobe input
CAS_n	Column address strobe input
WE_n	Write enable input
CS0_n	Chip Selects
CK0_t	Clock Inputs, positive line
CK0_c	Clock Inputs, negative line
CKE0	Clock Enables
C0~C2	Chip ID
ODT0	On-die termination control lines input
ACT_n	Command input: ACT_n indicates an ACTIVATE command.
DQ0~DQ63	Data Input /Output
DQS0_t~DQS7_t	Data strobes
DQS0_c~DQS7_c	Data strobes, negative line
DQM0 ~DQM7	Data Mask
SCL	Serial clock for temperature sensor/SPD EEPROM
SDA	SPD Data Input /Output
SA0~SA2	Serial address inputs
PARITY	Parity for command and address
VDD	Power supply
VPP	DRAM activating power supply
VREFCA	Reference voltage for control, command, and address pins.
VSS	Ground
VDDSPD	SPD Power
ALERT_n	Alert output
RESET_n	Active LOW asynchronous reset
EVENT_n	Temperature sensor Event Output
VTT	SDRAM I/O termination supply
VDDQ	DRAM DQ power supply
ZQ	Reference ball for ZQ calibration
NC	No Connect
NF	No function
RFU	Reserved for future use

PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VSS	2	VSS	133	A1	134	EVENT_n
3	DQ5	4	DQ4	135	VDD	136	VDD
5	VSS	6	VSS	137	CK0_t	138	CK1_t
7	DQ1	8	DQ0	139	CK0_c	140	CK1_c
9	VSS	10	VSS	141	VDD	142	VDD
11	DQS0_c	12	DQM0	143	PARITY	144	A0
13	DQS0_t	14	VSS	KEY			
15	VSS	16	DQ6	145	BA1	146	A10/AP
17	DQ7	18	VSS	147	VDD	148	VDD
19	VSS	20	DQ2	149	CS0_n	150	BA0
21	DQ3	22	VSS	151	WE_n/A14	152	RAS_n/A16
23	VSS	24	DQ12	153	VDD	154	VDD
25	DQ13	26	VSS	155	ODT0	156	CAS_n/A15
27	VSS	28	DQ8	157	CS1_n	158	A13
29	DQ9	30	VSS	159	VDD	160	VDD
31	VSS	32	DQS1_c	161	ODT1	162	C0,CS2_n,NC
33	DQM1	34	DQS1_t	163	VDD	164	VREFCA
35	VSS	36	VSS	165	NC,CS3_c,C1	166	SA2
37	DQ15	38	DQ14	167	VSS	168	VSS
39	VSS	40	VSS	169	DQ37	170	DQ36
41	DQ10	42	DQ11	171	VSS	172	VSS
43	VSS	44	VSS	173	DQ33	174	DQ32
45	DQ21	46	DQ20	175	VSS	176	VSS
47	VSS	48	VSS	177	DQS4_c	178	DQM4
49	DQ17	50	DQ16	179	DQS4_t	180	VSS
51	VSS	52	VSS	181	VSS	182	DQ39
53	DQS2_c	54	DQM2	183	DQ38	184	VSS
55	DQS2_t	56	VSS	185	VSS	186	DQ35
57	VSS	58	DQ22	187	DQ34	188	VSS
59	DQ23	60	VSS	189	VSS	190	DQ45
61	VSS	62	DQ18	191	DQ44	192	VSS
63	DQ19	64	VSS	193	VSS	194	DQ41
65	VSS	66	DQ28	195	DQ40	196	VSS
67	DQ29	68	VSS	197	VSS	198	DQS5_c
69	VSS	70	DQ24	199	DQM5	200	DQS5_t
71	DQ25	72	VSS	201	VSS	202	VSS
73	VSS	74	DQS3_c	203	DQ46	204	DQ47
75	DQM3	76	DQS3_t	205	VSS	206	VSS
77	VSS	78	VSS	207	DQ42	208	DQ43

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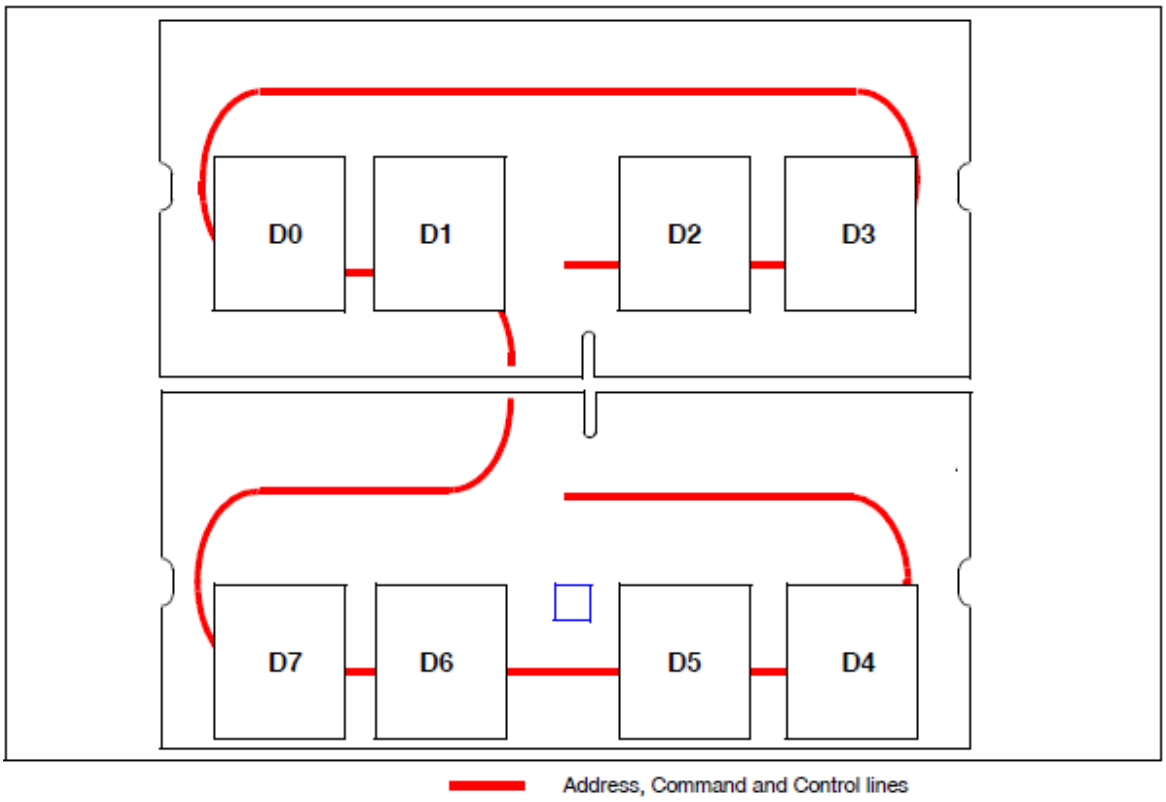
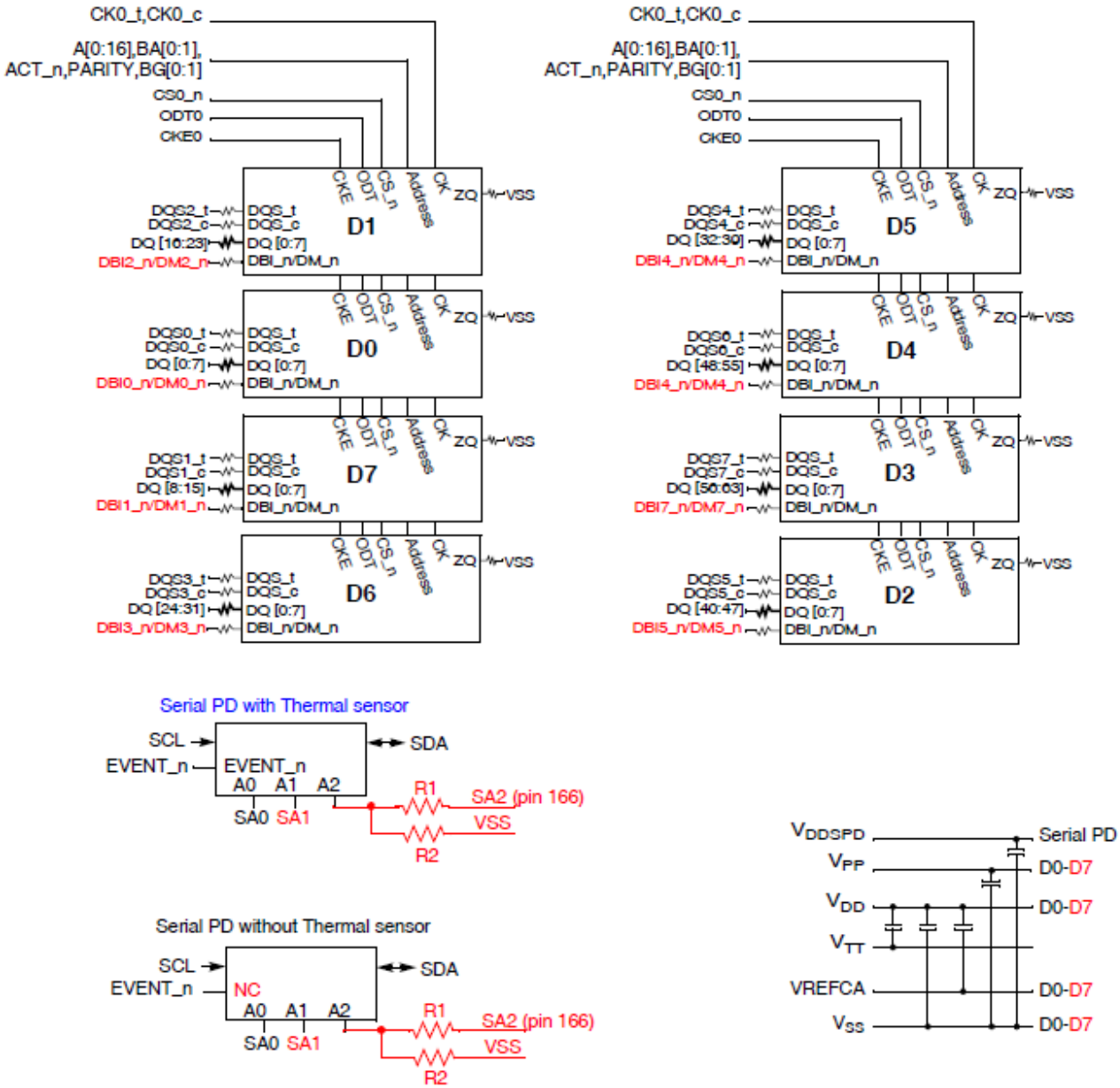
No.	Designation	No.	Designation	No.	Designation	No.	Designation
79	DQ30	80	DQ31	209	VSS	210	VSS
81	VSS	82	VSS	211	DQ52	212	DQ53
83	DQ26	84	DQ27	213	VSS	214	VSS
85	VSS	86	VSS	215	DQ49	216	DQ48
87	NC	88	NC	217	VSS	218	VSS
89	VSS	90	VSS	219	DQS6_c	220	DQM6
91	NC	92	NC	221	DQS6_t	222	VSS
93	VSS	94	VSS	223	VSS	224	DQ54
95	NC	96	NC	225	DQ55	226	VSS
97	NC	98	VSS	227	VSS	228	DQ50
99	VSS	100	NC	229	DQ51	230	VSS
101	NC	102	VSS	231	VSS	232	DQ60
103	VSS	104	NC	233	DQ61	234	VSS
105	NC	106	VSS	235	VSS	236	DQ57
107	VSS	108	RESET_n	237	DQ56	238	VSS
109	CKE0	110	CKE1	239	VSS	240	DQS7_c
111	VDD	112	VDD	241	DQM7	242	DQS7_t
113	BG1	114	ACT_n	243	VSS	244	VSS
115	BG0	116	ALERT_n	245	DQ62	246	DQ63
117	VDD	118	VDD	247	VSS	248	VSS
119	A12/BC_n	120	A11	249	DQ58	250	DQ59
121	A9	122	A7	251	VSS	252	VSS
123	VDD	124	VDD	253	SCL	254	SDA
125	A8	126	A5	255	VDDSPD	256	SA0
127	A6	128	A4	257	VPP	258	VTT
129	VDD	130	VDD	259	VPP	260	SA1
131	A3	132	A2				

Note:
1. VPP is 2.5V DC

FUNCTIONAL BLOCK DIAGRAM (PART1 OF 2)



FUNCTIONAL BLOCK DIAGRAM (PART2 OF 2)



Note 1: Unless otherwise noted, resistor values are 15Ω ± 5%.
Note 2: ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
Note 3: To connect the SPD A2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The values for R1 and R2 are not critical. Any value less than 100 Ohms may be used.

ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.5V	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.5V	V	1,3
Voltage on V_{PP} pin relative to V_{SS}	V_{PP}	-0.4V ~ 3.0V	V	4
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1
Storage Temperature	T_{STG}	-55 to +100	°C	1,2
Operating Temperature	T_{CASE}	0 to +95	°C	1,2

Note:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC OPERATING CONDITIONS

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage [1,2,3]	V_{DD}	1.14	1.2	1.26	V
Supply Voltage for Output [1,2,3]	V_{DDQ}	1.14	1.2	1.26	V
DRAM Activating Power Supply[3]	V_{PP}	2.375	2.5	2.75	V
Input reference voltage command/ address bus	V_{REFCA}(DC)	0.49 * V_{DD}	0.50 * V_{DD}	0.51 * V_{DD}	V
Termination reference voltage (DC) – command/address bus[4]	V_{TT}	0.49 * V_{DD}- 20mA	0.50 * V_{DD}	0.51 * V_{DD}+ 20mA	V
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.075	-	V_{DD}	V
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.1	-	-	V
Input Low Voltage (DC)	V_{IL} (DC)	V_{SS}	-	V_{REF} - 0.075	V
Input Low Voltage (AC)	V_{IL} (AC)	-	-	V_{REF} - 0.1	V

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.
4. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.

RELIABILITY

MTBF @25 °C (Hours) [1]	FIT @ 25 °C [2]	MTBF @40 °C (Hours) [1]	FIT @ 40 °C [2]
9,236,047	108	4,624,904	216

Note:
1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours

IDD SPECIFICATION PARAMETER & POWER CONSUMPTION (PART1 OF 2)

Values are for the DDR4 SDRAM only and are computed from values specified in the vendor's component data sheet)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	270	mA
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0	32	mA
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: sta-ble at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	350	mA
IDD2N	**Precharge Standby Current (AL=0)** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	130	mA
IDD2NT	**Precharge Standby ODT Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	150	mA
IDD2P	**Precharge Power-Down Current** CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	90	mA
IDD2Q	**Precharge Quiet Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	120	mA
IDD3N	**Active Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	240	mA
IPP3N	**Active Standby IPP Current** Same condition with IDD3N	24	mA
IDD3P	**Active Power-Down Current** CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	120	mA
IDD4R	**Operating Burst Read Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	760	mA
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current	284	mA

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IDD SPECIFICATION PARAMETER & POWER CONSUMPTION (PART2 OF 2)

Values are for the DDR4 SDRAM only and are computed from values specified in the vendor's component data sheet)

Symbol	Proposed Conditions	Value	Units
IDD4W	**Operating Burst Write Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	620	mA
IDD5B	**Burst Refresh Current (1X REF)** CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,230	mA
IPP5B	**Burst Refresh Write IPP Current (1X REF)** Same condition with IDD5B	144	mA
IDD6N	**Self Refresh Current: Normal Temperature Range** TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	100	mA
IDD6E	**Self-Refresh Current: Extended Temperature Range)** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	130	mA
IDD6R	**Self-Refresh Current: Reduced Temperature Range** TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	80	mA
IDD6A	**Auto Self-Refresh Current** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	100	mA
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,180	mA
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7	60	mA
IDD8	**Maximum Power Down Current**	60	mA
PDIMM	**Power Consumption per DIMM** System is operating at 1067MHz clock with VDD = 1.2V. This parameter is calculated at a common loading.	1,430	mW

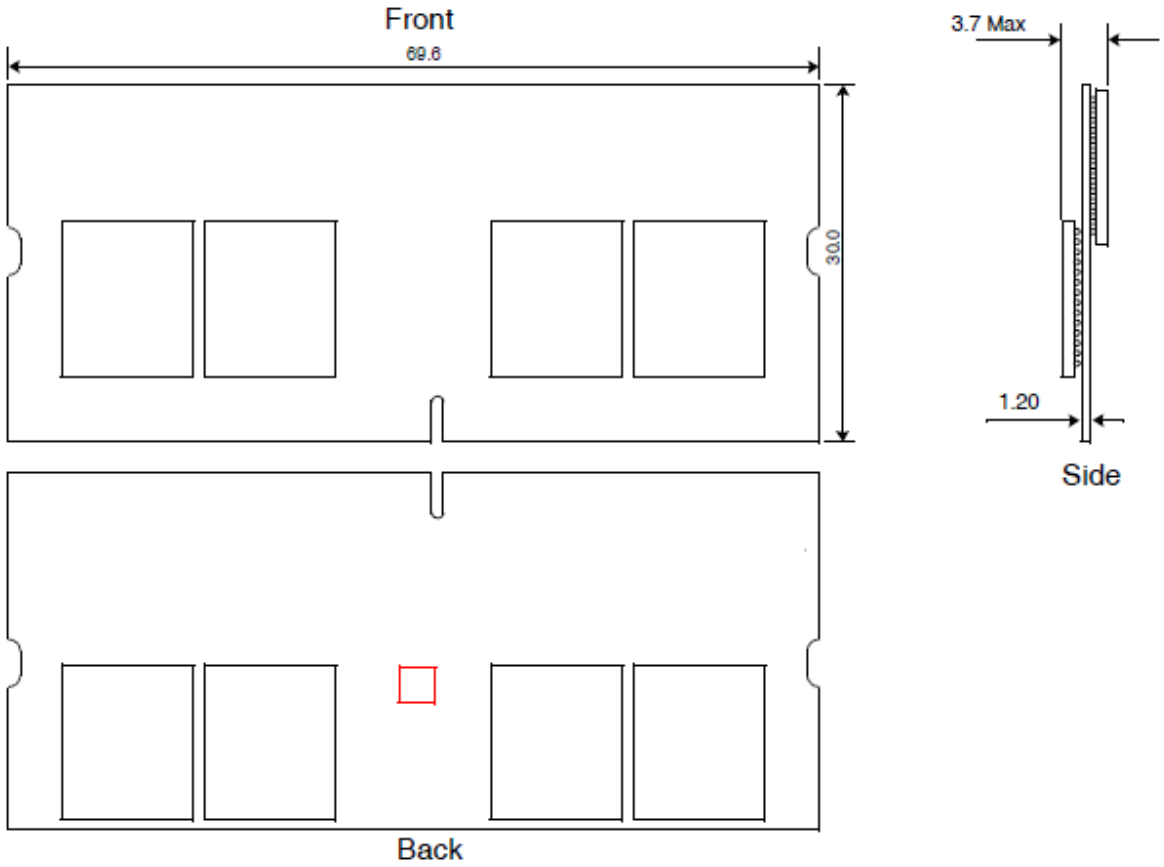
TIMING PARAMETER

Parameter	Symbol	DDR4-2133		Units
		Min	Max	
Clock cycle time at CL=15, CWL=11	tCK	0.938	<1.071	ns
Internal read command to first data	tAA	14.06	18	ns
ACT to internal read or write delay time	tRCD	14.06		ns
PRE command period	tRP	14.06		ns
ACT to ACT or REF command period	tRC	47.06		ns
ACTIVE to PRECHARGE command period	tRAS	33	9*tREFI	ns
Average clock high pulse width	tCH(avg)	0.48	0.52	tCK
Average clock low pulse width	tCL(avg)	0.48	0.52	tCK
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	TBD	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	TBD	-	tCK
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-360	180	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	180	ps
DQS, $\overline{DQS}$ READ Preamble	tRPRE	0.9	TBD	tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	TBD	TBD	tCK
DQS, $\overline{DQS}$ output high time	tQSH	0.4	-	tCK
DQS, $\overline{DQS}$ output low time	tQSL	0.4	-	tCK
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE	0.9	-	tCK
DQS, $\overline{DQS}$ WRITE Postamble	tWPST	TBD	TBD	tCK
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-360	180	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.27	0.27	tCK
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.18	-	tCK
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.18	-	tCK
DLL locking time	tDLLK	768	-	nCK[1]
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
Delay from start of internal write trans-action to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	
Delay from start of internal write trans-action to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	8	-	nCK[1]
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	tCCD	6	-	nCK[1]
Auto precharge write recovery + precharge time	tDAL	tWR + roundup (tRP / tCK)		nCK[1]
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK[1]
ACTIVE to ACTIVE command delay to same bank group for 1KB page size	tRRD	max(4nCK,5.3ns)	-	
Four activate window for 1KB page size	tFAW	max(20nCK,21ns)	-	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	80	-	ps
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	105	-	ps
Power-up and RESET calibration time	tZQinit	1024	-	nCK[1]
Normal operation Full calibration time	tZQoper	512	-	nCK[1]
Normal operation short calibration time	tZQCS	128	-	nCK[1]
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK
4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	260	-	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK[1]
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE	TBD	TBD	ns

Note:
1. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

PHYSICAL DIMENSIONS (UNITS IN INCHES)

(Drawing not to scale)



Note: Tolerance on all dimensions ±0.006 inch (0.15mm) unless otherwise noted

Your Ultimate Memory Solution!