APEX PRECISION POWER — Product Innovation From CIRRUS LOGIC

VRE4112
VRE4125
VRE4141

Precision Voltage Reference

FEATURES

- ♦ +1.250, +2.500, +4.096 V Output
- ♦ Initial Error: ± 0.05% Max.
- ♦ Temperature Drift: 1.0 ppm/ºC Max.
- ♦ Low Noise: 2.2 μV_{P-P} (0.1 Hz-10 Hz, 1.024 V)
- ♦ Low Thermal Hysteresis: 20 ppm
- ♦ ±8 mA Output Source
- ♦ Power Down Mode
- ♦ Industry Standard SOIC 8-pin Package
- ♦ Commercial and Industrial Temp Ranges
- ♦ Second source for ADR29X, REF19X ,LT1460, LT1461, LT1798, MAX616X, REF102

APPLICATIONS

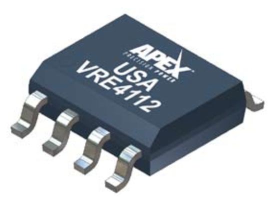
This series is recommended for use as a reference for 14, 16, or 18-bit data converters which require a precision reference. The series offers superior performance over standard on-chip references commonly found with data converters.

DESCRIPTION

The VRE4112/VRE4125/VRE4141 are low cost, high precision bandgap references that operate from +5 V. These devices feature low noise, digital error correction, and an SOIC-8 package. The ultra stable output is 0.05% accurate with a temperature coefficient as low as 1.0 ppm/ºC. The improvement in overall accuracy is made possible by using EEPROM registers and CMOS DAC's for temperature and initial error correction. The DAC trimming is done after assembly which eliminates assembly related shifts.

SELECTION GUIDE

Model	Output (V)	Temp. Coeff. (ppm/ºC)	Temp. Range (ºC)
VRE4112C	+1.250	2.0	0ºC to +70ºC
VRE4112K	+1.250	3.0	-40ºC to +85ºC
VRE4125B	+2.500	1.0	0ºC to +70ºC
VRE4125K	+2.500	3.0	-40ºC to +85ºC
VRE4141B	+4.096	1.0	0ºC to +70ºC
VRE4141K	+4.096	3.0	-40ºC to +85ºC



8-pin SOIC
Package Style FX

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply to any input pin ...... -0.3V to +5.6V
Operating Temp. (B,C) .... 0ºC to 70ºC
Operating Temp. (K) .... -40ºC to +85ºC
Storage Temperature Range ..... -65ºC to +150ºC

Output Short Circuit Duration .... Indefinite
ESD Susceptibility Human Body Model 2kV
ESD Susceptibility Machine Model 200V
Lead Temperature (soldering, 10 sec) .... +260ºC

ELECTRICAL SPECIFICATIONS

V_{PS} = +3 V for VRE4112, V_{PS} = +5 V for VRE4125 and VRE4141. T = +25ºC, I_{LOAD} = 1mA, C_{OUT} = 1µF Unless Otherwise Noted.

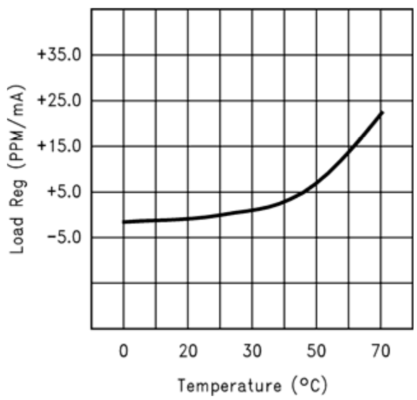
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		+1.8		+5.5	V
Output Voltage Error (Note 1)	V_{OUT}	B Grade		±0.025	±0.050	%
		C/K Grade		±0.040	±0.080	
Output Voltage Temperature Coefficient (Note 2)	TCV_{OUT}	B Grade		+0.5	+1.0	ppm/ºC
		C Grade		+1.0	+2.0	
		K Grade		+1.5	+3.0	
Dropout Voltage (Note 3)	$V_{IN} - V_{OUT}$	I_L = 8mA		160	235	mV
Turn-On Settling Time	T_{ON}	To 0.01% of final value		2		µs
Output Noise Voltage (Note 4)	E_n	0.1Hz < f < 10Hz		2.2		µVp-p
Temperature Hysteresis		Note 5		20		ppm
Long Term Stability	$\Delta V_{OUT/T}$	1000 Hours		50		ppm
Supply Current	I_{IN}	V_{LOAD} = 0mA		230	320	µA
Load Regulation (Note 6)	$\Delta V_{OUT} / \Delta I_{OUT}$	1mA ≤ I_{LOAD} ≤ 8mA		1	20	ppm/mA
Line Regulation (Note 6)	$\Delta V_{OUT} / \Delta V_{IN}$	V_{REF} + 200mV ≤ V_{IN} ≤ 5.5V		20	200	ppm/V
Logic High Input Voltage	V_H		0.8			V
Logic High Input Current	I_H			2		nA
Logic Low Input Voltage	V_L				0.4	V
Logic Low Input Current	I_L			1		nA

NOTES:

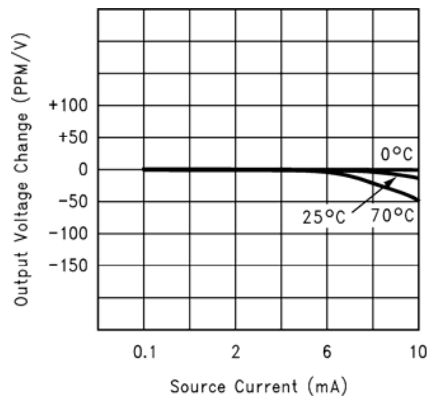
1. High temperature and mechanical stress can effect the initial accuracy of this reference series.See discussion on output accuracy.
2. The temperature coefficient is determined by the box method. See discussion on temperature performance. All units are 100% tested over temperature.
3. The minimum input to output differential voltage at which the output voltage drops by 0.5% from nominal.
4. Based on 1.024 V output. Noise is linearly proportional to V_{REF}.
5. Defined as change in 25ºC output voltage after cycling device over operating temperature range.
6. Line and load regulation are measured with pulses and do not include output voltage changes due to self heating.

2. TYPICAL PERFORMANCE CURVES

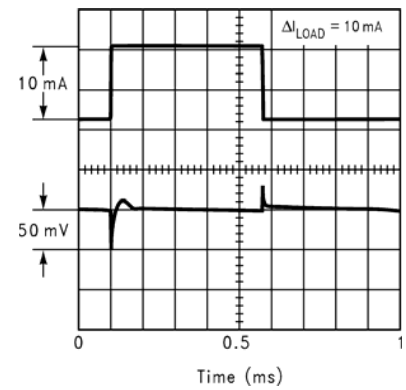
Load Regulation vs Temperature



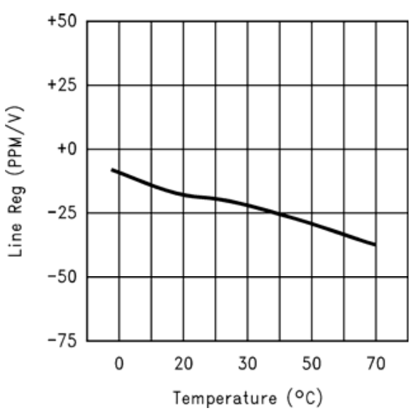
Output Voltage vs Load Current



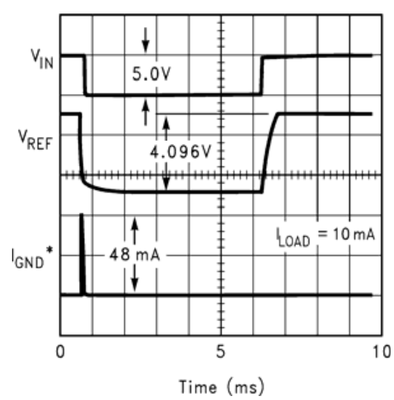
Load Transient Response



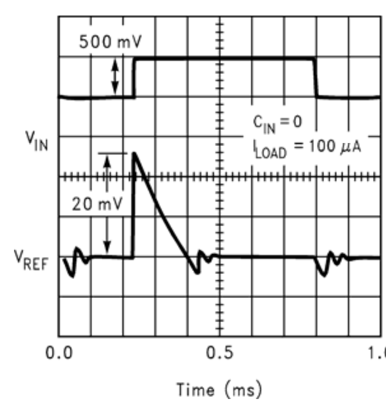
Line Regulation vs Temperature



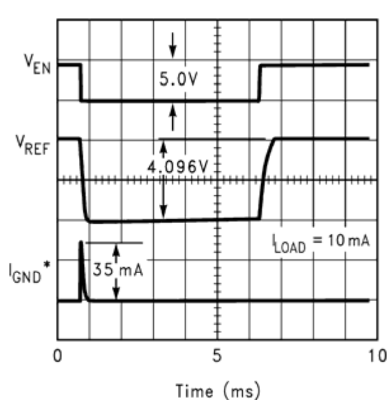
Power Up/Down Ground Current



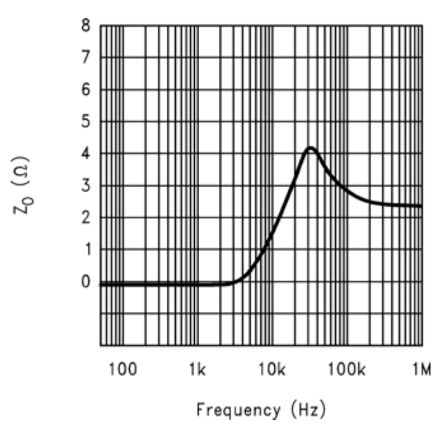
Line Transient Response



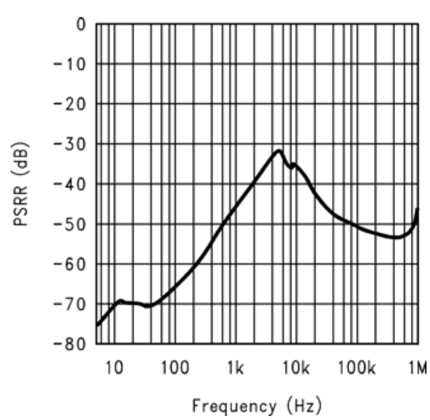
Enable Response



Output Impedance

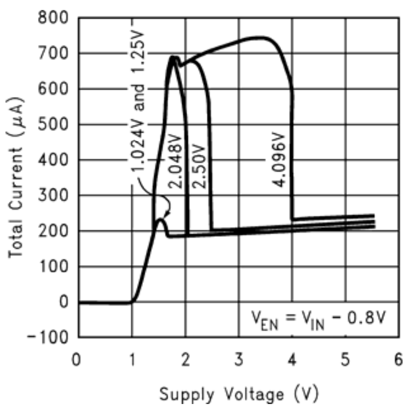


Power Supply Rejection Ratio

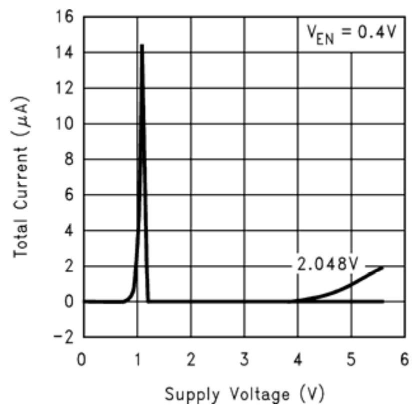


Product Innova tion From

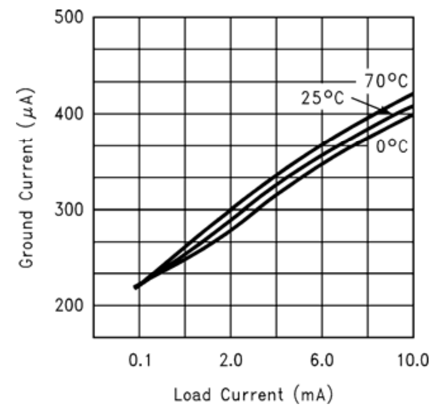
Total Current ($Is_{(ON)}$) vs Supply Voltage



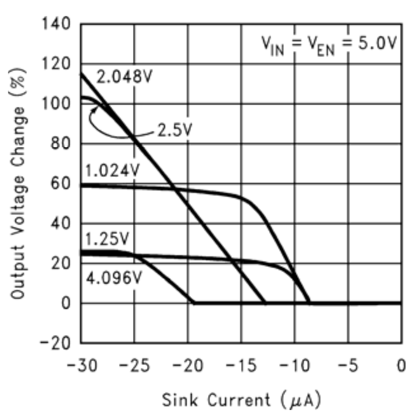
Total Current ($Is_{(OFF)}$) vs Supply Voltage



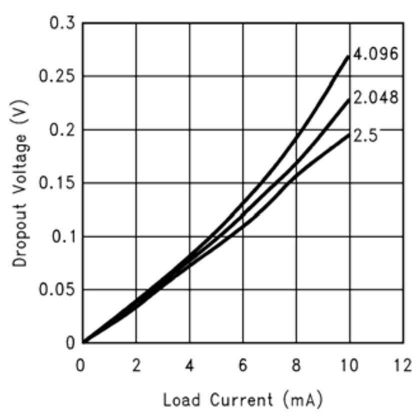
Ground Current vs Load Current



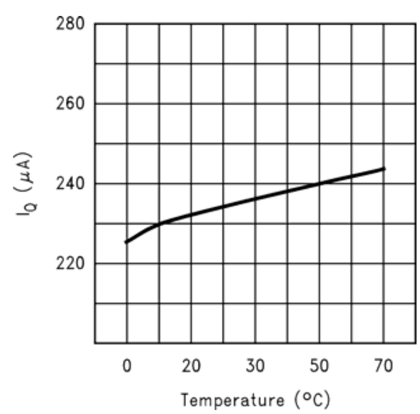
Output Voltage Change vs Sink Current $I_{(SINK)}$



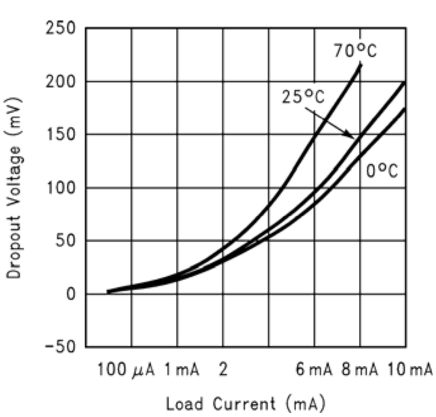
Dropout Voltage vs Load Current



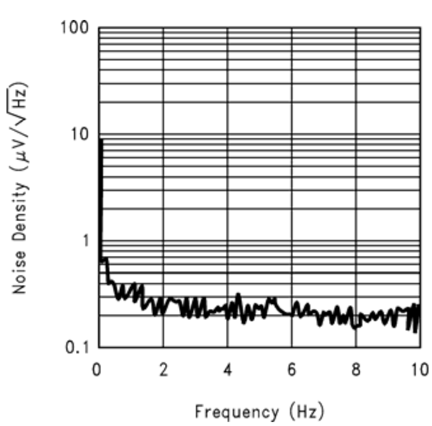
I_Q vs Temperature



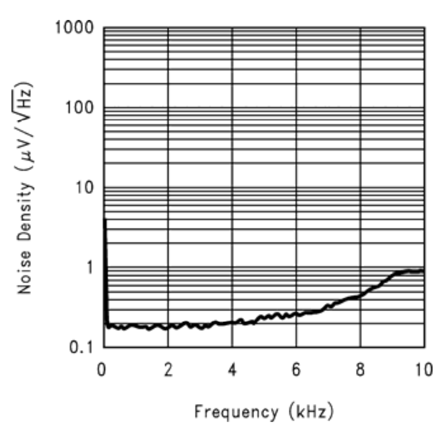
Dropout Voltage vs Load Current (V_{OUT}) = 2.0V



Spectral Noise Density (0.1Hz to 10Hz)



Spectral Noise Density (10Hz to 100kHz)



3. TEMPERATURE PERFORMANCE

This series is designed for applications where the initial error at room temperature and drift over temperature are important to the user. For many instrument manufacturers, a voltage reference with a temperature coefficient of 1ppm/ºC makes it possible to eliminate a system temperature calibration, a slow and costly process.

Of the three TC specification methods (slope, butterfly, and box), the box method is most commonly used. A box is formed by the min/max limits for the nominal output voltage over the operating temperature range. The equation follows:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method guarantees limits for the temperature error but does not specify the exact shape or slope of the device under test.

4. BASIC CIRCUIT CONNECTION

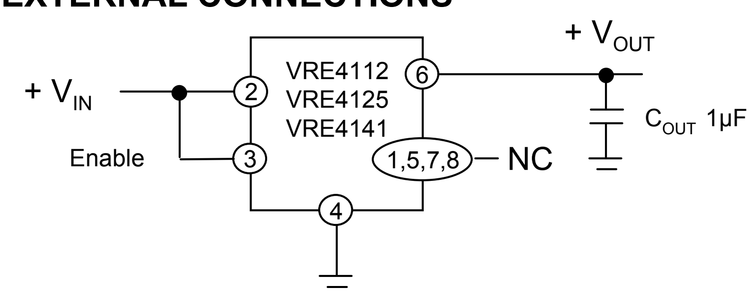
The proper connection for the VRE4112/VRE4125/VRE4141 series voltage references is shown below.

To achieve the specified performance, pay careful attention to the layout. Commons should be connected to a single point to minimize interconnect resistances. This will reduce voltage errors, noise pickup, and noise coupled from the power supply.

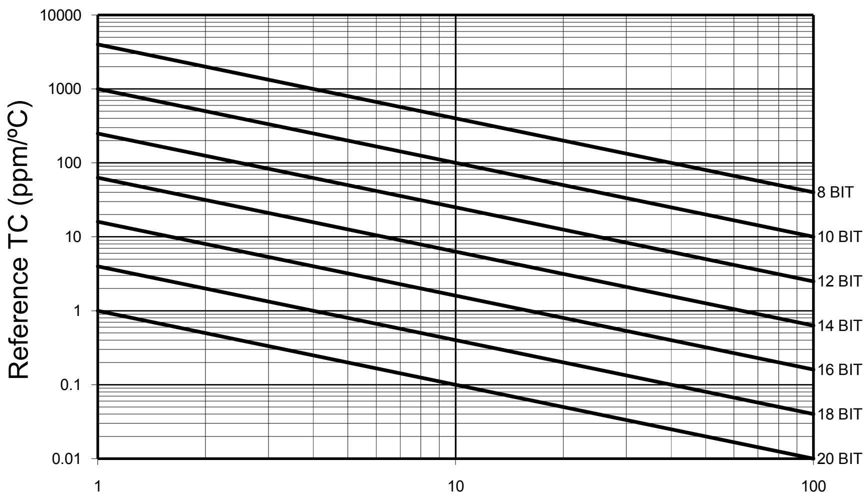
PIN DESCRIPTION

4	GND	These must be connected to ground
2	V_{IN}	Positive power supply input
3	Enable	Pulled to V_{IN} for nominal operation
1,5,7,8	NC	This pin must be left open
6	V_{OUT}	Reference output

EXTERNAL CONNECTIONS



For example a designer who needs a 14-bit accurate data acquisition system over the industrial temperature range (-40ºC to +85ºC), will need a voltage reference with a temperature coefficient (TC) of 1.0ppm/ºC if the reference is allowed to contribute an error equivalent to 1LSB. The required reference TC vs. ∆T change from 25ºC for resolution ranging from 8 bits to 20 bits is shown below.



Reference TC vs. ∆T change from 25°C for 1 LSB change

4. OPERATIONAL NOTES

INPUT CAPACITOR

An input capacitor is recommended for the VRE4112/VRE4125/VRE4141. A supply bypass capacitor on the input will assure that the reference is working from a low impedance source which will improve stability. It can improve the transient response when the load current is suddenly increased.

OUTPUT CAPACITOR

This series requires a 1 µF output capacitor for loop stabilization (compensation) as well as transient response. When the load current changes, the output capacitor must source or sink current during the time it takes the control loop of the device to respond.

The output capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR) range. See Capacitor Selection below.

CAPACITOR SELECTION

A minimum value of 0.2 µF over the operating temperature range is recommended. For a 0.22 µF capacitor the ESR range for 0°C to +70°C is 0.9 to 6.0; 1.0 µF is 0.8 to 6.0; and 10 µF is 0.4 to 7.0.

Surface mount tantalum capacitors offer small size for the value and ESR in the range required for this series. The optimum performance for the output capacitor is achieved with a 1.0 µF value.

Aluminum electrolytic capacitors have a relatively large size for the value. They meet the ESR requirements at 1.0 µF as long as the temperature is above 0°C. Below 0°C, the ESR increases and it may exceed the limits indicated in the figures.

Multilayer ceramic capacitors have a small size for the value, are available in surface mount, and have excellent RF characteristics. They may not meet the minimum ESR requirements and have a large change in value with temperature.

REVERSE CURRENT PATH

The P-channel pass transistor used in this series has an inherent diode connected between the Vin and VOUT pins. Forcing the output to voltages higher than the input or pulling Vin below the voltage stored in the output capacitor by more than the Vbe will forward bias this diode and current will flow from the Vout pin to Vin. This will not damage the device as long as the current does not exceed 50 mA.

ON/OFF OPERATION

This series features a sleep mode that is activated by pulling the enable pin low. To turn the reference on, the enable pin is pulled high. If this feature is not used, the enable pin should be tied to Vin to keep the reference on at all times. The enable pin must not be left unconnected (floating).

When powered off, these devices will quickly reduce both Vout and IQ to zero. During power down, the charge across the output capacitor is discharged to ground through the internal circuitry. On power up, the Vout is restored in less than 200 µs.

The signal source used to drive the enable pin can come from either a totem-pole output or an open collector output with a pull-up resistor to the input voltage. The signal source must be able to swing above and below the voltage thresholds to guarantee an ON or OFF state. It must not exceed the absolute maximum rating for the enable pin.

OUTPUT ACCURACY

The output accuracy after assembly at room temperature is made up of three components: initial accuracy of the device, thermal hysteresis, and mechanical stress. The initial accuracy is measured at the factory and may not reflect the actual output voltage when the devices are mounted to a PCB. The effects of mechanical stress and thermal hysteresis can shift the output voltage.

THERMAL HYSTERESIS

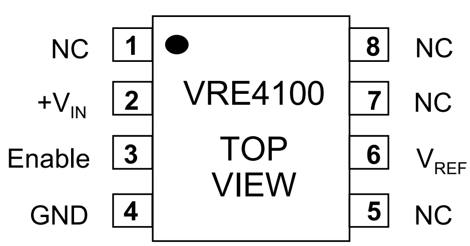
Thermal hysteresis is a change in output voltage as a result of a temperature change. When references experience a temperature change and return to the initial temperature, they do not always have the same initial voltage. Thermal hysteresis is difficult to correct and is a major error source in systems that experience temperature changes greater than 25°C. Reference vendors are starting to include this important specification in their datasheets

MECHANICAL HYSTERESIS

Recommendations to minimize mechanical stress:

1) Mount the VRE4112/VRE4125/VRE4141 near the edges or corners of the PCB. The center of the board generally has the highest mechanical and thermal stress.
2) Mechanically isolate the device by cutting a U shaped slot around the package. This provides some mechanical and thermal isolation from the rest of the circuit.

PIN CONFIGURATION



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