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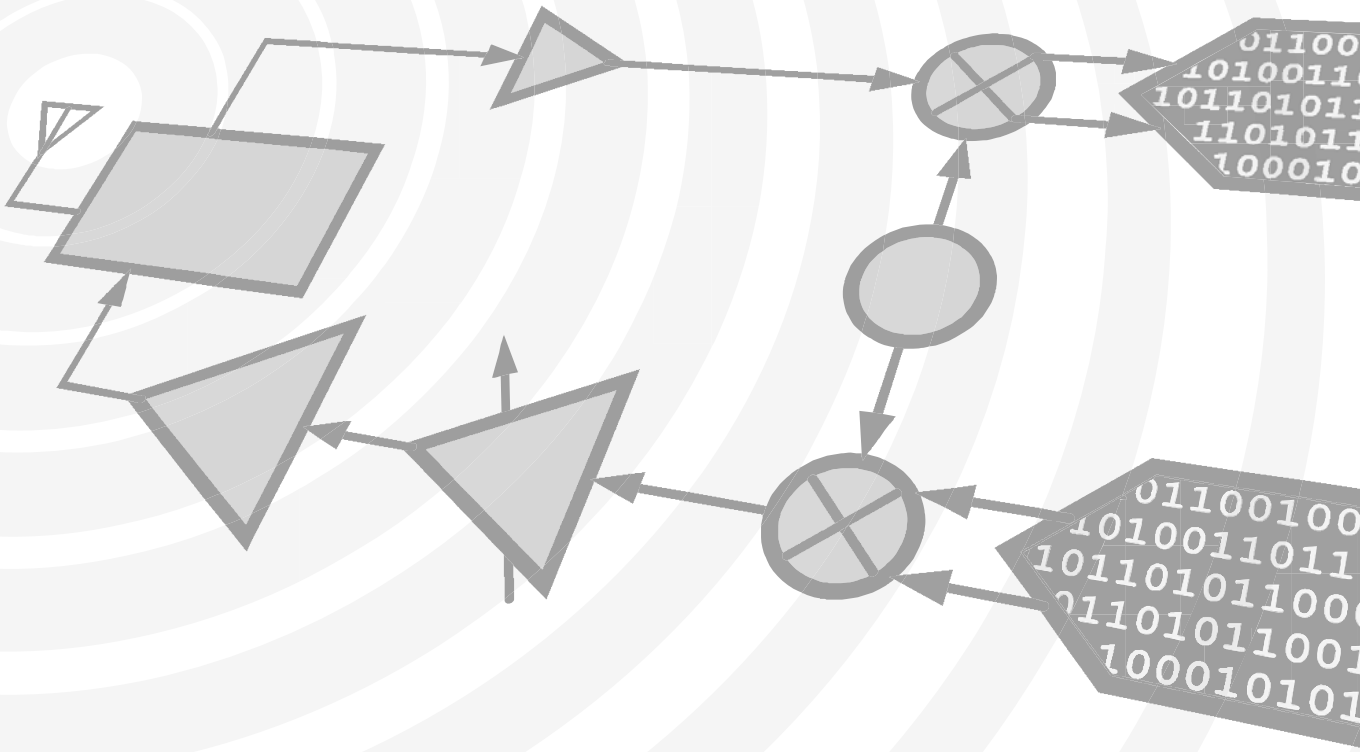
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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v04.0514

DISCONTINUED PRODUCT

HMC660LC4B

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Typical Applications

The HMC660LC4B is ideal for:

- RF ATE Applications
- Digital Sampling Oscilloscopes
- RF Demodulation Systems
- Digital Receiver Systems
- High Speed Peak Detectors
- Software Defined Radio
- Radar, ECM & ELINT Systems
- High Speed DAC De-Glitching

Features

4.5 GHz Input bandwidth (1 Vpp Full Scale)

3 GS/s Maximum Sampling Rate

61 dB SFDR (4 GHz / 0.5 Vpp Input, CLK = 1 GS/s)

55 dB SFDR (4 GHz / 1 Vpp Input, CLK = 1 GS/s)

Ultra-clean Output Waveforms, Minimal Glitching

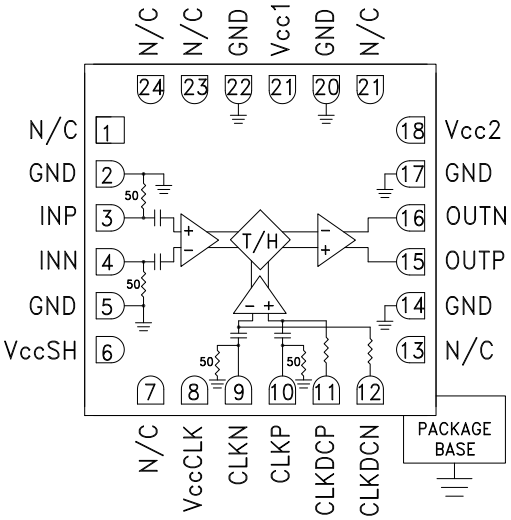
>60 dB Hold Mode Feedthrough Rejection

1.05 mV RMS Hold Mode Output Noise

Single / Dual Rank Evaluation Boards Available

RoHS Compliant 4x4 mm SMT Package

Functional Diagram



General Description

The HMC660LC4B is a SiGe monolithic, fully-differential, track-and-hold that provides unprecedented bandwidth and performance to wideband sampled signal systems. The novel design and low aperture jitter enable 9 to 10-bit signal capture from 20 MHz to 4.5 GHz while sampling to 3 GS/s. The narrow sampling aperture allows signal acquisition at frequencies well beyond the input bandwidth. The output can be held for 5 ns, enabling lower-speed ADCs to sub sample a high frequency wideband input signal.

Electrical Specifications T_A = +25C, See Test Conditions on following page herein.

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Analog Inputs (INP, INN)						
Differential Full Scale Range				1		Vpp
AC Coupling Low Frequency Corner				16		MHz
Input Resistance	Each lead to ground			50		Ω
Return Loss	0 to 5 GHz			12		dB
DC Clock Inputs (CLKDCP, CLKDCN)						
Common Mode Voltage			2	2.5	3	V
Differential Clock High Voltage (Track Mode)			20	40	2000	mV
Differential Clock Low Voltage (T/H Mode)			-20	-40	-2000	mV
Differential Input Current				10		µA
Common Mode Input Current	CLKDCP, CLKDCN @ 2.5V			6		µA
AC Clock Inputs (CLKP, CLKN)						
Amplitude (Sinusoidal Input)	Per input terminal		-10	0	10	dBm

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Electrical Specifications, (continued)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Clock Slew Rate	Recommended for best linearity			4		V/ns
Input Impedance				50		Ω
Return Loss	0 - 3 GHz			16		dB
Input Resistance				50		Ω
Analog Outputs (OUTP, OUTN)						
Differential Full Scale Range				1		Vpp
Common Mode Output Voltage				4.0		V
Output Impedance				50		Ω
Return Loss	0 - 4 GHz			15		dB
Track Mode Dynamics						
Gain				0		dB
Track Mode Bandwidth	@ 1 Vpp Input			3.95		GHz
Lower Frequency Corner				16		MHz
Single Tone SFDR @ 500 MHz	1 Vpp Input			54.8		dB
Single Tone SFDR @ 1000 MHz	1 Vpp Input			54.7		dB
Single Tone SFDR @ 2000 MHz	1 Vpp Input			52.6		dB
Single Tone SFDR @ 3000 MHz	1 Vpp Input			50.4		dB
Single Tone SFDR @ 4000 MHz	1 Vpp Input			49		dB
Two Tone SFDR @ 500 MHz	0.5 Vpp Input			57.4		dB
Two Tone SFDR @ 995/1005 MHz	0.5 Vpp Input per Tone			56.4		dB
Two Tone SFDR @ 1995/2005 MHz	0.5 Vpp Input per Tone			54.5		dB
Two Tone SFDR @ 2995/3005 MHz	0.5 Vpp Input per Tone			52.5		dB
Two Tone SFDR @ 3995/4005 MHz	0.5 Vpp Input per Tone			50.2		dB
Noise Spectral Density	@ 1 GHz			8.9		nV/√Hz
Integrated Noise [2]				0.95		mV RMS
Hold Mode Dynamics						
Sampling Bandwidth	@ -3 dB Gain, 1 Vpp Input Level			4.5		GHz
Differential Droop Rate				0.5		%/ns
Feedthrough Rejection	0 - 4000 MHz			≥ 60		dB
Integrated Noise [2]	500 MHz Clock Frequency			1.04		mV RMS
Maximum Hold Time				5		ns
Single Tone THD/SFDR 995 MHz	[1]			-54 / 54		dB
Single Tone THD/SFDR 1995 MHz	[1]			-58 / 58		dB
Single Tone THD/SFDR 2995 MHz	[1]			-59 / 61		dB
Single Tone THD/SFDR 3995 MHz	[1]			-54 / 54		dB
Track-to-Hold Switching						
Aperture Delay				-6		ps
Aperture Jitter	[1]			84		fs
Settling Time to 1 mV	Simulated Value			206		ps
Differential Pedestal	500 MHz Clock Frequency, 0 dBm Clock Power			-0.3		%
Clock Frequency			100		3000	MHz
Clock Buffer Pipeline Delay				38		ps

[1] 1 Vpp Input Level, 1 GS/s Clock, Clock Power = 6 dBm / input terminal.
[2] Noise bandwidth limited by output amplifier bandwidth of ~7 GHz.

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

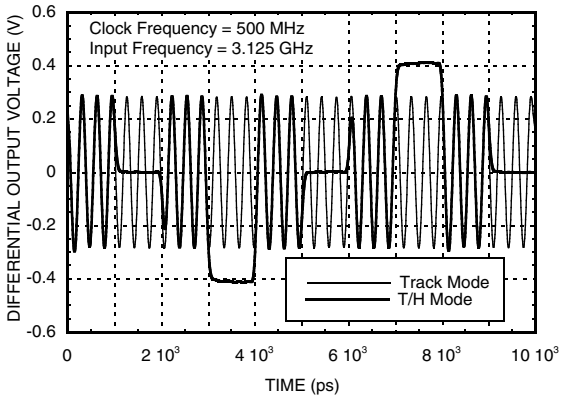
Electrical Specifications, (continued)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Hold-to-Track Switching						
Acquisition Time to 1 mV	Simulated Value			205		ps
Power Supply Requirements						
VccSH Voltage			4.75	5	5.25	V
VccSH Current				61		mA
Vcc1 Voltage			4.75	5	5.25	V
Vcc1 Current				50		mA
Vcc2 Voltage			5.7	6	6.3	V
Vcc2 Current				84		mA
VccCLK Voltage			4.75	5	5.25	V
VccCLK Current				20		mA
Power Dissipation				1.16		W

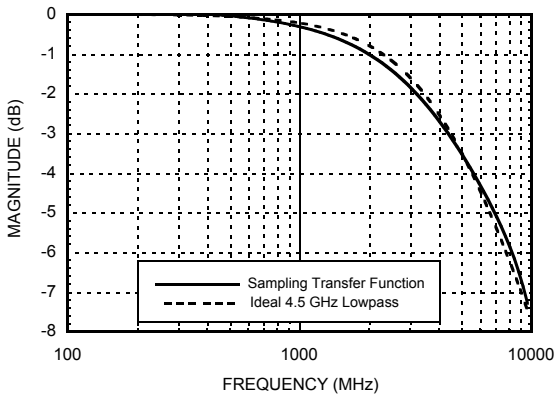
Test Levels

1. 100% production tested at T_A = +25C
2. Guaranteed by design/characterization testing
3. Sample Tested
4. Typical value only

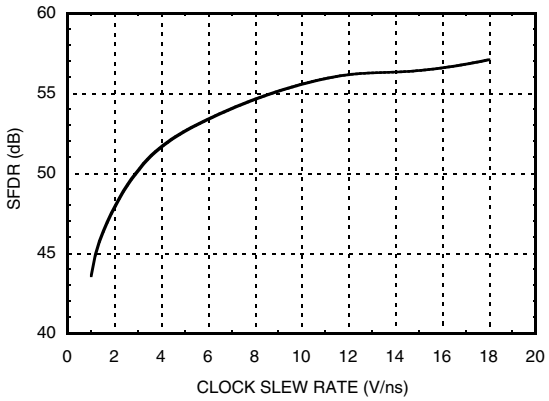
Time Domain Output Waveform



Sampling Transfer Function



Dual Rank Second Order SFDR vs. Clock Slew Rate @ 4 GHz Input Frequency [1]

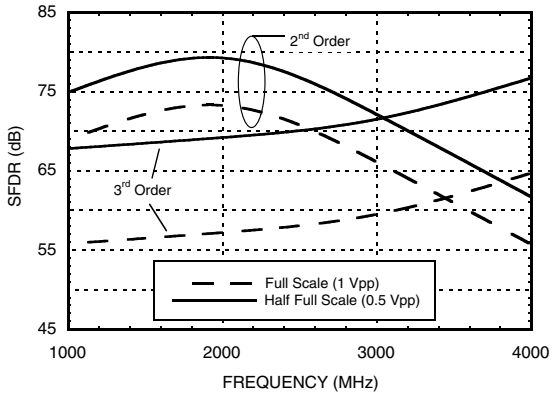


[1] Data is derived from linearity measurements at clock frequencies from 0.5 to 3.0 GHz.

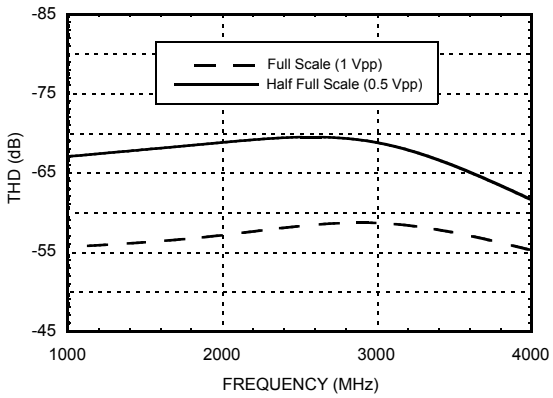
0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

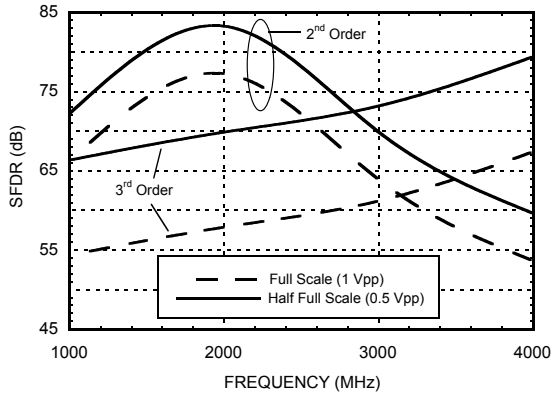
Hold-Mode SFDR vs. Frequency & Input Power [1]



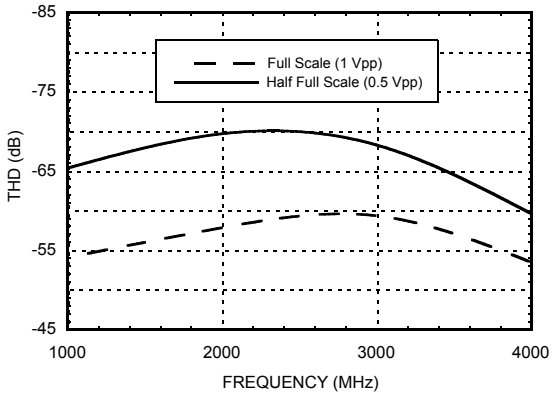
Hold-Mode THD vs. Frequency & Input Power [1]



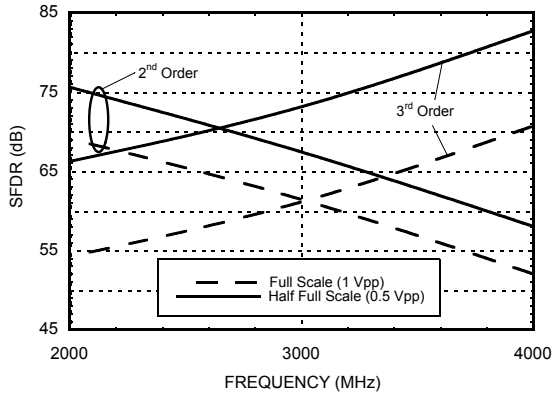
Hold-Mode SFDR vs. Frequency & Input Power [2]



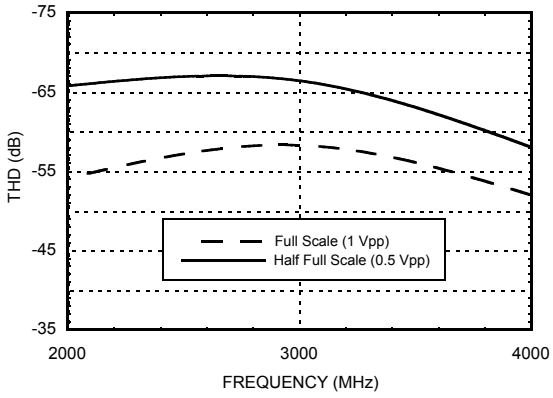
Hold-Mode THD vs. Frequency & Input Power [2]



Hold-Mode SFDR vs. Frequency & Input Power [3]



Hold-Mode THD vs. Frequency & Input Power [3]



[1] Square Wave Clock: 0.5 GS/s @ 6.3 V/ns Slew Rate

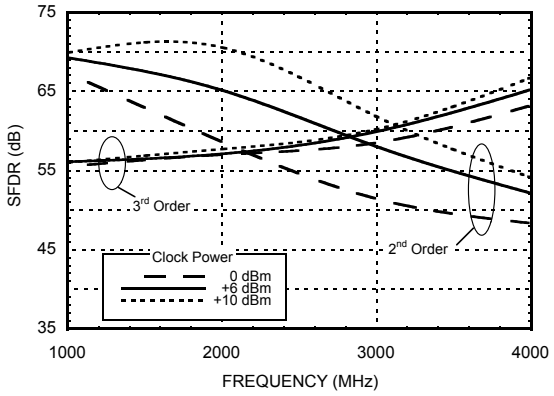
[2] Clock Power = +6 dBm, Clock Rate 1 GS/s

[3] Clock Power = 0 dBm, Clock Rate 2 GS/s

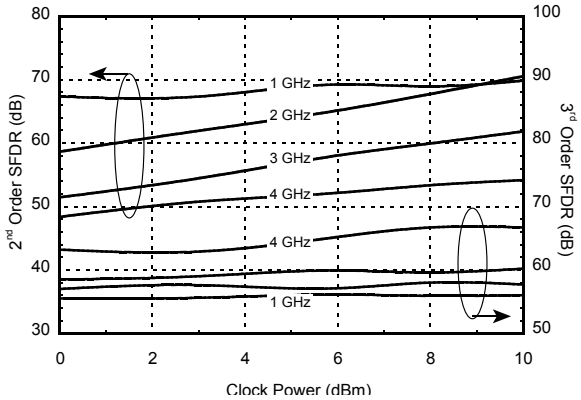
0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

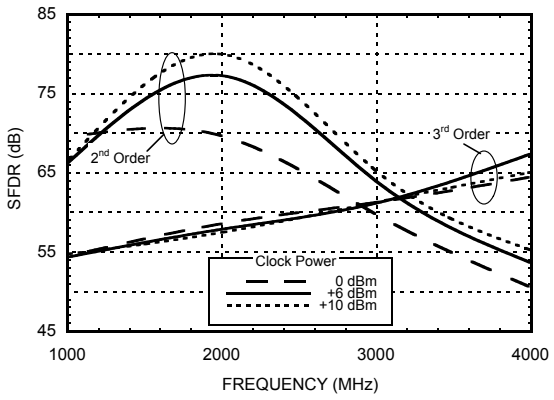
Hold-Mode SFDR vs. Frequency & Clock Power @ Full Scale (1Vpp) [1]



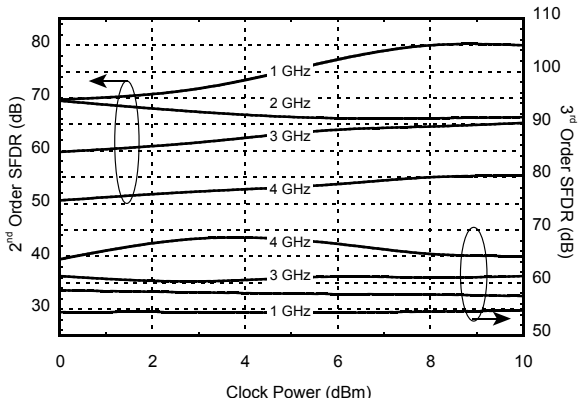
Hold-Mode SFDR vs. Clock Power & Clock Frequency @ Full Scale (1Vpp) [1]



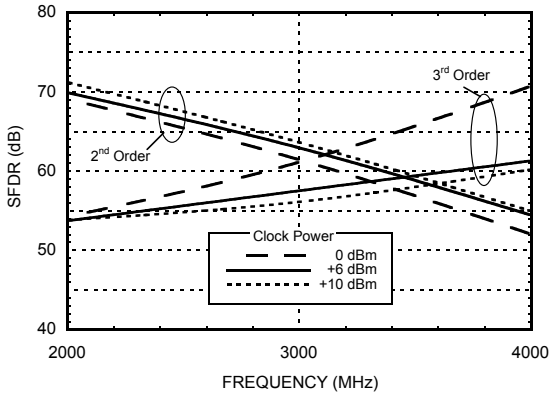
Hold-Mode SFDR vs. Frequency & Clock Power @ Full Scale (1Vpp) [2]



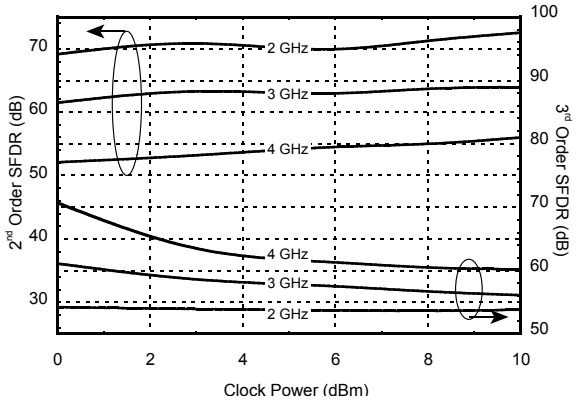
Hold-Mode SFDR vs. Clock Power & Clock Frequency @ Full Scale (1Vpp) [2]



Hold-Mode SFDR vs. Frequency & Clock Power @ Full Scale (1Vpp) [3]



Hold-Mode SFDR vs. Clock Power & Clock Frequency @ Full Scale (1Vpp) [3]



[1] Clock Rate 0.5 GS/s
[2] Clock Rate 1 GS/s
[3] Clock Rate 2 GS/s

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

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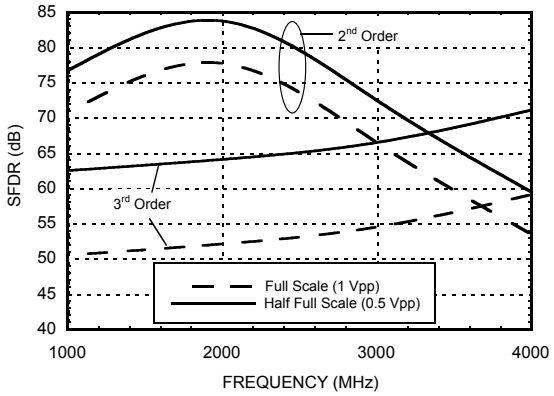
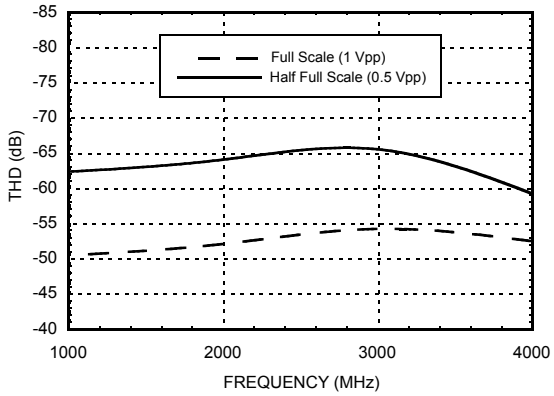
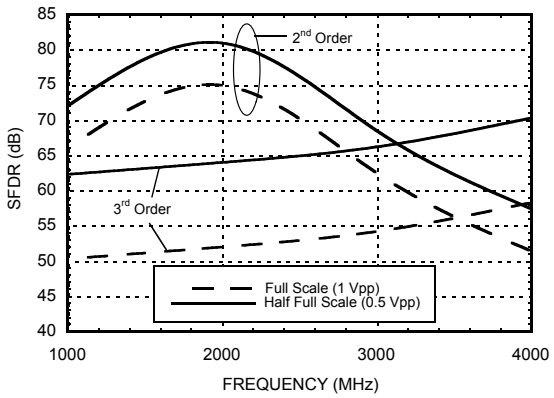
Dual Rank Hold-Mode SFDR vs. Frequency & Input Power [1]



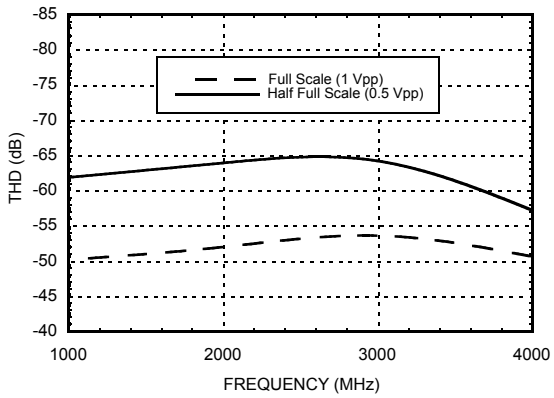
Dual Rank Hold-Mode THD vs. Frequency & Input Power [1]



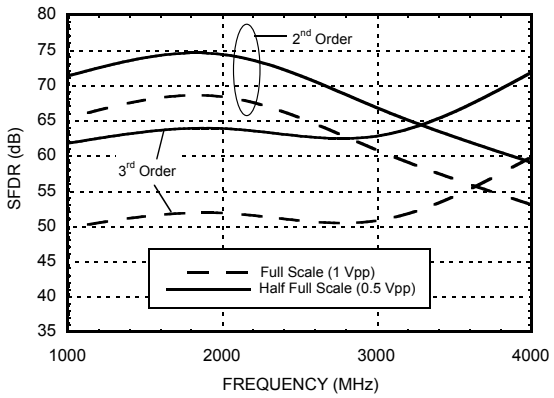
Dual Rank Hold-Mode SFDR vs. Frequency & Input Power [2]



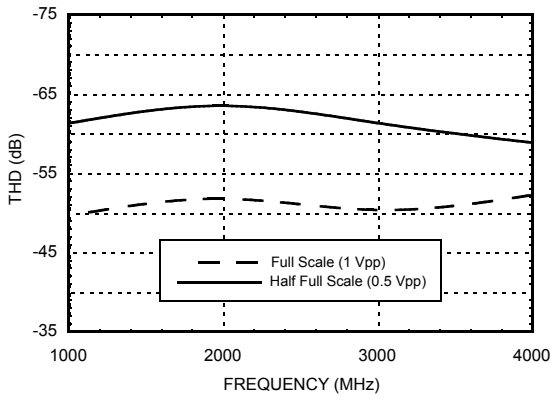
Dual Rank Hold-Mode THD vs. Frequency & Input Power [2]



Dual Rank Hold-Mode SFDR vs. Frequency & Input Power [3]



Dual Rank Hold-Mode THD vs. Frequency & Input Power [3]



[1] Square Wave Clock: 0.5 GS/s @ 6.3 V/ns Slew Rate

[2] Clock Power = +6 dBm, Clock Rate 1 GS/s

[3] Clock Power = 0 dBm, Clock Rate 2 GS/s

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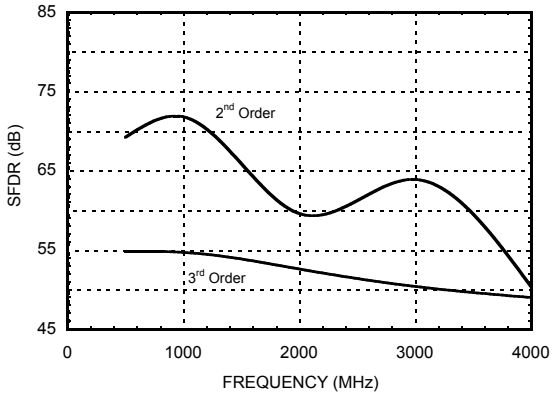
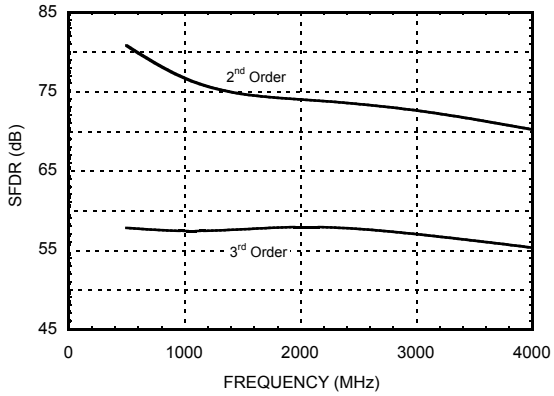
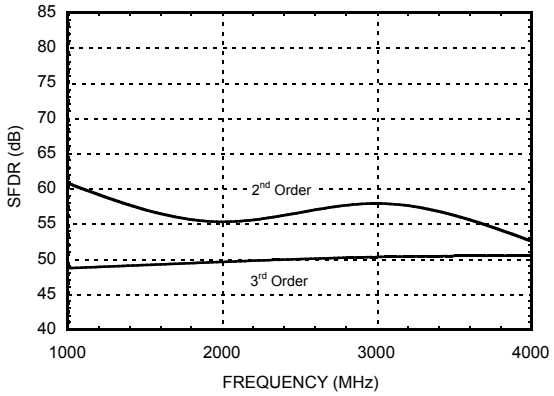
Track-Mode Single-Tone SFDR vs. Frequency [1]



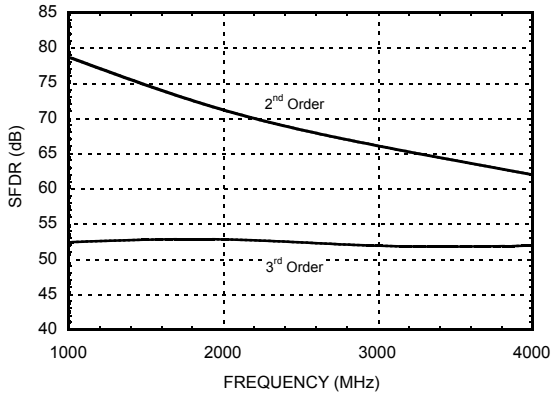
Track-Mode Two-Tone SFDR vs. Frequency [2]



Dual Rank Track-Mode Single-Tone SFDR vs. Frequency [1]



Dual Rank Track-Mode Two-Tone SFDR vs. Frequency [2]



[1] Input Voltage = 1 Vpp

[2] 10 MHz Tone Separation, 0.5 Vpp per Tone

Definition of Specifications

Aperture Delay: The delay of the exact sample time relative to the time that the hold command is applied to the device. It is the difference between the delay of the clock switching transition to the hold node and the input signal group delay to the hold node. If the input signal group delay to the hold node exceeds the clock delay this quantity can be negative.

Aperture Jitter: The standard deviation of the sample instant in time.

Acquisition Time: The interval between the internal hold-to-track transition and the time at which the hold-node signal is tracking the input signal within a specified accuracy. It does not include the pipeline delay of the clock buffer.

Differential Pedestal: An error term in the sample value caused by charge redistribution in the T/H switch during the sampling transition. In general, the pedestal can consist of three components: a fixed offset, a component that is linearly related to input signal amplitude, and a component that is nonlinearly related to input signal amplitude. The majority of the pedestal is usually linear. A small nonlinear component can cause sampling nonlinearity.

Differential Droop Rate: The slow drift in the differential output voltage of a held sample while the T/H is in hold-mode. It is typically caused by current leakage on the hold capacitors and corresponds to a decay in the held voltage with increasing time. The majority of the voltage droop over a given time is usually linearly related to the held sample voltage and is expressed as a percentage of initial amplitude per unit time. Since it is mostly linear, the droop causes little nonlinearity.

Feedthrough Rejection: A measure of the off-state (hold-mode) isolation of the T/H's internal switch. It is defined as the ratio of the amplitude of the output signal (for a sinusoidal input) feeding through during the hold mode to the amplitude of the output signal during track mode. Normalization by the track-mode signal gives the true switch isolation without the effects of the output amplifier bandwidth limiting.

Full Scale Range: The voltage range between the minimum and maximum signal levels that can be handled by the T/H while still meeting the specifications.

Gain Flatness: The deviation in gain over a specified input band relative to a specified mid-frequency gain.

Sampling Bandwidth: The -3 dB bandwidth of the sampled signal levels represented by the held sample amplitudes. It includes both the bandwidth of the transfer function from the signal input to the hold-node and any band-limiting effects associated with the finite time duration of the sampling aperture.

Settling Time: The interval between the internal track-hold transition and the time at which the held output signal is settled to within a specified accuracy. It does not include the pipeline delay of the clock buffer.

Spurious Free Dynamic Range (SFDR): The ratio (usually expressed in dB) between the sinusoidal output signal amplitude and the amplitude of the largest non-linearity product falling within one Nyquist bandwidth. It may be specified for both full scale input and some fraction(s) of full scale input. A SFDR based only on 2nd order nonlinear products is referred to as the 2nd order SFDR (SFDR2). A SFDR based only on 3rd order products is referred to as the 3rd order SFDR (SFDR3).

Total Harmonic Distortion (THD): The ratio of the total power in the non-linearity-generated harmonics and harmonic aliases (measured in one Nyquist band) to the output signal power.

Application Notes

ESD: On-chip ESD protection networks are incorporated on the terminals, but the RF/microwave compatible interfaces provide minimal protection and ESD precautions should be used.

Power Supply Sequencing: The recommended power supply startup sequence is Vcc2, Vcc1, VccSH, VccCLK, (CLKDCP, CLKDCN) if biased from independent supplies. Vcc1, VccSH, VccCLK can be connected to one +5V supply if desired.

Input Signal Drive: For best results, the inputs should be driven differentially. The input circuit has an on-chip resistive bias-T for separating the DC and RF components of the input. The low frequency corner of the RF path is approximately 16 MHz (Coupling=10 pF, Rdc=1.28 K ohm). The input can be driven single-ended but the linearity of the device will be degraded somewhat.

Clock Input: The clock inputs should be driven differentially if possible. The device is in track-mode when (CLKP – CLKN) is high and it is in hold-mode when (CLKP-CLKN) is low.

The T/H-mode 2nd order linearity of the device varies somewhat with clock slew rate as shown in the performance data plots. Because of the slew rate dependence, the 2nd order linearity will vary somewhat with clock power for sinusoidal signals. For optimal linearity, a clock zero-crossing slew rate of roughly 4 V/ns (per clock input) or more is recommended. For sinusoidal clock inputs, this corresponds to a sinusoidal clock power per differential half-circuit input of -3.5 dBm at 3 GHz, 0 dBm at 2 GHz, and 6 dBm at 1 GHz.

At clock frequencies lower than 1 GHz, a square wave clock will provide the best 2nd order linearity performance. The clock input circuit has an on-chip resistive bias-T for separating the DC and RF components of the input. The low frequency corner of the RF path is approximately 9 MHz (Coupling=10 pF, Rdc = 1.7 K ohm with clock DC shorted).

Outputs: The outputs should be sensed differentially for the cleanest output waveforms. The output impedance is 50Ω resistive returned to the Vcc2 supply. If the load is also 50Ω returned to the Vcc2 supply, then the Vcc2 supply should be 5V. If the output is capacitively coupled to 50Ω then the Vcc2 supply should be 6V. The bandwidth of the output amplifier (beyond the hold-node) is approximately 7 GHz. This produces approximately a 1 dB roll-off at the 3 dB bandwidth of the hold node (4.5 GHz) resulting in an overall track-mode 3 dB bandwidth of approximately 3.9 GHz. Hence, the output amplitude of the sampled waveform may be somewhat larger than the track mode response at high input frequencies due to the effect of the output amplifier bandwidth.

The output amplifier noise contribution to the total output noise is substantial. If desired, a significant reduction in output noise can be achieved by filtering the output to a lower bandwidth than the output amplifier bandwidth of 7 GHz. This is particularly effective if operating at lower clock rates. For example, the output noise can be reduced by approximately 4 dB if the output bandwidth is reduced by a factor of four from 7 GHz down to 1.75 GHz.

The output will have very sharp transitions at the clock edges due to the broad output amplifier bandwidth. The user should be aware that any significant length of cable between the chip output and the load will cause frequency response roll-off and dispersion that can produce low amplitude tails with relatively long time-constants in the settling of the output waveform into the load. This effect is most noticeable when operating in a lab setting with output cables of a few feet length, even with high quality cable. Output cables between the T/H and the load should be of very high quality and 2 ft or less in length.

Reflections between the load and the device will also degrade the hold mode response. The output cable length can be adjusted to minimize the reflection perturbations to some extent. In general, the round trip transit time of the cable should be an integer number of clock periods to obtain the minimal reflection perturbation in the hold mode portion of the waveform. The optimal performance is obtained when the T/H is within 50 ps or less of the load since this gives a reflection duration equal to the approximate settling time of the device.

Linearity Measurement and Calculation

When characterizing the linearity of a T/H, the transfer function linearity of the held samples (referred to as T/H-mode linearity) is usually the quantity of most interest to the user. These samples contain the signal information that is ultimately digitized by the downstream A/D converter. Since the T/H-mode linearity is often different than the track-mode linearity, this presents a unique measurement issue in that the linearity of only the hold-portion of the analog output waveform must be selectively measured.

This issue is aggravated for high speed T/Hs because there are few wide-band time domain instruments (oscilloscopes or A/D converters) with sufficient linearity to characterize a high linearity T/H. Therefore a frequency domain instrument (spectrum analyzer) and measurement technique are used which allow selective characterization of the hold-mode portion of the waveform

A common approach to this requirement has been to cascade two T/Hs in a dual rank configuration such that the second T/H (T/H 2) re-samples the output of the first T/H (T/H 1). The two T/Hs are usually clocked 180 degrees out-of-phase in master-slave operation to eliminate the track-mode portion of the output waveform from the first T/H. This arrangement produces an output waveform that consists of two time segments. The first segment is the T/H 1 hold-mode output as observed through the T/H 2 track-mode transfer function. The second time segment is the T/H 1 hold-mode output re-sampled and held by the T/H 2 device. This measurement approach is not a perfect representation of the linearity of a single T/H due to the impact of the second T/H on the overall linearity. However, it does eliminate the track-mode portion of the T/H 1 output and permits a spectrum analyzer linearity measurement of the cascaded devices. Since T/H 2 only has to sample the held waveform from T/H 1, the linearity impact of T/H 2 is primarily associated with its DC linearity. An often used approximation is that the DC linearity of T/H 2 is much higher than the slew-rate dependent, high frequency linearity of T/H 1 so that the total non-linearity of the cascade is dominated by the high frequency linearity of T/H 1. In this case, the dual rank configuration has a net linearity that closely resembles the linearity of a single T/H, particularly at high frequencies. However, this approximation is not always valid. If not, the dual rank configuration fails to represent the linearity of a single T/H. The HMC660LC4B represents such a case; the 3rd order nonlinearity of this device varies relatively slowly with frequency and is high enough over the T/H bandwidth that the DC linearity of the 2nd T/H significantly impacts the overall dual rank configuration.

Another linearity measurement issue unique to the T/H device is the need for output frequency response correction. In the case of a dual rank T/H, the output waveform resembles a square wave with duration equal to the clock period. Mathematically, the output can be viewed as the convolution of an ideal delta-function sample train with a single square pulse of duration equal to one clock period. This weights the output spectral content with a SIN(πf/fs)/(πf/fs) (Sinc) function frequency response envelope which has nulls at harmonics of the clock frequency fs and substantial response reduction beyond half the clock frequency. The spectral content of the held samples without the envelope weighting is required for proper measurement of the sample's linearity. Either the impact of the response envelope must be corrected in the data or a measurement method must be used that heterodynes the relevant nonlinear harmonic products to low frequencies to avoid significant envelope response weighting. This latter method is referred to as the beat-frequency technique.

The beat-frequency technique is commonly used for high-speed T/H linearity measurements, although the measurement does impose restrictions on the specific input signal and clock frequencies that can be used. For example, with a clock frequency of 512.5 MHz, a single tone input at 995 MHz beats with the 2nd harmonic of the sampling frequency (through the sampling process) to produce a 1st order beat product at 30 MHz. Likewise, the 2nd and 3rd harmonics of the input signal (generated via distortion in the T/H) beat with the 4th and 6th harmonics of the sampling frequency respectively to produce 2nd and 3rd order beat products at 60 MHz and 90 MHz. In this manner, the T/H nonlinearity in the vicinity of 1 GHz can be measured even though the 995 MHz fundamental and the 1.99 GHz and 2.985 GHz nonlinear harmonics are well beyond the 206 MHz bandwidth of the Sinc response envelope.

The possible input frequency choices are overly limited when the low frequency beat-product technique is used at high clock rates. A related high frequency beat-product measurement utilizing correction for the Sinc envelope weighting must be employed to measure linearity over a wide range of input frequencies. Hittite uses both low frequency and high frequency beat product methods to measure linearity for a wide range of clock and signal frequencies. Our high frequency beat-product measurement avoids excessive envelope correction error by maintaining all beat products within the 4 dB bandwidth of the Sinc function, where the envelope response is well behaved and easily modeled.

Hittite has also developed a method for accurately measuring the held-sample linearity of a single T/H using a beat-frequency technique that avoids errors due to nonlinear products associated with the track-mode portion of the

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

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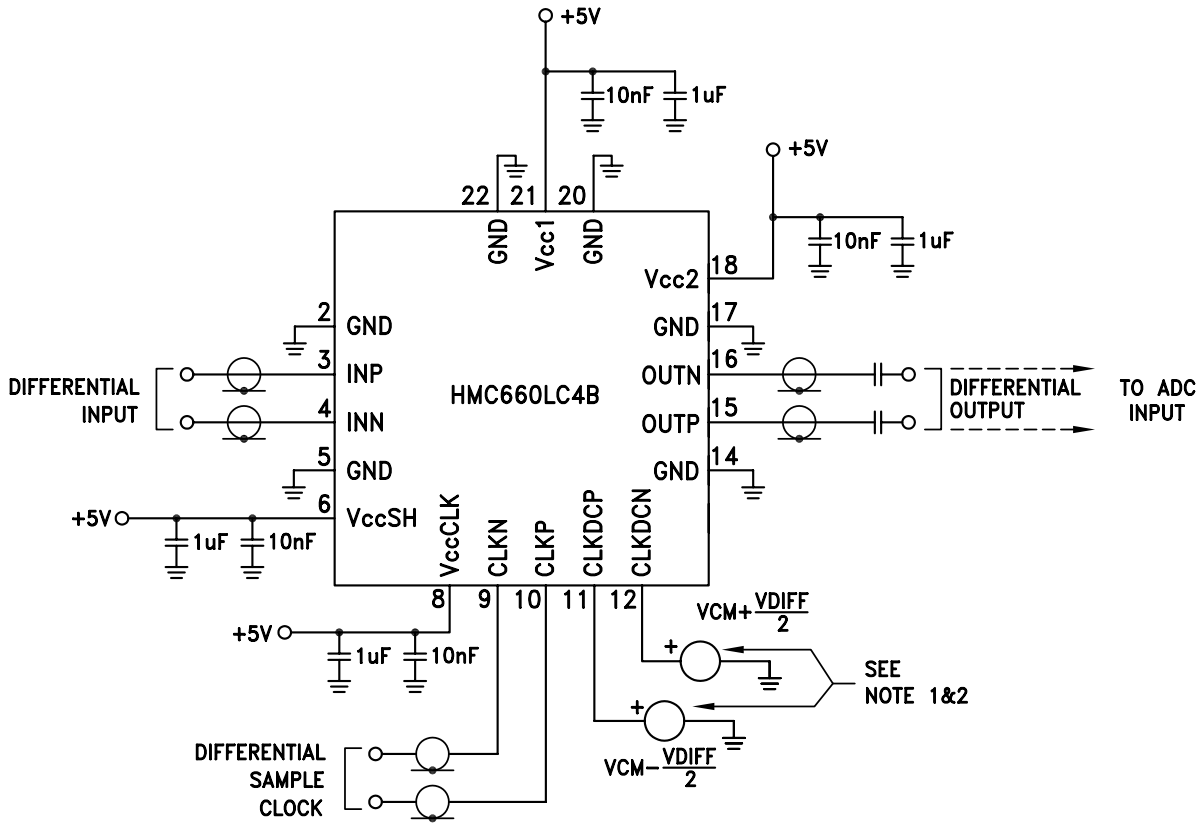
Linearity Measurement and Calculation (Continued)

waveform. This single T/H linearity measurement method provides accurate results for clock frequencies up to about 2 GHz. This method is used to characterize and specify the linearity of a single T/H in the data sheet, in addition to the usual dual rank configuration linearity measurements. Detailed information on the measurement technique and theory can be found in the Application Note *T/H Linearity Measurement Issues and Methods* available at www.hittite.com.

Typical Operating Circuit



Notes:

1. For track mode operation, CLKDCP and CLKDCN must be driven as shown above. VCM = 2.5V, VDIFF = 40mV typical.
2. For track-and-hold mode operation, pin 11 and 12 may be left floating, or V_{DIFF} can be set to zero.
3. All differential inputs are terminated on-chip with 50 ohms to ground.

HMC660LC4B

v04.0514

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

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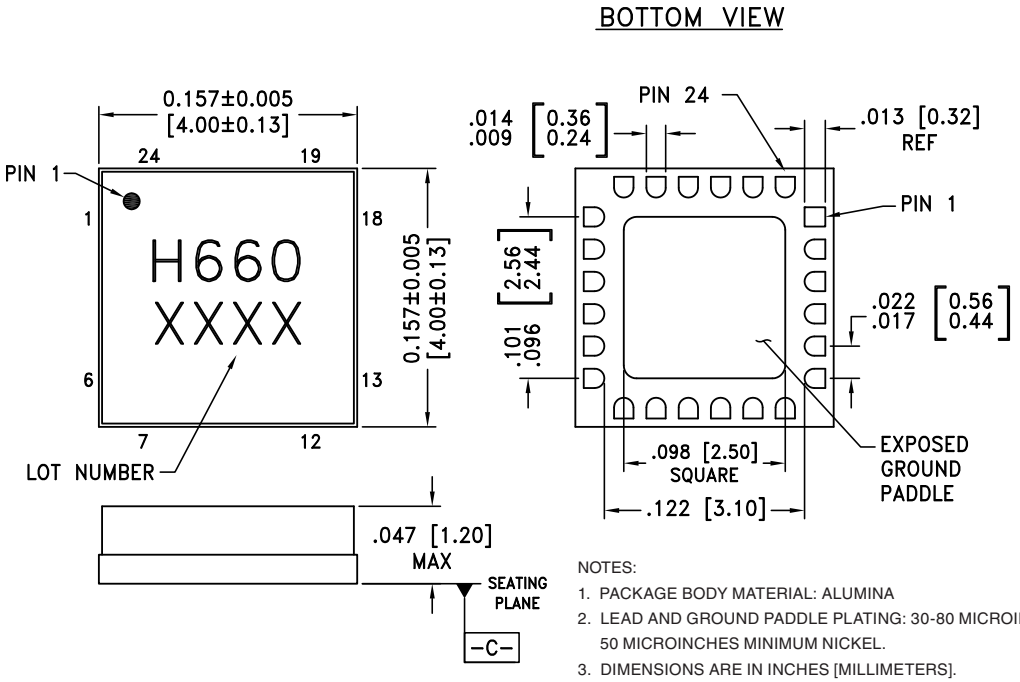
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

VccSH	5.5 Vdc
Vcc1	5.5 Vdc
Vcc2	6.5 Vdc
CLKP, CLKN Input Power	+10 dBm
Input Signal Amplitude	+10 dBm
Junction Temperature	125 °C
Continuous Pdiss (T= 85 °C)	1.22 W
Thermal Resistance (junction to package bottom)	32.8 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC660LC4B	Alumina, White	Gold over Nickel	MSL3 [1]	H660 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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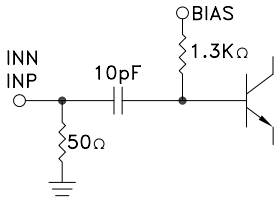
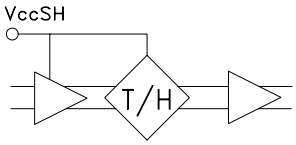
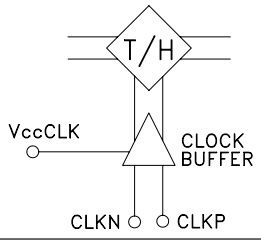
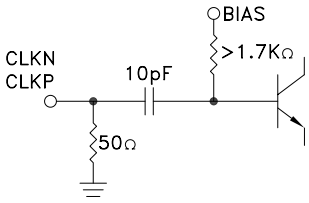
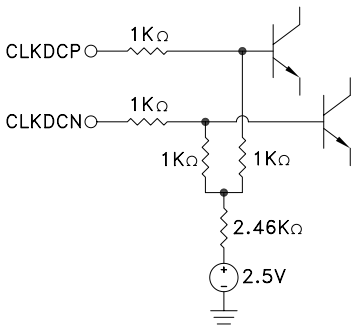
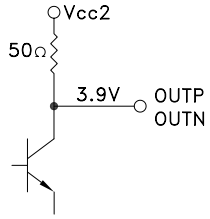
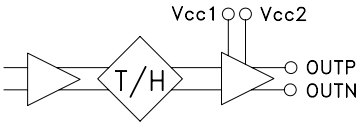
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 13, 19, 23, 24	N/C	Not connected.	
2, 5, 14, 17, 20, 22	GND	These pins must be connected to a high quality RF/DC ground.	
3	INP	Positive T/H RF input (input bias -T). Has on-chip DC 50Ω termination, nominal max single-ended input level = ±0.25V (-2 dBm) for specified performance. Input AC coupling time constant ~ 10 ns, +10 dBm max.	
4	INN	Negative T/H RF input (input bias -T). Has on-chip DC 50Ω termination, nominal max single-ended input level = ±0.25V (-2 dBm) for specified performance. Input AC coupling time constant ~ 10 ns, +10 dBm max.	
6	VccSH	T/H core supply. Requires nominal current of 61.5 mA at 5V. A 10 nF X7R dielectric chip capacitor close to the device is recommended.	
7	N/C	This pin must be left floating.	
8	VccCLK	Clock buffer power. Requires 19.8 mA nominal current at 5V.	
9, 10	CLKN, CLKP	Negative CLK RF input, Positive CLK RF input (CLK input bias -T). Has on-chip 50Ω termination, +10 dBm max. AC coupling time constant ~17 ns.	
11, 12	CLKDCP, CLKDCN	Positive CLKDC input and Negative CLKDC input (CLK input bias-T). A 10 n F X7R dielectric chip capacitor or equivalent should be used here. Internal bias -T isolation resistor = 1kΩ. May be floated for T/H operation. If biased use common mode voltage of 2.5 V. Apply differential voltage of (CLKDCP – CLKDCN) > 20 mV to force device in steady state track mode (in the absence of a clock). A 40 mV differential voltage can be continuously applied that allows the device to be biased in track mode whenever the clock is turned off.	

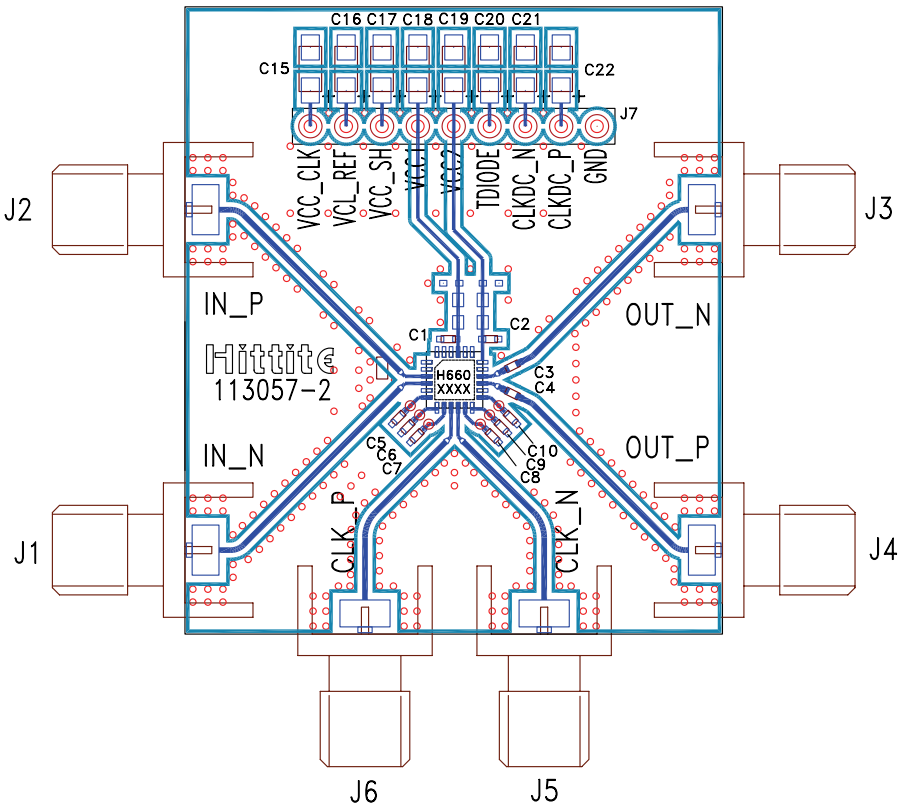
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
15, 16	OUTP, OUTN	Positive T/H RF output, Negative T/H RF output. 50 Ω output impedance, nominal DC output voltage = 3.9V. Can be returned to Vcc2 through 50 ohms or AC coupled. Device can be damaged if the output is shorted to ground.	
18	Vcc2	Output buffer 2 output driver power. The supply should be 5V if the output is DC coupled to the Vcc2 supply. The supply should be 6V if the output is AC coupled; Vcc2 current is 84 mA nominal. A 10 nF X 7R dielectric chip capacitor connected close to the device is recommended	
21	Vcc1	5V power for output buffers 1 and 2. Requires a nominal current of 49.8 mA at 5V. A 10 nF X7R dielectric chip capacitor connected close to the device is recommended.	

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Single Evaluation PCB



List of Materials for Evaluation PCB 113055 [1]

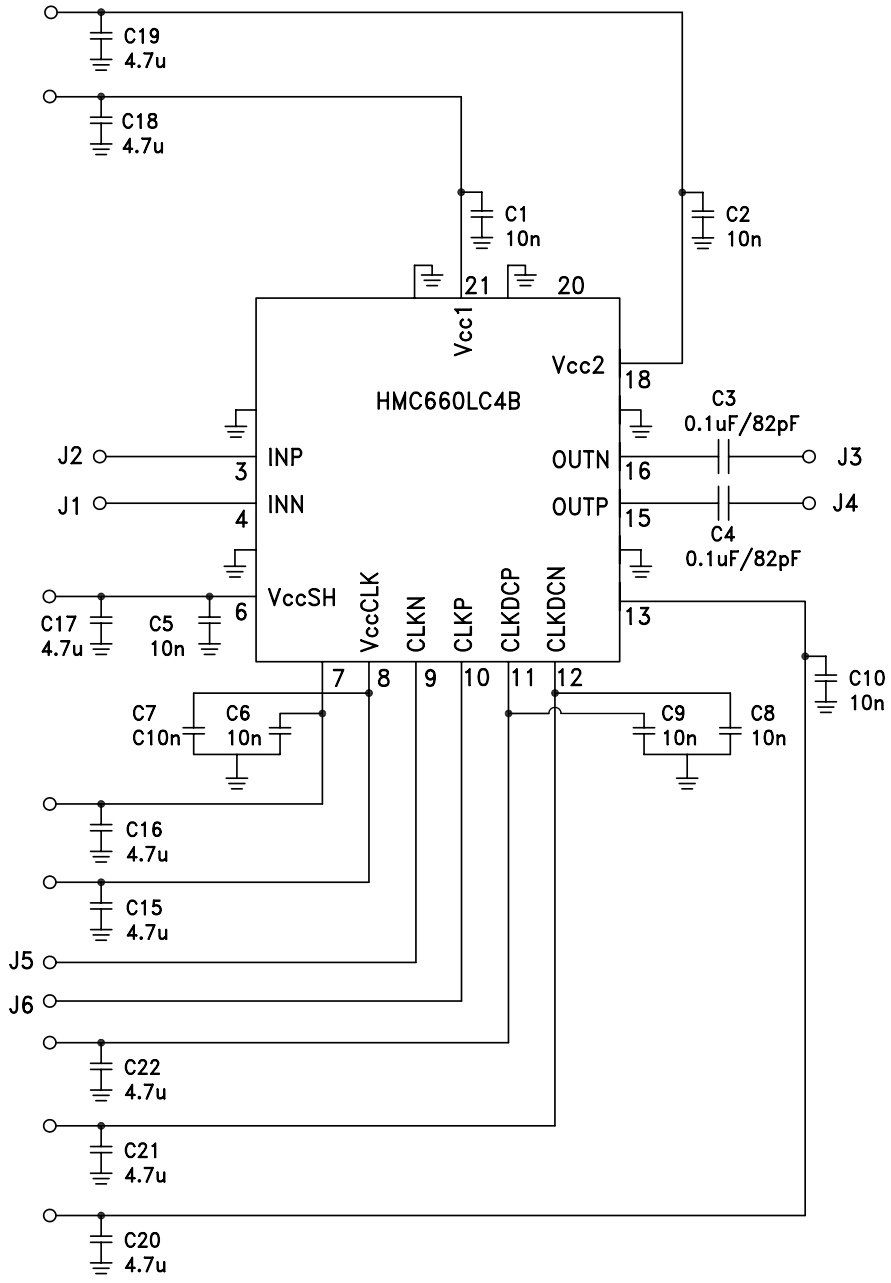
Item	Description
J1 - J6	Johnson SMA Connector
J7	9 pin DC Connector
C1, C2, C5 - C10	10K pF Chip Capacitor, 0402 Pkg.
C3, C4	1 uF & 82 pF, 16 kHz to 40 GHz Chip Capacitor, 0502 Pkg.
C15 - C22	4.7 uF, Case A, Tantulum Capacitor
U1	HMC660LC4B Track-and-Hold Amplifier
PCB [2]	113057 Single Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 10 GHz. The evaluation circuit board shown is available from Hittite upon request.

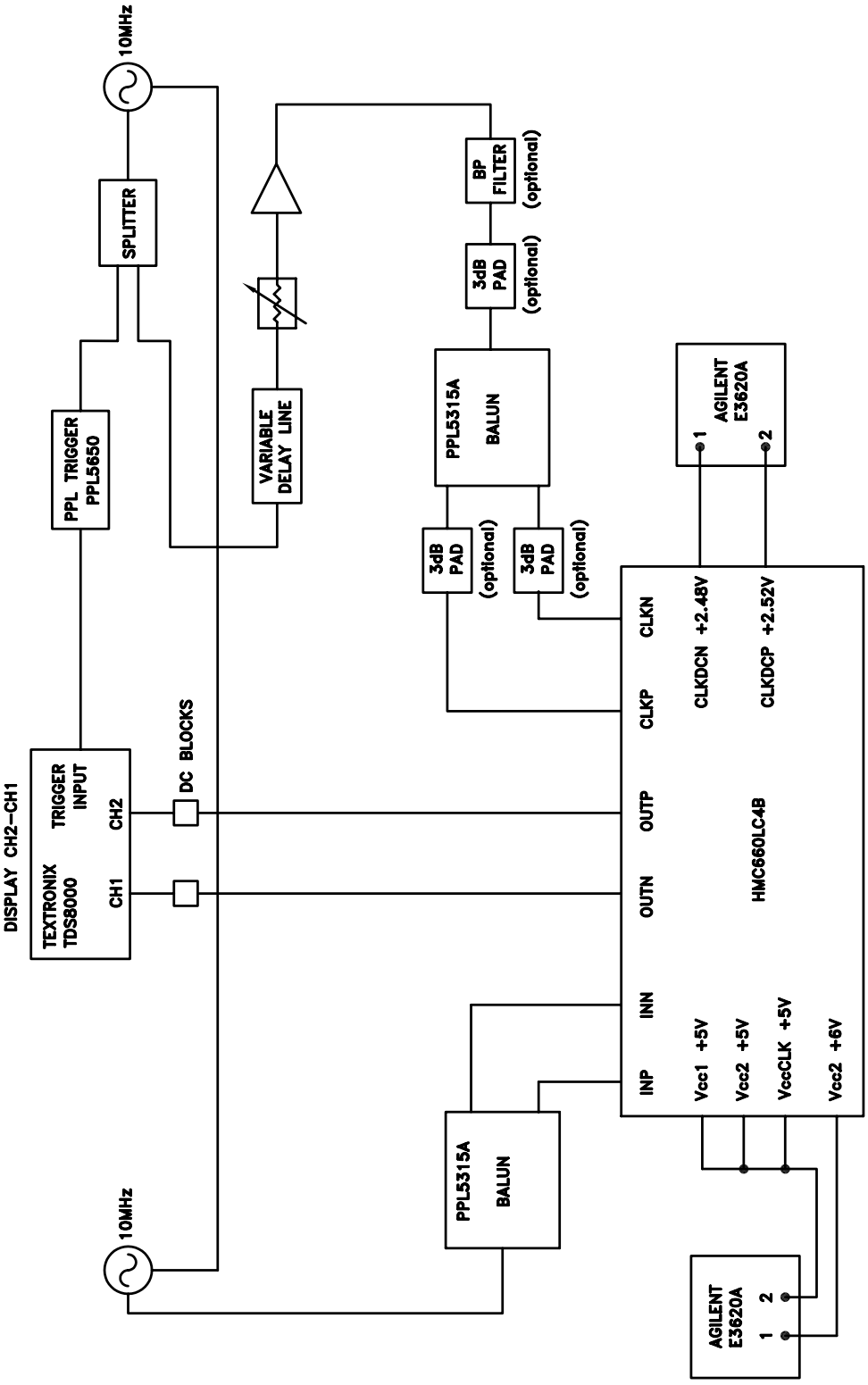
Application Circuit for Single Evaluation PCB



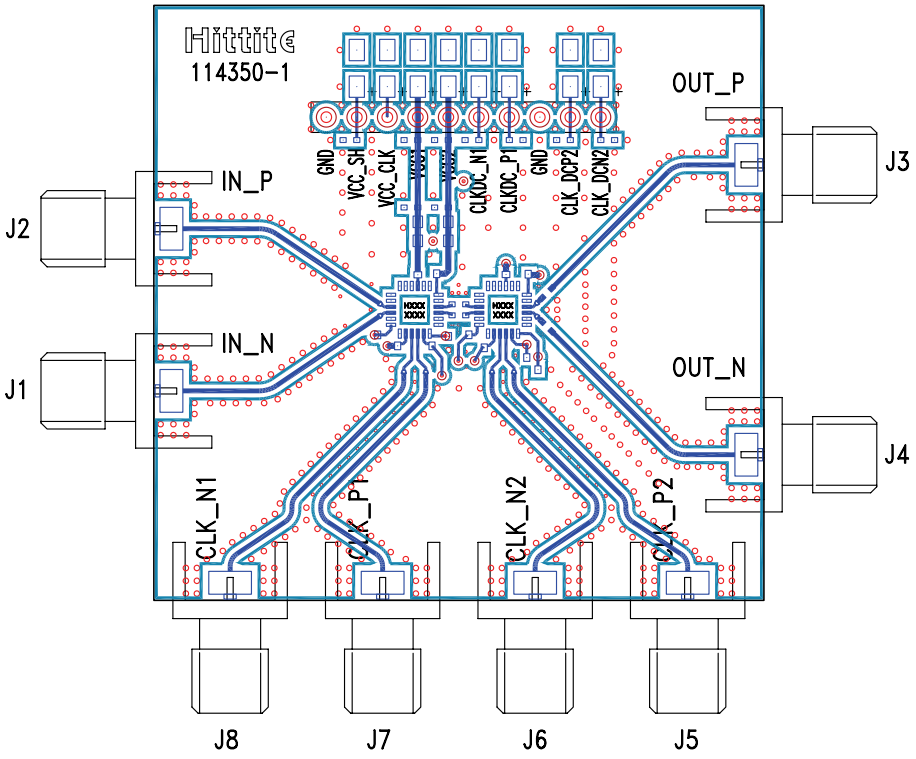
0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Characterization Set-up for Single Evaluation PCB



Dual Rank Evaluation PCB



List of Materials for Evaluation PCB 114352 [1]

Item	Description
J1 - J8	Johnson SMA Connector
J9	10 Pin DC Connector
C10, C11, C14, C15, C18 - C25	10K pF Chip Capacitor, 0402 Pkg.
C12, C13	Cap, Chip, 0302 Pkg. 12k pF and 82 pF 130 kHz to 100 GHz
C16, C17	1 uF & 82 pF, 16 KHz to 40 GHz Chip Capacitor, 0502 Pkg.
C28 - C35	4.7 uF, Case A, Tantulum Capacitor, Note Polarity
U1, U2	HMC660LC4B Track-and-Hold Amplifier
PCB [2]	114350 Eval Board

[1] Reference this number when ordering complete evaluation PCB

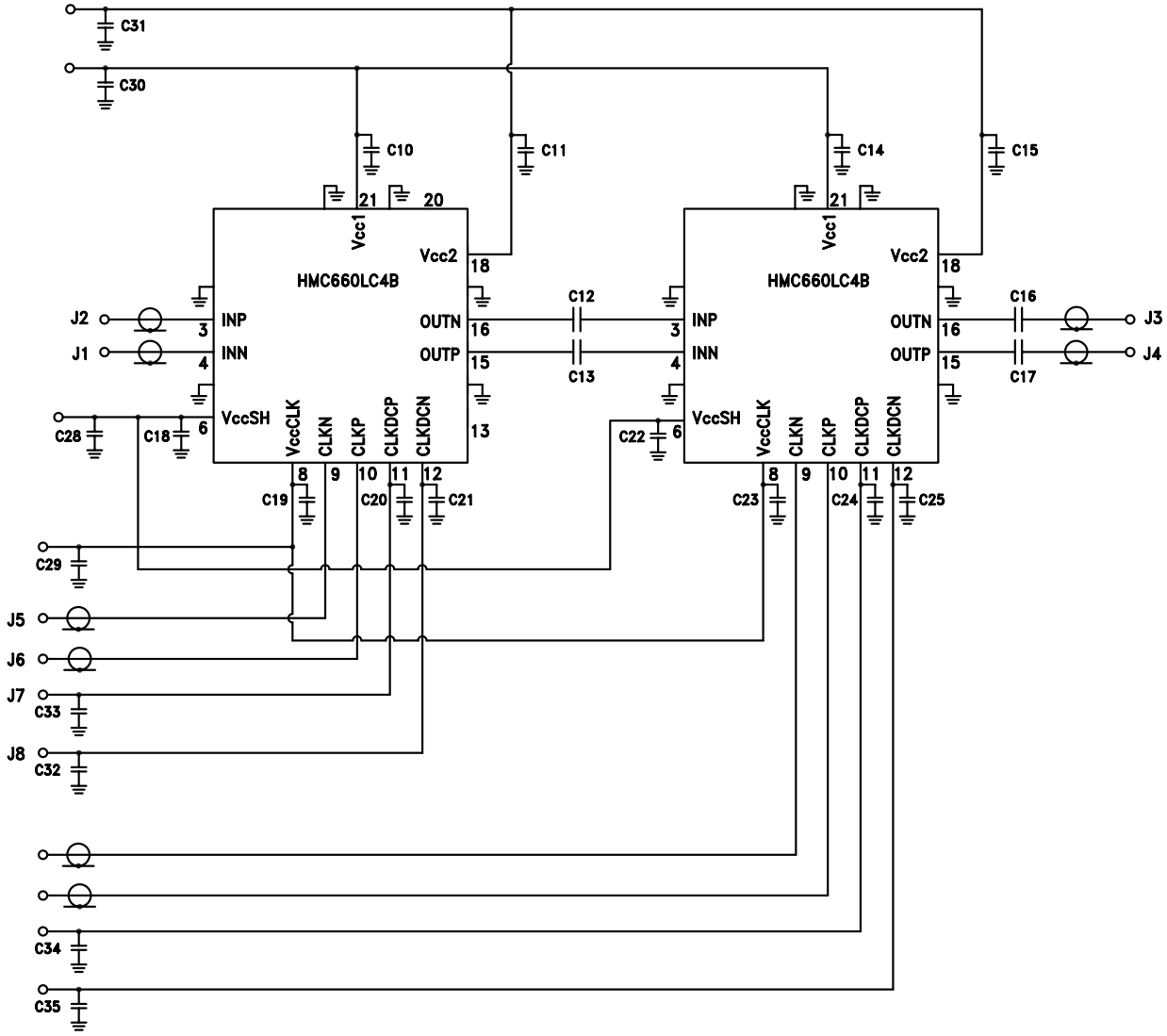
[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 10 GHz. The evaluation circuit board shown is available from Hittite upon request.

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

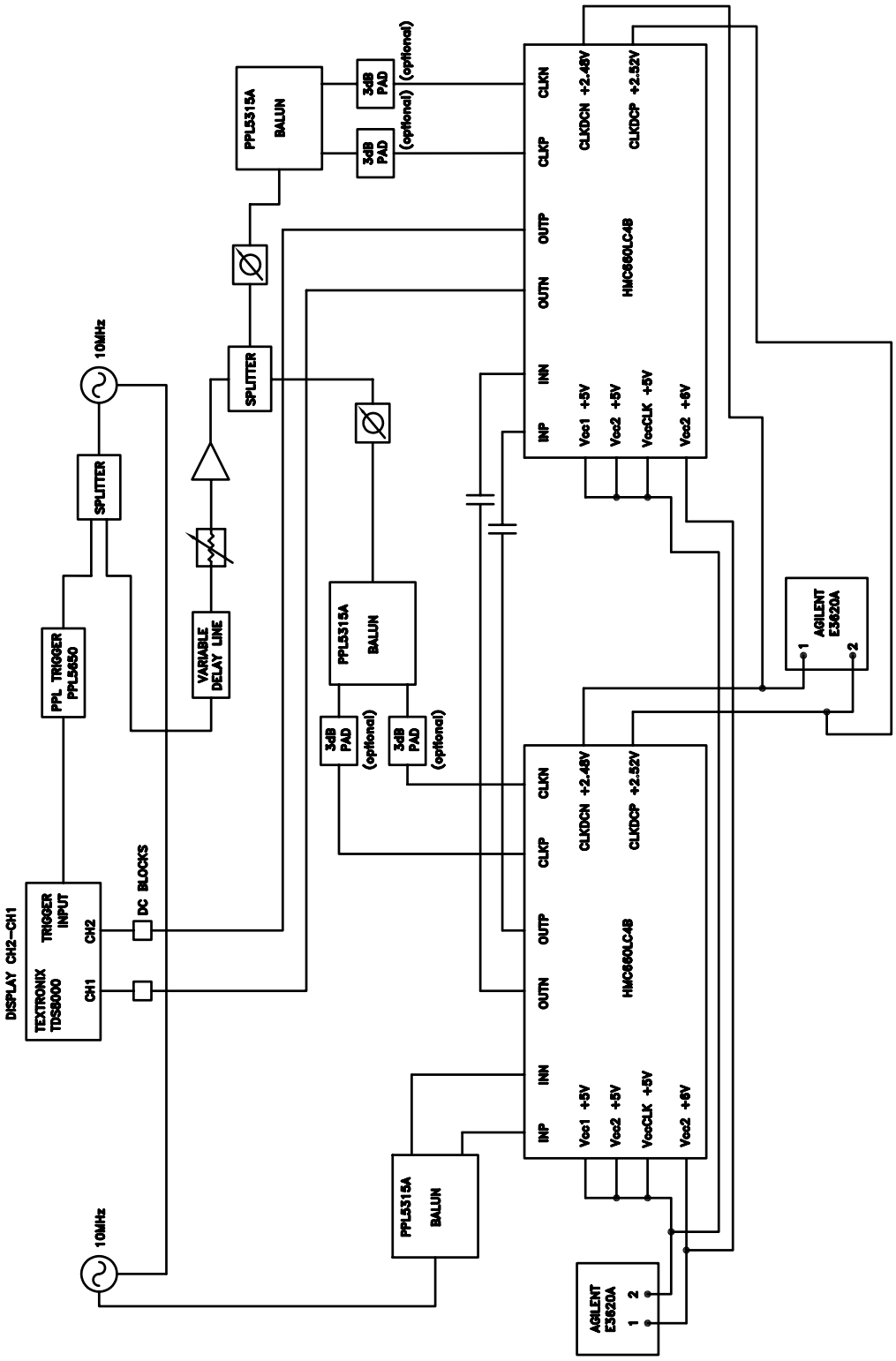
Application Circuit for Dual Rank Evaluation PCB



0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Characterization Set-up for Dual Rank Evaluation PCB

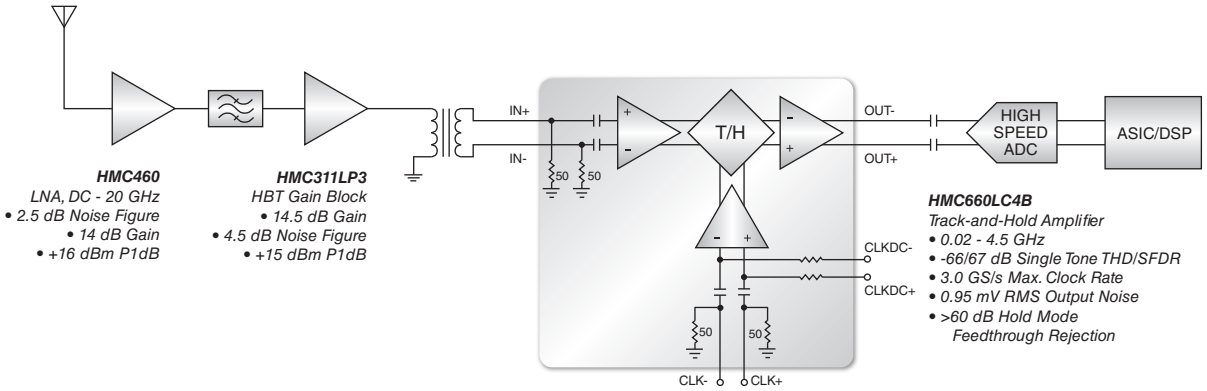


0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Product Application Circuits

Direct Conversion Receiver Track-and-Hold Amplifier Application



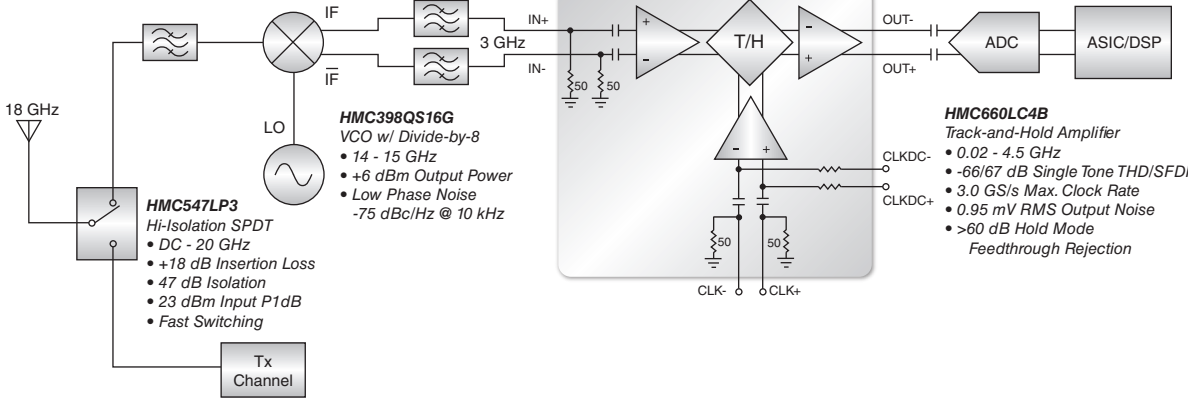
HMC460
LNA, DC - 20 GHz
- 2.5 dB Noise Figure
- 14 dB Gain
- +16 dBm P1dB

HMC311LP3
HBT Gain Block
- 14.5 dB Gain
- 4.5 dB Noise Figure
- +15 dBm P1dB

HMC660LC4B
Track-and-Hold Amplifier
- 0.02 - 4.5 GHz
- -66/67 dB Single Tone THD/SFDR
- 3.0 GS/s Max. Clock Rate
- 0.95 mV RMS Output Noise
- >60 dB Hold Mode Feedthrough Rejection

Generic Software Radio Track-and-Hold Amplifier Application

HMC523LC4
I/Q Mixer / IRM
- 15 - 23.6 GHz RF/LO
- 25 dB Image Rejection
- -8 dB Conversion Gain
- +25 dBm Input IP3
- DC - 3.5 GHz IF



HMC398QS16G
VCO w/ Divide-by-8
- 14 - 15 GHz
- +6 dBm Output Power
- Low Phase Noise -75 dBc/Hz @ 10 kHz

HMC547LP3
Hi-Isolation SPDT
- DC - 20 GHz
- +18 dB Insertion Loss
- 47 dB Isolation
- 23 dBm Input P1dB
- Fast Switching

HMC660LC4B
Track-and-Hold Amplifier
- 0.02 - 4.5 GHz
- -66/67 dB Single Tone THD/SFDR
- 3.0 GS/s Max. Clock Rate
- 0.95 mV RMS Output Noise
- >60 dB Hold Mode Feedthrough Rejection

0.02 - 4.5 GHz WIDEBAND 3 GS/s TRACK-AND-HOLD AMPLIFIER

Not Recommended for New Designs

Notes: