5-Bit Programmable 2-/3-Phase Synchronous Buck Controller

ADP3163

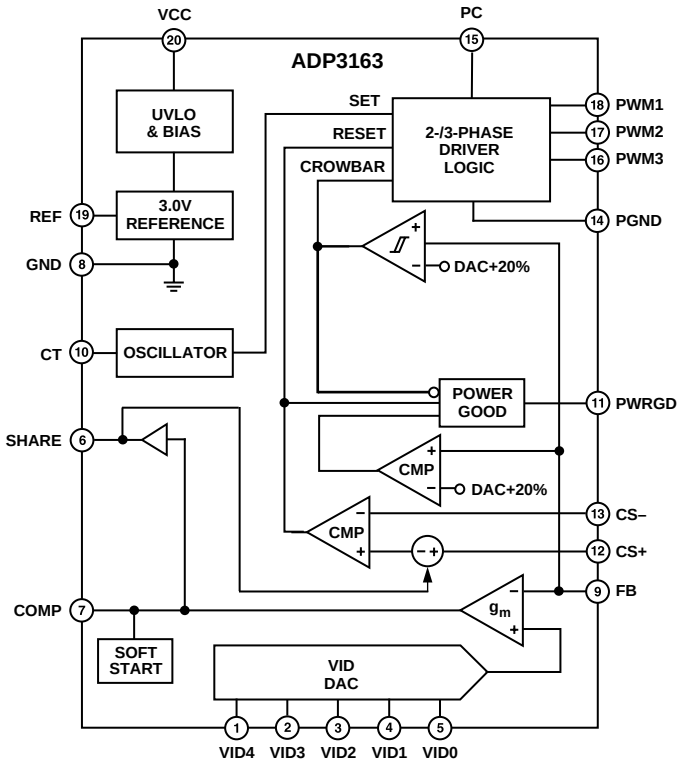
FEATURES

ADOPT™ Optimal Positioning Technology for Superior Load Transient Response and Fewest Output Capacitors
Complies with VRM 9.0 and Intel VR Down Guideline with Lowest System Cost
Digitally Selectable 2- or 3-Phase Operation at up to 500 kHz per Phase
Quad Logic-level PWM Outputs for Interface to External High-Power Drivers
Active Current Balancing between All Output Phases
Accurate Multiple VRM Module Current Sharing
5-Bit Digitally Programmable 1.1 V to 1.85 V Output
Total Output Accuracy ±0.8% Over Temperature
Current-Mode Operation
Short Circuit Protection
Enhanced Power Good Output Detects Open Outputs in Multi-VRM Power Systems
Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

APPLICATIONS

Desktop PC Power Supplies for:
Intel Pentium® 4 Processors
AMD Athlon Processors
VRM Modules

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3163 is a highly efficient multiphase synchronous buck switching regulator controller optimized for converting a 5 V or 12 V main supply into the core supply voltage required by high performance Intel processors. The ADP3163 uses an internal 5-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.1 V and 1.85 V. The ADP3163 uses a current mode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VRM size and efficiency. The phase relationship of the output signals can be programmed to provide 2- or 3-phase operation, allowing for the construction of up to three complementary buck switching stages. These stages share the dc output current to reduce overall output voltage ripple. An active current balancing function ensures that all phases carry equal portions of the total load current, even under large transient loads, to minimize the size of the inductors.

The ADP3163 also uses a unique supplemental regulation technique called active voltage positioning (ADOPT) to enhance load transient performance. Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for high performance processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3163 also provides accurate and reliable short circuit protection, adjustable current limiting, and an enhanced Power Good output that can detect open outputs in any phase for single or multi-VRM systems.

The ADP3163 is specified over the commercial temperature range of 0°C to 70°C and is available in a 20-lead TSSOP package.

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Pentium is a registered trademark of Intel Corporation.

REV. 0

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ADP3163–SPECIFICATIONS[1] (VCC = 12 V, I_{REF} = 150 μA, T_A = 0°C to 70°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FEEDBACK INPUT						
Accuracy	V_{FB}					
1.1 V Output			1.091	1.1	1.109	V
1.6 V Output			1.587	1.6	1.613	V
1.85 V Output			1.835	1.85	1.865	V
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.01		%
Input Bias Current	I_{FB}			5	50	nA
Crowbar Trip Point	$V_{CROWBAR}$	% of Nominal Output	115	120	125	%
Crowbar Reset Point		% of Nominal Output	40	50	60	%
Crowbar Response Time	$t_{CROWBAR}$	Overvoltage to PWM Going Low		400		ns
REFERENCE						
Output Voltage	V_{REF}		2.952	3.00	3.048	V
Output Current	I_{REF}		300			μA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$				0.8	V
Input High Voltage	$V_{IH(VID)}$		2.0			V
Input Current	I_{VID}	VID(X) = 0 V		70	90	μA
Pull-Up Resistance	R_{VID}		33	43		kΩ
Internal Pull-Up Voltage			2.7	3.0	3.3	V
OSCILLATOR						
Maximum Frequency[2]	$f_{CT(MAX)}$		3000			kHz
Frequency Variation	f_{CT}	T_A = 25°C, CT = 150 pF	475	575	675	kHz
		T_A = 25°C, CT = 68 pF	850	1000	1250	kHz
		T_A = 25°C, CT = 47 pF	1100	1300	1500	kHz
CT Charge Current	I_{CT}	T_A = 25°C, V_{FB} in Regulation	260	300	340	μA
		T_A = 25°C, V_{FB} = 0 V	40	65	80	μA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$			1		MΩ
Transconductance	$g_{m(ERR)}$		2.0	2.2	2.45	mmho
Output Current	$I_{O(ERR)}$	FB Forced to 0 V		575		μA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} – 3%		3.0		V
Output Disable Threshold	$V_{COMP(OFF)}$			800	875	mV
–3 dB Bandwidth	BW_{ERR}	COMP = Open		500		kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	CS+ = VCC, FB Forced to V_{OUT} – 3%	143	158	173	mV
		FB ≤ 750 mV	80	92	108	mV
		0.8 V ≤ SHARE ≤ 1 V		0	5	mV
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS– = VCC		1	5	μA
Response Time to PWM Going Low	t_{CS}	CS+ – (CS–) ≥ 173 mV		50		ns
CURRENT SHARING						
Output Source Current			2			mA
Output Sink Current				300	400	μA
Maximum Output Voltage	$V_{SHARE(MAX)}$	FB Forced to V_{OUT} – 3%		3.0		V
PHASE CONTROL						
Input Low Voltage	$V_{IL(PC)}$				0.8	V
Input High Voltage	$V_{IH(PC)}$		2.0			V
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Percent of Nominal Output	75	80	85	%
Overvoltage Threshold	$V_{PWRGD(OV)}$	Percent of Nominal Output	115	120	125	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 1 mA		375	525	mV
Response Time				250		ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM OUTPUTS						
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400 µA		100	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ =400 µA	4.0	5.0		V
Duty Cycle Limit Per Phase[2]	DC	PC = GND			50	%
		PC = REF			33	%
SUPPLY						
DC Supply Current						
Normal Mode	I_{CC}			3.75	5.5	mA
No CPU Mode	$I_{CC(NO\ CPU)}$	VID4 – VID0 = Open		3.5	5.5	mA
UVLO Mode	$I_{CC(UVLO)}$	VCC ≤ V_{UVLO}, VCC Rising		350	500	µA
UVLO Threshold Voltage	V_{UVLO}		5.9	6.4	6.9	V
UVLO Hysteresis			0.5	0.8	1.0	V

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
[2]Guaranteed by design, not tested in production.

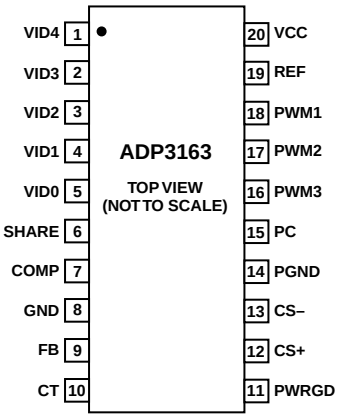
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

VCC . . . . . –0.3 V to +15 V
CS+, CS– . . . . . –0.3 V to VCC +0.3 V
All Other Inputs and Outputs . . . . . –0.3 V to +10 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
θ_{JA} . . . . . 143°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to PGND.

PIN CONFIGURATION
RU-20



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3163JRU	0°C to 70°C	Thin Shrink Small Outline	RU-20 (TSSOP-20)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3163 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1–5	VID4 – VID0	Voltage Identification DAC Inputs. These pins are pulled up to an internal 3 V reference, providing a Logic 1 if left open. The DAC output programs the FB regulation voltage from 1.1 V to 1.85 V. Leaving all five DAC inputs open results in the ADP3163 going into a "No CPU" mode, shutting off its PWM outputs.
6	SHARE	Current Sharing Output. This pin is connected to the SHARE pins of other ADP3163s in multiple VRM systems to ensure proper current sharing between the converters. The voltage at this output programs the output current control level between CS+ and CS–.
7	COMP	Error Amplifier Output and Compensation Point.
8	GND	Ground. FB, REF and the VID DAC of the ADP3163 are referenced to this ground. This is a low current ground that can also be used as a return for the FB pin in remote voltage sensing applications.
9	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
10	CT	External capacitor CT connection to ground sets the frequency of the device.
11	PWRGD	Open drain output that signals when the output voltage is outside of the proper operating range or when a phase is not supplying current even if the output voltage is in specification.
12	CS+	Current Sense Positive Node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–.
13	CS–	Current Sense Negative Node. Negative input for the current comparator.
14	PGND	Power Ground. All internal biasing and logic output signals of the ADP3163 are referenced to this ground.
15	PC	Phase Control Input. This logic-level input determines the number of active phases and the duty cycle limit of each phase.
16	PWM3	Logic-Level Output for the Phase 3 Driver.
17	PWM2	Logic-Level Output for the Phase 2 Driver.
18	PWM1	Logic-Level Output for the Phase 1 Driver.
19	REF	3.0 V Reference Output.
20	VCC	Supply Voltage for the ADP3163.

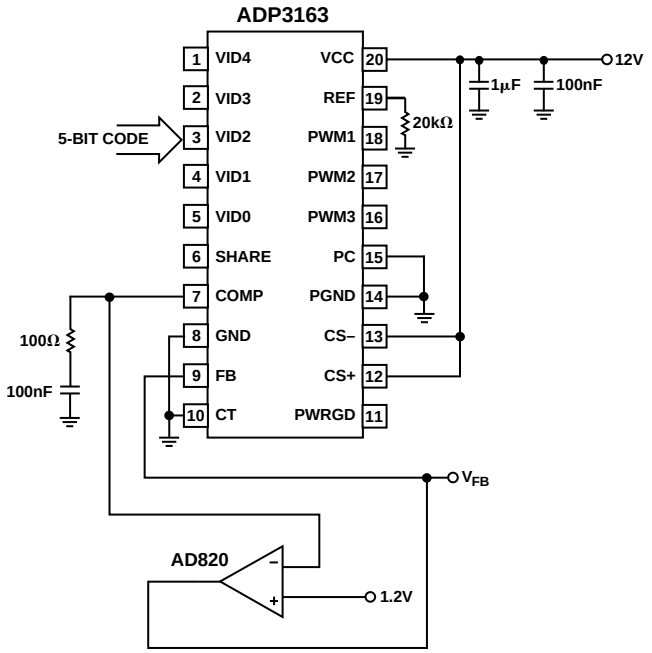
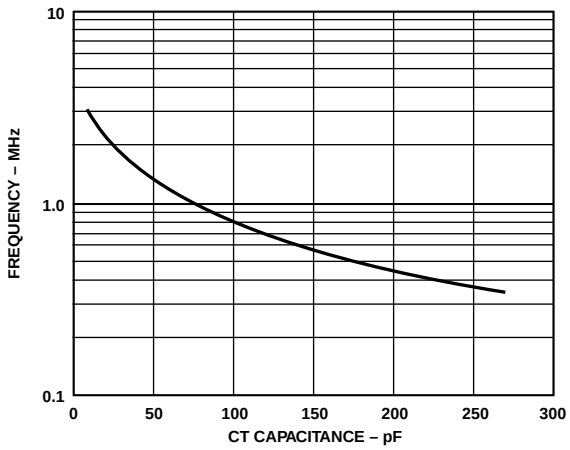


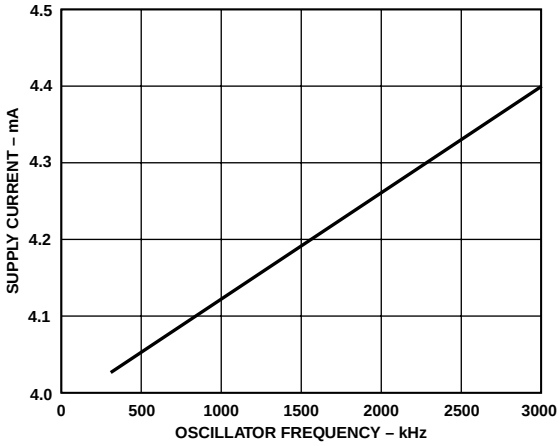
Figure 1. Closed-Loop Output Voltage Accuracy Test Circuit

Table I. PWM Outputs vs. Phase Control Code

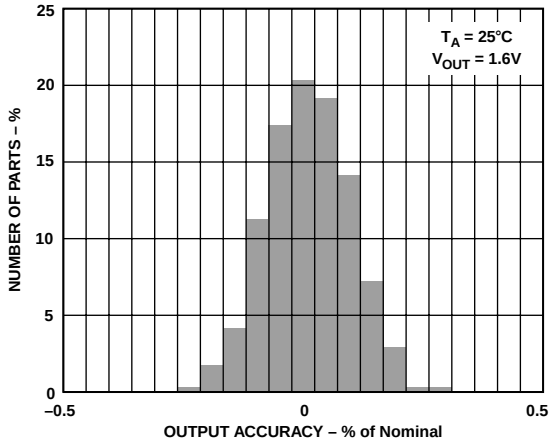
PC	PWM3	PWM2	PWM1	Maximum Duty Cycle
REF	ON	ON	ON	33%
GND	OFF	ON	ON	50%



TPC 1. Oscillator Frequency vs. Timing Capacitor (CT)



TPC 2. Supply Current vs. Oscillator Frequency



TPC 3. Output Accuracy Distribution

Table II. Output Voltage vs. VID Code

VID4	VID3	VID2	VID1	VID0	$V_{OUT(NOM)}$
1	1	1	1	1	No CPU
1	1	1	1	0	1.100 V
1	1	1	0	1	1.125 V
1	1	1	0	0	1.150 V
1	1	0	1	1	1.175 V
1	1	0	1	0	1.200 V
1	1	0	0	1	1.225 V
1	1	0	0	0	1.250 V
1	0	1	1	1	1.275 V
1	0	1	1	0	1.300 V
1	0	1	0	1	1.325 V
1	0	1	0	0	1.350 V
1	0	0	1	1	1.375 V
1	0	0	1	0	1.400 V
1	0	0	0	1	1.425 V
1	0	0	0	0	1.450 V
0	1	1	1	1	1.475 V
0	1	1	1	0	1.500 V
0	1	1	0	1	1.525 V
0	1	1	0	0	1.550 V
0	1	0	1	1	1.575 V
0	1	0	1	0	1.600 V
0	1	0	0	1	1.625 V
0	1	0	0	0	1.650 V
0	0	1	1	1	1.675 V
0	0	1	1	0	1.700 V
0	0	1	0	1	1.725 V
0	0	1	0	0	1.750 V
0	0	0	1	1	1.775 V
0	0	0	1	0	1.800 V
0	0	0	0	1	1.825 V
0	0	0	0	0	1.850 V

THEORY OF OPERATION

The ADP3163 combines a current-mode, fixed frequency PWM controller with multiphase logic outputs for use in a 2- or 3-phase synchronous buck power converter. Multiphase operation is important for switching the high currents required by high performance microprocessors. Handling the high current in a single-phase converter would place unreasonable requirements on the power components such as inductor wire size and MOSFET ON-resistance and thermal dissipation. The ADP3163's high-side current sensing topology ensures that the load currents are balanced in each phase, such that no single phase has to carry more than it's share of the power. An additional benefit of high side current sensing over output current sensing is that the average current through the sense resistor is reduced by the duty cycle of the converter allowing the use of a lower power, lower cost resistor. The outputs of the ADP3163 are logic drivers only and are not intended to directly drive external power MOSFETs. Instead, the ADP3163 should be paired with drivers such as the ADP3413 or ADP3414.

The frequency of the ADP3163 is set by an external capacitor connected to the CT pin. The phase relationship and number of active output phases is determined by the state of the phase control (PC) pin as shown in Table I. The error amplifier and current sense comparator control the duty cycle of the PWM outputs to maintain regulation. The maximum duty cycle per phase is inherently limited to 50% for 2-phase operation and 33% for 3-phase operation. While one phase is on, all other phases remain off. In no case can more than one output be high at any time.

Output Voltage Sensing

The output voltage is sensed at the FB pin allowing for remote sensing. To maintain the accuracy of the remote sensing, the GND pin should also be connected close to the load. A voltage error amplifier (g_m) amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed between 1.1 V and 1.85 V by an internal 5-bit DAC, which reads the code at the voltage identification (VID) pins. (Refer to Table II for the output voltage versus VID pin code information.)

Active Voltage Positioning

The ADP3163 uses Analog Devices Optimal Positioning Technology (ADOPT), a unique supplemental regulation technique that uses active voltage positioning and provides optimal compensation for load transients. When implemented, ADOPT adjusts the output voltage as a function of the load current, so that it is always optimally positioned for a load transient. Standard (passive) voltage positioning has poor dynamic performance, rendering it ineffective under the stringent repetitive transient conditions required by high performance processors. ADOPT, however, provides optimal bandwidth for transient response that yields optimal load transient response with the minimum number of output capacitors.

Reference Output

A 3.0 V reference is available on the ADP3163. This reference is normally used to set the voltage positioning accurately using a resistor divider to the COMP pin. In addition, the reference can be used for other functions such as generating a regulated voltage with an external amplifier. The reference is bypassed with a 1 nF capacitor to ground. It is not intended to supply large capacitive loads, and it should not be used to provide more than 300 μA of output current.

Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage-error amplifier and the current comparator are the main control elements. The voltage at the CT pin of the oscillator ramps between 0 V and 3 V. When that voltage reaches 3 V, the oscillator sets the driver logic, which sets PWM1 high. During the ON time of Phase 1, the driver IC turns on the Phase 1 high-side MOSFET. The CS+ and CS– pins monitor the current through the sense resistor that feeds all the high side MOSFETs. When the voltage between the two pins exceeds the threshold level, the driver logic is reset and the PWM1 output goes low. This signals the driver IC to turn off the Phase 1 high side MOSFET and turn on the Phase 1 low side MOSFET. On the next cycle of the oscillator, the driver logic toggles and sets PWM2 high. On each following cycle of the oscillator, the driver logic cycles between each of the active PWM outputs based on the logic state of the PC pin. In each case, the current comparator resets the PWM output low when its threshold is reached. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the g_m amplifier, which in turn leads to an increase in the current comparator threshold, thus programming more load current to be delivered so that voltage regulation is maintained.

Active Current Sharing
The ADP3163 ensures current balance in all the active phases by sensing the current through a single sense resistor. During one phase's ON time, the current through the respective high side MOSFET and inductor is measured through the sense resistor. When the comparator threshold is reached, the high side MOSFET turns off. On the next cycle the ADP3163 switches to the next phase. The current is measured with the same sense resistor and the same internal comparator, ensuring accurate matching. This scheme is immune to imbalances in the MOSFET's $R_{DS(ON)}$ and inductor parasitic resistance.

If for some reason one of the phases fails, the other phases will still be limited to their maximum output current (one over the total number phases times the total short circuit current limit). If this is not sufficient to supply the load, the output voltage will droop and cause the PWRGD output to signal that the output voltage has fallen out of its specified range. If one of the phases has an open circuit failure, the ADP3163 will detect the open phase and signal the problem via the PWRGD pin (see Power Good Monitoring section).

Current Sharing in Multi-VRM Applications
The ADP3163 includes a SHARE pin to allow multiple VRMs to accurately share load current. In multiple VRM applications, the SHARE pins should be connected together. This pin is a low impedance buffered output of the COMP pin voltage. The output of the buffer is internally connected to set the threshold of the current sense comparator. The buffer has a 400 μA sink current, and a 2 mA sourcing capability. The strong pull-up allows one VRM to control the current threshold set point for all ADP3163s connected together. The ADP3163's high accuracy current set threshold ensures good current balance between VRMs. Also, the low impedance of the buffer minimizes noise pick up on this trace which is routed to multiple VRMs. This circuit operates in addition to the active current sharing between phases of each VRM described above.

Short Circuit Protection
The ADP3163 has multiple levels of short circuit protection to ensure fail-safe operation. The sense resistor and the maximum current sense threshold voltage given in the specifications set the peak current limit.

When the load current exceeds the current limit, the excess current discharges the output capacitor. When the output voltage is below the foldback threshold, $V_{FB(LOW)}$, the maximum deliverable output current is cut by reducing the current sense threshold from the current limit threshold, $V_{CS(CL)}$, to the foldback threshold, $V_{CS(FOLD)}$. Along with the resulting current foldback, the oscillator frequency is reduced by a factor of five when the output is 0 V. This further reduces the average current in short circuit.

Power Good Monitoring
The Power Good comparator monitors the output voltage of the supply via the FB pin. The PWRGD pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the specified range of the nominal output voltage requested by the VID DAC. PWRGD will go low if the output is outside this range.

Short circuits in a VRM power path are relatively easy to detect in applications where multiple VRMs are connected to a common power plane. VRM power train open failures are not as easily spotted, since the other VRMs may be able to supply enough total current to keep the output voltage within the Power Good voltage specification even when one VRM is not functioning. The ADP3163 addresses this problem by monitoring both the output voltage and the switch current to determine the state of the PWRGD output.

The output voltage portion of the Power Good monitor dominates; as long as the output voltage is outside the specified window, PWRGD will remain low. If the output voltage is within specification, a second circuit checks to make sure that current is being delivered to the output by each phase. If no current is detected in a phase for three consecutive cycles, it is assumed that an open circuit exists somewhere in the power path, and PWRGD will be pulled low.

Output Crowbar
The ADP3163 includes a crowbar comparator that senses when the output voltage rises higher than the specified trip threshold, $V_{CROWBAR}$. This comparator overrides the control loop and sets both PWM outputs low. The driver ICs turn off the high side MOSFETs and turn on the low side MOSFETs, thus pulling the output down as the reversed current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action will current limit the input supply or blow its fuse, protecting the microprocessor from destruction. The crowbar comparator releases when the output drops below the specified reset threshold, and the controller returns to normal operation if the cause of the over voltage failure does not persist.

Output Disable
The ADP3163 includes an output disable function that turns off the control loop to bring the output voltage to 0 V. Because an extra pin is not available, the disable feature is accomplished by pulling the COMP pin to ground. When the COMP pin drops below 0.8 V, the oscillator stops and all PWM signals are driven low. When in this state, the reference voltage is still available. The COMP pin should be pulled down with an open drain structure capable of sinking at least 2 mA.

APPLICATION INFORMATION

The design parameters for a typical Intel Pentium 4 CPU application are as follows:

Input voltage (V_{IN}) = 12 V
VID setting voltage (V_{VID}) = 1.5 V
Nominal output voltage at no load (V_{ONL}) = 1.475 V
Nominal output voltage at 65 A load (V_{OFL}) = 1.377 V
Static output voltage drop based on a 1.5 mΩ load line (R_{OUT}) from no load to full load (V_{Δ}) = $V_{ONL} - V_{OFL}$ = 1.475 V – 1.377 V = 98 mV
Maximum Output Current (I_O) = 65 A
Number of Phases (n) = 3

CT Selection—Choosing the Clock Frequency
The ADP3163 uses a fixed-frequency control architecture. The frequency is set by an external timing capacitor, CT. The clock frequency and the state of the PC pin determine the switching frequency, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. With PC tied to REF, a clock frequency of 600 kHz sets the switching frequency of each phase, f_{SW}, to 200 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. To achieve a 600 kHz oscillator frequency, the required timing capacitor value is 150 pF. For good frequency stability and initial accuracy, it is recommended to use a capacitor with low temperature coefficient and tight

tolerance, e.g., an MLC capacitor with NPO dielectric and with 5% or less tolerance.

Inductance Selection

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, output capacitors with less total capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In a three-phase converter, a practical value for the peak-to-peak inductor ripple current is under 50% of the dc current in the same inductor. A choice of 50% for this particular design example yields a total peak-to-peak output ripple current of 12% of the total dc output current. The following equation shows the relationship between the inductance, oscillator frequency, peak-to-peak ripple current in an inductor and input and output voltages.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{L(RIPPLE)}} \quad (1)$$

For an 11 A peak-to-peak ripple current, which corresponds to 50% of the 22 A full-load dc current in an inductor, Equation 1 yields an inductance of:

$$L = \frac{(12\,V - 1.5\,V) \times 1.5\,V}{12\,V \times \frac{600\,kHz}{3} \times 11\,A} = 596\,nH$$

A 600 nH inductor can be used, which gives a calculated ripple current of 10.9 A at no load. The inductor should not saturate at the peak current of 27 A, and should be able to handle the sum of the power dissipation caused by the average current of 22 A in the winding and the core loss.

The output ripple current is smaller than the inductor ripple current due to the three phases partially canceling. This can be calculated as follows:

$$I_{O\Delta} = \frac{n \times V_{OUT} \times (V_{IN} - n \times V_{OUT})}{V_{IN} \times L \times f_{OSC}}$$

$$I_{O\Delta} = \frac{3 \times 1.5\,V \times (12\,V - 3 \times 1.5\,V)}{12\,V \times 600\,nH \times 600\,kHz} = 7.81\,A \quad (2)$$

Designing an Inductor

Once the inductance is known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-Mμ® from Magnetics, Inc.) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

Two main core types can be used in this application. Open magnetic loop types, such as beads, beads on leads, and rods and slugs, provide lower cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed-loop types, such as pot cores, PQ, U, and E cores, or toroids, cost more, but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table III gives some examples.

Table III. Magnetics Design References

Magnetic Designer Software Intusoft (http://www.intusoft.com)
Designing Magnetic Components for High-Frequency DC-DC Converters McLyman, Kg Magnetics ISBN 1-883107-00-08

Selecting a Standard Inductor

The companies listed in Table IV can provide design consultation and deliver power inductors optimized for high power applications upon request.

Table IV. Power Inductor Manufacturers

Coilcraft (847)639-6400 http://www.coilcraft.com
Coiltronics (561)752-5000 http://www.coiltronics.com
Sumida Electric Company (408)982-9660 http://www.sumida.com

R_{SENSE}

The value of R_{SENSE} is based on the maximum required output current. The current comparator of the ADP3163 has a minimum current limit threshold of 143 mV. Note that the 143 mV value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and tolerances.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, I_O, which equals the peak inductor current value less half of the peak-to-peak inductor ripple current. From this, the maximum value of R_{SENSE} is calculated as:

$$R_{SENSE} \le \frac{V_{CSCL(MIN)}}{\frac{I_O}{n} + \frac{I_{L(RIPPLE)}}{2}} = \frac{143\,mV}{\frac{65\,A}{3} + \frac{10.9\,A}{2}} = 5.3\,m\Omega \quad (3)$$

In this case, 5 mΩ was chosen as the closest standard value. Once R_{SENSE} has been chosen, the output current at the point where current limit is reached, $I_{OUT(CL)}$, can be calculated using the maximum current sense threshold of 173 mV:

$$I_{OUT(CL)} = n \times \frac{V_{CSCL(MAX)}}{R_{SENSE}} - \frac{n \times I_{L(RIPPLE)}}{2}$$

$$I_{OUT(CL)} = 3 \times \frac{173\,mV}{5\,m\Omega} - \frac{3 \times 10.9\,A}{2} = 87.5\,A \quad (4)$$

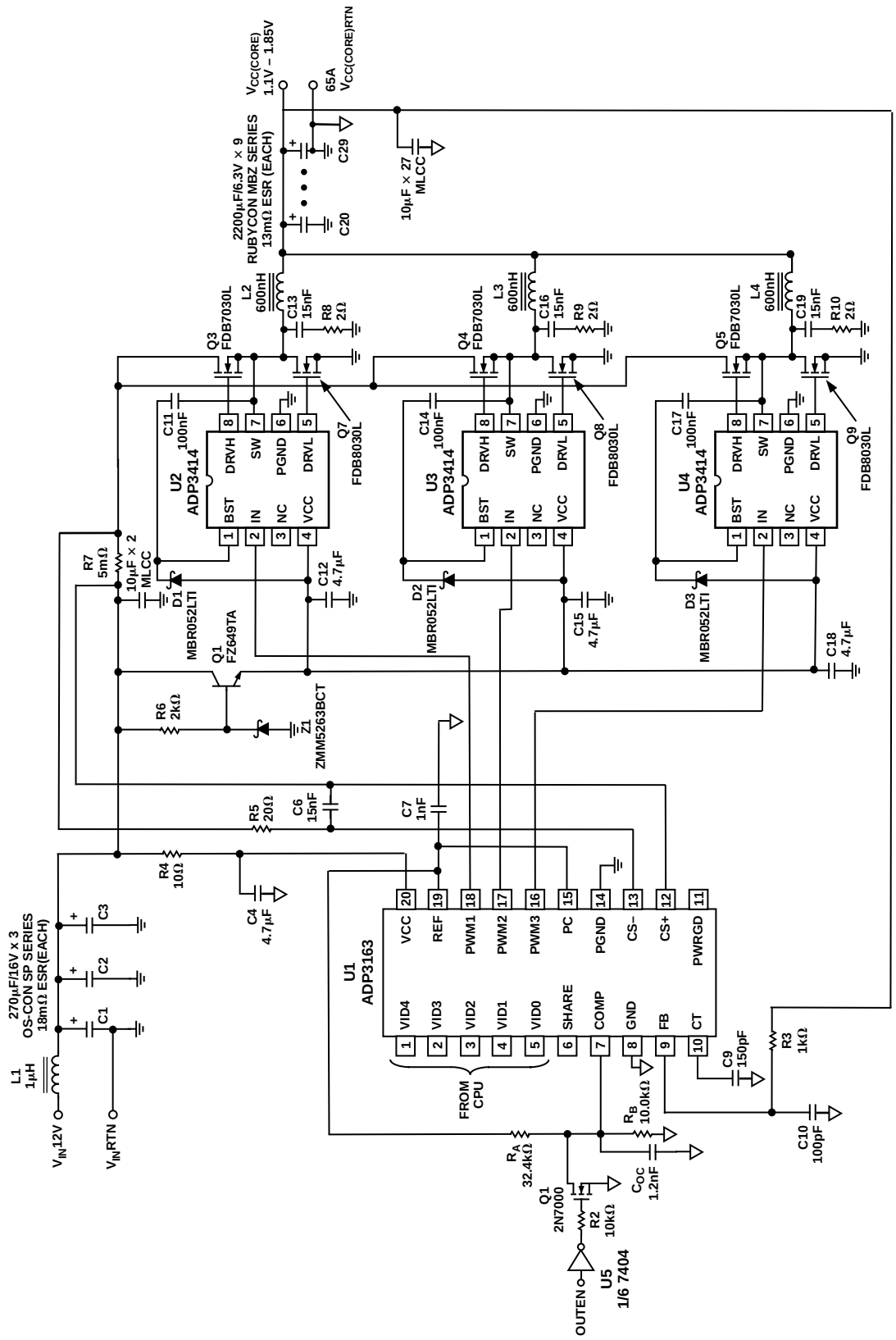


Figure 2. 65A Intel Pentium 4CPU Supply Circuit, VR Down Guideline Design

At output voltages below 750 mV, the current sense threshold is reduced to 108 mV, and the ripple current is negligible. Therefore, at dead short the output current is reduced to:

$$I_{OUT(SC)} = n \times \frac{V_{CS(SC)}}{R_{SENSE}} = 3 \times \frac{108\ mV}{5\ m\Omega} = 65\ A \quad (5)$$

To safely carry the current under maximum load conditions, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = I_{SENSE(RMS)}{}^2 \times R_{SENSE} \quad (6)$$

where:

$$I_{SENSE(RMS)}{}^2 = \frac{I_O{}^2}{n} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (7)$$

In this formula, n is the number of phases, and η is the converter efficiency, in this case assumed to be 85%. Combining Equations 6 and 7 yields:

$$P_{R_{SENSE}} = \frac{65\ A^2}{3} \times \frac{1.5\ V}{0.85 \times 12\ V} \times 5\ m\Omega = 1.0\ W$$

Output Resistance

This design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a dc output resistance of:

$$R_{OUT} = \frac{V_{ONL} - V_{OFL}}{I_{O\Delta}} = \frac{1.475\ V - 1.377\ V}{65\ A} = 1.5\ m\Omega \quad (8)$$

The required dc output resistance can be achieved by terminating the g_m amplifier with a resistor. The value of the total termination resistance that will yield the correct dc output resistance:

$$R_T = \frac{n_I \times R_{SENSE}}{n \times g_m \times R_{OUT}} = \frac{12.5 \times 5\ m\Omega}{3 \times 2.2\ mmho \times 1.5\ m\Omega} = 6.31\ k\Omega \quad (9)$$

where n_I is the division ratio from the output voltage signal of the g_m amplifier to the PWM comparator CMP1, g_m is the transconductance of the g_m amplifier itself, and n is the number of phases.

Output Offset

Intel's specification requires that at no load the nominal output voltage of the regulator be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is introduced by realizing the total termination resistance of the g_m amplifier with a divider connected between the REF pin and ground. The resistive divider introduces an offset to the output of the g_m amplifier that, when reflected back through the gain of the g_m stage, accurately positions the output voltage near its allowed maximum at light load. Furthermore, the output of the g_m amplifier sets the current sense threshold voltage. At no load, the current sense threshold is increased by the peak of the ripple current in the inductor and reduced by the delay between sensing when the current threshold has been reached and when the high side MOSFET actually turns off. These two factors are combined with the inherent voltage (V_{GNL0}), at the output of the g_m amplifier that commands a current sense threshold of 0 mV:

$$V_{GNL} = V_{GNL0} + \frac{I_{L(RIPPLE)} \times R_{SENSE} \times n_I}{2} - \frac{V_{IN} - V_{OUT}}{L} \times n \times t_D \times R_{SENSE} \times n_I$$

$$V_{GNL} = 1V + \frac{10.9\ A \times 5\ m\Omega \times 12.5}{2} - \frac{12\ V - 1.5\ V}{600\ nH} \times 2 \times 60\ ns \times 5\ m\Omega \times 12.5 = 1.144\ V \quad (10)$$

The divider resistors (R_A for the upper and R_B for the lower) can now be calculated, assuming that the internal resistance of the g_m amplifier (R_{OGM}) is 1 MΩ:

$$R_B = \frac{V_{REF}}{\frac{V_{REF} - V_{GNL}}{R_T} - g_m \times (V_{ONL} - V_{VID})}$$

$$R_B = \frac{3\ V}{\frac{3\ V - 1.144\ V}{6.31\ k\Omega} - 2.2\ mmho \times (1.475\ V - 1.5\ V)} = 8.59\ k\Omega \quad (11)$$

Choosing the nearest 1% resistor value gives R_B = 8.66 kΩ. Finally, R_A is calculated:

$$R_A = \frac{1}{\frac{1}{R_T} - \frac{1}{R_{OGM}} - \frac{1}{R_B}} = \frac{1}{\frac{1}{6.31\ k\Omega} - \frac{1}{1\ M\Omega} - \frac{1}{8.66\ k\Omega}} = 23.8\ k\Omega \quad (12)$$

Choosing the nearest 1% resistor value gives R_A = 23.7 kΩ.

C_{OUT} Selection

The required equivalent series resistance (ESR) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be less than or equal to the specified output resistance (R_{OUT}), in this case 1.5 mΩ. The capacitance must be large enough that the voltage across the capacitors, which is the sum of the resistive and capacitive voltage deviations, does not deviate beyond the initial resistive step while the inductor current ramps up or down to the value corresponding to the new load current.

One can, for example, use nine MBZ-type capacitors from Rubycon, with 2200 µF capacitance, a 6.3 V voltage rating, and 13 mΩ ESR. The nine capacitors have a maximum total ESR of 1.44 mΩ when connected in parallel.

As long as the capacitance of the output capacitor bank is above a critical value and the regulating loop is compensated with Analog Devices' proprietary compensation technique (ADOPT), the actual capacitance value has no influence on the peak-to-peak deviation of the output voltage to a full step change in the load current. The critical capacitance can be calculated as follows:

$$C_{OUT(CRIT)} = \frac{I_O}{R_{OUT} \times V_{OUT}} \times \frac{L}{n} = \frac{65\ A}{1.5\ m\Omega \times 1.5\ V} \times \frac{600\ nH}{3} = 5.78\ mF \quad (13)$$

The critical capacitance limit for this circuit is 6.93 mF, while the actual capacitance of the nine Rubycon capacitors is 9 × 2200 µF = 19.8 mF. In this case, the capacitance is safely above the critical value.

Multilayer ceramic capacitors are also required for high-frequency decoupling of the processor. The exact number of these MLC capacitors is a function of the board layout space and parasitics. Typical designs use twenty to thirty 10 µF MLC capacitors located as close to the processor power pins as is practical.

Feedback Loop Compensation Design for ADOPT

Optimized compensation of the ADP3163 allows the best possible containment of the peak-to-peak output voltage deviation. Any practical switching power converter is inherently limited by the inductor in its output current slew rate to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and assuming that the capacitance of the output capacitor is larger than the critical value defined by Equation 13, this will produce a peak output voltage deviation equal to the ESR of the output capacitor times the load current change.

The optimal implementation of voltage positioning, ADOPT, will create an output impedance of the power converter that is entirely resistive over the widest possible frequency range, including dc, and equal to the maximum acceptable ESR of the output capacitor array. With the resistive output impedance, the output voltage will droop in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output capacitor bank.

With an ideal current-mode-controlled converter, where the average inductor current would respond without delay to the command signal, the resistive output impedance could be achieved by having a single-pole roll-off of the voltage gain of the voltage-error amplifier. The pole frequency must coincide with the ESR zero of the output capacitor bank. The ADP3163 uses constant frequency current-mode control, which is known to have a nonideal, frequency dependent command signal to inductor current transfer function. The frequency dependence manifests in the form of a pair of complex conjugate poles at one-half of the switching frequency. A purely resistive output impedance could be achieved by canceling the complex conjugate poles with zeros at the same complex frequencies and adding a third pole equal to the ESR zero of the output capacitor. Such a compensating network would be quite complicated. Fortunately, in practice it is sufficient to cancel the pair of complex conjugate poles with a single real zero placed at one-half of the switching frequency. Although the end result is not a perfectly resistive output impedance, the remaining frequency dependence causes only a small percentage of deviation from the ideal resistive response. The single-pole and single-zero compensation can be easily implemented by terminating the g_m error amplifier with the parallel combination of a resistor (R_T) and a series RC network. The value of the terminating resistor R_T was determined previously; the capacitance and resistance of the series RC network are calculated as follows:

$$C_{OC} = \frac{C_{OUT} \times R_{OUT}}{R_T} - \frac{n}{\pi \times f_{OSC} \times R_T} = \frac{19.8\ mF \times 1.5\ m\Omega}{6.31\ k\Omega} - \frac{3}{\pi \times 600\ kHz \times 6.31\ k\Omega} = 4.4\ nF \quad (14)$$

The nearest standard value of C_{OC} is 4.7 nF. The resistance of the zero-setting resistor in series with the compensating capacitor is:

$$R_Z = \frac{n}{\pi \times f_{OSC} \times C_{OC}} = \frac{3}{\pi \times 600\ kHz \times 4.7\ nF} = 338\ \Omega \quad (15)$$

The nearest standard 5% resistor value is 330 Ω. Note that this resistor is only required when C_{OUT} approaches C_{CRIT} (within 25% or less). In this example, $C_{OUT} >> C_{CRIT}$, and R_Z can therefore be omitted.

Power MOSFETs

In this example, six N-channel power MOSFETs must be used; three as the main (control) switches, and the remaining three as the synchronous rectifier switches. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3414) dictates whether standard threshold or logic-level threshold MOSFETs must be used. Since V_{GATE} <8 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are strongly recommended.

The maximum output current I_O determines the $R_{DS(ON)}$ requirement for the power MOSFETs. When the ADP3163 is operating in continuous mode, the simplifying assumption can be made that in each phase one of the two MOSFETs is always conducting the average inductor current. For V_{IN} = 12 V and V_{OUT} = 1.45 V, the duty ratio of the high-side MOSFET is:

$$D_{HSF} = \frac{V_{OUT}}{V_{IN}} = \frac{1.5\ V}{12\ V} = 12.5\% \quad (16)$$

The duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF} = 1 - D_{HSF} = 87.5\% \quad (17)$$

The maximum rms current of the high-side MOSFET during normal operation is:

$$I_{HSF(MAX)} = \frac{I_O}{n} \times \sqrt{D_{HSF} \times \left(1 + \frac{I_{L(RIPPLE)}^2}{3 \times I_O^2}\right)} = \frac{65\ A}{3} \times \sqrt{0.125 \times \left(1 + \frac{10.9\ A^2}{3 \times 65\ A^2}\right)} = 7.7\ A \quad (18)$$

The maximum rms current of the low-side MOSFET during normal operation is:

$$I_{LSF(MAX)} = I_{HFS(MAX)} \times \sqrt{\frac{D_{LSF}}{D_{HSF}}} = 7.7\ A \times \sqrt{\frac{0.875}{0.125}} = 20.4\ A \quad (19)$$

The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation in the eight MOSFETs of the four-phase converter will be:

$$P_{FET(TOTAL)} = 0.1 \times V_{MIN} \times I_O = 0.1 \times 1.394\ V \times 65\ A = 9.06\ W \quad (20)$$

Allocating half of the total dissipation for the four high-side MOSFETs and half for the four low-side MOSFETs, and assuming that the resistive and switching losses of the high-side MOSFETs are equal, the required maximum MOSFET resistances will be:

$$R_{DS(ON)HSF} = \frac{P_{FET(TOTAL)}}{4 \times n \times I_{HSF(MAX)}^{2}} = \frac{9.06\ W}{4 \times 3 \times 7.7\ A^2} = 12.7\ m\Omega \quad (21)$$

and:

$$R_{DS(ON)LSF} = \frac{P_{FET(TOTAL)}}{2 \times n \times I_{LSF(MAX)}^{2}} = \frac{9.06\ W}{2 \times 3 \times 20.4\ A^2} = 3.63\ m\Omega \quad (22)$$

Note that there is a trade-off between converter efficiency and cost. Larger MOSFETs reduce the conduction losses and allow higher efficiency, but increase the system cost. A Fairchild FDB7030L ($R_{DS(ON)}$ = 7 mΩ nominal, 10 mΩ worst-case) for the high-side and a Fairchild FDB8030L ($R_{DS(ON)}$ = 3.1 mΩ nominal, 5.6 mΩ worst-case) for the low-side are good choices. The high-side MOSFET dissipation is:

$$P_{HSF} = R_{DS(ON)HSF} \times I_{HSF(MAX)}^{2} \frac{V_{IN} \times I_{L(PK)} \times Q_G \times f_{SW}}{2 \times I_G} + V_{IN} \times Q_{RR} \times f_{SW} = 10\ m\Omega \times 7.7\ A^2 + \frac{12\ V \times 29\ A \times 35\ nC \times 200\ kHz}{2 \times 1\ A} + 12\ V \times 150\ nC \times 200\ kHz = 2.17\ W \quad (23)$$

Where the first term is the conduction loss of the MOSFET, the second term represents the turn-off loss of the MOSFET and the third term represents the turn-on loss due to the stored charge in the body diode of the low-side MOSFET. In the second term, Q_G is the gate charge to be removed from the gate for turn-off and I_G is the gate turn-off current. From the data sheet, for the FDB7030L the value of Q_G is about 35 nC and the peak gate drive current provided by the ADP3414 is about 1 A. In the third term, Q_{RR}, is the charge stored in the body diode of the low-side MOSFET at the valley of the inductor current. The data sheet of the FDB8030L does not give that information, so an estimated value of 150 nC is used. This estimate is based on information found on data sheets of similar devices. In both terms, f_{SW} is the actual switching frequency of the MOSFETs, or 200 kHz. $I_{L(PK)}$ is the peak current in the inductor, or 27 A.)

The worst-case low-side MOSFET dissipation is:

$$P_{LSF} = R_{DS(ON)LSF} \times I_{LSF(MAX)}^{2} = 5.6\ m\Omega \times 20.4\ A^2 = 2.33\ W \quad (24)$$

Note that there are no switching losses in the low-side MOSFET.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to V_{OUT}/V_{IN} and an amplitude of one-half of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{C(RMS)} = \frac{I_O}{n} \times \sqrt{n \times D_{HSF} - (n \times D_{HSF})^2} = \frac{65\ A}{3} \times \sqrt{3 \times 0.125 - (3 \times 0.125)^2} = 10.5\ A \quad (25)$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 270 µF, 16 V OS-CON capacitors with a ripple current rating of 4.4 A each.

The ripple voltage across the three paralleled capacitors is:

$$V_{C(RIPPLE)} = \frac{I_O}{n} \times \left(\frac{ESR_C}{n_C} + \frac{D_{HSF}}{n_C \times C_{IN} \times f_{SW}} \right) = \frac{65\ A}{3} \times \left(\frac{18\ m\Omega}{3} + \frac{0.125}{3 \times 270\ \mu F \times 200\ kHz} \right) = 147\ mV \quad (26)$$

Multilayer ceramic input capacitors are also required. These capacitors should be placed between the input side of the current sense resistor and the sources of the low side synchronous MOSFETS. These capacitors decouple the high frequency leading edge current spike which supplies the reverse recovery charge of the low side MOSFETS body diode. The exact number required is a function of board layout. Typical designs will use two 10 µF MLC capacitors.

To reduce the input-current di/dt to below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 1 µH @ 15 A) should be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For good results, at least a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 12 V), and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the voltage and current sense lines of the ADP3163) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
4. The power ground plane should not extend under signal components, including the ADP3163 itself. If necessary, follow the preceding guideline to use the signal ground plane as a shield between the power ground plane and the signal circuitry.
5. The GND pin of the ADP3163 should be connected first to the timing capacitor (on the CT pin), and then into the signal ground plane. In cases where no signal ground plane can be used, short interconnections to other signal ground circuitry in the power converter should be used.
6. The output capacitors of the power converter should be connected to the signal ground plane even though power current flows in the ground of these capacitors. For this reason, it is advised to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
7. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.
8. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

9. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the power MOSFETs, and the power Schottky diode, if used (see next), including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.
10. MLC input capacitors should be placed between V_{IN} and power ground as close to the sources of the low-side MOSFETS as possible.
11. To dampen ringing, an RC snubber circuit should be placed from the SW hole of each phase to ground.
12. An optional power Schottky diode (3 A–5 A dc rating) from each lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFETs. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body diode prevents the drain voltage from being pulled high quickly. The upper MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time. The Schottky diode has to be connected with very short copper traces to the MOSFET to be effective.
13. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.

14. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the current sensing resistor, the inductors, the output capacitors, and back to the input capacitors.
15. For best EMI containment, the power ground plane should extend fully under all the power components except the output capacitors. These components are: the input capacitors, the power MOSFETs and Schottky diodes, the inductors, the current sense resistor, and any snubbing element that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

Signal Circuitry

16. The output voltage is sensed and regulated between the FB pin and the GND pin (which connects to the signal ground plane). The output current is sensed (as a voltage) by the CS+ and CS– pins. In order to avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB trace should be routed atop the signal ground plane and the CS+ and CS– pins. (The CS+ pin should be over the signal ground plane as well.)
17. The CS+ and CS– traces should be Kelvin-connected to the current sense resistor, so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections, does not affect the sensed voltage.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

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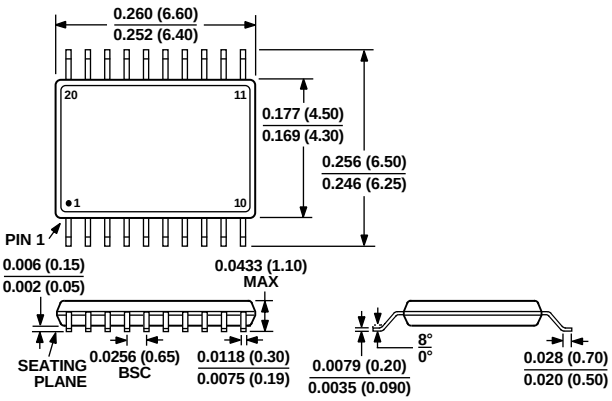
(RU-20)



PRINTED IN U.S.A.

C02483–1.5–7/01(0)