

FEATURES

- 56 MSPS correlated double sampler (CDS) with 6 dB gain
- On-chip horizontal and RG timing driver
- Single-supply operation (2.7 V min)
- Precision Timing™* core with 0.37 ns resolution at 56 MSPS
- Low power CMOS: 105 mW at 2.7 V (115 mW at 3.0 V)
- 48-lead LQFP and 48-lead LFCSP packages

APPLICATIONS

- Professional HDTV camcorders
- Professional/high end digital cameras
- Broadcast cameras
- Industrial high speed cameras
- High speed data-acquisition systems

GENERAL DESCRIPTION

The AD9940 is a high speed, correlated double sampler for high speed digital imaging applications. Integrated with a programmable timing driver using the *Precision Timing* core, the AD9940 features a 56 MHz CDS amplifier with 6 dB of fixed gain, an internal voltage reference supply, and timing control for all the high speed clocks necessary for CCD imaging systems. The Precision Timing core allows adjustment of high speed clocks with a resolution of 0.37 ns. Output buffers are also included, providing drive strength for PCB traces and direct connection to an image signal processor such as the AD9941.

The AD9940 is ideal for applications that need to place the CDS and VGA/ADC circuits on separate PC boards. The fully differential outputs of the AD9940 provide good signal integrity when interfaced with the differential input AD9941. The AD9940 operates from a single 2.7 V power supply, typically dissipates 105 mW (excluding the H/RG drive current), and is packaged in 48-lead LQFP and 48-lead LFCSP packages.

FUNCTIONAL BLOCK DIAGRAM

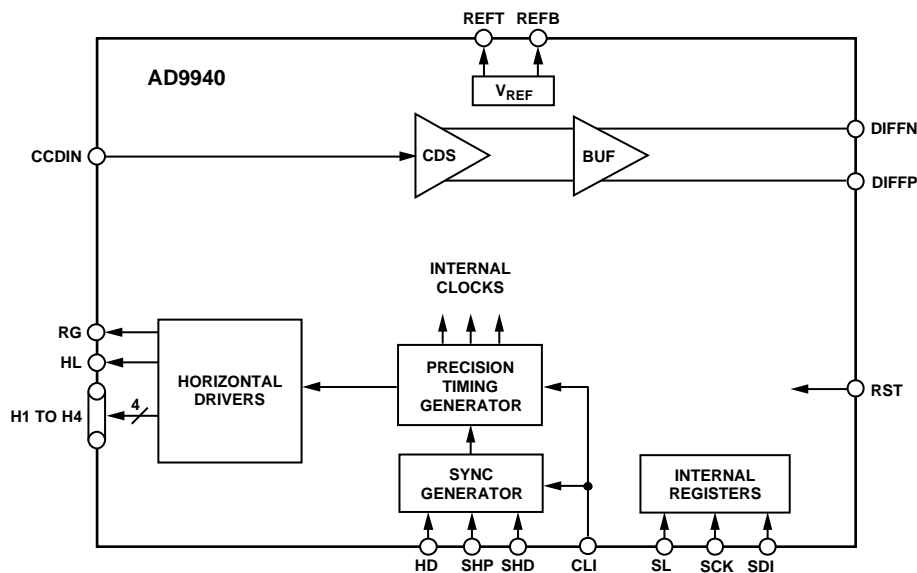


Figure 1.

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

| Parameter | Min | Typ | Max | Unit |
|---|-----|-----|------|------|
| TEMPERATURE RANGE | | | | |
| Operating | -25 | | +85 | °C |
| Storage | -65 | | +150 | °C |
| MAXIMUM CLOCK RATE | 56 | | | MHz |
| POWER SUPPLY VOLTAGE | | | | |
| AVDD, TCVD (AFE, Timing Core) | 2.7 | 3.0 | 3.6 | V |
| OVDD (Analog Buffer) | 2.7 | 3.0 | 3.6 | V |
| DVDD (Digital) | 2.7 | 3.0 | 3.6 | V |
| HVDD (H1 to H4 Drivers) | 2.7 | 3.0 | 3.6 | V |
| RGVDD (RG Driver) | 2.7 | 3.0 | 3.6 | V |
| POWER DISSIPATION ¹ | | | | |
| 56 MHz, AFE supplies = 2.7 V, HVDD = RGVDD = 3.2 V, 70 pF, H1 to H4 Loading | | 265 | | mW |
| 56 MHz, AFE supplies = 3.0 V, HVDD = RGVDD = 3.2 V, 70 pF, H1 to H4 Loading | | 275 | | mW |
| 56 MHz, AFE supplies = 2.7 V, no H or RG drivers | | 105 | | mW |
| 56 MHz, AFE supplies = 3.0 V, no H or RG drivers | | 115 | | mW |
| Standby Mode | | 2 | | mW |

¹ The total power dissipated by the HVDD supply can be approximated using the following equation:

$$\text{Total HVDD Power} = (C_{\text{LOAD}} \times \text{HVDD} \times \text{Pixel Frequency}) \times \text{HVDD}$$

Reducing the H-loading and/or using a lower HVDD supply reduces the power dissipation.

AD9940

ANALOG SPECIFICATIONS

$f_{CL1} = 56 \text{ MHz}$, $AVDD = OVDD = DVDD = TCVD = 3.0 \text{ V}$, -25°C to $+85^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Min | Typ | Max | Unit | Notes |
|--|-------|----------|-----|----------|--|
| CDS | | | | | |
| Gain | 5.0 | 5.5 | 6.0 | dB | |
| Allowable CCD Reset Transient ¹ | | 500 | | mV | |
| Maximum Input Range Before Saturation ¹ | | 1 | | V p-p | |
| Maximum CCD Black Pixel Amplitude ¹ | | ± 50 | | mV | |
| Peak Nonlinearity, 500 mV Input Signal | | 0.2 | | % FS | |
| Power Supply Rejection (PSR) | | 36 | | dB | Measured with step change on supply |
| ANALOG OUTPUTS ² | | | | | |
| Typical DIFFP Output Signal Range | 1.2 | | 2.2 | V | 1.2 V corresponds to black level |
| Typical DIFFN Output Signal Range | 1.2 | | 2.2 | V | 2.2 V corresponds to black level |
| Typical Common Mode Level | | 1.7 | | V | Midscale voltage where DIFFP = DIFFN |
| Maximum Differential Output Voltage Swing | | 2 | | V | Defined as DIFFP – DIFFN |
| Output Voltage Compliance | 1.0 | | 2.4 | V | Limitation of output swing into external load |
| Maximum Load Capacitance | | 24 | | pF | Value for each output (AD9941 C_{IN} is $< 24 \text{ pF}$) |
| Minimum Load Resistance (if required) | 5,000 | | | Ω | Only use resistive loading if required by the differential receiver. Proper dc biasing should be used to be compatible with levels in Figure 3 |

¹ Input signal characteristics are defined in Figure 2.

² Output signal characteristics are defined in Figure 3.

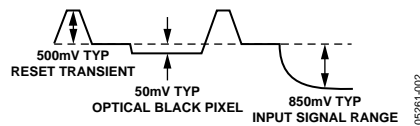


Figure 2. Input Signal Characteristics

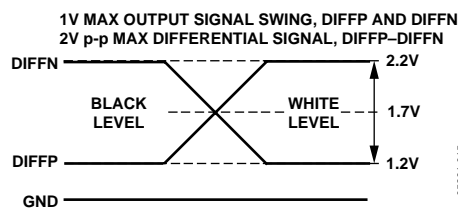


Figure 3. Output Signal Characteristics

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX} , $AVDD = DVDD = OVDD = TCVDD = HVDD = RGVDD = 2.7$ V, -25°C to $+85^{\circ}\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|-------------|-----|------|---------------|
| LOGIC INPUTS | | | | | |
| High Level Input Voltage | V_{IH} | 2.1 | | | V |
| Low Level Input Voltage | V_{IL} | | | 0.6 | V |
| High Level Input Current | I_{IH} | | 10 | | μA |
| Low Level Input Current | I_{IL} | | 10 | | μA |
| Input Capacitance | C_{IN} | | 10 | | pF |
| LOGIC OUTPUTS | | | | | |
| High Level Output Voltage, $I_{OH} = 2$ mA | V_{OH} | 2.2 | | | V |
| Low Level Output Voltage, $I_{OL} = 2$ mA | V_{OL} | | | 0.5 | V |
| CLI INPUT | | | | | |
| High Level Input Voltage | V_{IH-CLI} | 1.85 | | | V |
| Low Level Input Voltage | V_{IL-CLI} | | | 0.85 | V |
| RG-DRIVER AND H-DRIVER OUTPUTS (powered by HVDD, RGVDD) | | | | | |
| High Level Output Voltage (at max output current) | V_{OH} | $VDD - 0.5$ | | | V |
| Low Level Output Voltage (at max output current) | V_{OL} | | | 0.5 | V |
| Maximum Output Current (programmable) | | | | | |
| H-Driver (per output) | | 64 | | | mA |
| RG-Driver, HL-Driver | | 15 | | | mA |
| Maximum Load Capacitance | | | | | |
| H-Driver (per output) | | 100 | | | pF |
| RG-Driver, HL-Driver | | 50 | | | pF |

TIMING SPECIFICATIONS (SLAVE TIMING MODE)

See Figure 10 for Timing Diagram.

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|--------------|-----|-----|-----|------|
| MASTER CLOCK (CLI) | | | | | |
| CLI Clock Period | T_{CLI} | 18 | | | ns |
| CLI High Pulse Width | T_{ADC} | | 9 | | ns |
| Internal Delay from CLI to First Tap | T_{CLIDLY} | | 6 | | ns |
| SAMPLE CLOCKS | | | | | |
| SHP Rising to SHD Rising | T_{S1} | 7.4 | 9 | | ns |
| ADCLK Edge Placement for AD9941 | T_{REC} | | 3 | | ns |
| SERIAL INTERFACE | | | | | |
| Maximum SCK Frequency | f_{SCLK} | 10 | | | MHz |
| SL to SCK Setup Time | t_{LS} | 10 | | | ns |
| SCK to SL Hold Time | t_{LH} | 10 | | | ns |
| SDATA Valid to SCK Rising Edge Setup | t_{DS} | 10 | | | ns |
| SCK Rising Edge to SDATA Valid Hold | t_{DH} | 10 | | | ns |

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|----------------------------------|-------------------------|
| AVDD and TCVDD to AVSS | −0.3 V to +3.9 V |
| HVDD and RGVDD to HVSS and RGVSS | −0.3 V to +3.9 V |
| DVDD and OVDD to DVSS and OVSS | −0.3 V to +3.9 V |
| Any VSS to Any VSS | −0.3 V to +0.3 V |
| CLPOB/HBLK to DVSS | −0.3 V to DVDD + 0.3 V |
| SCK, SL, and SDI to DVSS | −0.3 V to DVDD + 0.3 V |
| RG to RGVSS | −0.3 V to RGVDD + 0.3 V |
| H1–H4 to HVSS | −0.3 V to HVDD + 0.3 V |
| REFT, REFB, and CCDIN to AVSS | −0.3 V to AVDD + 0.3 V |
| Junction Temperature | 150°C |
| Lead Temperature (10 sec) | 350°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is measured using a 4-layer PCB with the exposed paddle soldered to the board.

Thermal resistance for 48-lead LQFP package:

$$\theta_{JA} = 92^{\circ}\text{C/W}$$

Thermal resistance for 48-lead LFCSP package:

$$\theta_{JA} = 24^{\circ}\text{C/W}^1$$

¹ θ_{JA} is measured using a 4-layer PCB with the exposed paddle soldered to the board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

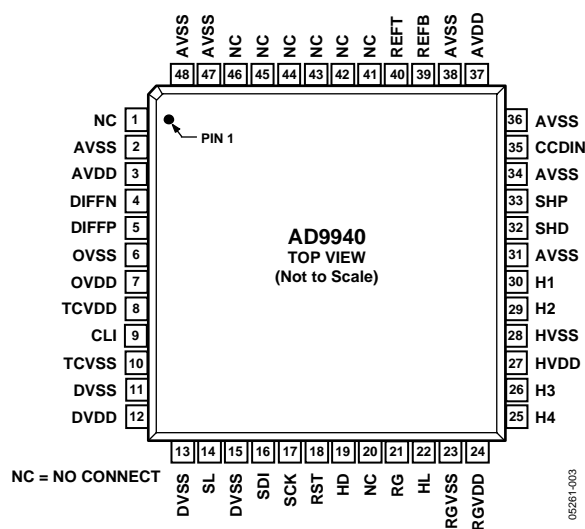


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Memnemonic | Type ¹ | Description |
|---------|------------|-------------------|--|
| 1 | NC | NC | No Connect. Connect to GND. |
| 2 | AVSS | P | Analog Ground. |
| 3 | AVDD | P | Analog Supply. |
| 4 | DIFFN | AO | CDS Output, Data (Negative). |
| 5 | DIFFP | AO | CDS Output, Data (Positive). |
| 6 | OVSS | P | Analog Output Buffer Ground. |
| 7 | OVDD | P | Analog Output Buffer Supply. |
| 8 | TCVDD | P | Analog Supply for Timing Core. |
| 9 | CLI | DI | Reference Clock Input. |
| 10 | TCVSS | P | Analog Ground for Timing Core. |
| 11 | DVSS | P | Digital Ground. |
| 12 | DVDD | P | Digital Logic Power Supply. |
| 13 | DVSS | P | Digital Ground. |
| 14 | SL | DI | 3-Wire Serial Load Pulse. |
| 15 | DVSS | P | Digital Ground. |
| 16 | SDI | DI | 3-Wire Serial Data Input. |
| 17 | SCK | DI | 3-Wire Serial Clock. |
| 18 | RST | DI | Hardware Reset (Low Active). Low = Reset state, High = Normal operation. |
| 19 | HD | DI | Horizontal Sync Pulse. |
| 20 | NC | NC | Do No Connect. Should be left floating. |
| 21 | RG | DO | CCD Reset Gate Clock. |
| 22 | HL | DO | HL Horizontal Clock. |
| 23 | RGVSS | P | RG Driver Ground. |
| 24 | RGVDD | P | RG Driver Power Supply. |
| 25 | H4 | DO | CCD Horizontal Clock 4. |
| 26 | H3 | DO | CCD Horizontal Clock 3. |
| 27 | HVDD | P | Horizontal Clock Driver Supply. |
| 28 | HVSS | P | Horizontal Clock Driver Ground. |
| 29 | H2 | DO | CCD Horizontal Clock 2. |
| 30 | H1 | DO | CCD Horizontal Clock 1. |
| 31 | AVSS | P | Analog Ground. |
| 32 | SHD | DI | Test Clock Input for CCD Data Phase Sampling. |

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| Pin No. | Menemonic | Type ¹ | Description |
|----------|-----------|-------------------|--|
| 33 | SHP | DI | Test Clock Input for CCD Reset Phase Sampling. |
| 34 | AVSS | P | Analog Ground. |
| 35 | CCDIN | AI | CCD Signal Input. |
| 36 | AVSS | P | Analog Ground (CCD Signal Input Reference). |
| 37 | AVDD | P | Analog Supply. |
| 38 | AVSS | P | Analog Ground. |
| 39 | REFB | AO | Voltage Reference Bottom By-Pass. Decoupled to analog ground with a 0.1 μ F capacitor. |
| 40 | REFT | AO | Voltage Reference Top By-Pass. Decoupled to analog ground with a 0.1 μ F capacitor. |
| 41 to 46 | NC | NC | No Connect. Connect to GND. |
| 47, 48 | AVSS | P | Analog Ground. |

¹ Type: AI = analog input; AO = analog output; DI = digital input; DO = digital output; P = power.

DATA BIT DESCRIPTIONS

Table 7.

| Address | Data Bit Content | Default Value | Name | Description |
|---------|------------------|---------------|-----------------------|---|
| 0 | [0] | 0 | PARTSEL | Part Select: 0 = select AD9940 1 = select AD9941 |
| | [1] | 0 | TESTMODE | Always set = 0 |
| | [2] | 0 | SW RESET | Reset registers: 1 = reset all registers to the default values |
| | [3] | 0 | MODE | 0 = slave mode 1 = master mode |
| | [4] | 0 | STANDBY | 0 = normal operation 1 = standby operation |
| | [6:5] [7] | 0 0 | TESTMODE WRITEMODE | Always Set = 0 0 = write to Address 1 to Address 13 1 = write to Address 14 to Address 26 |
| 1 | [6:0] | 0 | TESTMODE | Always set = 0 |
| | [7] | 0 | HBLKMASKPOL | HBLK mask polarity: 0 = H1/H3 low, H2/H4 high 1 = H1/H3 high, H2/H4 low |
| 2 | [0] | 0 | HBLKTOG1_0 [8] | HBLKTOG1 position for Sequence 0 (Bit 8) |
| | [1] | 0 | HBLKTOG1_0 [9] | HBLKTOG1 position for Sequence 0 (Bit 9) |
| | [2] | 0 | HBLKTOG1_0 [10] | HBLKTOG1 position for Sequence 0 (Bit 10) |
| | [3] | 0 | HBLKTOG1_0 [11] | HBLKTOG1 position for Sequence 0 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |
| 3 | [0] | 0 | HBLKTOG1_0 [0] | HBLKTOG1 position for Sequence 0 (Bit 0) |
| | [1] | 0 | HBLKTOG1_0 [1] | HBLKTOG1 position for Sequence 0 (Bit 1) |
| | [2] | 0 | HBLKTOG1_0 [2] | HBLKTOG1 position for Sequence 0 (Bit 2) |
| | [3] | 0 | HBLKTOG1_0 [3] | HBLKTOG1 position for Sequence 0 (Bit 3) |
| | [4] | 0 | HBLKTOG1_0 [4] | HBLKTOG1 position for Sequence 0 (Bit 4) |
| | [5] | 0 | HBLKTOG1_0 [5] | HBLKTOG1 position for Sequence 0 (Bit 5) |
| | [6] | 1 | HBLKTOG1_0 [6] | HBLKTOG1 position for Sequence 0 (Bit 6) |
| | [7] | 0 | HBLKTOG1_0 [7] | HBLKTOG1 position for Sequence 0 (Bit 7) |
| 4 | [0] | 0 | HBLKTOG2_0 [8] | HBLKTOG2 position for Sequence 0 (Bit 8) |
| | [1] | 0 | HBLKTOG2_0 [9] | HBLKTOG2 position for Sequence 0 (Bit 9) |
| | [2] | 0 | HBLKTOG2_0 [10] | HBLKTOG2 position for Sequence 0 (Bit 10) |
| | [3] | 0 | HBLKTOG2_0 [11] | HBLKTOG2 position for Sequence 0 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |
| 5 | [0] | 0 | HBLKTOG2_0 [0] | HBLKTOG2 position for Sequence 0 (Bit 0) |
| | [1] | 0 | HBLKTOG2_0 [1] | HBLKTOG2 position for Sequence 0 (Bit 1) |
| | [2] | 0 | HBLKTOG2_0 [2] | HBLKTOG2 position for Sequence 0 (Bit 2) |
| | [3] | 0 | HBLKTOG2_0 [3] | HBLKTOG2 position for Sequence 0 (Bit 3) |
| | [4] | 0 | HBLKTOG2_0 [4] | HBLKTOG2 position for Sequence 0 (Bit 4) |
| | [5] | 0 | HBLKTOG2_0 [5] | HBLKTOG2 position for Sequence 0 (Bit 5) |
| | [6] | 1 | HBLKTOG2_0 [6] | HBLKTOG2 position for Sequence 0 (Bit 6) |
| | [7] | 0 | HBLKTOG2_0 [7] | HBLKTOG2 position for Sequence 0 (Bit 7) |
| 6 | [0] | 0 | HBLKTOG1_1 [8] | HBLKTOG1 position for Sequence 1 (Bit 8) |
| | [1] | 0 | HBLKTOG1_1 [9] | HBLKTOG1 position for Sequence 1 (Bit 9) |
| | [2] | 0 | HBLKTOG1_1 [10] | HBLKTOG1 position for Sequence 1 (Bit 10) |
| | [3] | 0 | HBLKTOG1_1 [11] | HBLKTOG1 position for Sequence 1 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |

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| Address | Data Bit Content | Default Value | Name | Description |
|---------|------------------|---------------|-----------------|---|
| 7 | [0] | 0 | HBLKTOG1_1 [0] | HBLKTOG1 position for Sequence 1 (Bit 0) |
| | [1] | 0 | HBLKTOG1_1 [1] | HBLKTOG1 position for Sequence 1 (Bit 1) |
| | [2] | 0 | HBLKTOG1_1 [2] | HBLKTOG1 position for Sequence 1 (Bit 2) |
| | [3] | 0 | HBLKTOG1_1 [3] | HBLKTOG1 position for Sequence 1 (Bit 3) |
| | [4] | 0 | HBLKTOG1_1 [4] | HBLKTOG1 position for Sequence 1 (Bit 4) |
| | [5] | 0 | HBLKTOG1_1 [5] | HBLKTOG1 position for Sequence 1 (Bit 5) |
| | [6] | 1 | HBLKTOG1_1 [6] | HBLKTOG1 position for Sequence 1 (Bit 6) |
| | [7] | 0 | HBLKTOG1_1 [7] | HBLKTOG1 position for Sequence 1 (Bit 7) |
| 8 | [0] | 0 | HBLKTOG2_1 [8] | HBLKTOG2 position for Sequence 1 (Bit 8) |
| | [1] | 0 | HBLKTOG2_1 [9] | HBLKTOG2 position for Sequence 1 (Bit 9) |
| | [2] | 0 | HBLKTOG2_1 [10] | HBLKTOG2 position for Sequence 1 (Bit 10) |
| | [3] | 0 | HBLKTOG2_1 [11] | HBLKTOG2 position for Sequence 1 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |
| 9 | [0] | 0 | HBLKTOG2_1 [0] | HBLKTOG2 position for Sequence 1 (Bit 0) |
| | [1] | 0 | HBLKTOG2_1 [1] | HBLKTOG2 position for Sequence 1 (Bit 1) |
| | [2] | 0 | HBLKTOG2_1 [2] | HBLKTOG2 position for Sequence 1 (Bit 2) |
| | [3] | 0 | HBLKTOG2_1 [3] | HBLKTOG2 position for Sequence 1 (Bit 3) |
| | [4] | 0 | HBLKTOG2_1 [4] | HBLKTOG2 position for Sequence 1 (Bit 4) |
| | [5] | 0 | HBLKTOG2_1 [5] | HBLKTOG2 position for Sequence 1 (Bit 5) |
| | [6] | 1 | HBLKTOG2_1 [6] | HBLKTOG2 position for Sequence 1 (Bit 6) |
| | [7] | 0 | HBLKTOG2_1 [7] | HBLKTOG2 position for Sequence 1 (Bit 7) |
| 10 | [0] | 0 | HBLKTOG1_2 [8] | HBLKTOG1 position for Sequence 2 (Bit 8) |
| | [1] | 0 | HBLKTOG1_2 [9] | HBLKTOG1 position for Sequence 2 (Bit 9) |
| | [2] | 0 | HBLKTOG1_2 [10] | HBLKTOG1 position for Sequence 2 (Bit 10) |
| | [3] | 0 | HBLKTOG1_2 [11] | HBLKTOG1 position for Sequence 2 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |
| 11 | [0] | 0 | HBLKTOG1_2 [0] | HBLKTOG1 position for Sequence 2 (Bit 0) |
| | [1] | 0 | HBLKTOG1_2 [1] | HBLKTOG1 position for Sequence 2 (Bit 1) |
| | [2] | 0 | HBLKTOG1_2 [2] | HBLKTOG1 position for Sequence 2 (Bit 2) |
| | [3] | 0 | HBLKTOG1_2 [3] | HBLKTOG1 position for Sequence 2 (Bit 3) |
| | [4] | 0 | HBLKTOG1_2 [4] | HBLKTOG1 position for Sequence 2 (Bit 4) |
| | [5] | 0 | HBLKTOG1_2 [5] | HBLKTOG1 position for Sequence 2 (Bit 5) |
| | [6] | 1 | HBLKTOG1_2 [6] | HBLKTOG1 position for Sequence 2 (Bit 6) |
| | [7] | 0 | HBLKTOG1_2 [7] | HBLKTOG1 position for Sequence 2 (Bit 7) |
| 12 | [0] | 0 | HBLKTOG2_2 [8] | HBLKTOG2 position for Sequence 2 (Bit 8) |
| | [1] | 0 | HBLKTOG2_2 [9] | HBLKTOG2 position for Sequence 2 (Bit 9) |
| | [2] | 0 | HBLKTOG2_2 [10] | HBLKTOG2 position for Sequence 2 (Bit 10) |
| | [3] | 0 | HBLKTOG2_2 [11] | HBLKTOG2 position for Sequence 2 (Bit 11) |
| | [7:4] | 0 | TESTMODE | Always set = 0 |
| 13 | [0] | 0 | HBLKTOG2_2 [0] | HBLKTOG2 position for Sequence 2 (Bit 0) |
| | [1] | 0 | HBLKTOG2_2 [1] | HBLKTOG2 position for Sequence 2 (Bit 1) |
| | [2] | 0 | HBLKTOG2_2 [2] | HBLKTOG2 position for Sequence 2 (Bit 2) |
| | [3] | 0 | HBLKTOG2_2 [3] | HBLKTOG2 position for Sequence 2 (Bit 3) |
| | [4] | 0 | HBLKTOG2_2 [4] | HBLKTOG2 position for Sequence 2 (Bit 4) |
| | [5] | 0 | HBLKTOG2_2 [5] | HBLKTOG2 position for Sequence 2 (Bit 5) |
| | [6] | 1 | HBLKTOG2_2 [6] | HBLKTOG2 position for Sequence 2 (Bit 6) |
| | [7] | 0 | HBLKTOG2_2 [7] | HBLKTOG2 position for Sequence 2 (Bit 7) |

| Address | Data Bit Content | Default Value | Name | Description |
|---------|------------------|---------------|----------|--|
| 14 | [2:0] | 3 | RGDRV | RG drive strength (resolution = 2.2 mA/Step): 0 = Off 1 = 2.2 mA 2 = 4.4 mA ... 7 = 15.4 mA |
| | [3] | 0 | RGPOL | RG polarity: 0 = normal 1 = inverted |
| | [6:4] | 3 | HLDRV | HL drive strength (Resolution = 2.2 mA/Step): 0 = off 1 = 2.2 mA 2 = 4.4 mA ... 7 = 15.4 mA |
| | [7] | 0 | HLPOL | HL polarity: 0 = normal 1 = inverted |
| 15 | [5:0] | 0 | HLPOSLOC | HL rising edge location |
| | [7:6] | — | Unused | |
| 16 | [5:0] | 24 | HLNEGLOC | HL negative edge location |
| | [7:6] | 0 | Unused | |
| 17 | [5:0] | 0 | RGPOSLOC | RG rising edge location |
| | [7:6] | — | Unused | |
| 18 | [5:0] | 24 | RGNEGLOC | RG negative edge location |
| | [7:6] | — | Unused | |
| 19 | [3:0] | 7 | H2/H4DRV | H2/H4 drive strength (resolution = 4.3 mA/Step): 0 = Off 1 = 4.3 mA 2 = 8.6 mA ... 15 = 64.5 mA |
| | [7:4] | 7 | H1/H3DRV | H1/H3 drive strength (resolution = 4.3 mA/Step): 0 = Off 1 = 4.3 mA 2 = 8.6 mA ... 15 = 64.5 mA |
| 20 | [5:0] | 0 | H1POSLOC | H1 positive edge location |
| | [6] | — | Unused | |
| | [7] | 0 | H1/H3POL | H1/H3 polarity: 0 = normal 1 = inverted (H2/H4 is opposite polarity of H1/H3) |
| 21 | [5:0] | 32 | H1NEGLOC | H1 negative edge location |
| | [7:6] | — | Unused | |
| 22 | [5:0] | 32 | SHPLOC | SHP sampling location |
| | [7:6] | 0 | Unused | |
| 23 | [5:0] | 0 | SHDLOC | SHD sampling location |
| | [7:6] | — | Unused | |
| 24 | [7:0] | 0 | TESTMODE | Always set = 0 |
| 25 | [7:0] | 0 | TESTMODE | Always set = 0 |
| 26 | [7:0] | 0 | TESTMODE | Always set = 0 |

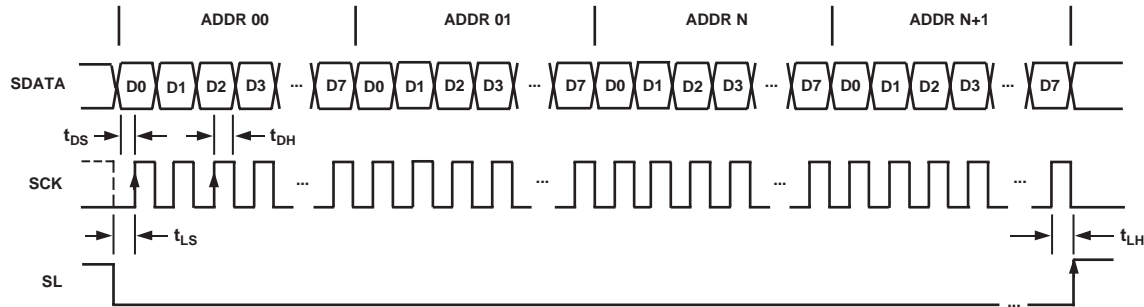
SERIAL INTERFACE TIMING

All the internal registers of the AD9940 are accessed through a 3-wire serial interface. Each register consists of an 8-bit data byte starting with the LSB bit. As shown in Figure 5, the data bits are clocked in on the rising edge of SCK after SL is asserted low and the entire 8-bit word is latched in on the rising edge of SL after the last MSB bit. Consecutive serial writes are performed starting with Address 0 and ending with an address MSB bit prior to asserting SL high.

The AD9940 contains two banks of registers, which are programmed independently. Bank 1 consists of the registers located at Address 0 to Address 13, and Bank 2 consists of Address 14 to Address 26. The WRITEMODE register located at Address 0 is used to select which register bank is written to.

Every write operation must begin with a write to Address 0 to specify Part select bit and Bank location, then followed with any number of consecutive data words. Address 0 is always followed by Address 01 or Address 14 depending on the value specified for WRITEMODE (used for Bank selection).

A hard reset is recommended after power-up to reset the AD9940 prior to performing a serial interface write. A hard reset is performed by asserting the RST pin low for a minimum of 10 μ s. The serial interface pins SCK, SL, and SDI must be in a know state after the RST has been applied.



NOTES

1. ANY NUMBER OF ADJACENT REGISTERS CAN BE LOADED SEQUENTIALLY, BEGINNING WITH THE LOWEST ADDRESS 00.
2. WHEN SEQUENTIALLY LOADING MULTIPLE REGISTERS, THE EXACT REGISTER LENGTH (SHOWN ABOVE) MUST BE USED FOR EACH REGISTER.
3. ALL LOADED REGISTERS ARE SIMULTANEOUSLY UPDATED ON THE RISING EDGE OF SL.

Figure 5. Serial Interface Operation

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SYSTEM OVERVIEW

Figure 6 shows the typical system block diagram for the AD9940. The CCD output is processed by the AD9940's AFE circuitry, which consists of a correlated double sampler (CDS) and output buffer. The differential output of the AD9940 provides good signal integrity when interfaced with the AD9941.

To operate the AD9940, all CCD and AFE timing parameters are programmed into the AD9940 from the system micro-processor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9940 generates the CCD's horizontal and reset gate clocks and all internal AFE clocks.

The H-drivers for H1 to H4, HL and RG, are included in the AD9940, allowing these clocks to be directly connected to the CCD. An H-drive voltage of up to 3.6 V is supported.

ANALOG FRONT END OPERATION

The AD9940 signal-processing chain is shown in Figure 7, consisting of a dc restore circuit, CDS, and output buffer.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external $0.1\ \mu\text{F}$ series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V to be compatible with the 3 V analog supply of the AD9940.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing diagram in Figure 10 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and the data level, respectively, of the CCD signal. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC (Address 22) and SHDLOC (Address 23) control registers. Placement of these two clock edges is critical to achieve the best performance from the CCD.

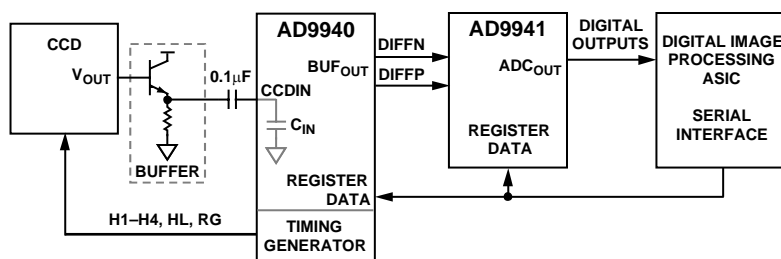


Figure 6. Typical System Block Diagram

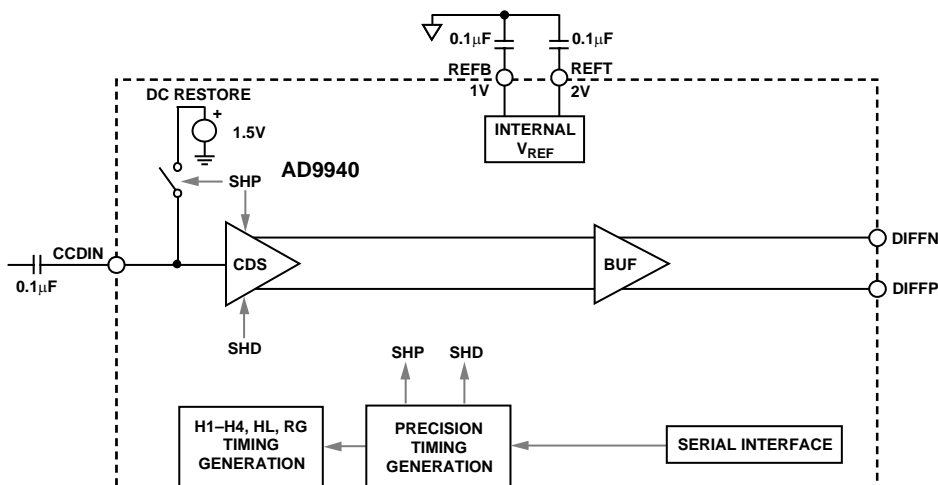


Figure 7. AD9940 Signal-Processing Chain

PRECISION TIMING, HIGH SPEED TIMING GENERATION

The AD9940 generates flexible, high speed timing signals using the Precision Timing core. This core is the foundation for generating the timing used for both the CCD and the AFE: the reset gate RG, horizontal drivers H1 to H4, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

TIMING RESOLUTION

The Precision Timing core uses a $1\times$ master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 8 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Therefore, the edge resolution of the Precision Timing core is $(t_{CLI}/48)$.

HIGH SPEED CLOCK PROGRAMMABILITY

Figure 9 shows how the high speed clocks, RG, HL, H1–H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges, and can be inverted using the polarity control. The horizontal clocks H1/H3 have programmable rising and falling edges, and polarity control. The H2/H4 clocks are always inverses of the H1/H3 H-driver outputs.

Table 8 summarizes the high speed timing registers and their parameters. Each edge location setting is 6 bits wide, but only 48 valid edge locations are available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table 9 shows the correct register values for the corresponding edge locations.

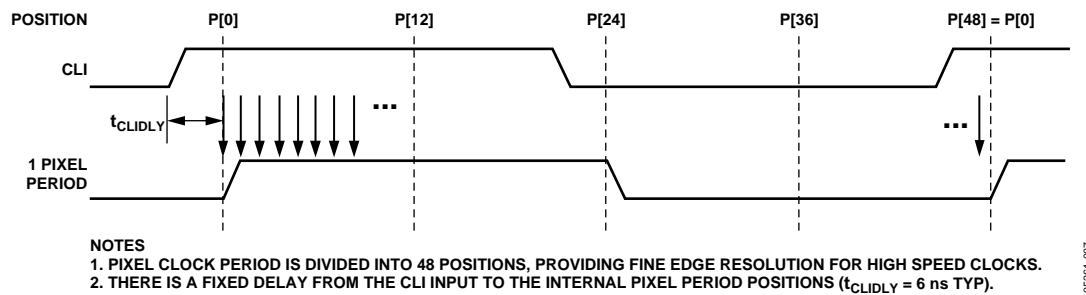


Figure 8. High Speed Clock Resolution from CLI Master Clock Input

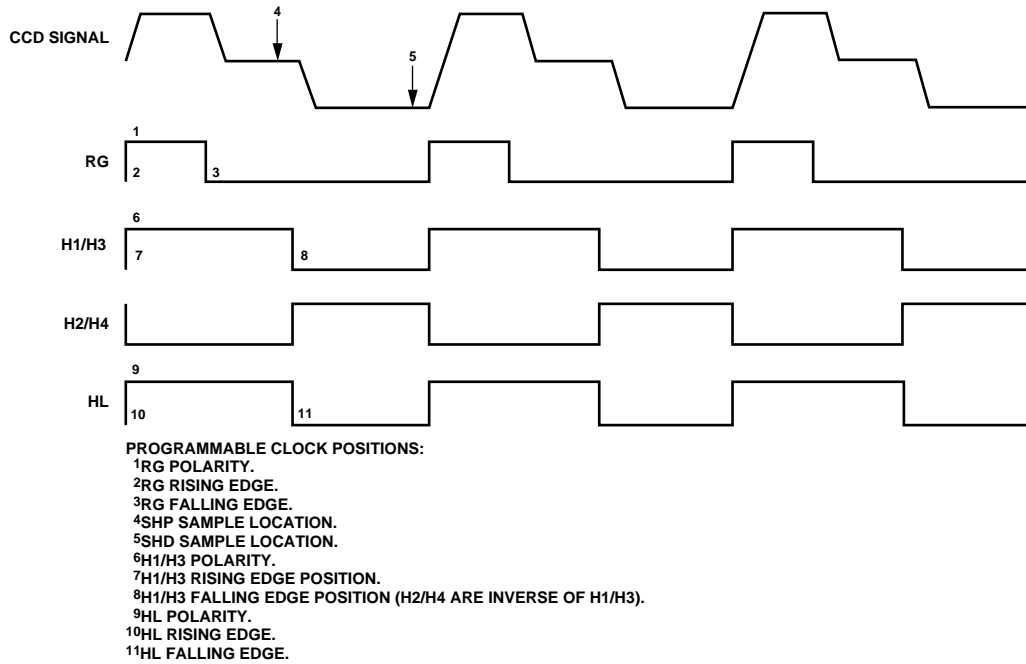


Figure 9. High Speed Clock Programmable Locations

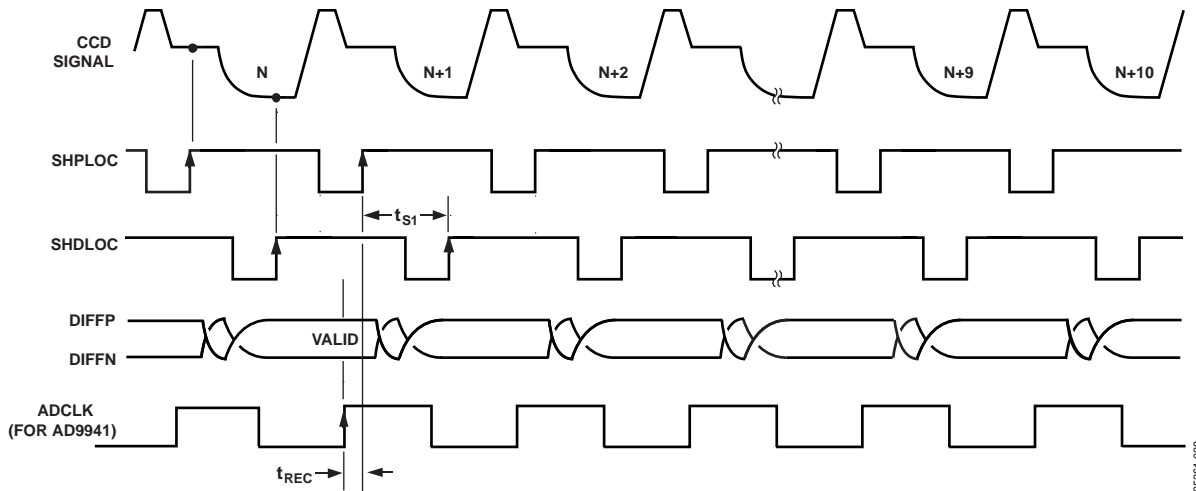


Figure 10. SHP, SHD, and Data Output Timing

H-DRIVER AND RG OUTPUTS

In addition to the programmable timing positions, the AD9940 features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG driver current can be adjusted for optimum rise/fall time into a particular load using the H1/H3DRV, H2/H4DRV, RGDRV, and HLDREV registers. The horizontal output drive strength register is divided into fifteen different 4-bit values, each one adjustable in 4.3 mA increments. The minimum setting of 0 is off or three-state, and the maximum setting of 15 is 64.5 mA.

The RG and HL output drive strength registers are divided into seven 3-bit values, each adjustable in 2.2 mA increments. The minimum setting of 0 is equal to off or three-state, and the maximum setting of 7 is 15.4 mA.

As shown in Figure 11, the H2/H4 outputs are inverses of H1/H3. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results in an H1/H2 crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

Table 8. Timing Core Register Parameters for H1, H3, RG1, RG2, and SHP/SHD

| Parameter | Length (Bits) | Range | Description |
|------------------|---------------|-------------------------|--|
| Polarity | 1 | High/low | Polarity control for H1/H3, RG1, and RG2: 0 = no inversion. 1 = inversion. |
| Positive Edge | 6 | 0 to 47 edge location | Positive edge location for H1/H3, RG1, and RG2. |
| Negative Edge | 6 | 0 to 47 edge location | Negative edge location for H1/H3, RG1, and RG2. |
| Sample Location | 6 | 0 to 47 sample location | Sampling location for SHP and SHD. |
| H-Drive Control | 4 | 0 to 15 current steps | Drive current for H1 to H4, 0 to 15 steps of 4.3 mA each. |
| RG-Drive Control | 3 | 0 to 7 current steps | Drive current for RG, 0 to 7 steps of 2.2 mA each. |
| HL-Drive Control | 3 | 0 to 7 current steps | Drive current for HL, 0 to 7 steps of 2.2 mA each. |

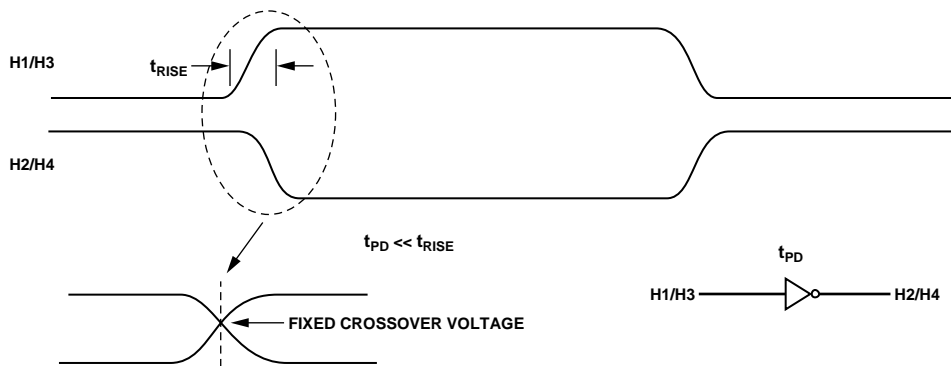


Figure 11. H-Clock Inverse Phase Relationship

Table 9. Precision Timing Edge Locations

| Quadrant | Edge Location (Decimal) | Register Value (Decimal) | Register Value (Binary) |
|----------|-------------------------|--------------------------|-------------------------|
| I | 0 to 11 | 0 to 11 | 00 0000 to 00 1011 |
| II | 12 to 23 | 16 to 27 | 01 0000 to 01 1011 |
| III | 24 to 35 | 32 to 43 | 10 0000 to 10 1011 |
| IV | 36 to 47 | 48 to 59 | 11 0000 to 11 1011 |

HBLK SEQUENCES

The HBLK programmable timing shown in Figure 12 is programmed using the HBLKTOG registers. Only the toggle positions are used to designate the start and the stop positions of the blanking period. Additionally, a polarity control, HBLKMASKPOL, designates the polarity of the horizontal clock signals H1 to H4 during the blanking period. Setting HBLKMASKPOL high sets H1 = H3 = high and H2 = H4 = low during the blanking.

Individual HBLK Sequences

Up to three individual HBLK sequences are available in each line. This allows special H-blanking as shown in Figure 14. The HBLK sequences are sequential starting with Sequence 0. To ensure proper HBLK operation, the following sequence is required for values programmed in the HBLKTOG registers:

$$\begin{aligned} & \text{HBLKTOG1}_0 < \text{HBLKTOG2}_0 < \text{HBLKTOG1}_1 < \\ & \text{HBLKTOG2}_1 < \text{HBLKTOG1}_2 < \text{HBLKTOG2}_2 \end{aligned}$$

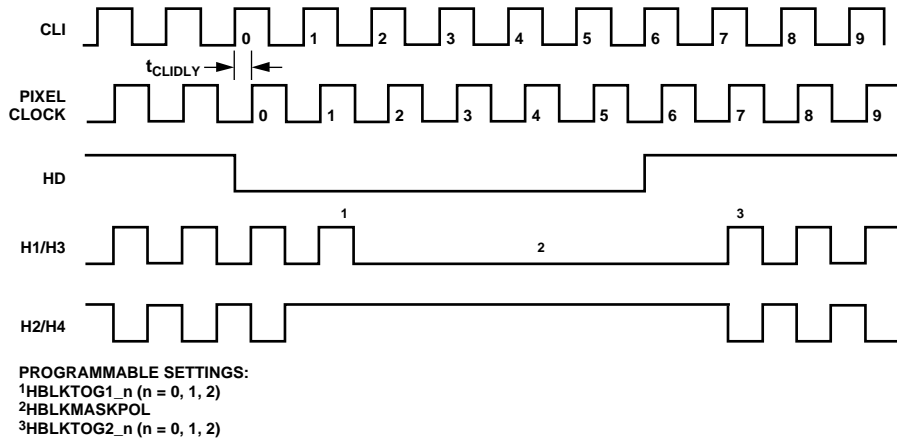
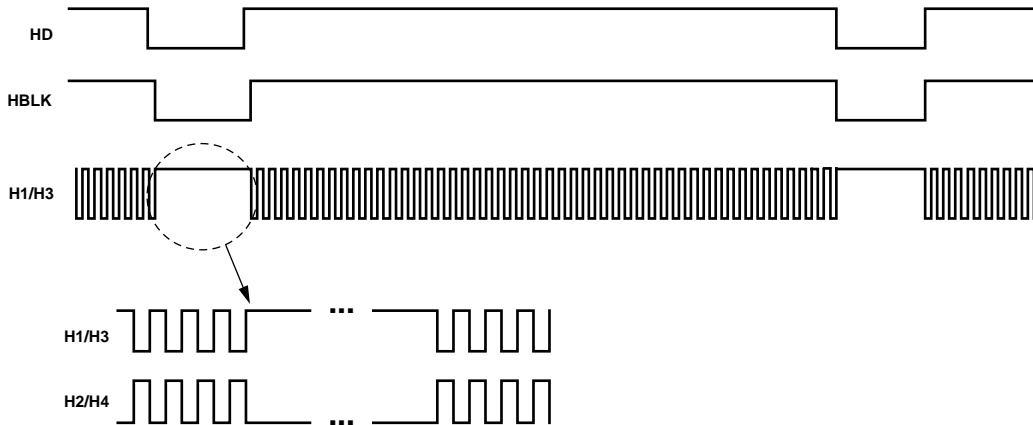
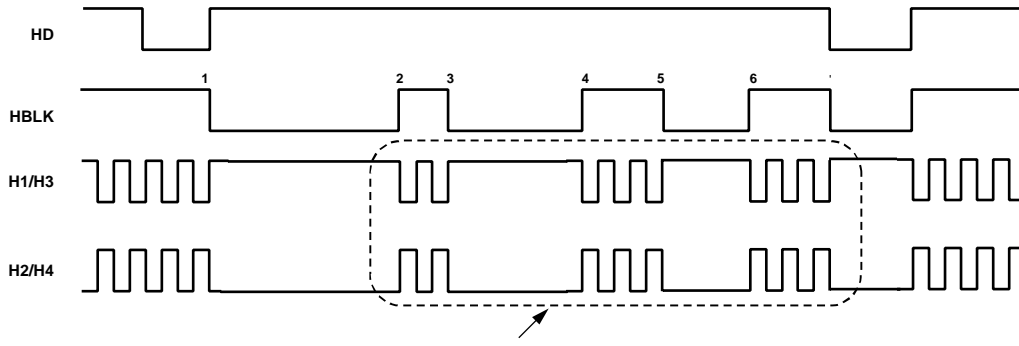


Figure 12. Horizontal Blanking Example Showing HBLKTOG1_0 = 0, HBLKMASKPOL = 0, and HBLKTOG2_0 = 3



NOTE
 1. THE POLARITY OF H1 DURING THE BLANKING REGION IS PROGRAMMABLE (H2 HAS THE OPPOSITE POLARITY OF H1).

Figure 13. HBLK Masking Control



SPECIAL H-BLANK PATTERN IS CREATED USING MULTIPLE HBLK TOGGLE POSITIONS.

PROGRAMMABLE SETTINGS:

- ¹HBLKTOG1_0
- ²HBLKTOG2_0
- ³HBLKTOG1_1
- ⁴HBLKTOG2_1
- ⁵HBLKTOG1_2
- ⁶HBLKTOG2_2

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Figure 14. Generating Special HBLK Patterns

APPLICATIONS INFORMATION

All signals should be carefully routed on the PCB to maintain low noise performance. The CCD output signal should be connected to the CCDIN pin through a 0.1 μF capacitor. The CCD timing signals H1A/B to H2A/B and RG1 to RG2 should be routed directly to the CCD with minimum trace lengths. The clock inputs are located on the other side of the package, where the analog pins are located, and should be connected to the digital ASIC away from the analog and CCD clock signals.

A single ground plane is recommended for the AD9940. This ground plane should be as continuous as possible, particularly where analog pins are concentrated, to ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins.

All decoupling capacitors should be located as close as possible to the package pins. Careful use of a split ground plane can be effective to avoid the return current of horizontal driver flows into analog ground, thereby reducing coupling noise.

Power-supply decoupling is very important for achieving low noise performance. Figure 15 shows the local high frequency decoupling capacitors, but additional capacitance is recommended for lower frequencies. Additional capacitors and ferrite beads can further reduce noise.

When using the LFCSP package, it is recommended that the exposed paddle on the bottom of the package be soldered to a large pad, with multiple vias connecting the pad to the ground plane.

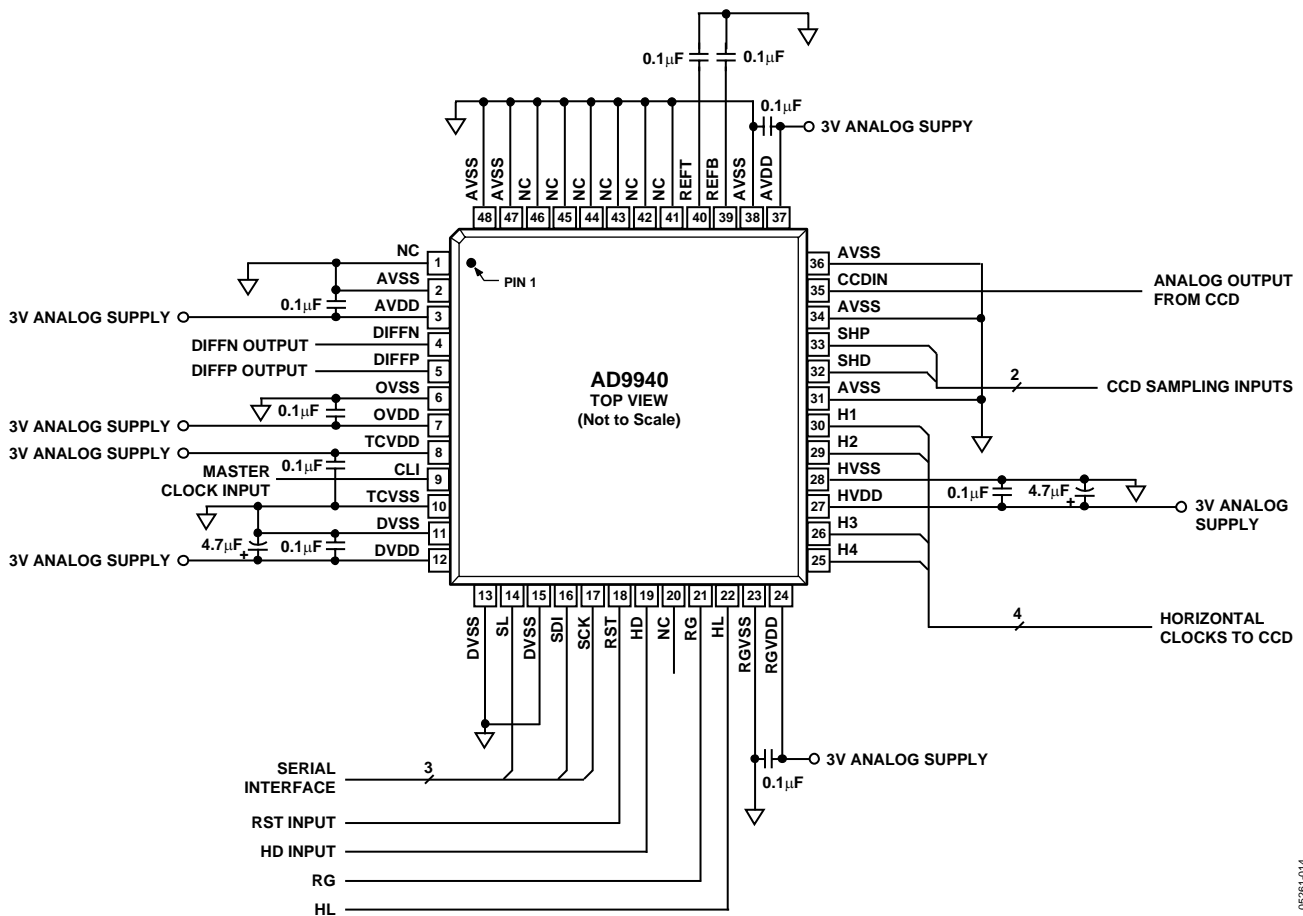
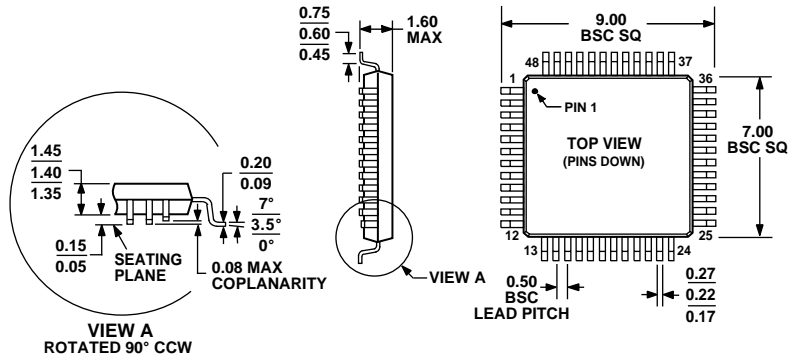


Figure 15. Recommended Circuit Configuration NC pin and supply name consistency

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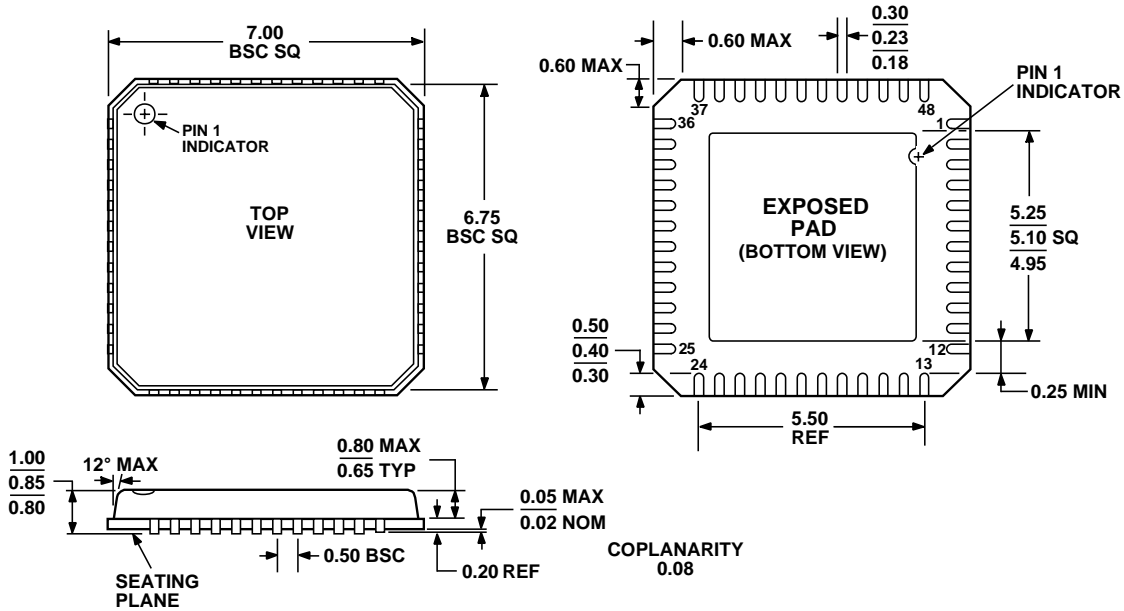
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 16. 48-Lead Low Profile Quad Flat Package [LQFP] (ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 17. 48-Lead Lead Frame Chip Scale Package [LF CSP_VQ] 7 mm x 7mm Body, Very Thin Quad (CP-48-1)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------------------|-------------------|---|----------------|
| AD9940BSTZ ¹ | -25°C to +85°C | 48-lead Low Profile Quad Flat Package [LQFP] | ST-48 |
| AD9940BSTZRL ¹ | -25°C to +85°C | 48-lead Low Profile Quad Flat Package [LQFP] | ST-48 |
| AD9940BCPZ ¹ | -25°C to +85°C | 48-lead Lead Frame Chip Scale Package [LF CSP_VQ] | CP-48-1 |
| AD9940BCPZRL ¹ | -25°C to +85°C | 48-lead Lead Frame Chip Scale Package [LF CSP_VQ] | CP-48-1 |

¹ Z = Pb-free part.