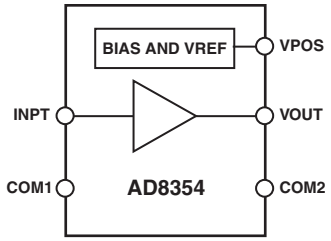
100 MHz to 2.7 GHz RF Gain Block

AD8354

FEATURES
Fixed Gain of 20 dB
Operational Frequency of 100 MHz to 2.7 GHz
Linear Output Power-Up to 4 dBm
Input/Output Internally Matched to 50 Ω
Temperature and Power Supply Stable
Noise Figure 4.2 dB
Power Supply 3 V or 5 V

APPLICATIONS
VCO Buffers
General Tx/Rx Amplification
Power Amplifier Predriver
Low Power Antenna Driver

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8354 is a broadband, fixed-gain linear amplifier that operates at frequencies from 100 MHz up to 2.7 GHz. It is intended for use in a wide variety of wireless devices including cellular, broadband, CATV, and LMDS/MMDS applications. By taking advantage of Analog Devices' high performance complementary Si bipolar process, these gain blocks provide excellent stability over process, temperature, and power supply. This amplifier is single-ended and internally matched to 50 Ω with a return loss of greater than 10 dB over the full operating frequency range.

The AD8354 provides linear output power of nearly 4.3 dBm with 20 dB of gain at 900 MHz when biased at 3 V and an external RF choke is connected between the power supply and the output pin. The dc supply current is 24 mA. At 900 MHz, the output third order intercept (OIP3) is greater than 18 dBm; at 2.7 GHz, the OIP3 is 14 dBm. The noise figure is 4.2 dB at 900 MHz. The reverse isolation (S_{12}) is –33 dB at 900 MHz.

The AD8354 can also operate with a 5 V power supply, in which case no external inductor is required. Under these conditions, the AD8354 delivers 4.8 dBm with 20 dB of gain at 900 MHz. The dc supply current is 26 mA. At 900 MHz, the OIP3 is greater than 19 dBm, and at 2.7 GHz, the OIP3 is 15 dBm. The noise figure is 4.4 dB at 900 MHz. The reverse isolation (S_{12}) is –33 dB.

The AD8354 is fabricated on Analog Devices' proprietary, high performance 25 GHz Si complementary bipolar IC process. The AD8354 is available in a chip scale package that utilizes an exposed paddle for excellent thermal impedance and low impedance electrical connection to ground. It operates over a –40°C to +85°C temperature range.

An evaluation board is available.

REV. A

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AD8354—SPECIFICATIONS (V_S = 3 V, T_A = 25°C, 100 nH external inductor between VOUT and VPOS, Z_0 = 50 Ω, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.1		2.7	GHz
Gain	f = 900 MHz		19.5		dB
	f = 1.9 GHz		18.6		dB
	f = 2.7 GHz		17.1		dB
Delta Gain	f = 900 MHz, –40°C ≤ T_A ≤ +85°C		–0.97		dB
	f = 1.9 GHz, –40°C ≤ T_A ≤ +85°C		–1.05		dB
	f = 2.7 GHz, –40°C ≤ T_A ≤ +85°C		–1.33		dB
Gain Supply Sensitivity	VPOS ± 10%, f = 900 MHz		0.54		dB/V
	f = 1.9 GHz		0.37		dB/V
	f = 2.7 GHz		0.2		dB/V
Reverse Isolation (S_{12})	f = 900 MHz		–33.5		dB
	f = 1.9 GHz		–38		dB
	f = 2.7 GHz		–32.9		dB
RF INPUT INTERFACE	Pin RFIN				
Input Return Loss	f = 900 MHz		24.4		dB
	f = 1.9 GHz		23		dB
	f = 2.7 GHz		12.7		dB
RF OUTPUT INTERFACE	Pin VOUT				
Output Compression Point	f = 900 MHz, 1 dB compression		4.6		dBm
	f = 1.9 GHz		3.7		dBm
	f = 2.7 GHz		2.7		dBm
Delta Compression Point	f = 900 MHz, –40°C ≤ T_A ≤ +85°C		0.7		dB
	f = 1.9 GHz, –40°C ≤ T_A ≤ +85°C		0.7		dB
	f = 2.7 GHz, –40°C ≤ T_A ≤ +85°C		0.8		dB
Output Return Loss	f = 900 MHz		23.6		dB
	f = 1.9 GHz		16.5		dB
	f = 2.7 GHz		14.6		dB
DISTORTION/NOISE					
Output Third Order Intercept	f = 900 MHz, Δf = 1 MHz, P_{IN} = –28 dBm		19		dBm
	f = 1.9 GHz, Δf = 1 MHz, P_{IN} = –28 dBm		16		dBm
	f = 2.7 GHz, Δf = 1 MHz, P_{IN} = –28 dBm		14.2		dBm
Output Second Order Intercept	f = 900 MHz, Δf = 1 MHz, P_{IN} = –28 dBm		29.7		dBm
Noise Figure	f = 900 MHz		4.2		dB
	f = 1.9 GHz		4.8		dB
	f = 2.7 GHz		5.4		dB
POWER INTERFACE	Pin VPOS				
Supply Voltage		2.7	3	3.3	V
Total Supply Current		16	23	31	mA
Supply Voltage Sensitivity			6.2		mA/V
Temperature Sensitivity	–40°C ≤ T_A ≤ +85°C		33		µA/°C

Specifications subject to change without notice.

SPECIFICATIONS (V_S = 5 V, T_A = 25°C, no external inductor between VOUT and VPOS, Z_0 = 50 Ω, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.1		2.7	GHz
Gain	f = 900 MHz		19.5		dB
	f = 1.9 GHz		18.7		dB
	f = 2.7 GHz		17.3		dB
Delta Gain	f = 900 MHz, –40°C ≤ T_A ≤ +85°C		–0.93		dB
	f = 1.9 GHz, –40°C ≤ T_A ≤ +85°C		–0.99		dB
	f = 2.7 GHz, –40°C ≤ T_A ≤ +85°C		–1.21		dB
Gain Supply Sensitivity	VPOS ±10%, f = 900 MHz		0.32		dB/V
	f = 1.9 GHz		0.21		dB/V
	f = 2.7 GHz		0.08		dB/V
Reverse Isolation (S_{12})	f = 900 MHz		–33.5		dB
	f = 1.9 GHz		–37.6		dB
	f = 2.7 GHz		–32.9		dB
RF INPUT INTERFACE	Pin RFIN				
Input Return Loss	f = 900 MHz		24.4		dB
	f = 1.9 GHz		23.9		dB
	f = 2.7 GHz		13.5		dB
RF OUTPUT INTERFACE	Pin VOUT				
Output 1 dB Compression	f = 900 MHz		4.8		dBm
	f = 1.9 GHz		4.6		dBm
	f = 2.7 GHz		3.6		dBm
Delta Compression Point	f = 900 MHz, –40°C ≤ T_A ≤ +85°C		0.37		dB
	f = 1.9 GHz, –40°C ≤ T_A ≤ +85°C		–0.14		dB
	f = 2.7 GHz, –40°C ≤ T_A ≤ +85°C		–0.05		dB
Output Return Loss	f = 900 MHz		23.7		dB
	f = 1.9 GHz		22.5		dB
	f = 2.7 GHz		17.6		dB
DISTORTION/NOISE					
Output Third Order Intercept	f = 900 MHz, Δf = 50 MHz, P_{IN} = –30 dBm		19.3		dBm
	f = 1.9 GHz, Δf = 50 MHz, P_{IN} = –30 dBm		17.3		dBm
	f = 2.7 GHz, Δf = 50 MHz, P_{IN} = –30 dBm		15.3		dBm
Output Second Order Intercept	f = 900 MHz, Δf = 1 MHz, P_{IN} = –28 dBm		28.7		dBm
Noise Figure	f = 900 MHz		4.4		dB
	f = 1.9 GHz		5		dB
	f = 2.7 GHz		5.6		dB
POWER INTERFACE	Pin VPOS				
Supply Voltage		4.5	5	5.5	V
Total Supply Current	T_A = 27°C	17	25	34	mA
Supply Voltage Sensitivity			4		mA/V
Temperature Sensitivity	–40°C ≤ T_A ≤ +85°C		28		µA/°C

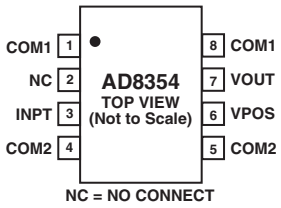
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage VPOS . . . . . 5.5 V
Input Power (re: 50 Ω) . . . . . 10 dBm
  Equivalent Voltage . . . . . 700 mV rms
Internal Power Dissipation
  Paddle Not Soldered . . . . . 325 mW
  Paddle Soldered . . . . . 812 mW
θ_{JA} (Paddle Not Soldered) . . . . . 200°C/W
θ_{JA} (Paddle Soldered) . . . . . 80°C/W
Maximum Junction Temperature . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 240°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

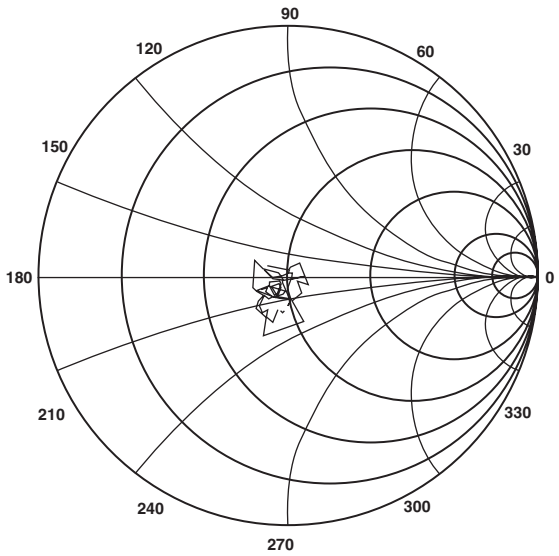
Pin No.	Mnemonic	Description
1, 8	COM1	Device Common. Connect to low impedance ground.
2	NC	No Connection.
3	INPT	RF Input Connection. Must be ac-coupled.
4, 5	COM2	Device Common. Connect to low impedance ground.
6	VPOS	Positive Supply Voltage.
7	VOUT	RF Output Connection. Must be ac-coupled.

ORDERING GUIDE

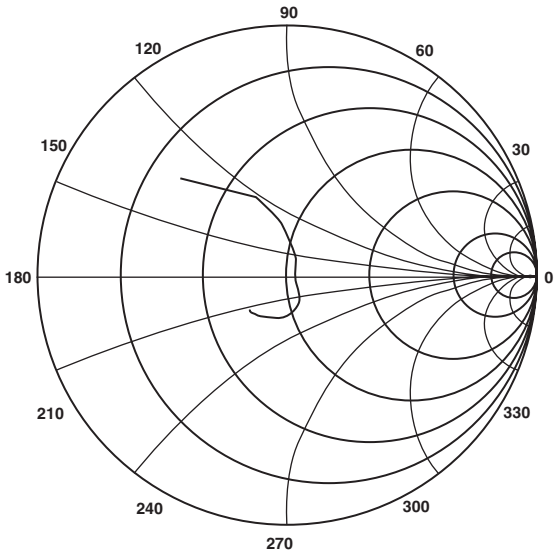
Model	Temperature Range	Package Description	Package Option	Branding
AD8354ACP-R2	–40°C to +85°C	8-Lead LFCSP	CP-8	JCA
AD8354ACP-REEL7	–40°C to +85°C	8-Lead LFCSP	CP-8	JCA
AD8354-EVAL		Evaluation Board		

CAUTION

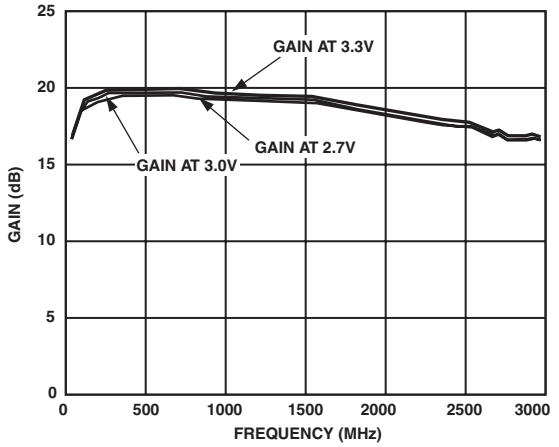
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8354 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



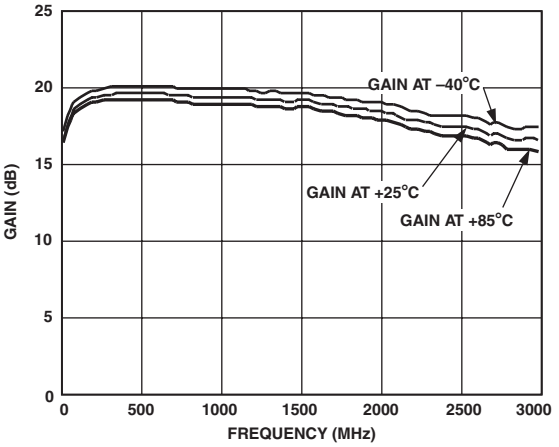
TPC 1. S_{11} vs. Frequency, V_S = 3 V, T_A = 25°C, 100 MHz ≤ f ≤ 3.0 GHz



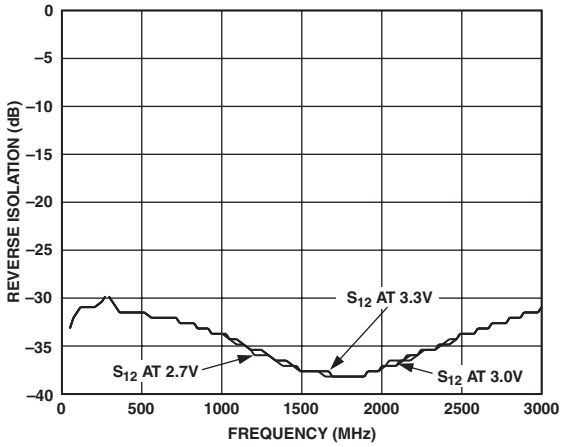
TPC 4. S_{22} vs. Frequency, V_S = 3 V, T_A = 25°C, 100 MHz ≤ f ≤ 3.0 GHz



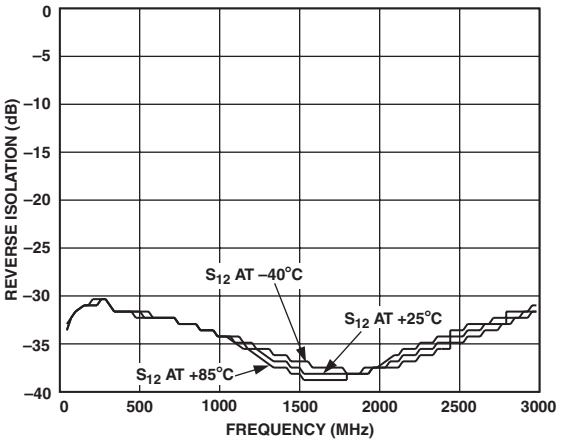
TPC 2. Gain vs. Frequency, V_S = 2.7 V, 3.0 V, and 3.3 V, T_A = 25°C



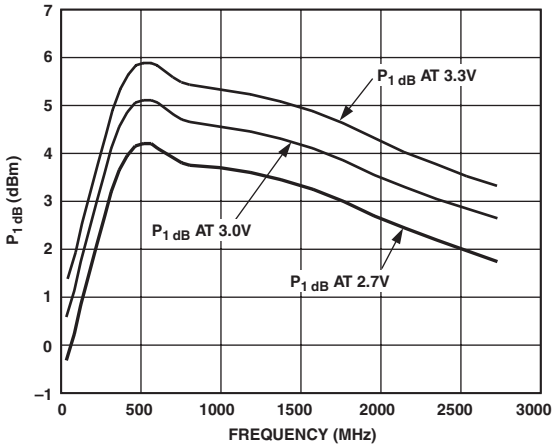
TPC 5. Gain vs. Frequency, V_S = 3 V, T_A = –40°C, +25°C, and +85°C



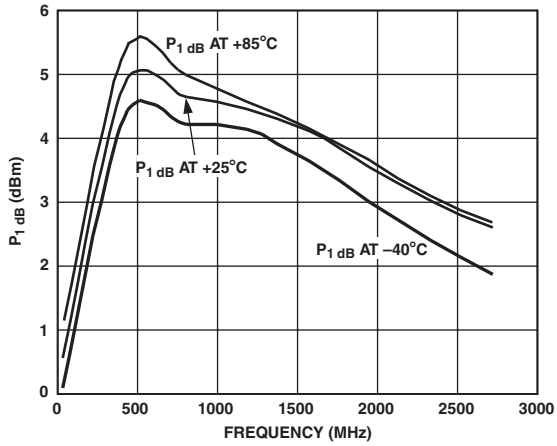
TPC 3. Reverse Isolation vs. Frequency, V_S = 2.7 V, 3 V, and 3.3 V, T_A = 25°C



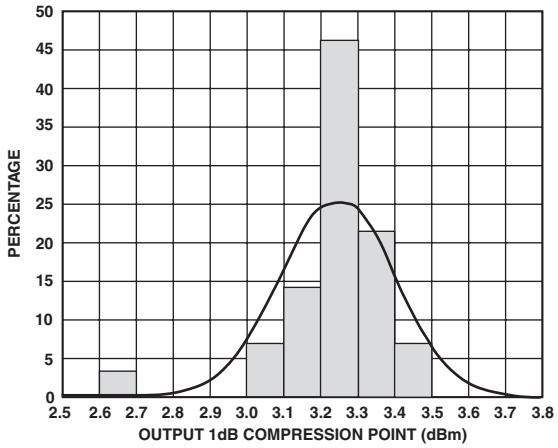
TPC 6. Reverse Isolation vs. Frequency, V_S = 3 V, T_A = –40°C, +25°C, and +85°C



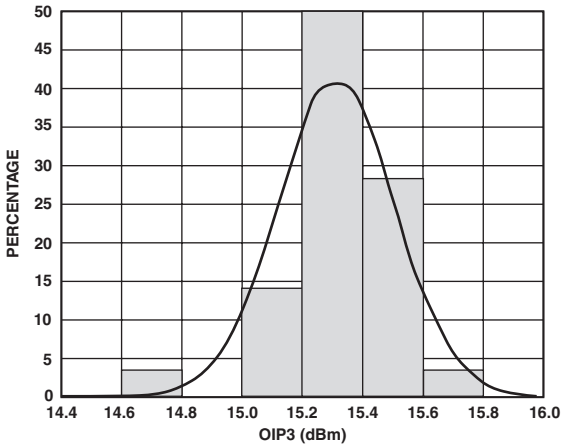
TPC 7. $P_{1\,dB}$ vs. Frequency, V_S = 2.7 V, 3 V, and 3.3 V, T_A = 27°C



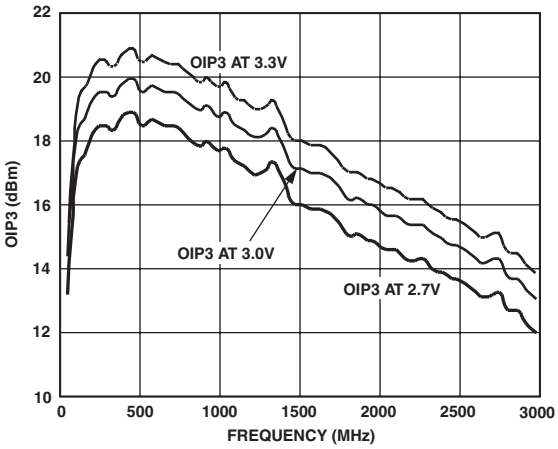
TPC 10. $P_{1\,dB}$ vs. Frequency, V_S = 3 V, T_A = –40°C, +27°C, and +85°C



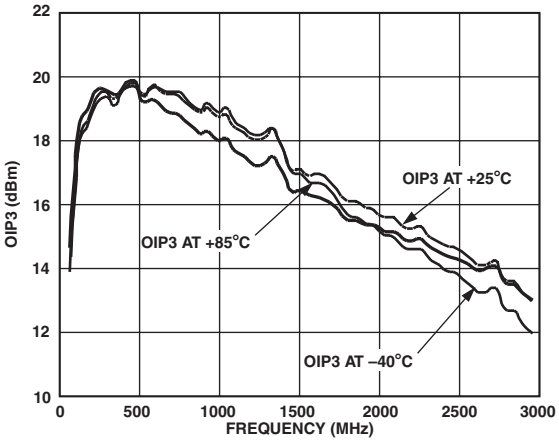
TPC 8. Distribution of $P_{1\,dB}$, V_S = 3 V, T_A = 25°C, f = 2.2 GHz



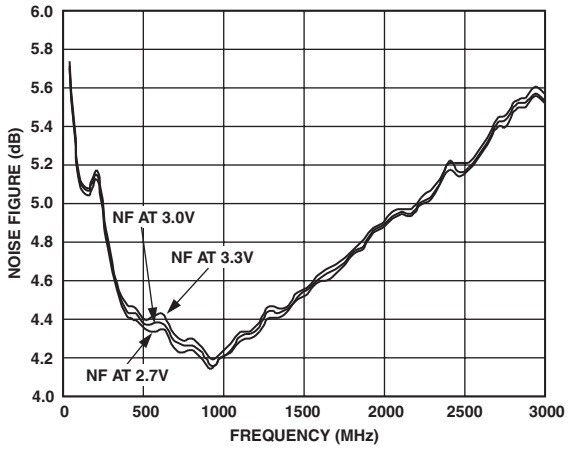
TPC 11. Distribution of OIP3, V_S = 3 V, T_A = 25°C, f = 2.2 GHz



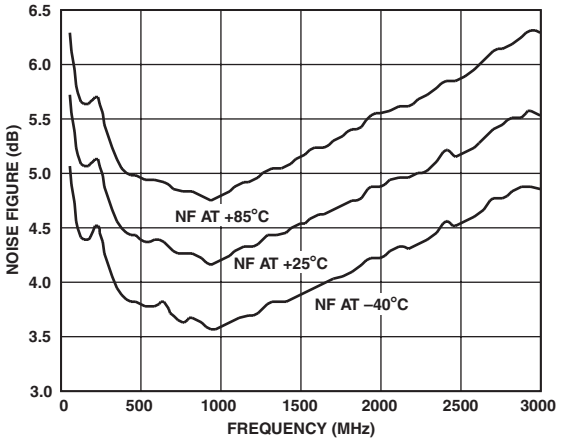
TPC 9. OIP3 vs. Frequency, V_S = 2.7 V, 3 V, and 3.3 V, T_A = 25°C



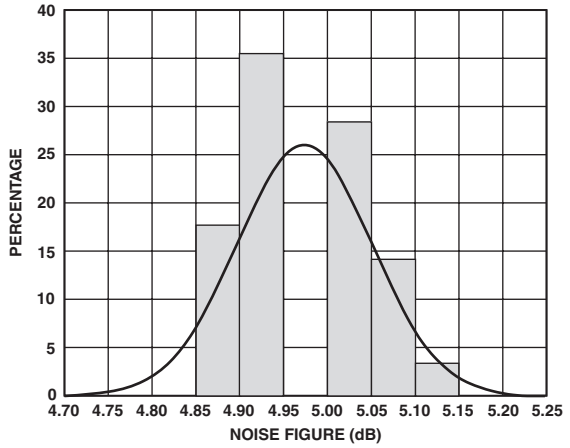
TPC 12. OIP3 vs. Frequency, V_S = 3 V, T_A = –40°C, +25°C, and +85°C



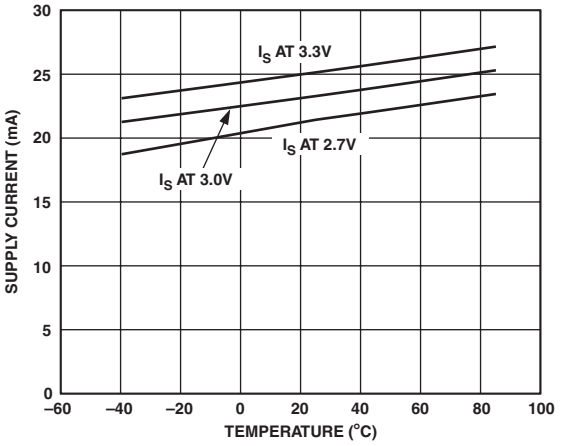
TPC 13. Noise Figure vs. Frequency, V_S = 2.7 V, 3 V, and 3.3 V, T_A = 25°C



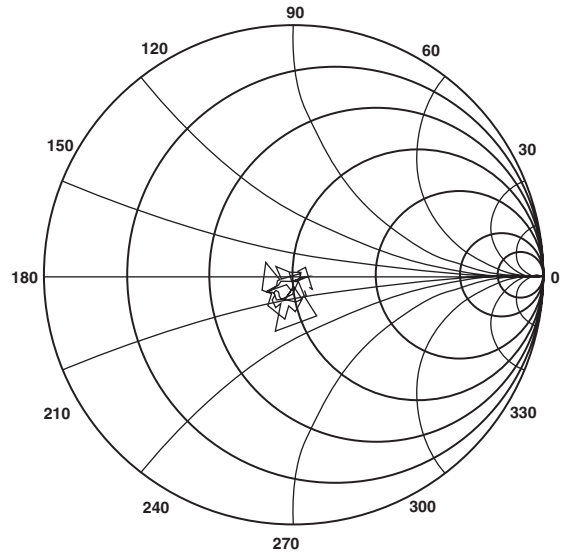
TPC 16. Noise Figure vs. Frequency, V_S = 3 V, T_A = –40°C, +25°C, and +85°C



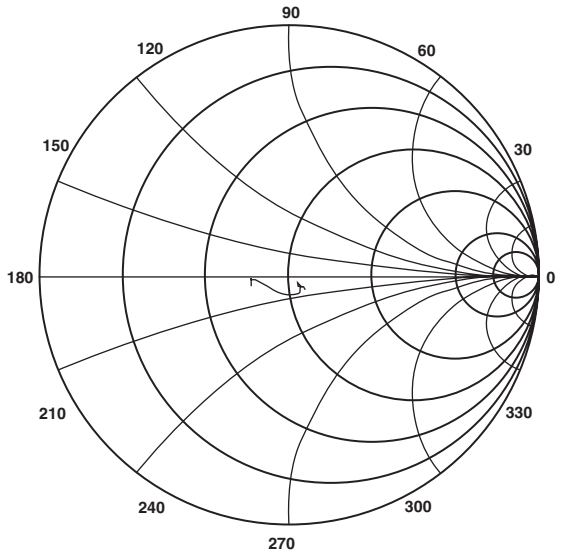
TPC 14. Distribution of Noise Figure, V_S = 3 V, T_A = 25°C, f = 2.2 GHz



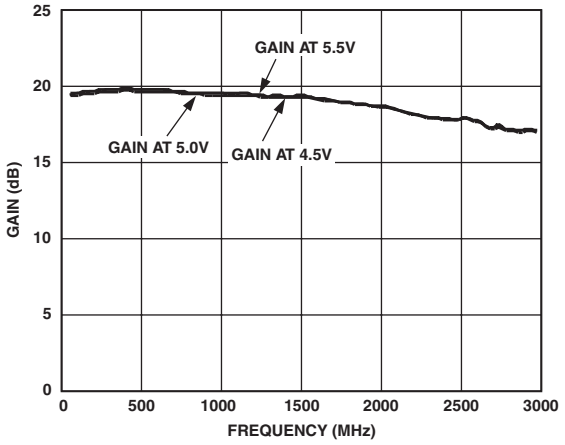
TPC 17. Supply Current vs. Temperature, V_S = 2.7 V, 3 V, and 3.3 V



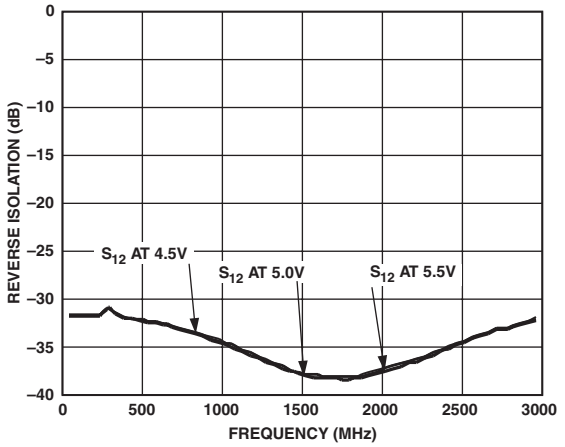
TPC 15. S_{11} vs. Frequency, V_S = 5 V, T_A = 25°C, 100 MHz ≤ f ≤ 3 GHz



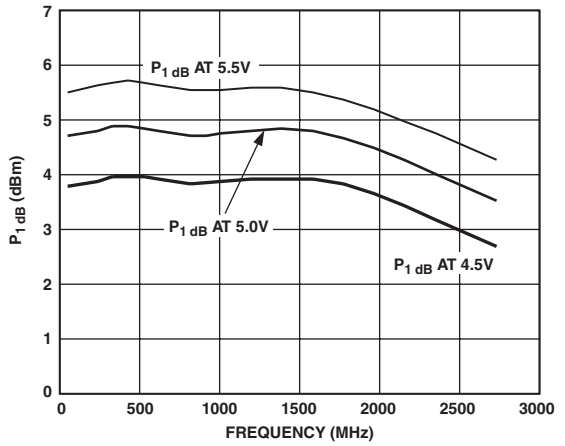
TPC 18. S_{22} vs. Frequency, V_S = 5 V, T_A = 25°C, 100 MHz ≤ f ≤ 3 GHz



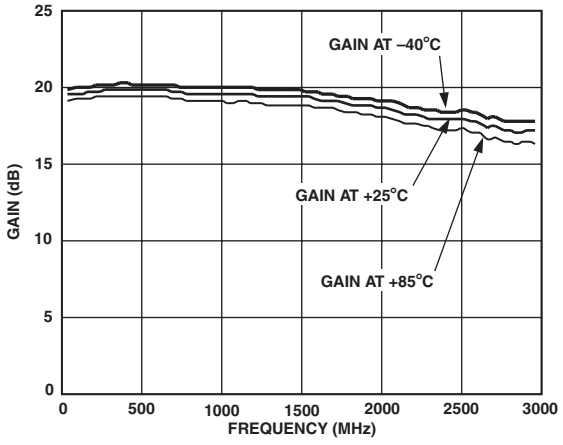
TPC 19. Gain vs. Frequency, V_S = 4.5 V, 5.0 V, and 5.5 V, T_A = 25°C



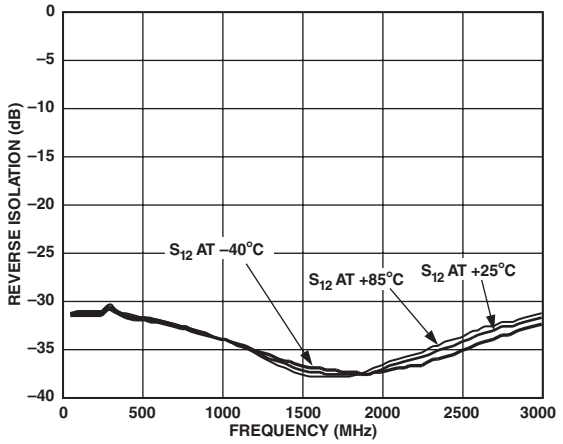
TPC 20. Reverse Isolation vs. Frequency, V_S = 4.5 V, 5 V, and 5.5 V, T_A = 25°C



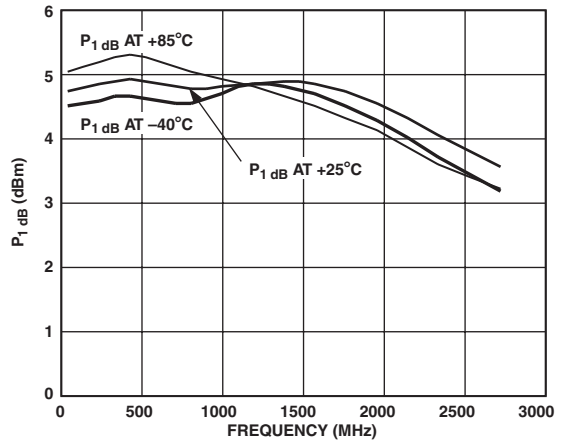
TPC 21. $P_{1\ dB}$ vs. Frequency, V_S = 4.5 V, 5 V, and 5.5 V, T_A = 25°C



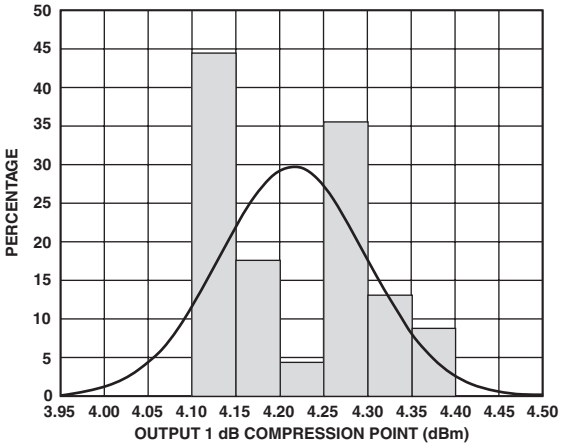
TPC 22. Gain vs. Frequency, V_S = 5 V, T_A = –40°C, +25°C, and +85°C



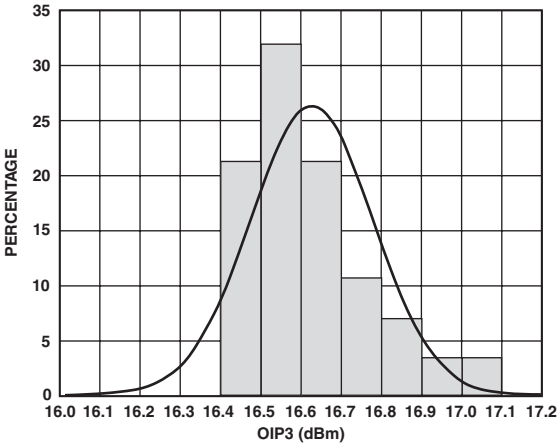
TPC 23. Reverse Isolation vs. Frequency, V_S = 5 V, T_A = –40°C, +25°C, and +85°C



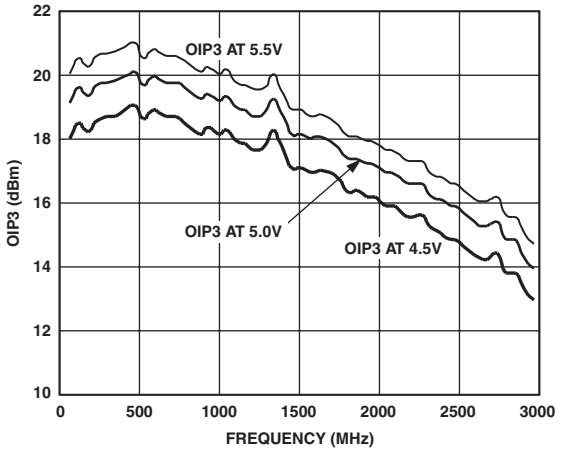
TPC 24. $P_{1\ dB}$ vs. Frequency, V_S = 5 V, T_A = –40°C, +25°C, and +85°C



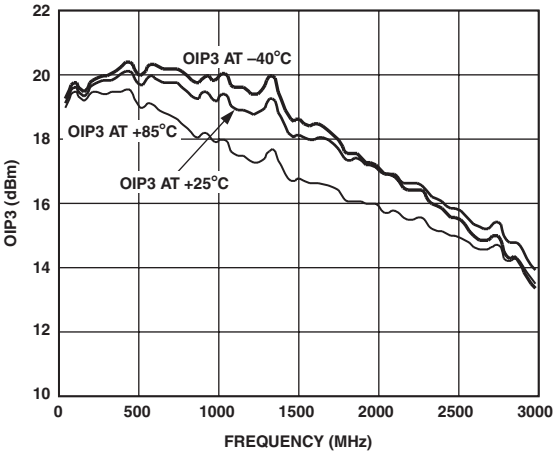
TPC 25. Distribution of $P_{1\,dB}$, V_S = 5 V, T_A = 25°C, f = 2.2 GHz



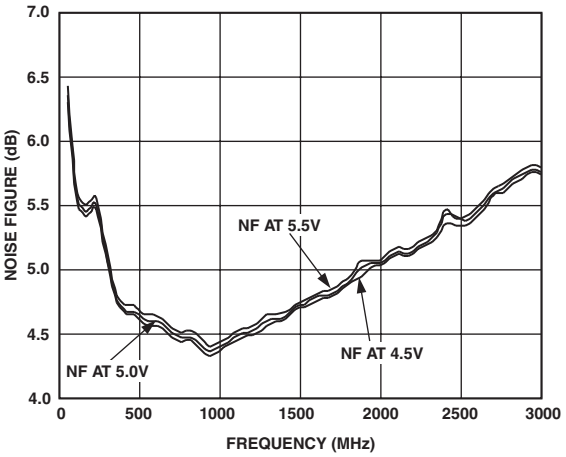
TPC 28. Distribution of OIP3, V_S = 5 V, T_A = 25°C, f = 2.2 GHz



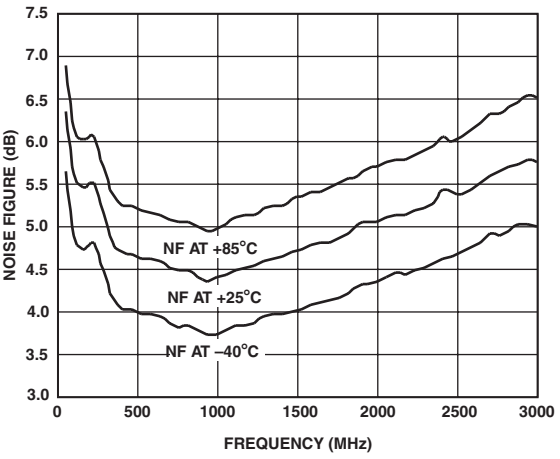
TPC 26. OIP3 vs. Frequency, V_S = 4.5 V, 5 V, and 5.5 V, T_A = 25°C



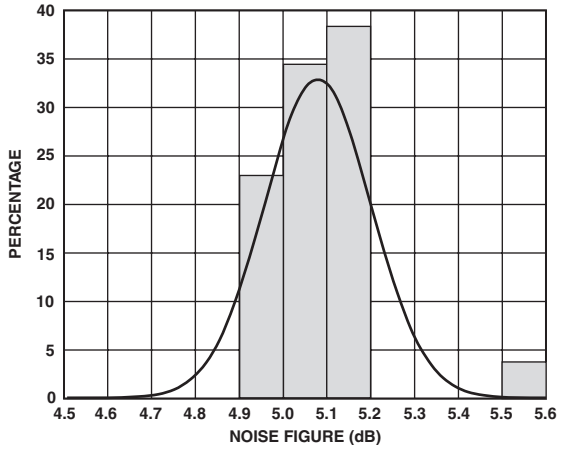
TPC 29. OIP3 vs. Frequency, V_S = 5 V, T_A = –40°C, +25°C, and +85°C



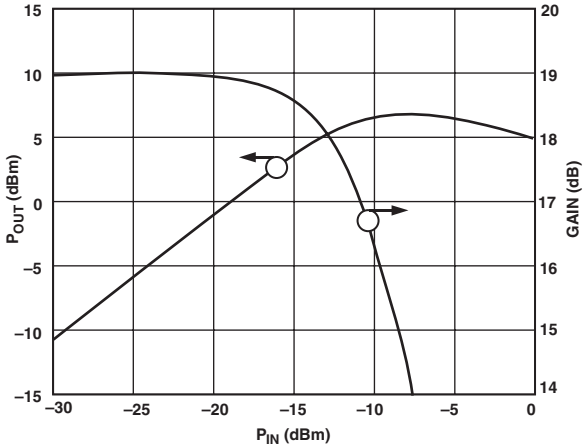
TPC 27. Noise Figure vs. Frequency, V_S = 4.5 V, 5 V, and 5.5 V, T_A = 25°C



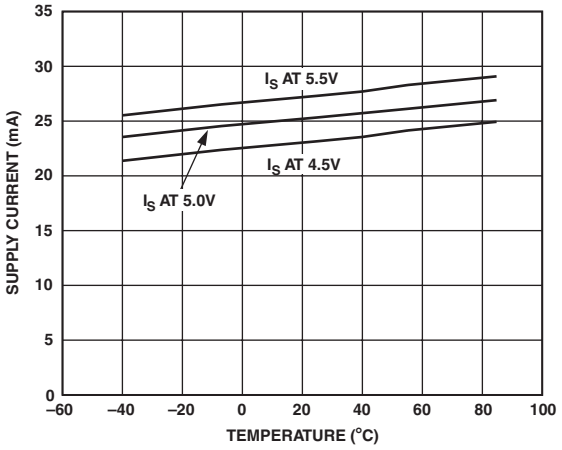
TPC 30. Noise Figure vs. Frequency, V_S = 5 V, T_A = –40°C, +25°C, and +85°C



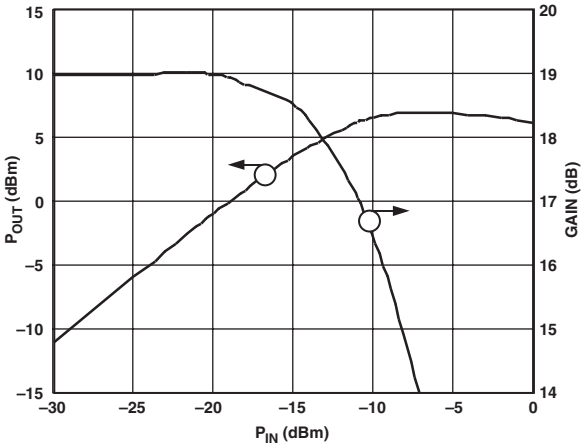
TPC 31. Distribution of Noise Figure, V_S = 5 V, T_A = 25°C, f = 2.2 GHz



TPC 33. Output Power and Gain vs. Input Power, V_S = 3 V, T_A = 25°C, f = 900 MHz



TPC 32. Supply Current vs. Temperature, V_S = 4.5 V, 5 V, and 5.5 V



TPC 34. Output Power and Gain vs. Input Power, V_S = 5 V, T_A = 25°C, f = 900 MHz

THEORY OF OPERATION

The AD8354 is a two-stage feedback amplifier employing both shunt-series and shunt-shunt feedback. The first stage is degenerated and resistively loaded, and provides approximately 10 dB of gain. The second stage is a PNP-NPN Darlington output stage, which provides another 10 dB of gain. Series-shunt feedback from the emitter of the output transistor sets the input impedance to 50 Ω over a broad frequency range. Shunt-shunt feedback from the amplifier output to the input of the Darlington stage helps to set the output impedance to 50 Ω. The amplifier can be operated from a 3 V supply by adding a choke inductor from the amplifier output to VPOS. Without this choke inductor, operation from a 5 V supply is also possible.

BASIC CONNECTIONS

The AD8354 RF gain block is a fixed-gain amplifier with single-ended input and output ports whose impedances are nominally equal to 50 Ω over the frequency range 100 MHz to 2.7 GHz. Consequently, it can be directly inserted into a 50 Ω system with no impedance matching circuitry required. The input and output impedances are sufficiently stable versus variations in temperature and supply voltage that no impedance matching compensation is required. A complete set of scattering parameters is available at the Analog Devices website (www.analog.com).

The input pin (INPT) is connected directly to the base of the first amplifier stage, which is internally biased to approximately 1 V, so a dc-blocking capacitor should be connected between the source that drives the AD8354 and the input pin, INPT.

It is critical to supply very low inductance ground connections to the ground pins (Pins 1, 4, 5, and 8) as well as to the backside exposed paddle. This will ensure stable operation.

The AD8354 is designed to operate over a wide supply voltage range from 2.7 V to 5.5 V. The output of the part, VOUT, is taken directly from the collector of the output amplifier stage. This node is internally biased to approximately 3.2 V when the supply voltage is 5 V. Consequently, a dc-blocking capacitor should be connected between the output pin, VOUT, and the load that it drives. The value of this capacitor is not critical, but it should be 100 pF or larger.

When the supply voltage is 3 V, it is recommended that an external RF choke be connected between the supply voltage and the output pin, VOUT. This will increase the dc voltage applied to the collector of the output amplifier stage, which will improve performance of the AD8354 to be very similar to the performance produced when 5 V is used for the supply voltage. The inductance of the RF choke should be approximately 100 nH. Care should be taken to ensure that the lowest series self-resonant frequency of this choke is well above the maximum frequency of operation for the AD8354.

The supply voltage input, VPOS, should be bypassed using a large value capacitance (approximately 0.47 µF or larger) and a smaller, high frequency bypass capacitor (approximately 100 pF) physically located close to the VPOS pin.

The recommended connections and components are shown in the schematic of the AD8354 evaluation board (Figure 3).

APPLICATIONS

The AD8354 RF gain block may be used as a general-purpose fixed-gain amplifier in a wide variety of applications, such as a driver for a transmitter power amplifier (Figure 1). Its excellent reverse isolation also makes this amplifier suitable for use as a local oscillator buffer amplifier that would drive the local oscillator port of an up or down converter mixer (Figure 2).

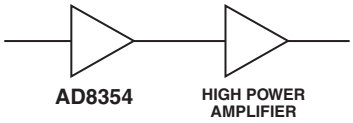


Figure 1. AD8354 as a Driver Amplifier

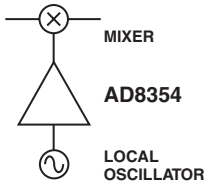


Figure 2. AD8354 as a LO Driver Amplifier

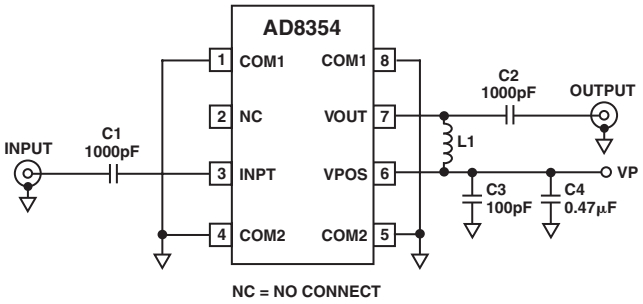


Figure 3. Evaluation Board Schematic

EVALUATION BOARD

Figure 3 shows the schematic of the AD8354 evaluation board. Note that L1 is shown as an optional component, which is used to obtain maximum gain only when V_P = 3 V. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 0.47 µF and 100 pF capacitors.

Table I. Evaluation Board Configuration Options

Component	Function	Default Value
C1, C2	AC Coupling Capacitors.	1000 pF, 0603
C3	High Frequency Bypass Capacitor.	100 pF, 0603
C4	Low Frequency Bypass Capacitor.	0.47 µF, 0603
L1	Optional RF Choke. Used to increase current through output stage when V_P = 3 V. Not recommended for use when V_P = 5 V.	100 nH, 0603

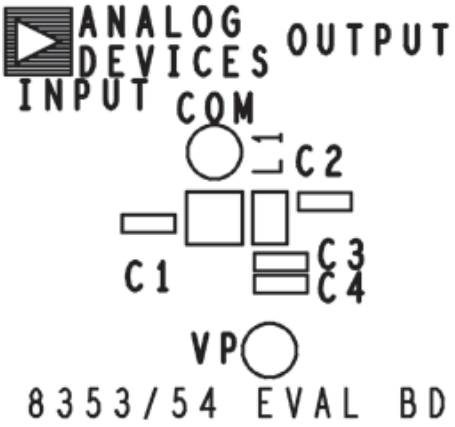


Figure 4. Silkscreen Top

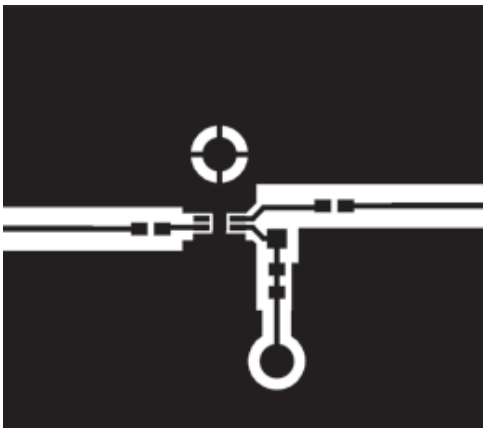
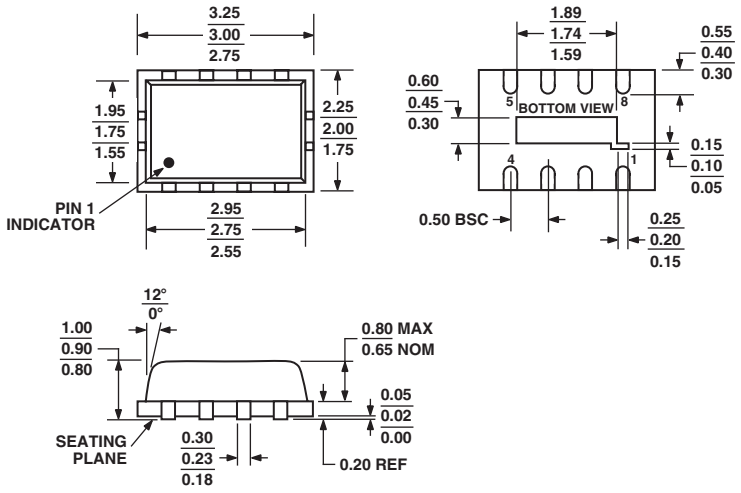


Figure 5. Component Side

OUTLINE DIMENSIONS

8-Lead Lead Frame Chip Scale Package [LFCSP]
2mm x 3 mm Body
(CP-8)
Dimensions shown in millimeters



NOTES
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PADDLE IS COPPER PLATED WITH LEAD FINISH.

Revision History

Location	Page
6/02—Data Sheet changed from REV. 0 to REV. A.	
Change to ORDERING GIUIDE	4
Replaced TPC 34	10
Updated OUTLINE DIMENSIONS	13